AHB Lite to Can Bus Module

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Purpose and Functionality

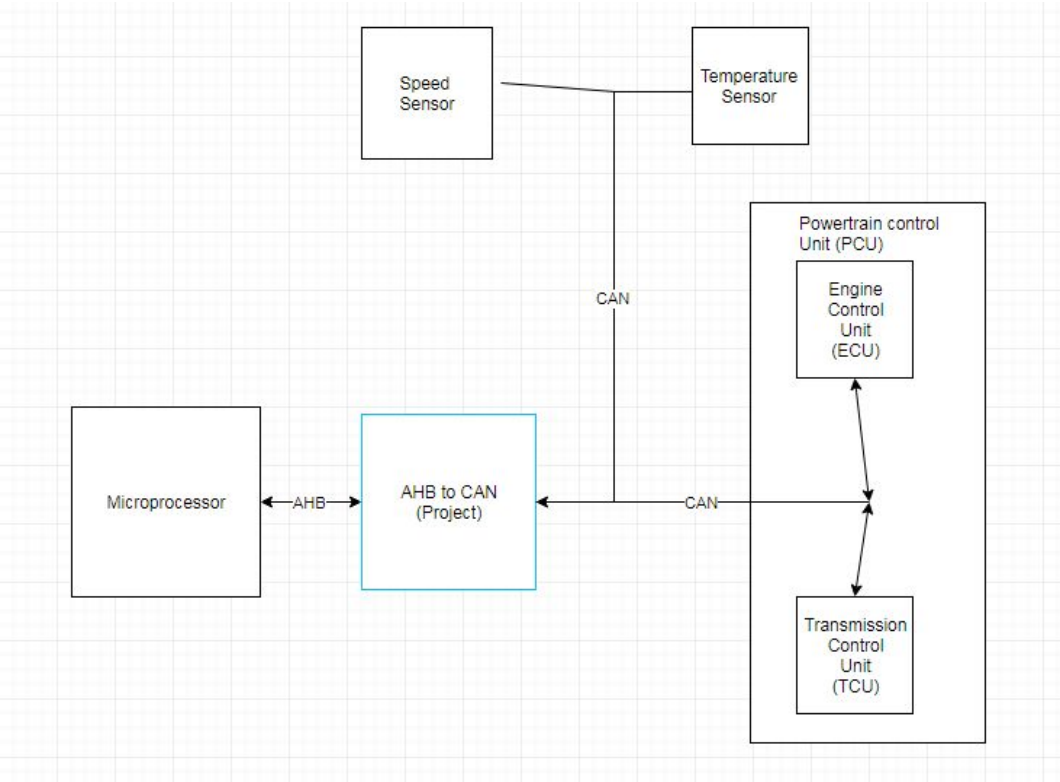
Purpose:

To convert data from the AHB Lite protocol to the Can Bus protocol and vice-versa.

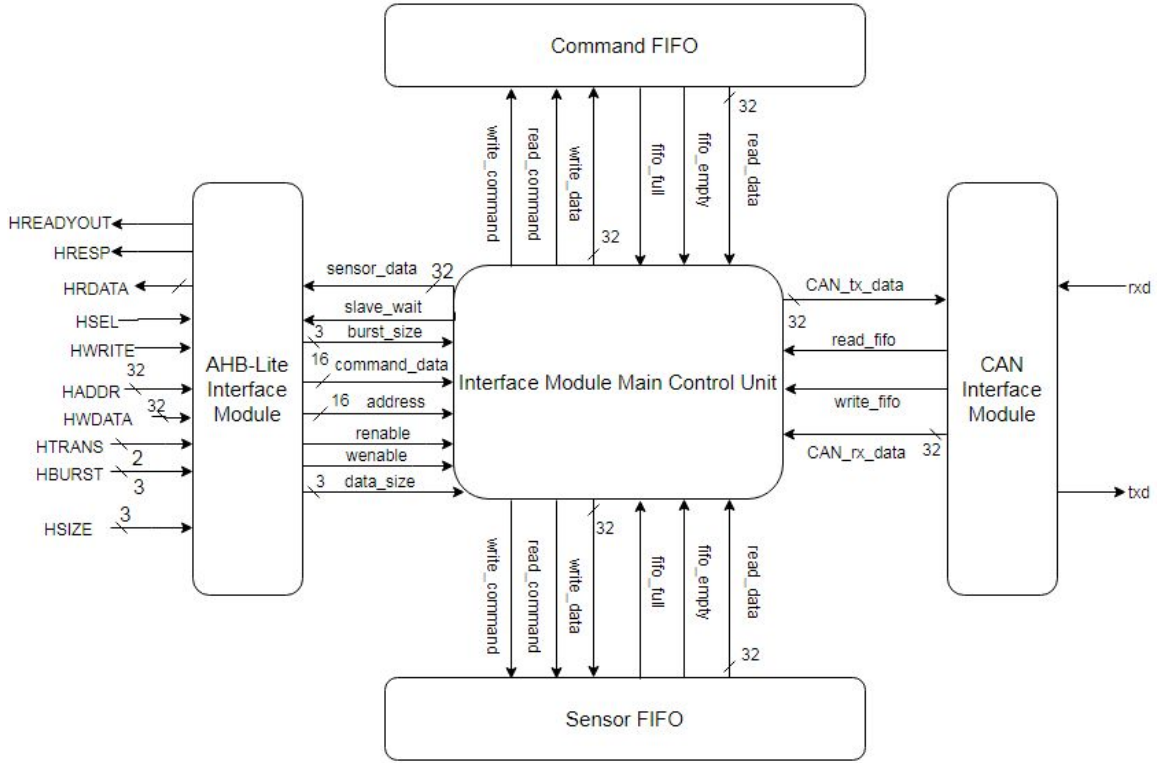
Functionality:

- Optimized for Area.
- Two FIFOs to store the inputs of the CAN and AHB Bus.
- Central module to control the timing of all devices.

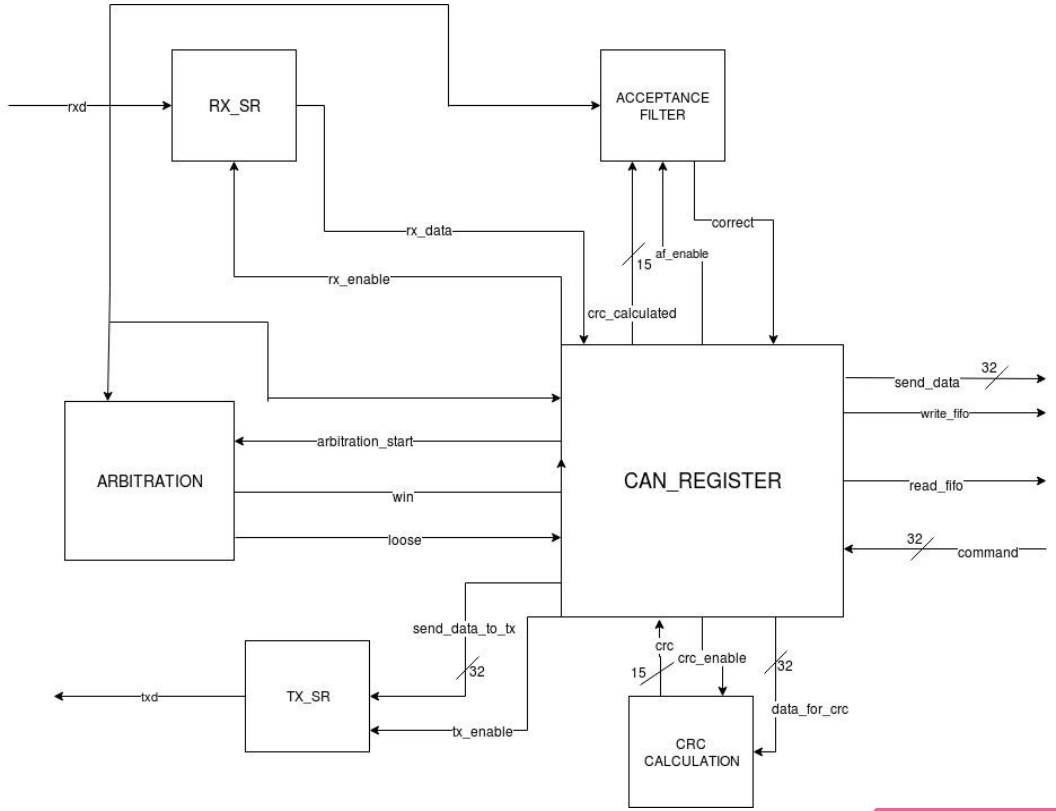
System Design



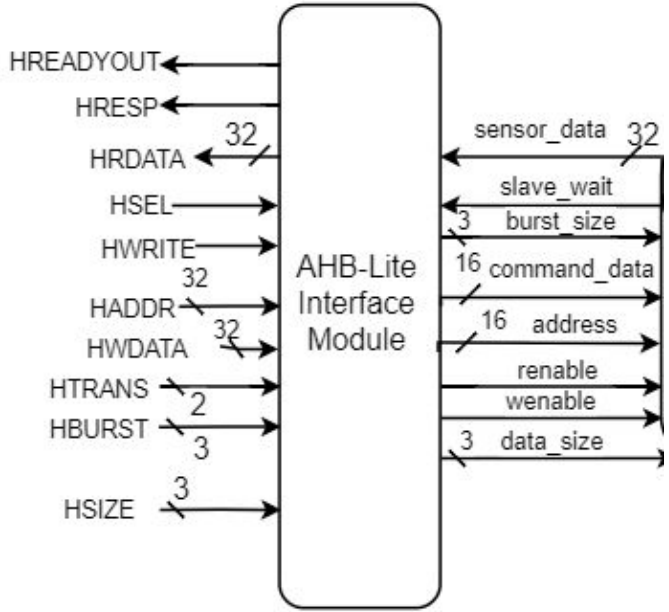
Design Architecture



CAN Module


rxd
RX_SR
ACCEPTANCE FILTER
rx_data
correct
15
af_enable
rx_enable
crc_calculated
send_data
32
write_fifo
ARBITRATION
arbitration_start
CAN_REGISTER
win
read_fifo
loose
32
command
send_data_to_tx
crc
15
crc_enable
32
32
txd
TX_SR
data_for_crc
tx_enable
CRC CALCULATION

AHB - Lite Module



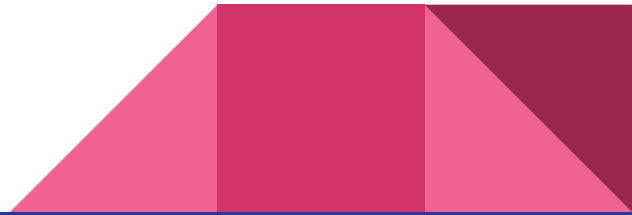
Fixed Success Criteria

1) Test benches exist for all top level components and the entire design: Successful

2) Entire design synthesizes completely, without any inferred latches, timing arcs ,and, sensitivity list warnings: Successful
3) Source and mapped version of the complete design behave the same for all test cases: Successful

4) A complete IC layout is produced that passes all geometry and connectivity checks: Successful

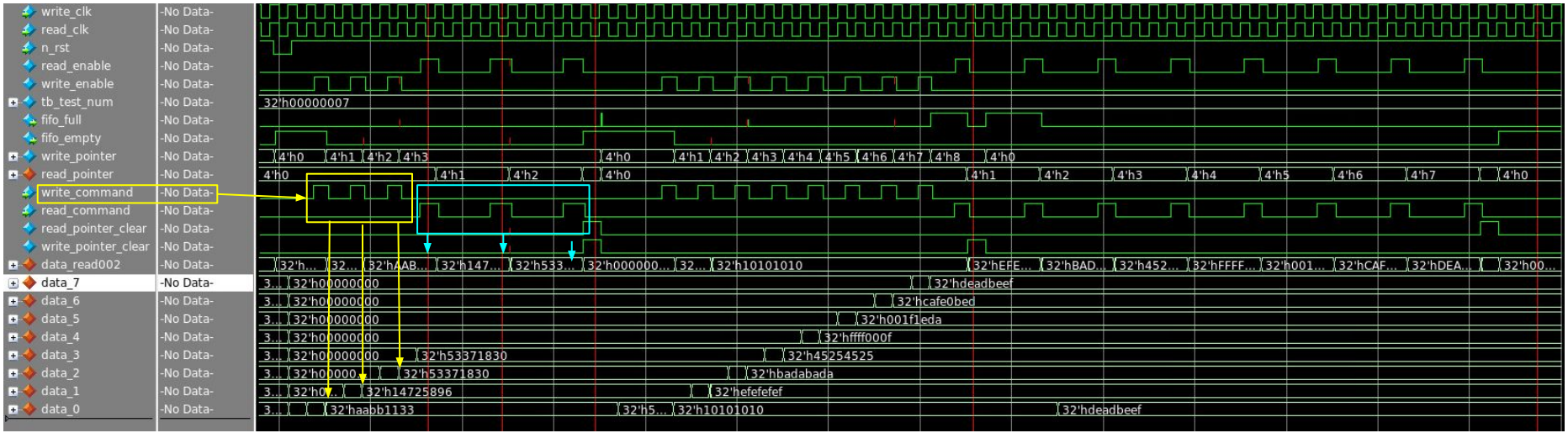
5) Correct area, pin count and clock rate:
    a) Area : 4mm x 4mm
    b) Pin Count: 112
    c) Clock Period: 10ns



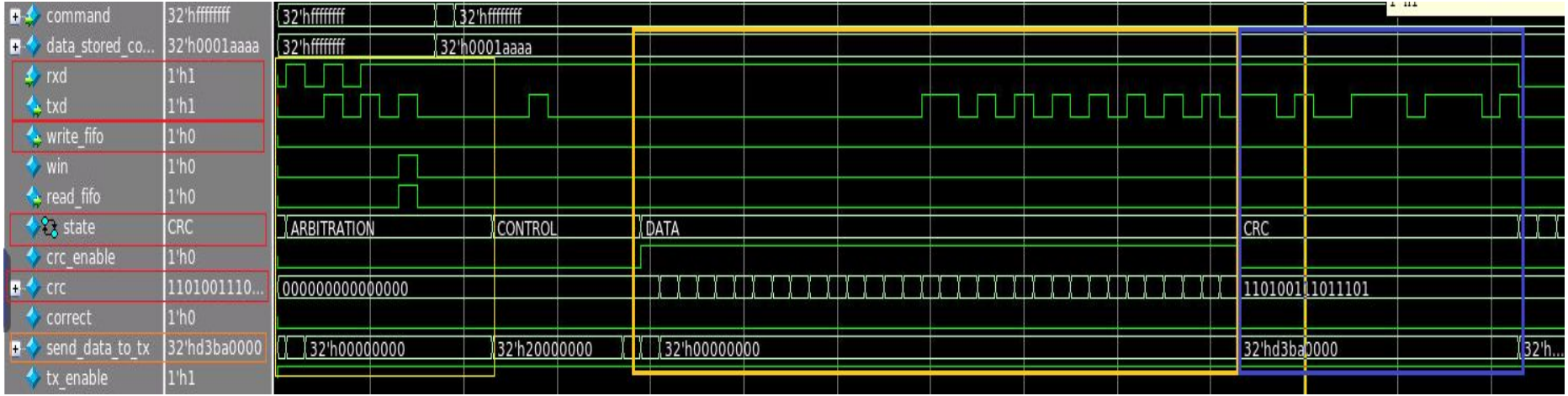
Design Specific Success Criteria

1) Design is capable of transmitting data from CAN protocol to AHB protocol (2 points): Successful
2) Design is capable of transmitting data from AHB protocol to CAN protocol (2 points): Successful
3) Design is capable of queuing up responses from the CAN bus to to the sensor FIFO (2 points): Successful
4) Design is capable of queuing up inputs sent by the AHB Lite master to command FIFO (2 points): Successful

Results (Command FIFO Data queue & Dequeue)



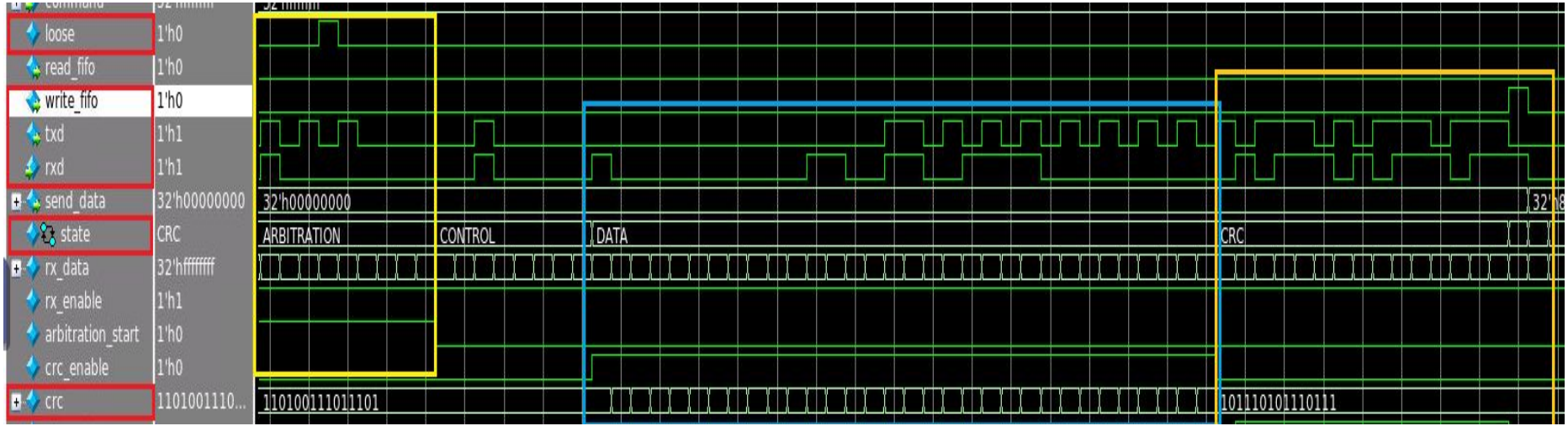
CAN Bus Write Cycle



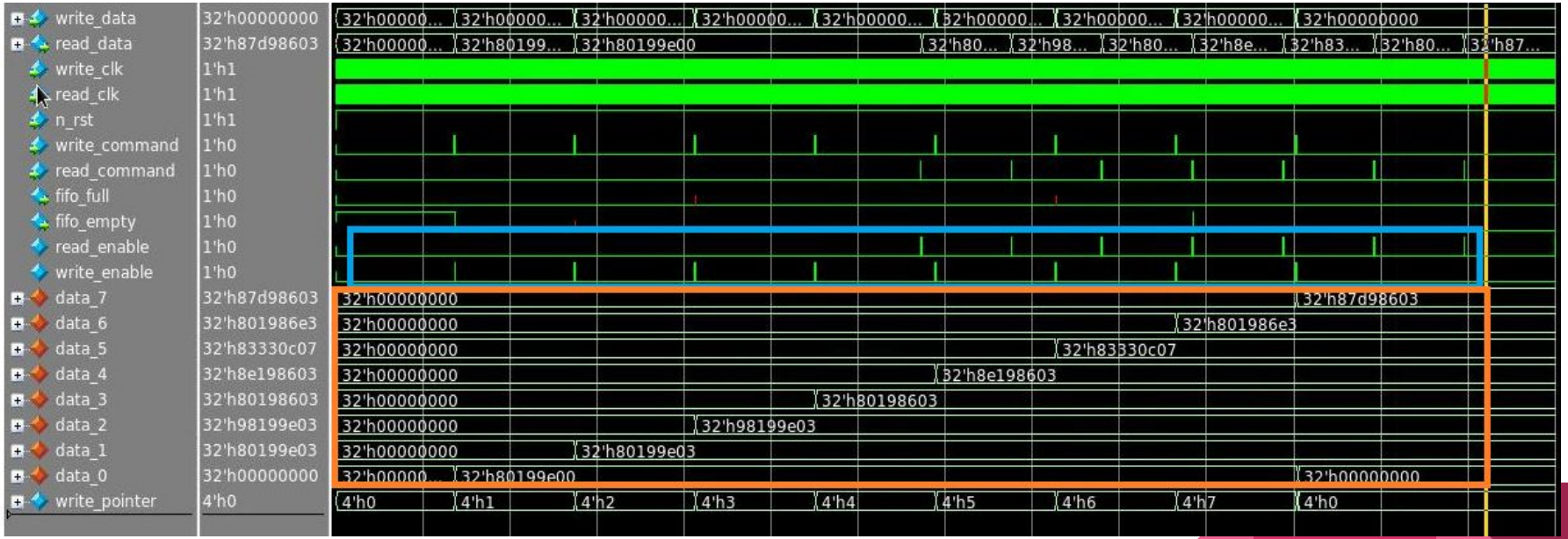
CAN Bus Write Cycle

```
Write cycle started at Time:                    0ps
    SOF started at Time:                  0ps
    SOF ended at Time:                 5000ps
    Arbitration started at Time:                5000ps
    Arbitration is won
    Arbitration Ended cycle Time:              115000ps
    Control field started at Time:              115000ps
    Control field finished reading at Time:                195000ps
    Data cycle started at Time:               195000ps
    Data read correctly
    Data cycle finihsed writing at Time:                515000ps
    Value read: 00000000000000011010101010101010
    CRC cycle started at Time:                515000ps
    Code calculated 110100111011101 , at Time:                515000ps
    CRC cycle finished reading (110100111011101) at Time:                    0ps
    Ack = 0
    ACK cycle started at Time:                   0ps
    EOF cycle started at Time:                675000ps
    EOF cycle finished at Time:                685000ps
Write cycle ended at Time:                  685000ps
```

CAN Bus Read Cycle



Sensor FIFO Enqueueing data



CAN bus Read Cycle

```
--------------------------
Read cycle started at Time:              685000ps
    SOF started at Time:               685000ps
    SOF ended at Time:                695000ps
    Arbitration started at Time:               695000ps
    Arbitration is lost
    Arbitration Ended cycle Time:               805000ps
    Control field started at Time:               805000ps
    Control field finished writing at Time:                885000ps
    Data cycle started at Time:               885000ps
    Data cycle finihsed reading at Time:                1205000ps
    Data read 80199e00
    CRC cycle started at Time:              1205000ps
    Code calculated 101110101110111 , at Time:                1205000ps
    CRC cycle writing at Time:              1355000ps
    ACK cycle started at Time:                 1000ps
    ACK cycle finished reading at Time:                1365000ps
    EOF cycle started at Time:              1365000ps
    EOF cycle finished at Time:               1375000ps
Read cycle ended at Time:              1375000ps
--------------------------
```

```
Data cycle started at Time:              6405000ps
||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||||VALUE RETRIEVED AT TIME
```

```
6720000 is 80199e00
```

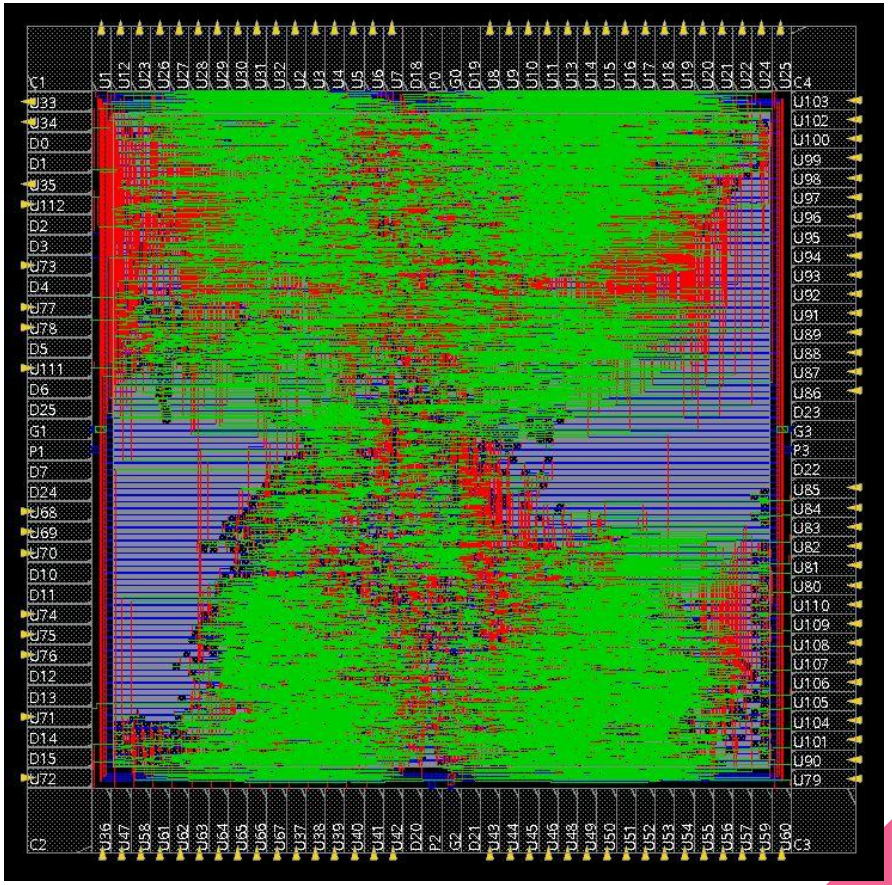
Layout

Synthesis Critical Path Delay:
4ns

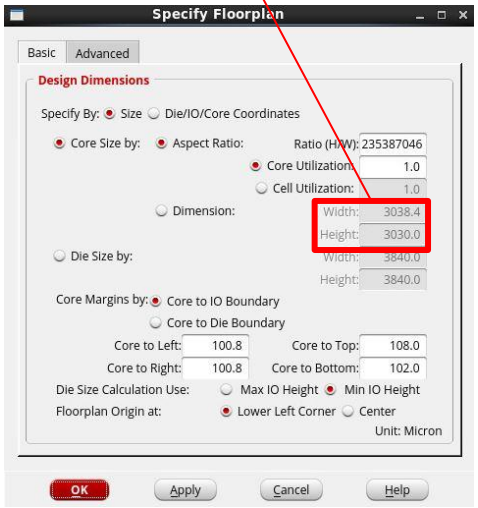
Layout Critical Path Delay:
12.957ns

Budgeted Critical Path Delay:
10ns

Dimensions: **3mm x 3mm**



Width: 3038.4um
Height: 3030.0um

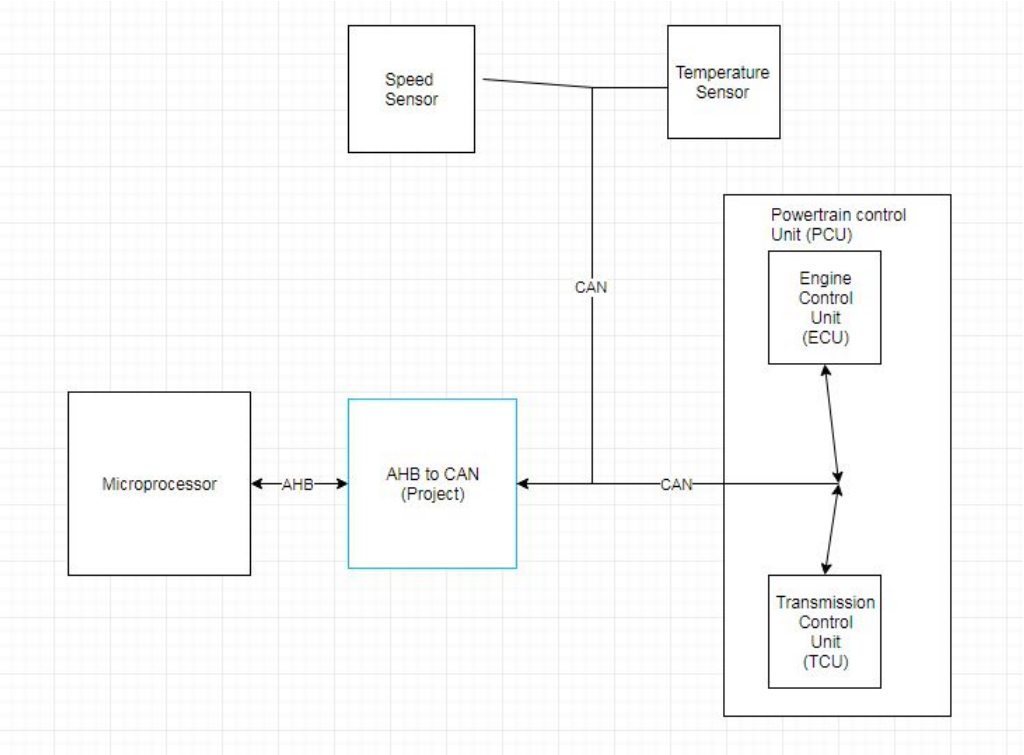


Conclusions

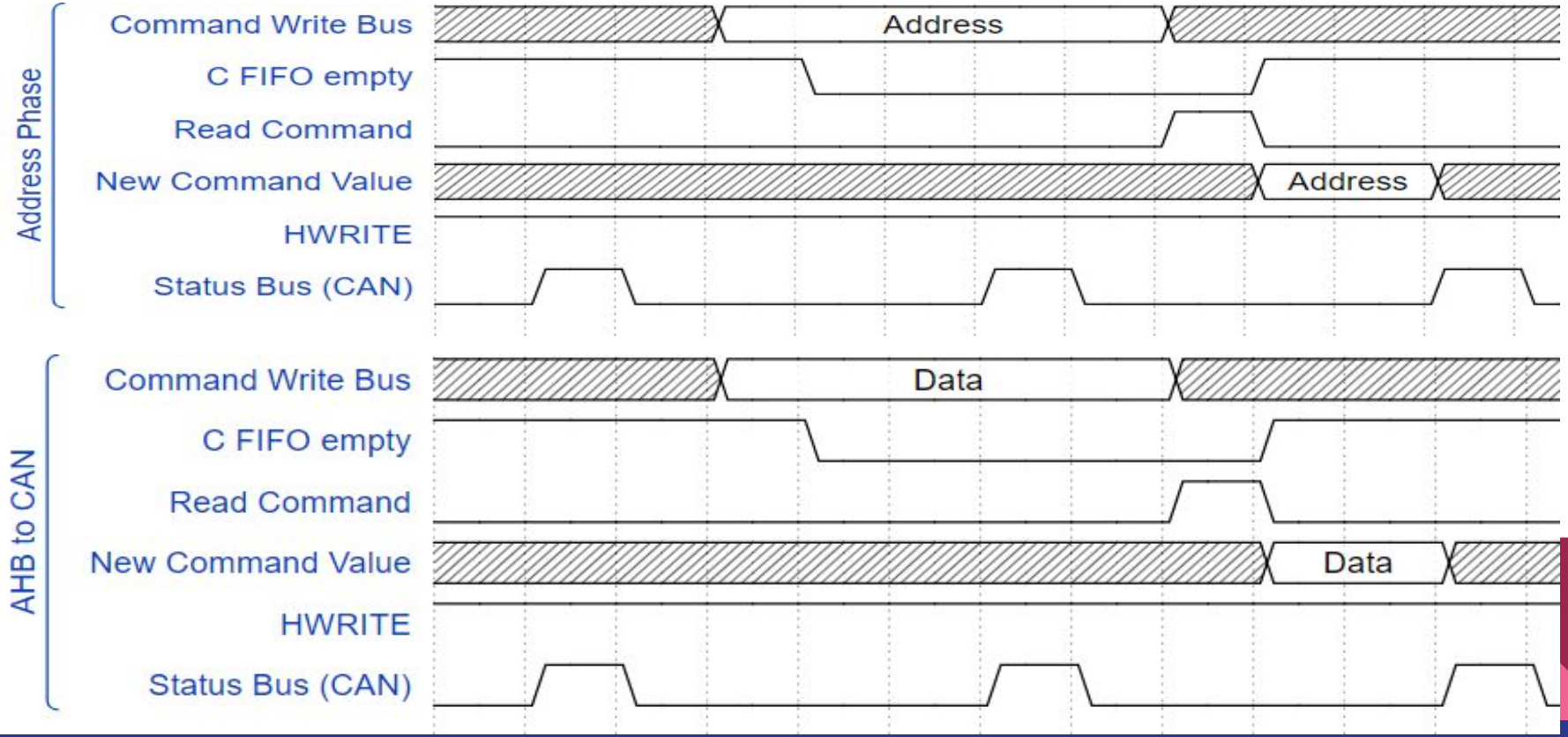
- Challenges
  - Getting the layout timing delay to match our 10ns timing constraint.
  - Matching timing of simulated CAN Node and CAN Node.
- Different Approach
  - Using more registers instead of combinational logic
  - Faster Performance
- Improvements:
  - Implementing Burst Write and Read for AHB Bus.
  - Use AHB addressing when reading from and writing to the two FIFOs.
  - Variable size transmission for CAN bus.

Thank you for your time

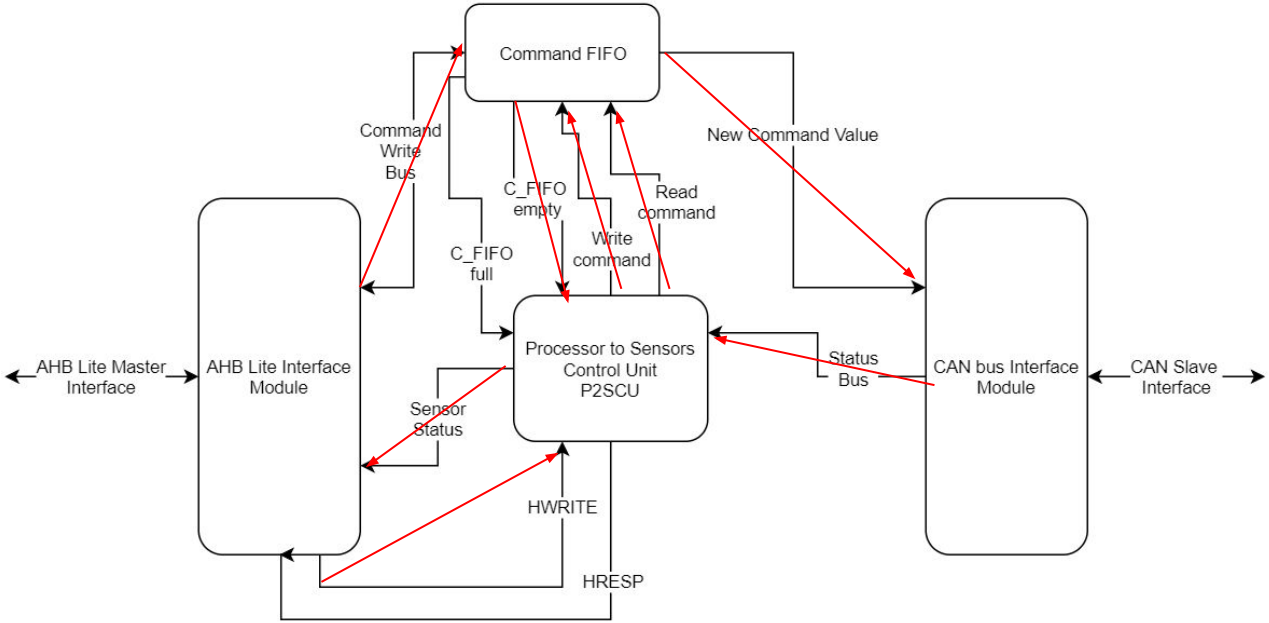
System Level Usage



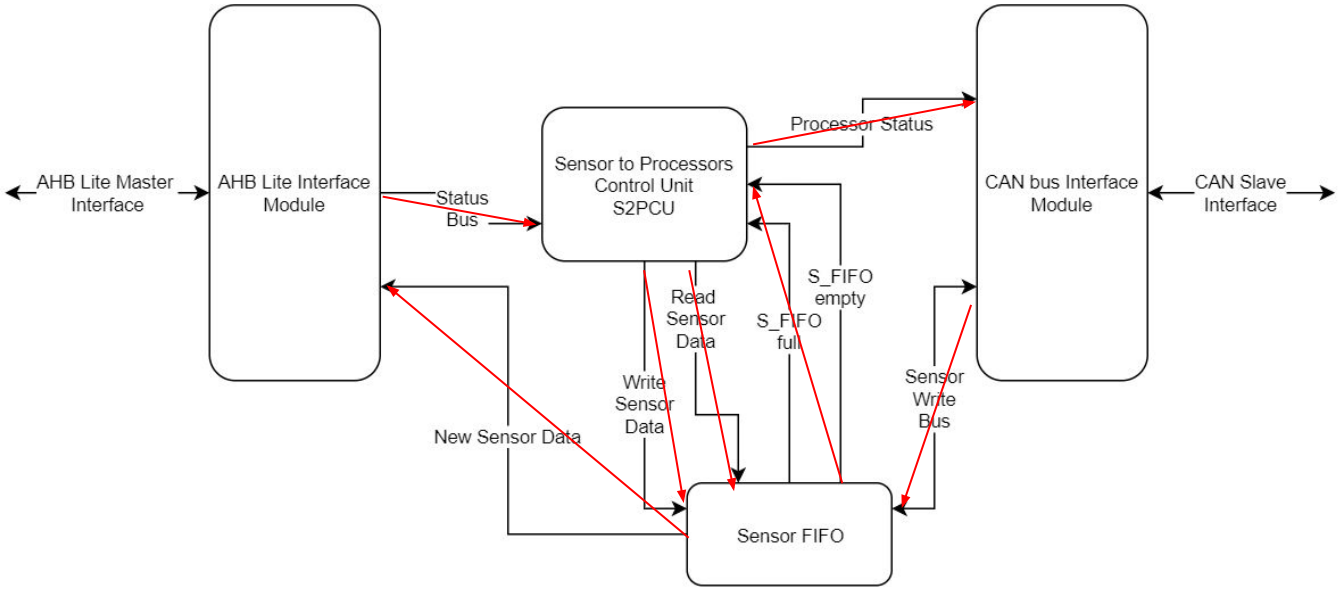
Timing Diagram



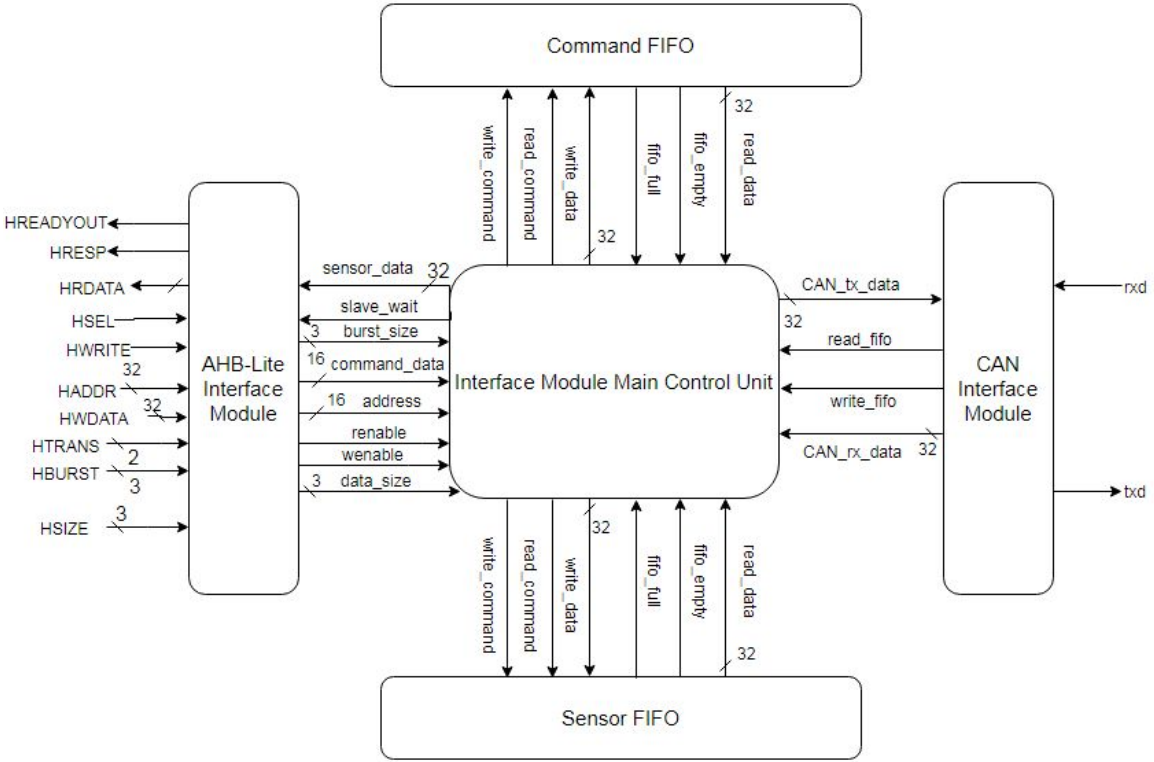
Top Level Architecture (AHB to CAN)



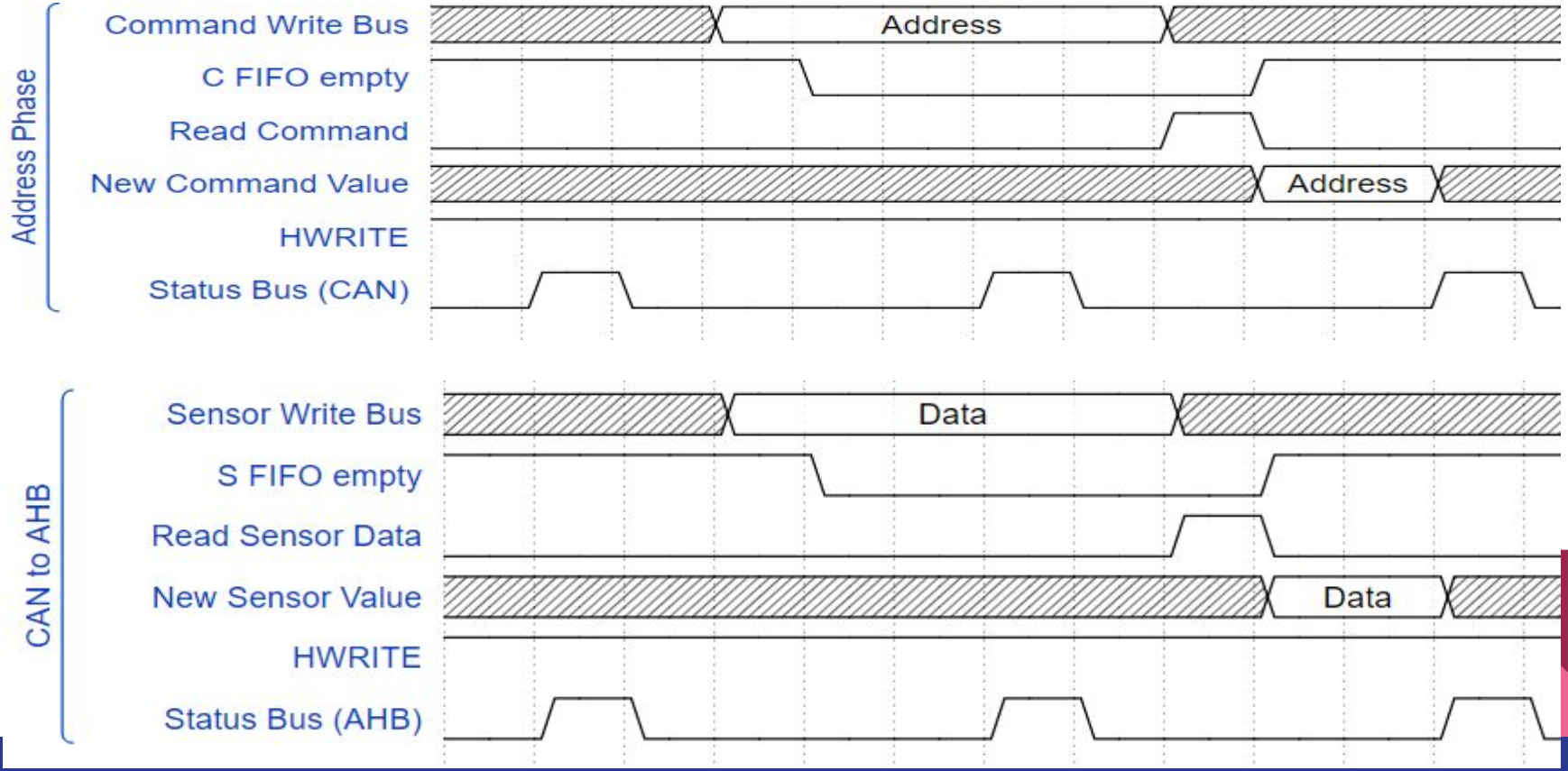
Top Level Architecture (CAN to AHB)



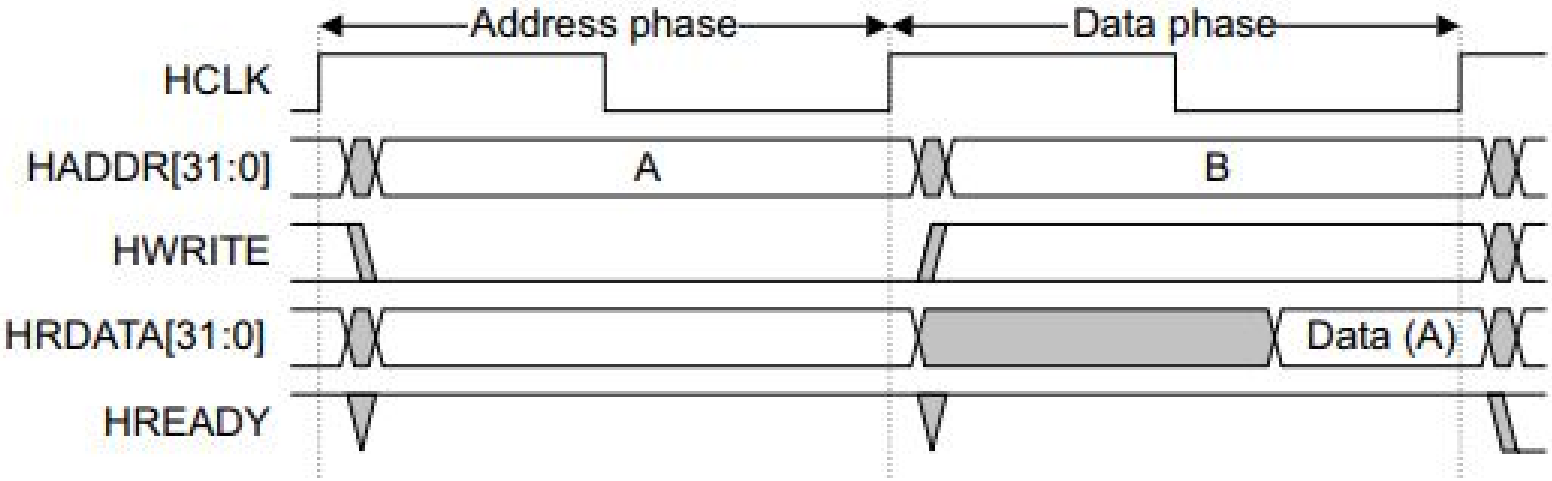
Overall Architecture



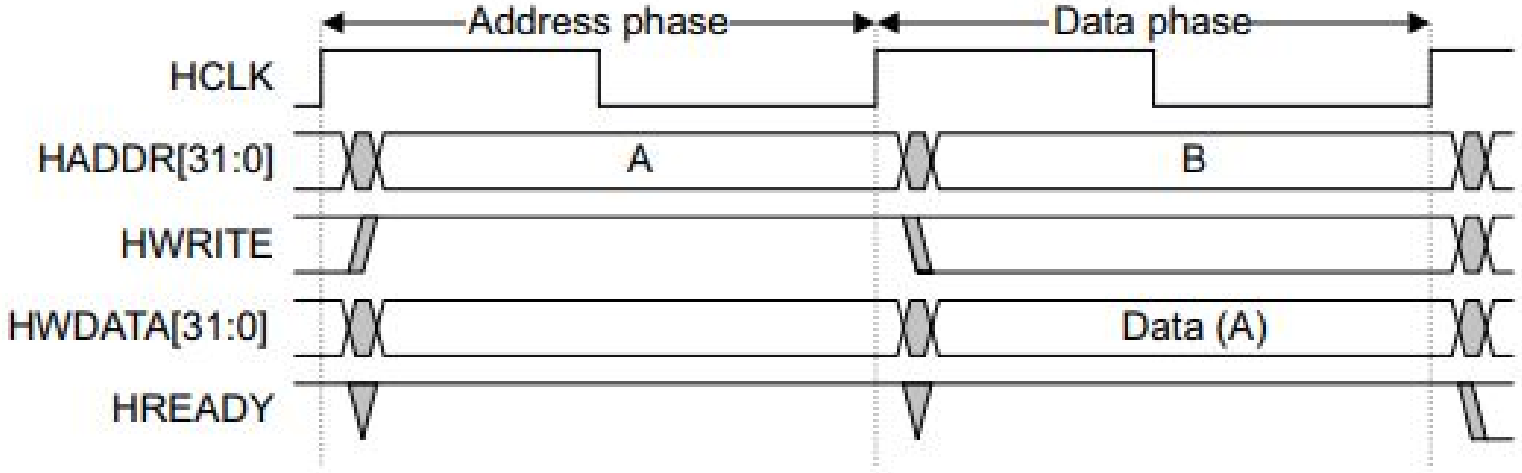
Timing Diagram



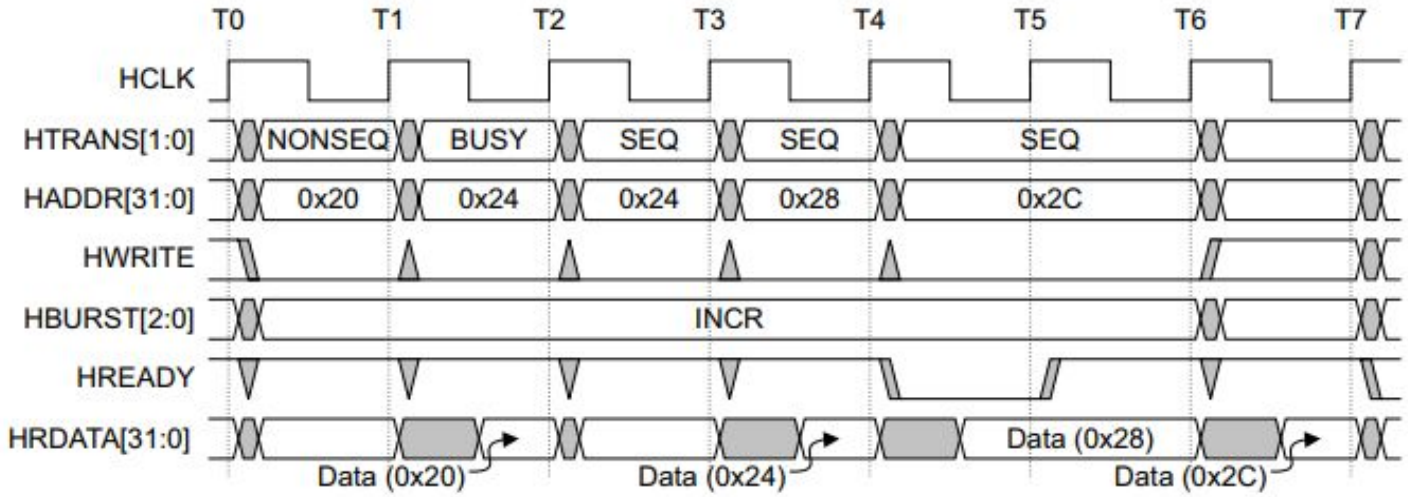
AHB Bus Basic Read Mode



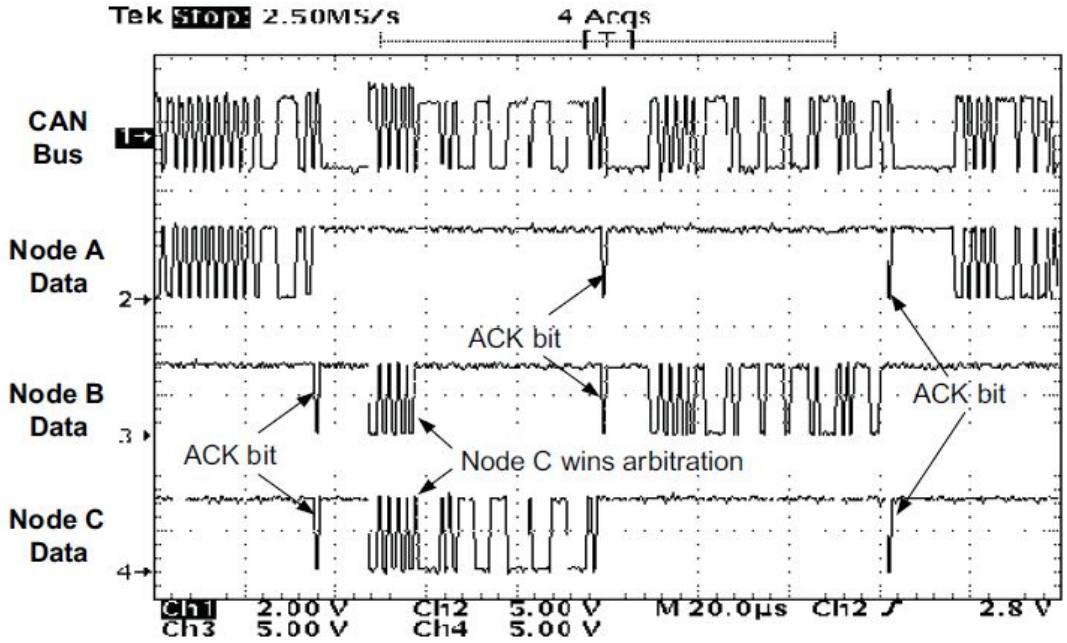
AHB Bus Basic Write Mode



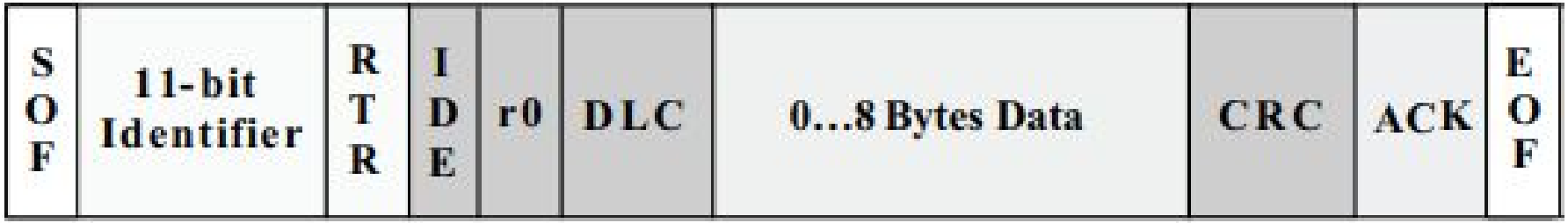
AHB Bus Burst Read Mode (Skip)



CAN Bus Priority Assignment

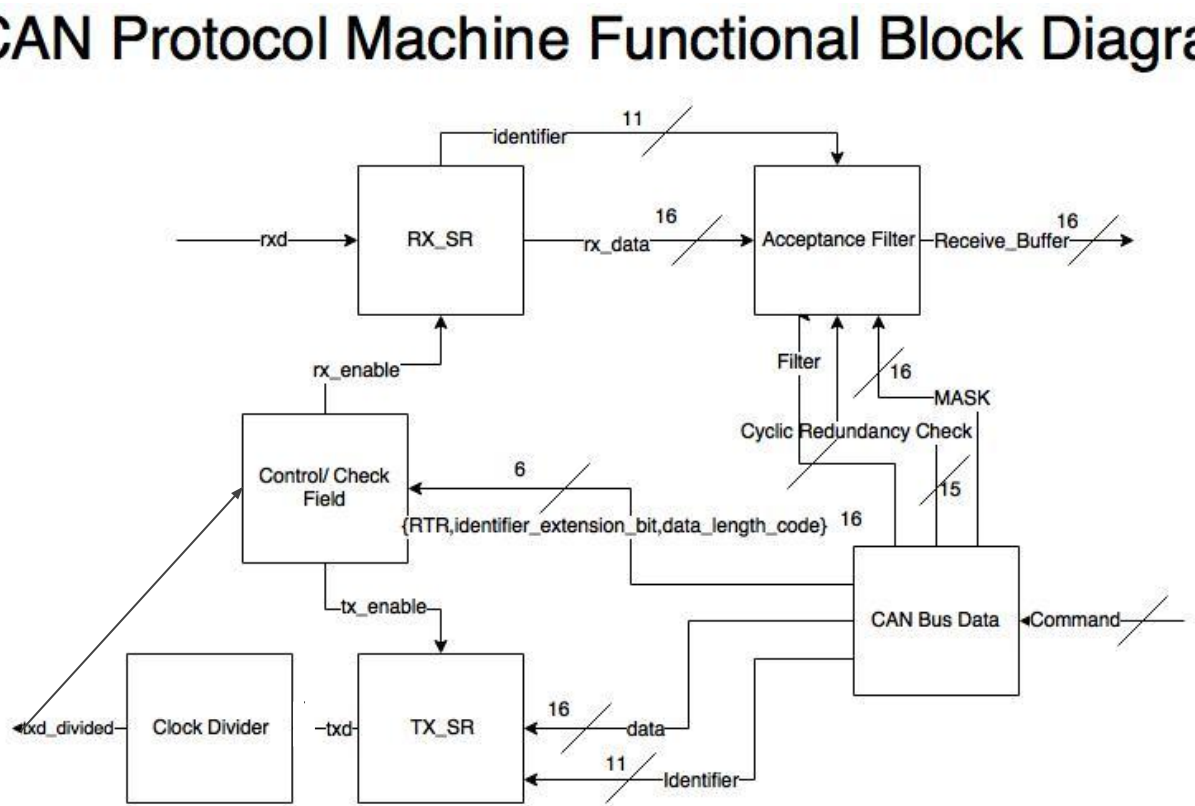


CAN Bus Data Transfer

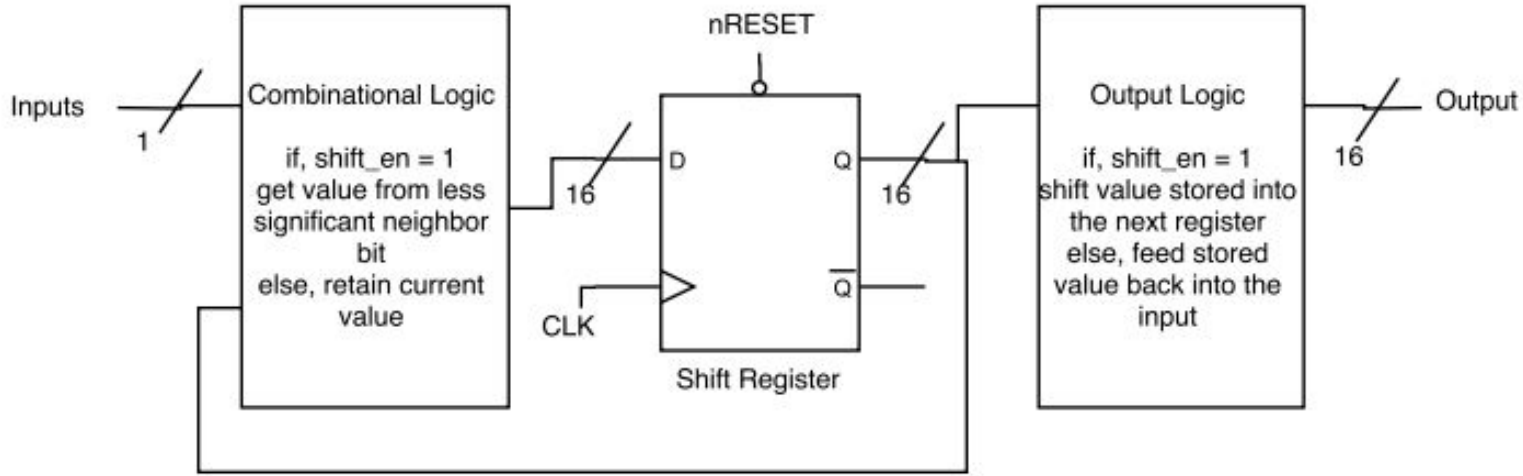


CAN Bus Implementation

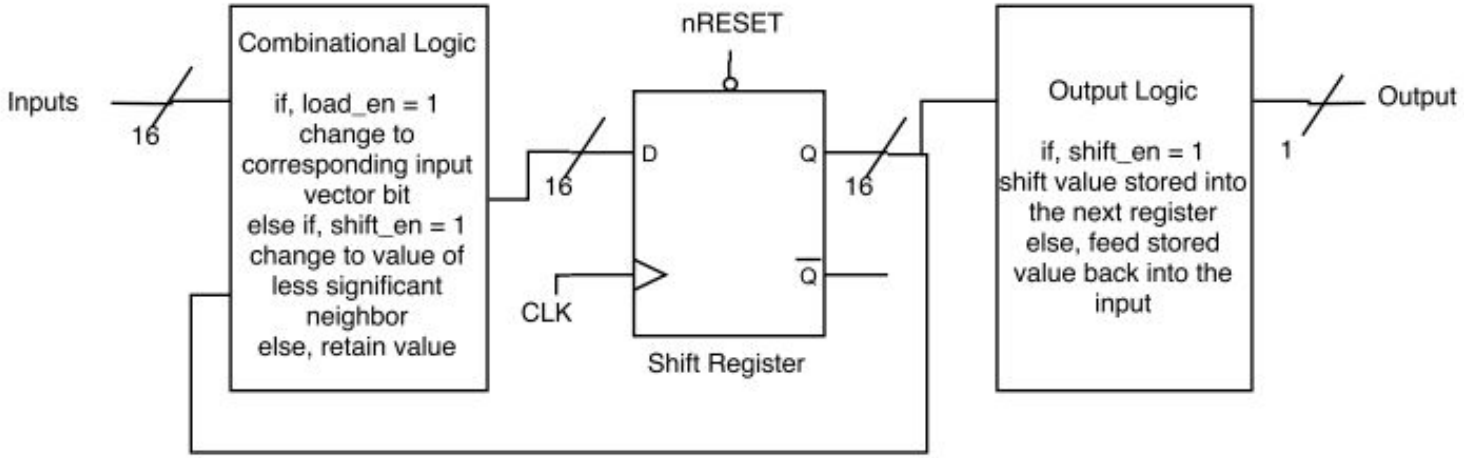
CAN Bus Module



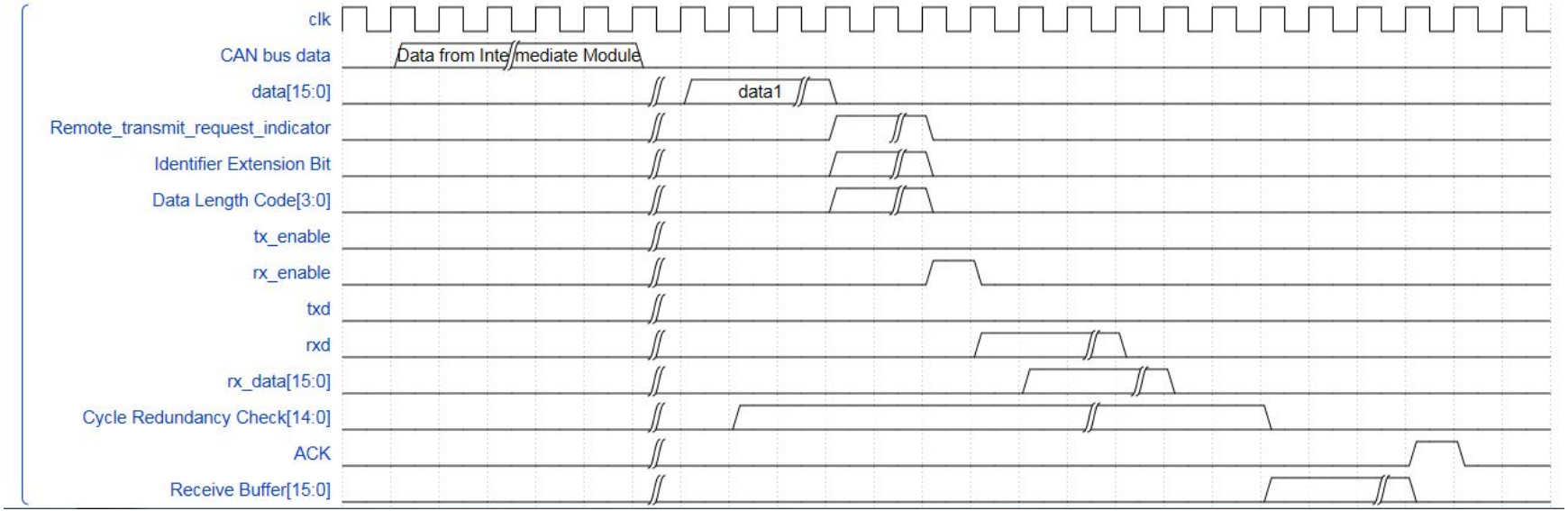
Series to Parallel Shift Register (Skip)



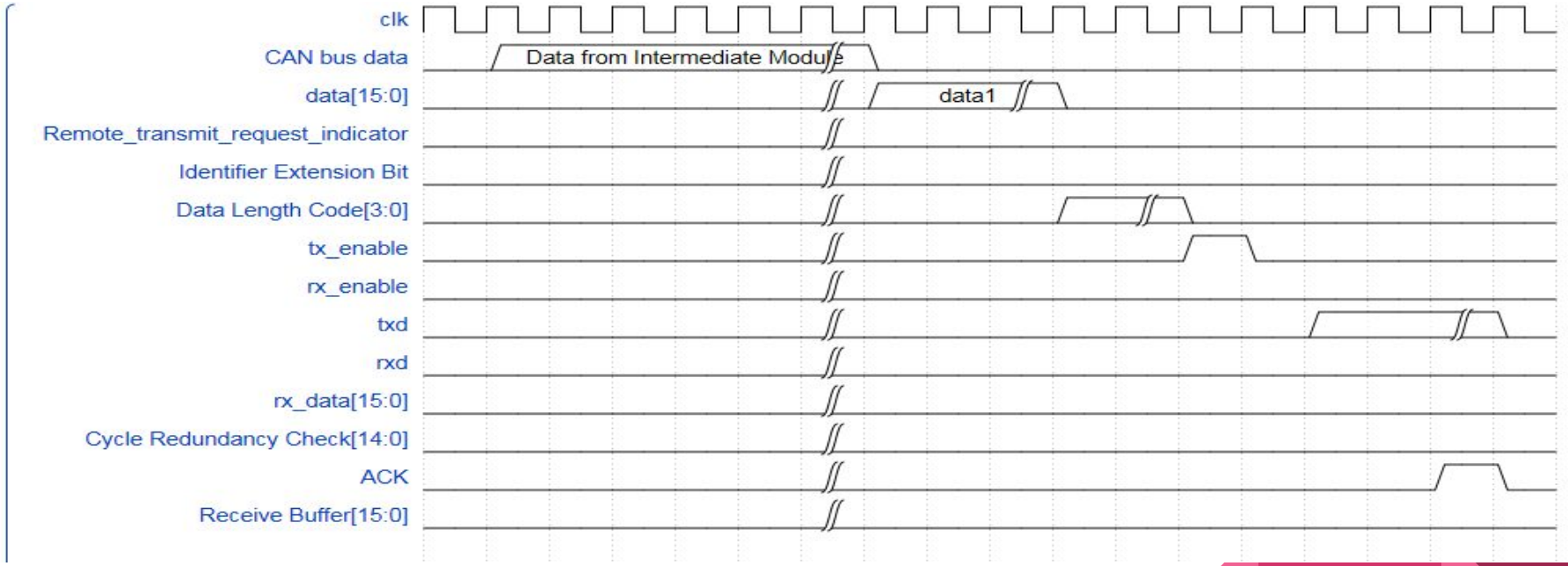
Parallel to Serial Shift Register



CAN Bus Read Mode Timing Diagram

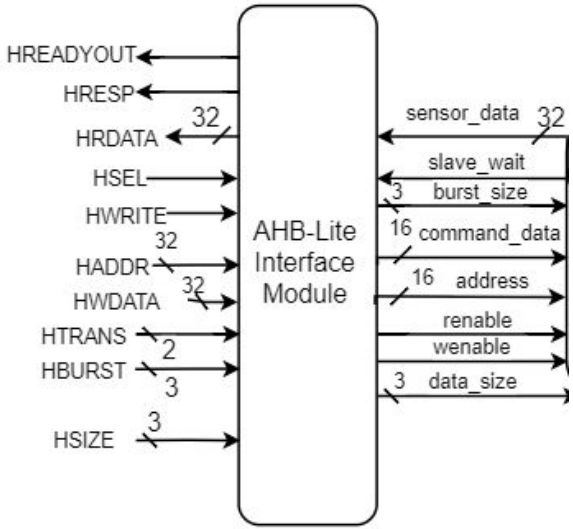


CAN Bus Write Mode Timing Diagram

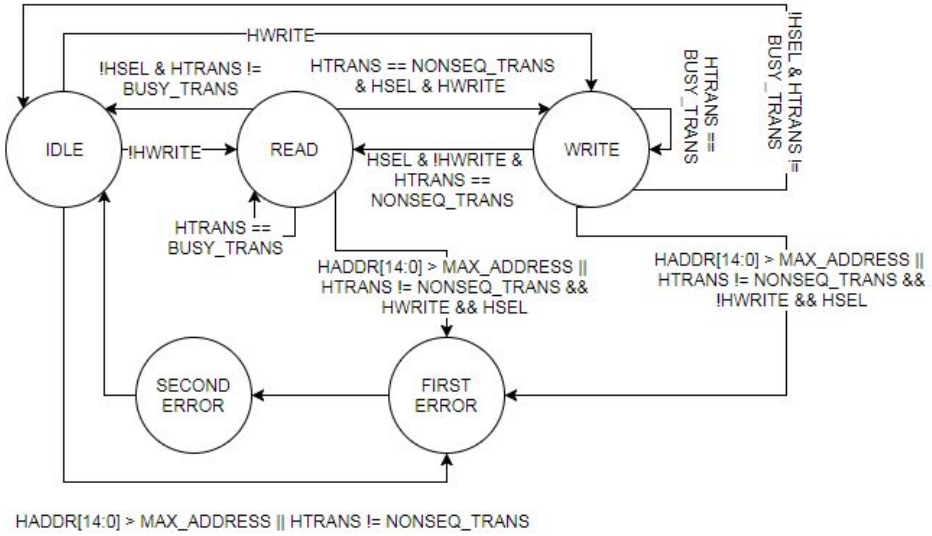


AHB Lite Bus Implementation

AHB-Lite Slave Module



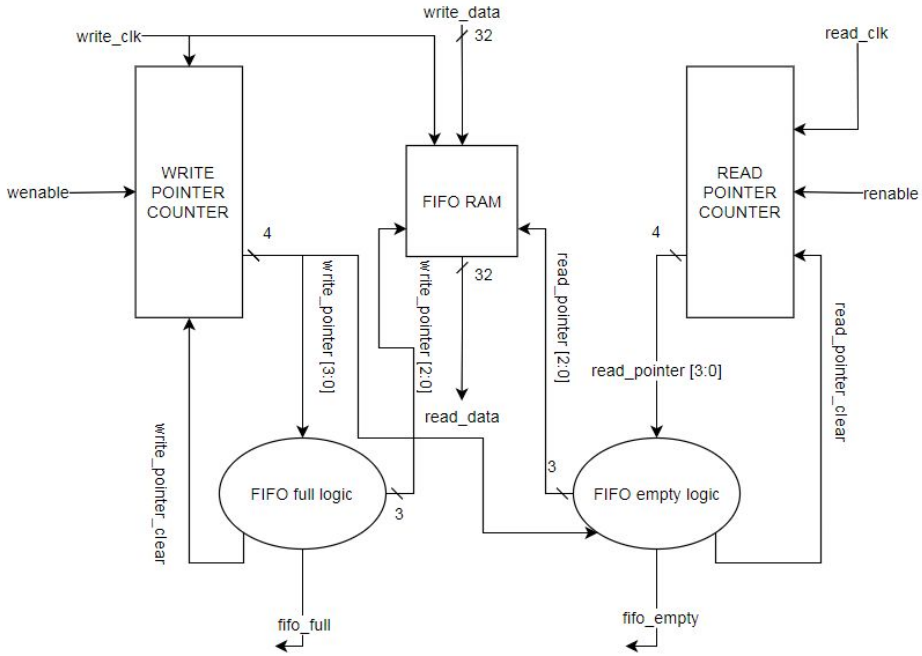
Slave Module State Machine



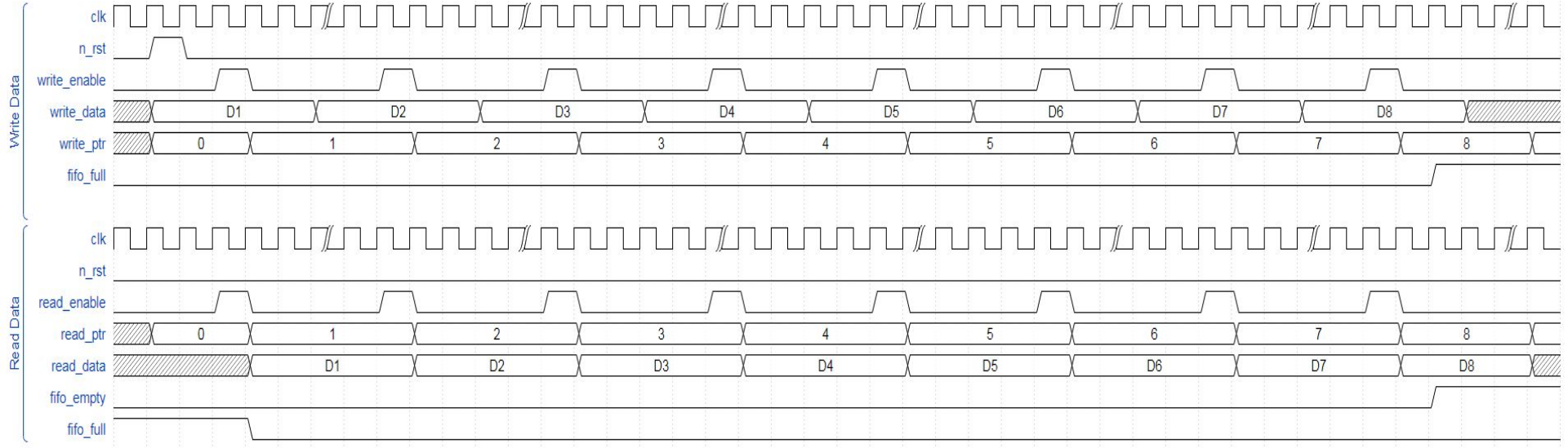
Timing Diagrams AHB Bus

FIFO Implementation

Functional Block Diagram For FIFO



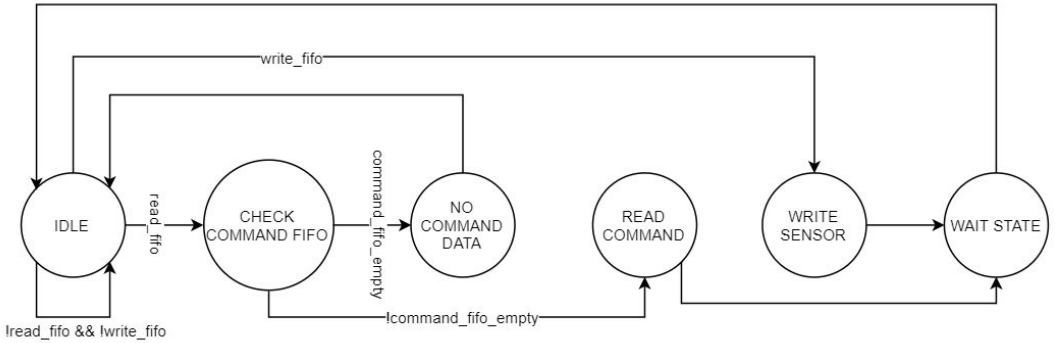
Timing Diagram for FIFO

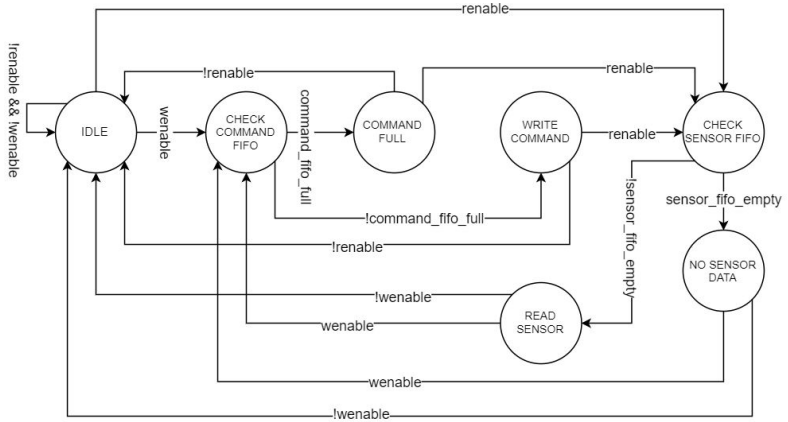


Sensor to Processor and Processor to Sensor Control Unit

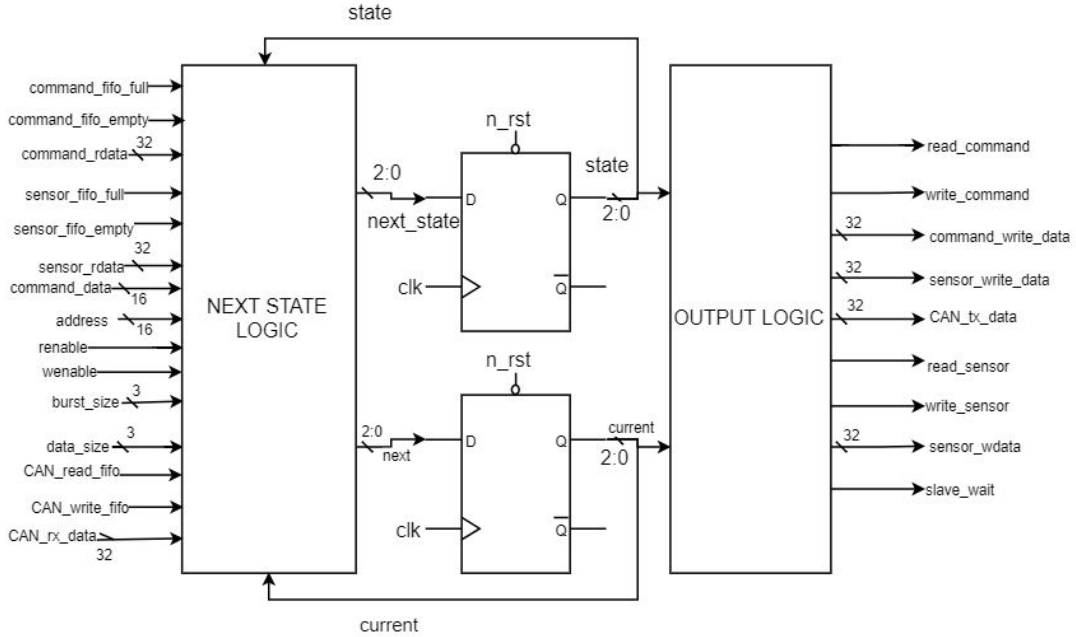
State Machine

- Requires 13 States
- 15 inputs
- 9 outputs





RTL Diagram


state
command_fifo_full
command_fifo_empty
command_rdata
32
sensor_fifo_full
sensor_fifo_empty
32
sensor_rdata
command_data
16
address
16
renable
wenable
burst_size
3
data_size
3
CAN_read_fifo
CAN_write_fifo
CAN_rx_data
32
NEXT STATE LOGIC
n_rst
2:0
next_state
D
Q
clk
Q
state
2:0
n_rst
2:0
next
D
Q
clk
Q
current
2:0
current
OUTPUT LOGIC
read_command
write_command
32
command_write_data
32
sensor_write_data
32
CAN_tx_data
read_sensor
write_sensor
32
sensor_wdata
slave_wait

Overall Design Budgeting (Estimate)

- 2x Fifo (slide 26): 524 regs + 126 logic gates = ~1,371,600(um^2)
- AHB Lite Master (slide 20): 35 regs + 60 gates = ~129,000(um^2)
- CAN bus (slide 14): 24 regs + 92 logic gates = ~127,450(um^2)
- Main control unit (slide 29) = 4 regs + 65 gates = ~58,350(um^2)

Timing Analysis

- From Receive Shift Register from CAN BUS to Sensor FIFO Storage
  - Approximately 1.5 ns
- From Command FIFO Storage to CAN BUS Transfer Shift Register
  - Approximately 2.0 ns
- From AHB-Lite Master to Command FIFO Storage
  - Approximately 2.4 ns
- From Sensor FIFO Storage to AHB-Lite Master
  - Approximately 2.4 ns
- From Main Control Unit To AHB-Lite Master (HRESP)
  - Approximately 2.2ns