

Operating RS-485 Transceivers at Fast Signaling Rates

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HPL-D - Interface

ABSTRACT

The TIA/EIA-485-A standard specifies characteristics for RS-485 signaling. Most applications operate below 10 Mbps but it is often possible to signal at higher rates. This application report examines the constraints on high-speed signaling and presents results using the SN65HVD10 transceiver as one example transceiver. Our method is to measure the eye patterns at the end of a 10-m cable under varying conditions. Signaling at rates up to 100 Mbps is demonstrated under limited circumstances. Signaling at 40 Mbps is possible with the SN65HVD05; eye patterns show how jitter increases for various lengths of cable.

Contents

1	Introduction	2
2	Receiver Operation at Fast Signaling Rates	2
3	Driver Operation at Fast Signaling Rates	4
4	Eye-Pattern Data – HVD10 Transceiver Only (No Cable Effects)	7
5	Effects of Cable on the Differential Signal.....	8
6	Results With a Typical Data Transmission System	9
7	Thermal Considerations	11
8	Conclusions	12
9	References	12

List of Figures

1	HVD10 Receiver Operation at 50 Mbps, With Less Than 200-mV Differential Input	3
2	Receiver Operation at 50 Mbps With $V_{ID} = 1$ V, Giving Little Pulse-Width Distortion.....	4
3	HVD10 Receiver Operating at 100 Mbps, With 1-V Input Amplitude	4
4	Temperature Variation of Typical HVD10 Driver Rise and Fall Times	5
5	HVD10 Driver Operating at 100 Mbps With Load of 50 Ω and 50 pF	6
6	HVD Driver and Receiver Operating at 50 Mbps.....	6
7	HVD Driver and Receiver Operating at 100 Mbps	7
8	Eye Pattern of the HVD10 Driver and Receiver With 50-Mbps Data	7
9	Eye Pattern of the HVD10 Driver and Receiver With 100-Mbps Data.....	8
10	Attenuation of the 50-Mbps HVD10 Driver Output Across a 10-Meter Cable	8
11	Detail of the Attenuation of 100-Mbps HVD10 Driver Output Signal Across a 10-Meter Length of CAT-5 Cable	9
12	Data Transmission Chain	9
13	Data Transmission of 50-Mbps Square Wave Across a 10-Meter CAT-5 Cable	10
14	Data Transmission of 100-Mbps Square Wave Across a 10-Meter CAT-5 Cable.....	10
15	Eye Pattern of HVD10 Data Transmission Across 10-Meter CAT-5 Cable With 50-Mbps Signaling Rate.....	11

List of Tables

1	Summary of Jitter vs Signaling Rate and Cable Length.....	9
2	Power Dissipation Comparisons	12

1 Introduction

The data sheets for some of Texas Instruments RS-485 transceivers specify signaling rates up to 30 Mbps. This is over all recommended operating conditions and with full compliance to the provisions of the ANSI/TIA/EIA-485-A standard.

Many applications do not require specification to all worst-case conditions of temperature, cable distance, power supply variation, etc. For these applications, it is often possible to signal at faster rates. This application report examines the constraints on high-speed signaling and demonstrates operation at speeds of 50 Mbps and faster.

The SN65HVD10 transceiver (hereafter referred to as the HVD10) is used as an example, but the basic discussions are valid for any of Texas Instruments RS-485 transceivers and line driver/line receiver circuits. ⁽¹⁾

The principal requirements for an RS-485 transceiver to operate at fast signaling rates are that the receiver must accurately detect valid signal levels on the bus, and the driver must successfully generate valid bus states. Another concern at fast signaling rates is that the transceiver dissipates more power than at slower rates.

⁽¹⁾ Several of Texas Instruments RS-485 devices include a feature which intentionally limits the driver slew rate. Although the basic discussions are still valid for these devices, drivers with slew-rate limiting are optimized for slower signaling rates.

2 Receiver Operation at Fast Signaling Rates

The ANSI/TIA/EIA-485-A standard requires a receiver to detect any differential bus voltage ($V_A - V_B$) with amplitude of greater than 200 mV as a valid data state. Therefore, the worst-case input for a receiver has amplitude of only 200 mV.

Figure 1 shows the HVD10 receiver detecting a differential bus signal consisting of a square wave with zero-to-peak amplitude of slightly less than 200 mV at nominal conditions ⁽²⁾. The signal frequency is 25 MHz, corresponding to a signaling rate of 50 Mbps. Although the HVD10 receiver output is changing state correctly in response to the bus signal, there is significant pulse-width distortion due to the offset in the HVD10 receiver thresholds. That is, the passive fail-safe feature requires that a 0-mV differential signal be detected as a known state. Therefore, the receiver thresholds (V_{IT+} and V_{IT-}) for the HVD10 are centered on -105 mV. Because the input signal is centered on zero and has finite edge transition times, more of the input signal is above the receiver threshold than is below it. This causes significant pulse-width distortion for the specific case of high data rates with low signal amplitudes.

⁽²⁾ All the following oscilloscope plots were taken at room temperature with V_{CC} set to 3.3 V.

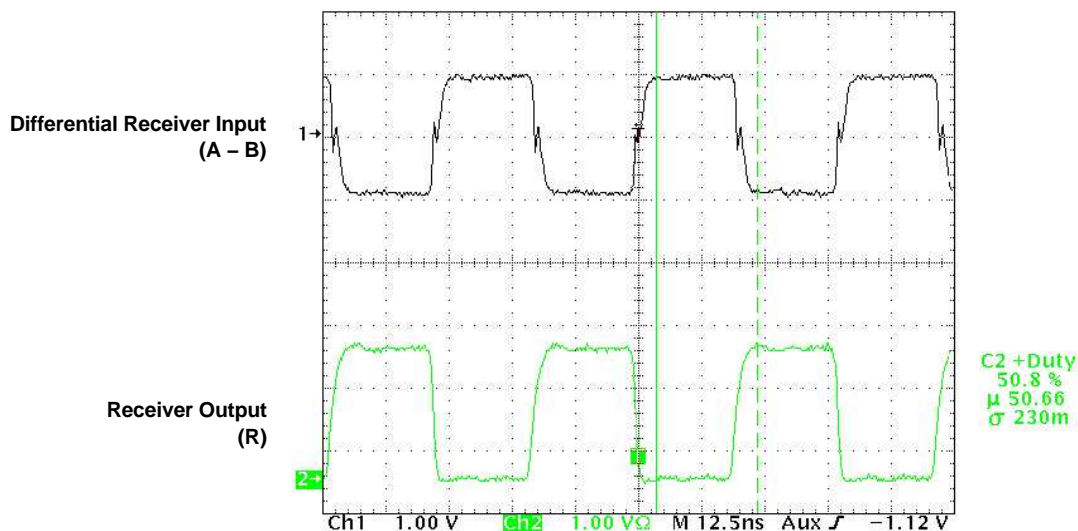


Figure 2. Receiver Operation at 50 Mbps With $V_{ID} = 1$ V, Giving Little Pulse-Width Distortion

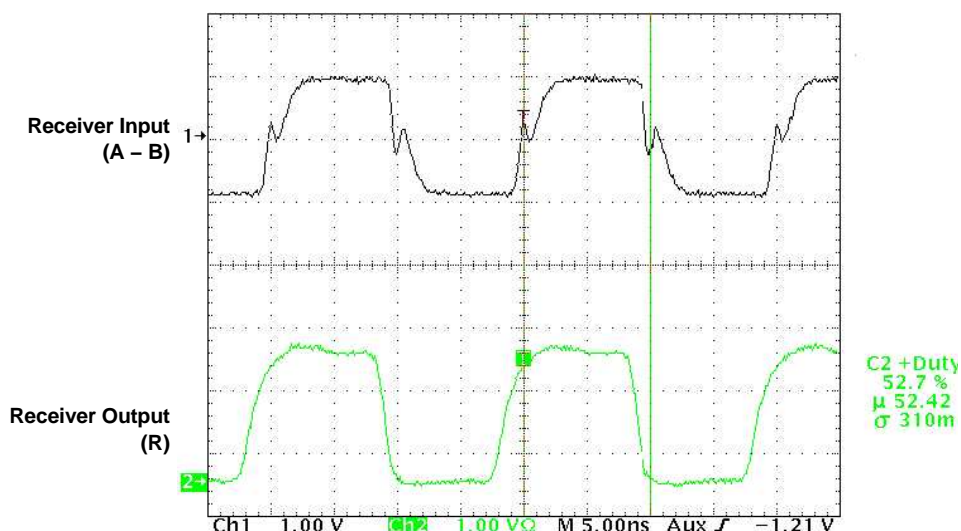


Figure 3. HVD10 Receiver Operating at 100 Mbps, With 1-V Input Amplitude

3 Driver Operation at Fast Signaling Rates

In order to comply with the TIA/EIA-485-A standard, a driver must meet several criteria. One of these is to generate balanced differential voltage levels. Another requirement restricts the 10%-to-90% transition time to 30% of the unit interval (bit time). Therefore, there is an inverse relationship between the driver output rise and fall times and the maximum achievable signaling rate.

Under all recommended operating conditions, the HVD10 driver is specified to have rise and fall times not exceeding 10 nanoseconds. This corresponds to a maximum achievable signaling rate (for ALL recommended operating conditions) of 30 Mbps. However, reasonable assumptions can be made which extend the possible signaling rate for many applications

One reasonable assumption is that in some applications the driver may not be subjected to the entire temperature range for which the HVD10 is specified. The HVD10 is available in different temperature grades:

Different Temperature Grades	
SN75	0°C to 70°C
SN65	–40°C to 85°C
SN65_Q	–40°C to 125°C

As can be seen from the curves shown in Figure 4, the rise and fall times for the HVD10 driver typically are well below 8 nanoseconds. If the application does not encounter temperatures below 0°C, a time of 7.5 nanoseconds seems reasonable. System designers should expect that signaling rate performance will show a similar sensitivity to temperature. Note that a rise/fall time of 7.5 nanoseconds corresponds to an RS-485 signaling rate of 40 Mbps

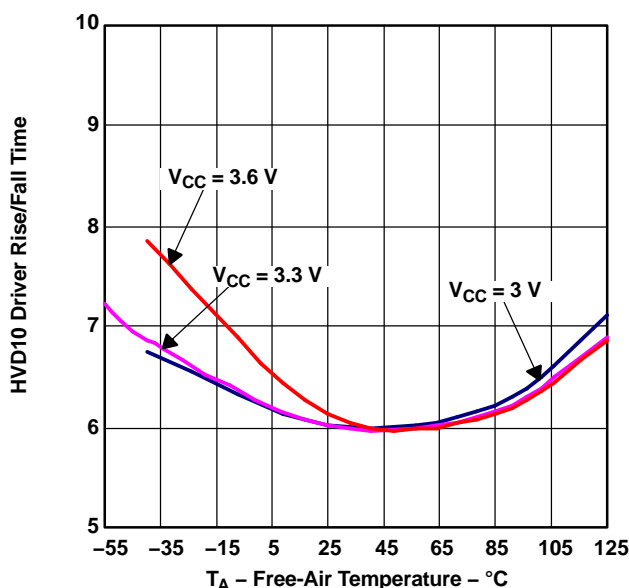


Figure 4. Temperature Variation of Typical HVD10 Driver Rise and Fall Times

For signaling rates beyond 40 Mbps, it may be feasible in some applications to increase the fraction of bit time allowed for the signal transition. If the standard 30% constraint is relaxed, the HVD10 can exhibit signaling rates up to 100 Mbps. The system designer must decide if the corresponding decrease in timing margin is acceptable.

Figure 5 shows the driver performance at 100 Mbps when loaded with 50 Ω and 50 pF across the differential driver outputs. Note that the 10%-to-90% rise time is reasonably consistent with the data shown in Figure 4. Based purely on the shape of this waveform, most designers would not accept this as a reliable data signal. Certainly, the driver output waveform does not meet the requirements of the TIA/EIA standard.

If the details of the data transmission path are examined closely, it can be seen that several possible trade-offs may allow faster signaling rates with these transceivers. One consideration is whether the system of interest is best modeled with the test loading. Another consideration is whether the signal reaching the receiver has sufficient amplitude that the receiver thresholds are always reliably exceeded and sufficient setup and hold time is available.

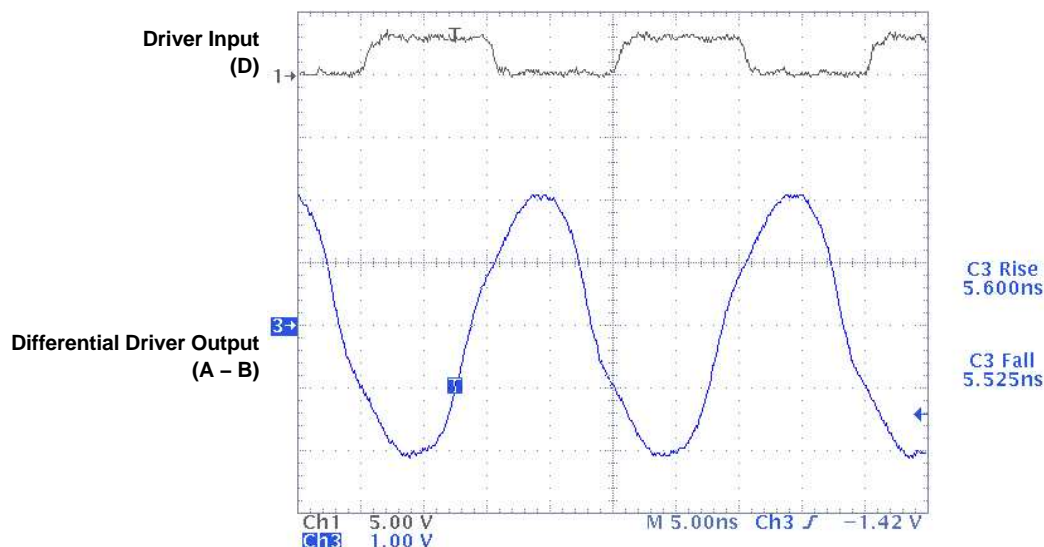


Figure 5. HVD10 Driver Operating at 100 Mbps With Load of 50 Ω and 50 pF

To illustrate the first consideration, Figure 6 and Figure 7 show the outputs of a driver and a receiver, with negligible cable length connecting them. Note that in these cases there is only the 51 Ω load and the capacitance of the test board, cable, and connectors across the outputs. Comparing Figure 7 to Figure 5, it is obvious that the load capacitance plays a significant role in signal transition time and quality, affecting the maximum possible signaling rate. Therefore, it is important to model the system of interest in terms of load capacitance. Subsequent sections discuss the results with actual cable, rather than with a lumped capacitive load. In Figure 6 and Figure 7, channel 1 is the differential driver output with a 51- Ω load, and channel 2 is the receiver output.

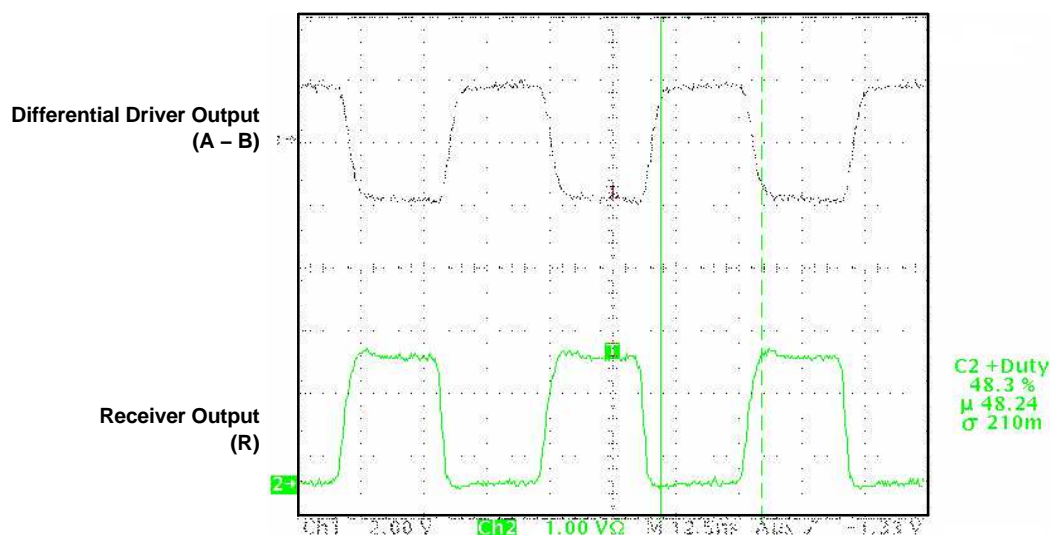


Figure 6. HVD Driver and Receiver Operating at 50 Mbps

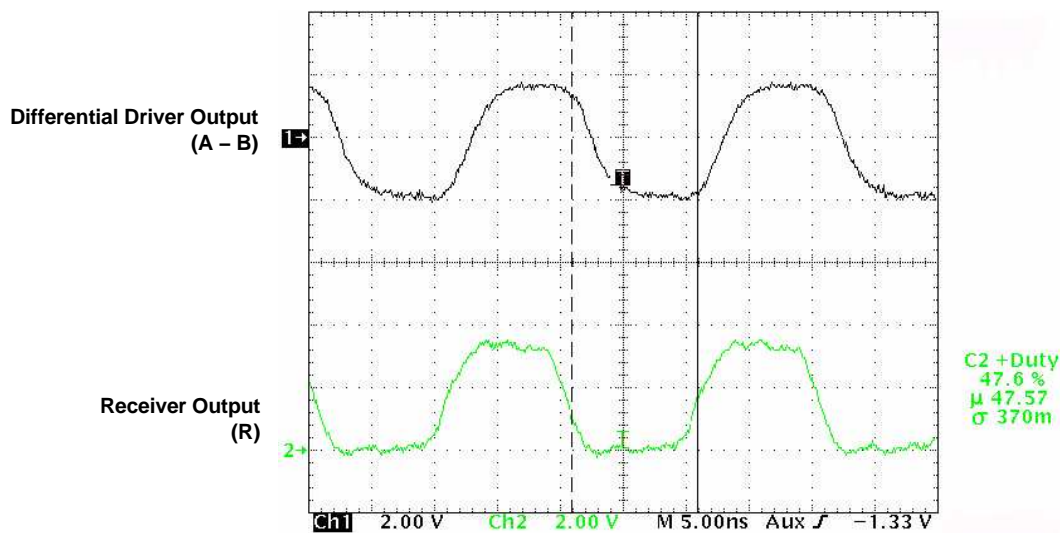


Figure 7. HVD Driver and Receiver Operating at 100 Mbps

4 Eye-Pattern Data – HVD10 Transceiver Only (No Cable Effects)

One measure of system performance at high signaling rates is data signal jitter. Eye patterns⁽¹⁾ can be used to visualize the jitter at various points in the system. Jitter at the driver output is one component of total system jitter. Figure 8 and Figure 9 illustrate that the HVD10 contributes a small amount of jitter at 50 Mbps, and a larger contribution at signaling rates of 100 Mbps. Channel 1 is the driver output; channel 2 is the receiver output.

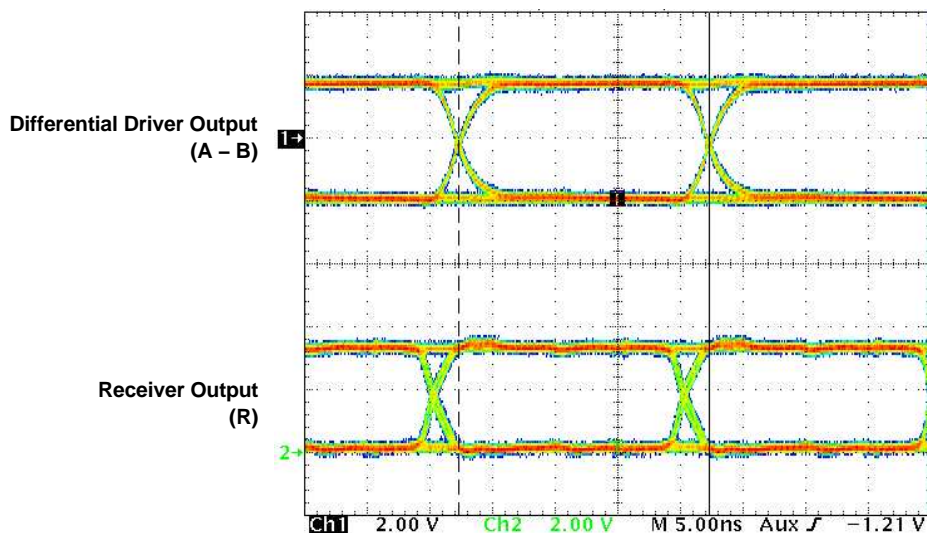


Figure 8. Eye Pattern of the HVD10 Driver and Receiver With 50-Mbps Data

⁽¹⁾ For a discussion of eye-pattern measurements, see Section 4 of Texas Instruments application report, *Interface Circuits for TIA/EIA-485 (RS-485)* (SLLA036)

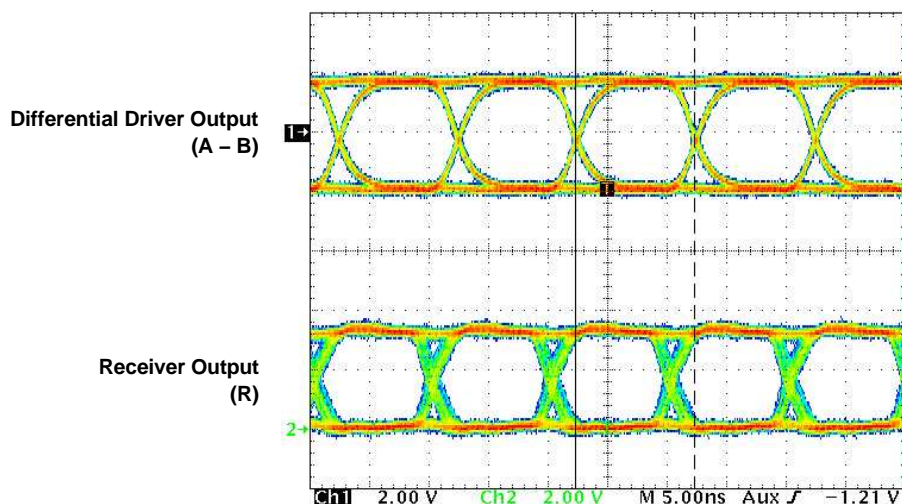


Figure 9. Eye Pattern of the HVD10 Driver and Receiver With 100-Mbps Data

5 Effects of Cable on the Differential Signal

Another variable to be considered is the effect of the transmission media (cable, connectors, and circuit board traces) on the differential signal. The RS-485 standard is intended for applications with cable lengths up to 1200 meters. Long cable applications can have significant signal attenuation between the driver and receiver. This is the basis for the large margins between driver output amplitude (at least 1.5 V) and receiver input sensitivity (200 mV or smaller)

For applications with shorter cable lengths, the signal attenuation is less significant, and the receiver may see a large fraction of the amplitude generated by the driver. See [Figure 10](#) and [Figure 11](#), which show operation with a 10-meter cable. In these figures, channel 1 shows the differential voltage at the output of the HVD10 driver, and channel 2 shows the differential voltage which reaches the other end of the cable.

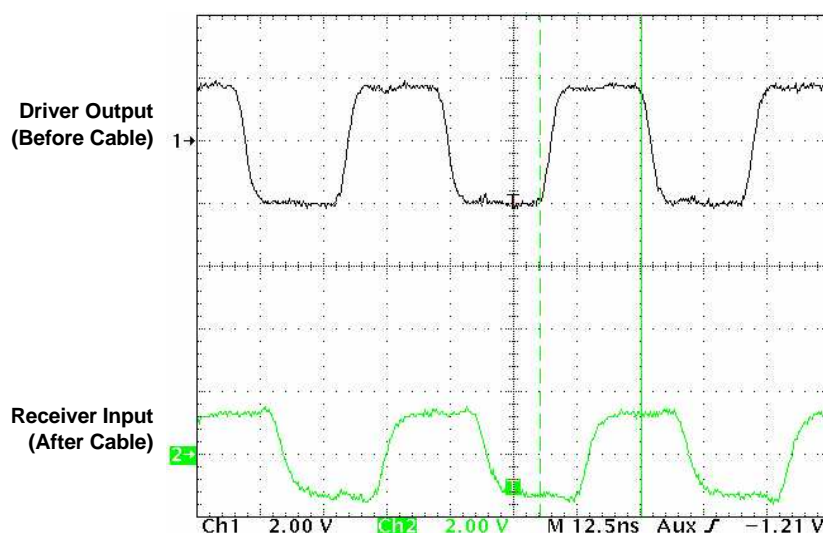


Figure 10. Attenuation of the 50-Mbps HVD10 Driver Output Across a 10-Meter Cable

For all applications, the dependence on the overall driver rise and fall time is of less importance than the transition time through the receiver threshold region. Examining the details of Figure 11 shows that although the overall rise and fall times of the differential signal at the receiver are relatively slow, the time of transition through the -200-mV to 200-mV receiver threshold window is much shorter. This implies that because the signal amplitude is large, the receiver sensitivity helps recover the original signal with less degradation than if a long cable were used.

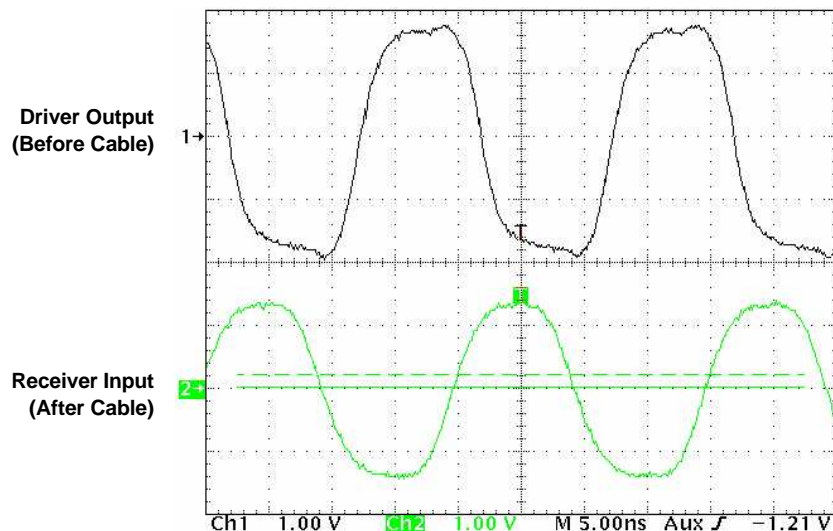


Figure 11. Detail of the Attenuation of 100-Mbps HVD10 Driver Output Signal Across a 10-Meter Length of CAT-5 Cable

Table 1 shows how jitter varies as a function of cable length and signaling rate. Here, the driver and receiver were SN65HVD05 devices, which are RS-485 transceivers similar in design to the HVD10.

Table 1. Summary of Jitter vs Signaling Rate and Cable Length

SIGNALING RATE (Mbps)	CABLE LENGTH (Belden Mediatwist 1872A)		
	10 METERS	30 METERS	80 METERS
40	3%	9%	24%
60	5%		
80	20%		
100	35%		

6 Results With a Typical Data Transmission System

Figure 12 shows a simple diagram of a typical data transmission chain. Although only one driver and one receiver are shown, the following results can be extended to a more complex system.

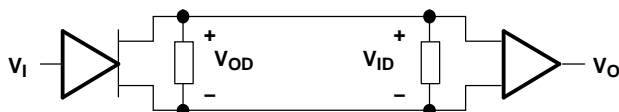


Figure 12. Data Transmission Chain

Figure 13 illustrates the signals throughout the entire data transmission chain with a signaling rate of 50 Mbps. The transmission path was an unshielded, twisted-pair wire (Belden 1583A CAT-5) terminated at

Results With a Typical Data Transmission System

each end with an approximate 100- Ω resistor. Channel 1 is the TTL input to the driver, and channel 2 shows the differential driver output. Channel 3 shows the differential signal that reaches the input to the HVD10 receiver after the 10-meter length of cable. Note that the signal that reaches the receiver has been attenuated, especially the high-frequency components, reducing both the amplitude and the edge rates. Channel 4 shows the output of the receiver.

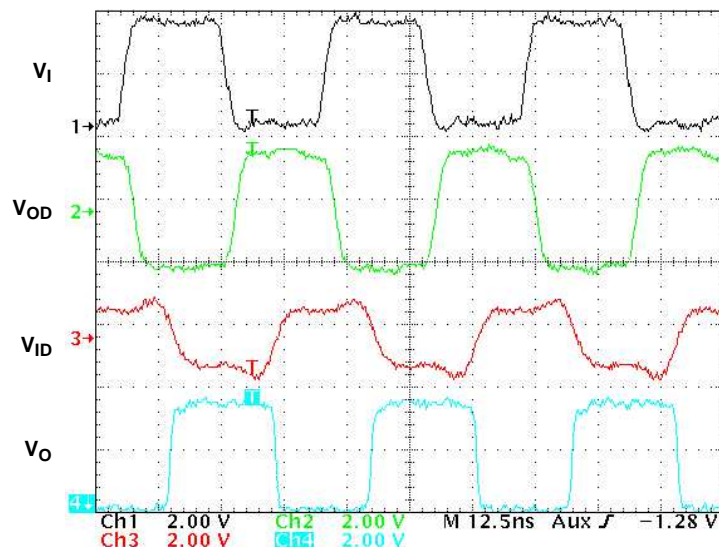


Figure 13. Data Transmission of 50-Mbps Square Wave Across a 10-Meter CAT-5 Cable

Although the transmission channel has degraded the signal, the final digital signal matches the original input. This illustrates that the HVD10 can achieve signaling rates of 50 Mbps. Signaling rates as high as 100 Mbps are possible, as shown in Figure 14.

Figure 14 shows the operation at 100 Mbps through the same signal chain as previously described. Here, the input signal to the receiver appears more as a sinusoid than a square wave, due to the combined effects of the driver's finite rise and fall times, and the high-frequency attenuation of the cable

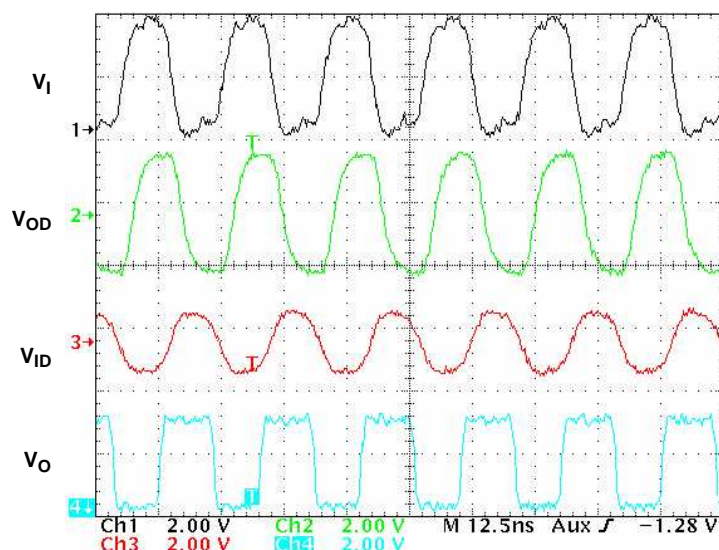


Figure 14. Data Transmission of 100-Mbps Square Wave Across a 10-Meter CAT-5 Cable

In spite of the appearance of the receiver's input, the receiver output is a reasonable square wave, reflecting the original signal at the source of the driver. This indicates that 100-Mbps data transmission is possible using the HVD10 transceiver.

Practically, the square-wave signals (clock signals) shown in Figure 13 and Figure 14 are not representative of most RS-485 applications. A more general signal is represented by a pseudo-random bit stream (PRBS) of binary data. Such a PRBS signal typically includes all significant combinations of bits and is used to generate an *eye pattern* as a measure of data transmission system quality.

The oscilloscope traces in Figure 15 illustrate successful 50-Mbps data transmission using two HVD10 transceivers and a cable length of 10 meters. The signal was a PRBS. Channel 1 shows the TTL input to the driver; channel 2 shows the differential driver output. Channel 3 shows the differential signal that reaches the input to the HVD10 receiver and channel 4 shows the TTL output of the receiver.

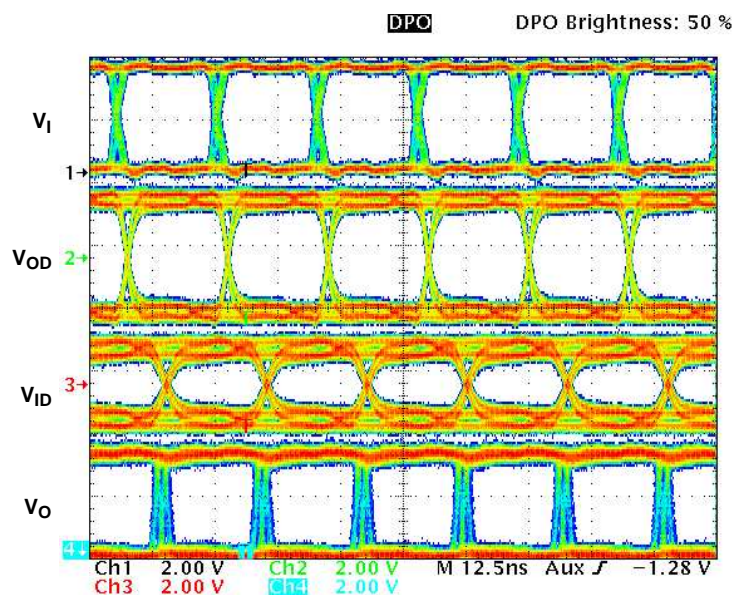


Figure 15. Eye Pattern of HVD10 Data Transmission Across 10-Meter CAT-5 Cable With 50-Mbps Signaling Rate

7 Thermal Considerations

Power dissipation and thermal issues must always be considered, especially in industrial applications where RS-485 transceivers are commonly used. Designers for fast-signaling rate applications should pay close attention to the increased power dissipation inherent in those cases.

In a data bus network, power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS-485 bus configuration, the steady-state load that an active driver must drive consists of all the receiving nodes, plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of each receiver. The TIA/EIA-485-A standard defines a unit load⁽¹⁾ allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. Many transceivers now are designed with reduced unit loading; for example, the HVD10 is a 1/2-unit-load device, and the SN65HVD3088E is rated as a 1/8 unit-load device. These reduced unit-loading devices have correspondingly lower input current.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25 mA in the termination resistors whenever the bus is active. Texas Instruments transceivers typically can drive more than 25 mA to a 60-Ω load, resulting in a differential output voltage higher than the minimum required by the standard.

Overall, the total steady-state load current can typically be 60 mA to a fully loaded RS-485 bus. This is in addition to the current required by the transceiver.

⁽¹⁾ For more details on the unit load, see TI application report *The RS-485 Unit Load and Maximum Number of Bus Connections*, (SLLA166).

Conclusions

Supply current increases with signaling rate primarily due to the totem-pole outputs of the driver. When these outputs change state, for a moment, both the high-side and low-side output transistors are conducting. This creates a short spike in the supply current. As the frequency of state changes increases, more power is used as these short spikes of current occur more frequently, leading to a marked increase in the overall power dissipation.

A secondary increase in power consumption occurs due to capacitive effects. The capacitive elements are found both internal to the transceiver and in the external load. The external load capacitance is often modeled as a lumped 50 pF, as shown in the data sheet test circuit schematics. This 50 pF represents test fixture and instrumentation capacitance because the inductance of the short interconnect is negligible. The internal capacitance is due to the transceiver circuitry and is typically approximately 5 pF to 10 pF.

[Table 2](#) illustrates how power dissipation is affected by signaling rate, as well as by the mode of operation. In each case, the maximum power dissipation takes into account variations in power supply, temperature, etc., while the typical values reflect the power dissipation under nominal conditions.

Table 2. Power Dissipation Comparisons

SIGNALING RATE	DRIVER LOAD	RECEIVER LOAD	MODE	TRANSCIEVER POWER DISSIPATION
100 Mbps	60 Ω, 50 pF	15 pF	Driver enabled and Receiver enabled	387 mW (maximum)
50 Mbps			Driver enabled and Receiver enabled	296 mW (maximum)
32 Mbps			Driver enabled and Receiver enabled	256 mW (maximum)
			Driver enabled and Receiver disabled	245 mW (maximum)
			Driver disabled and Receiver enabled	32 mW (maximum) 20 mW (typical)
25 Mbps			Driver enabled and Receiver enabled	233 mW (maximum) 198 mW (typical)

Designers should take the higher power dissipation at fast signaling rates into account. For additional information on thermal design, see the individual device data sheets and Texas Instruments application notes *IC Package Thermal Metrics* ([SPRA953](#)) and *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* ([SZZA017](#)).

8 Conclusions

Texas Instruments data sheets are intentionally conservative in regard to the highest possible signaling rate and the signal-quality requirements of TIA/EIA-485-A. The HVD10 transceiver can successfully operate at fast signaling rates, up to 50 Mbps or even 100 Mbps. The system designer must consider limiting constraints, such as compliance to RS-485 standards, application temperature, and cable effects when determining how far to push the envelope in terms of signaling rate.

Similarly, system designers must consider the parametric limitations of other RS-485 devices in extending the performance beyond worst-case minimums. Depending on the application, signaling rates significantly higher than the minimum claims may be possible. The ultimate top signaling rate can only be determined at the final installation.

9 References

1. *Interface Circuits for TIA/EIA-485 (RS-485)* application report ([SLLA036](#))
2. *The RS-485 Unit Load and Maximum Number of Bus Connections* application report ([SLLA166](#))

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