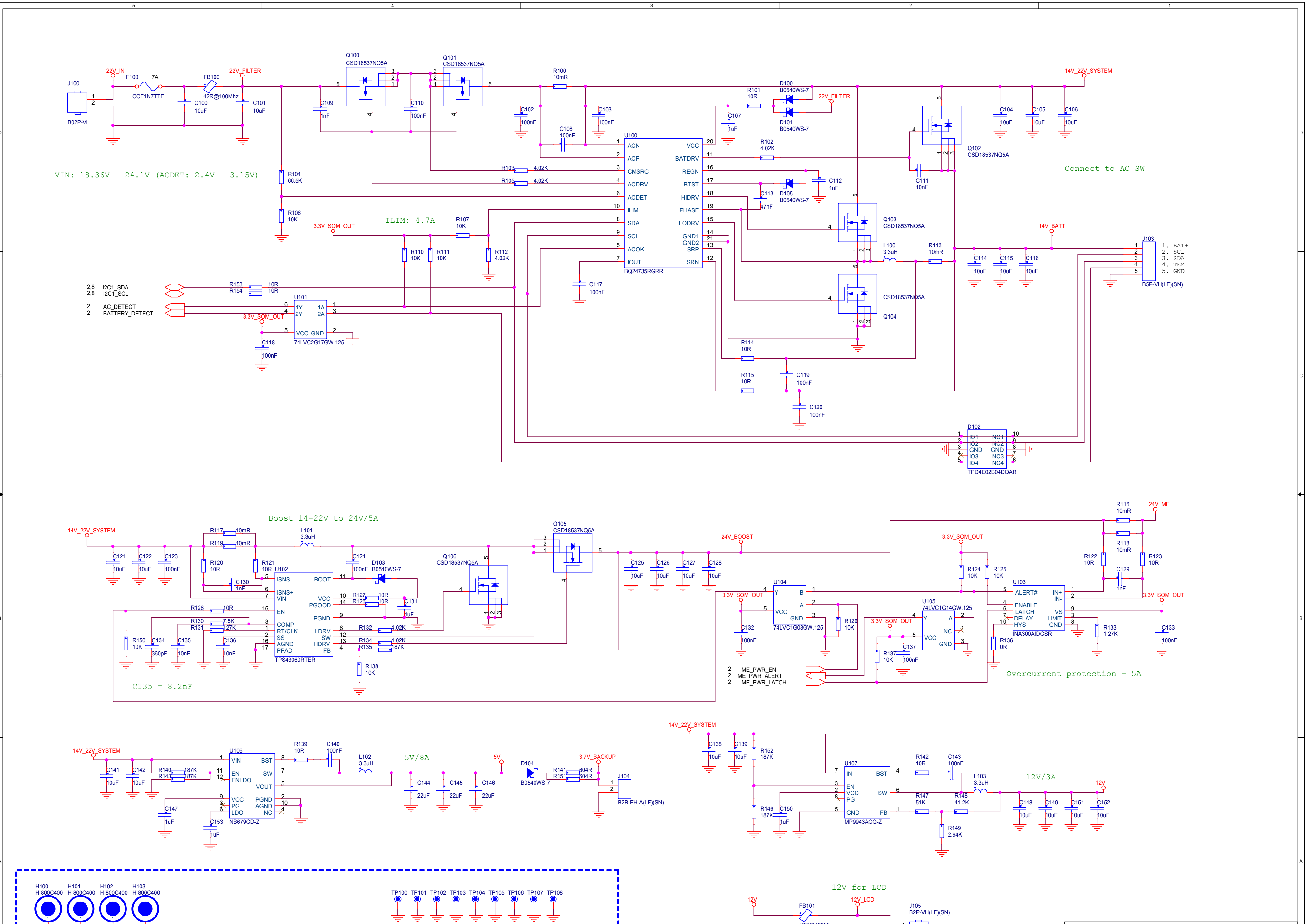
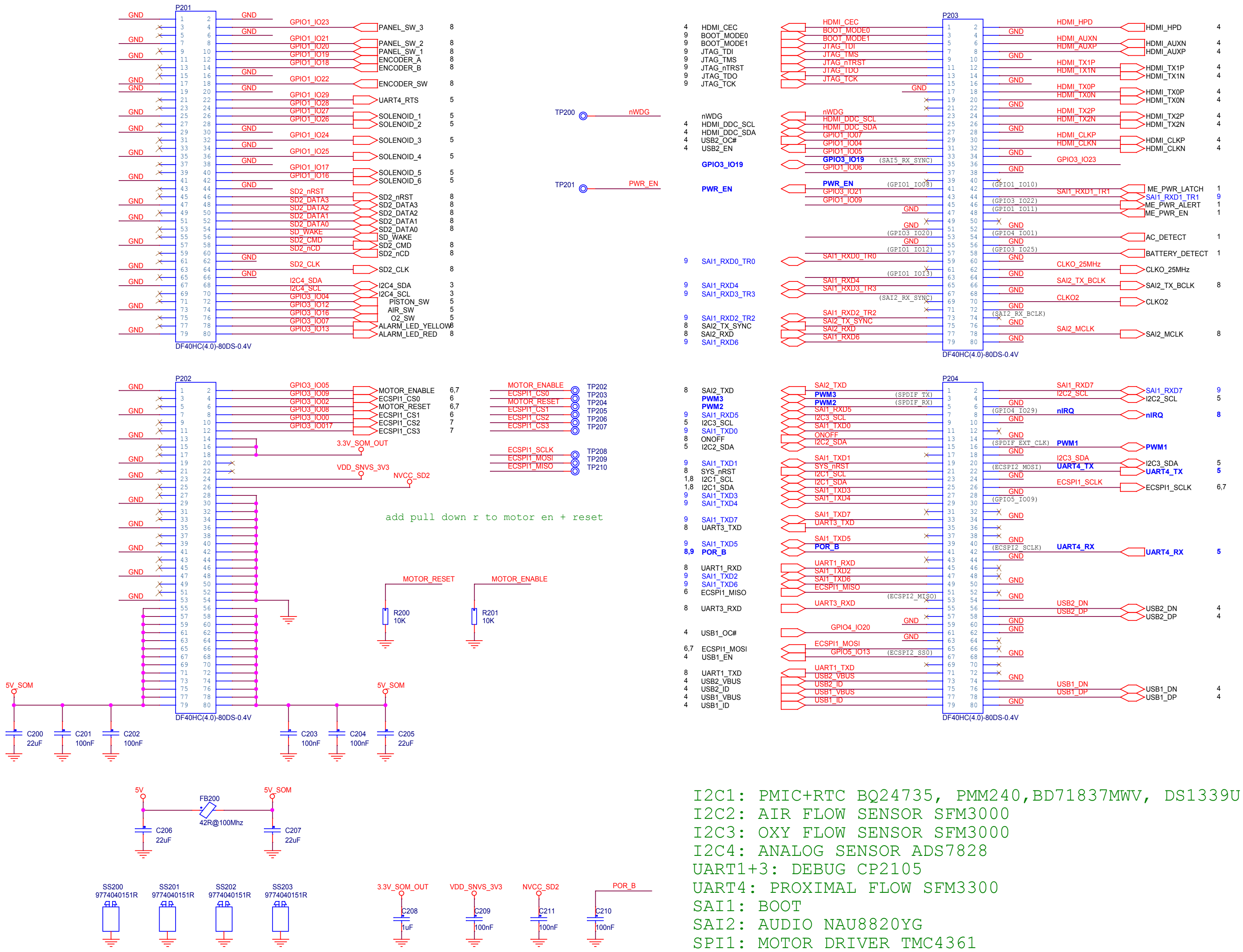


Title		
	NewVueLPC	
Size C	Document Number Power Supply	Rev 1.0
Date:	Sunday, December 30, 2018	Sheet 1 of 9

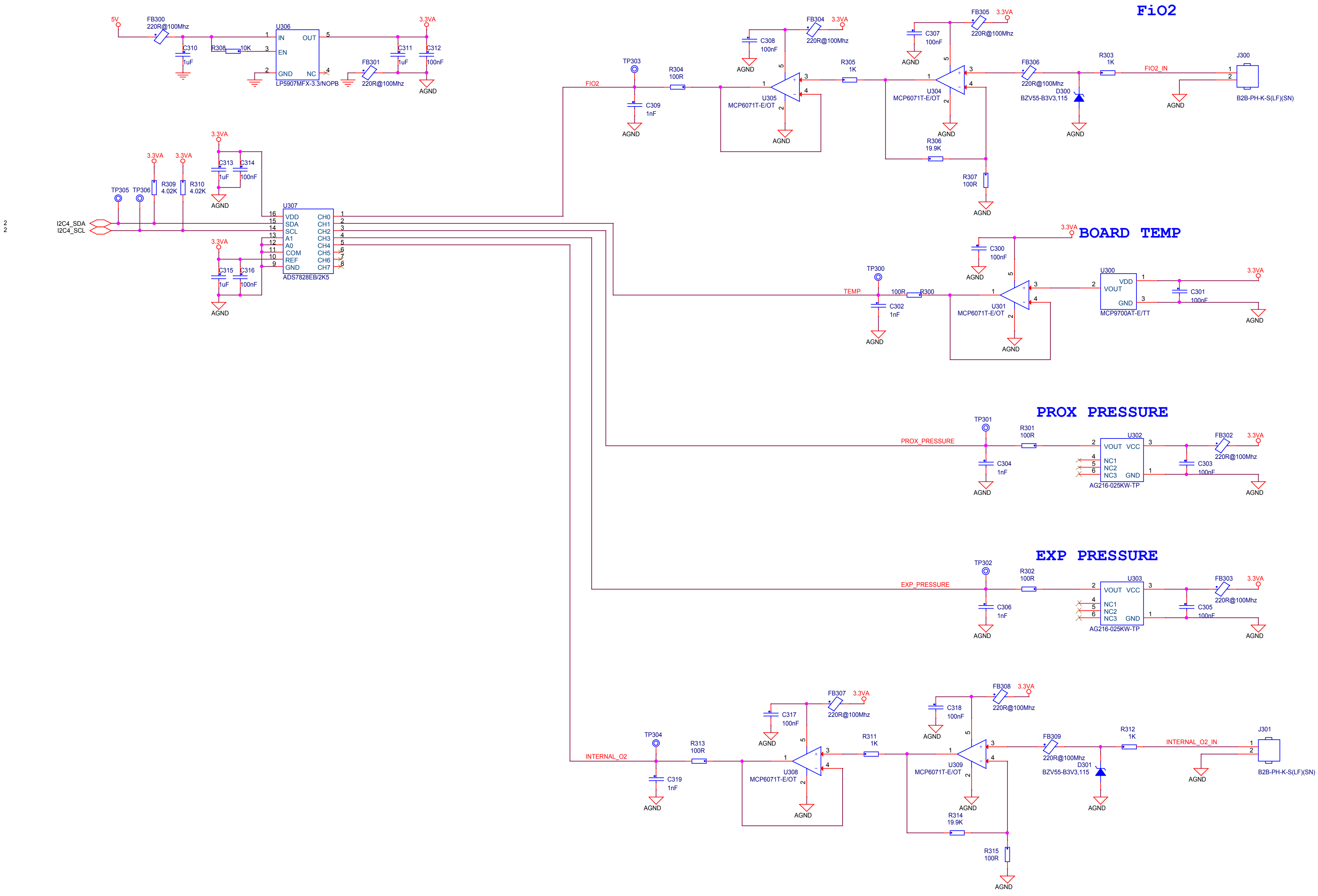


add pull down r to motor en + reset

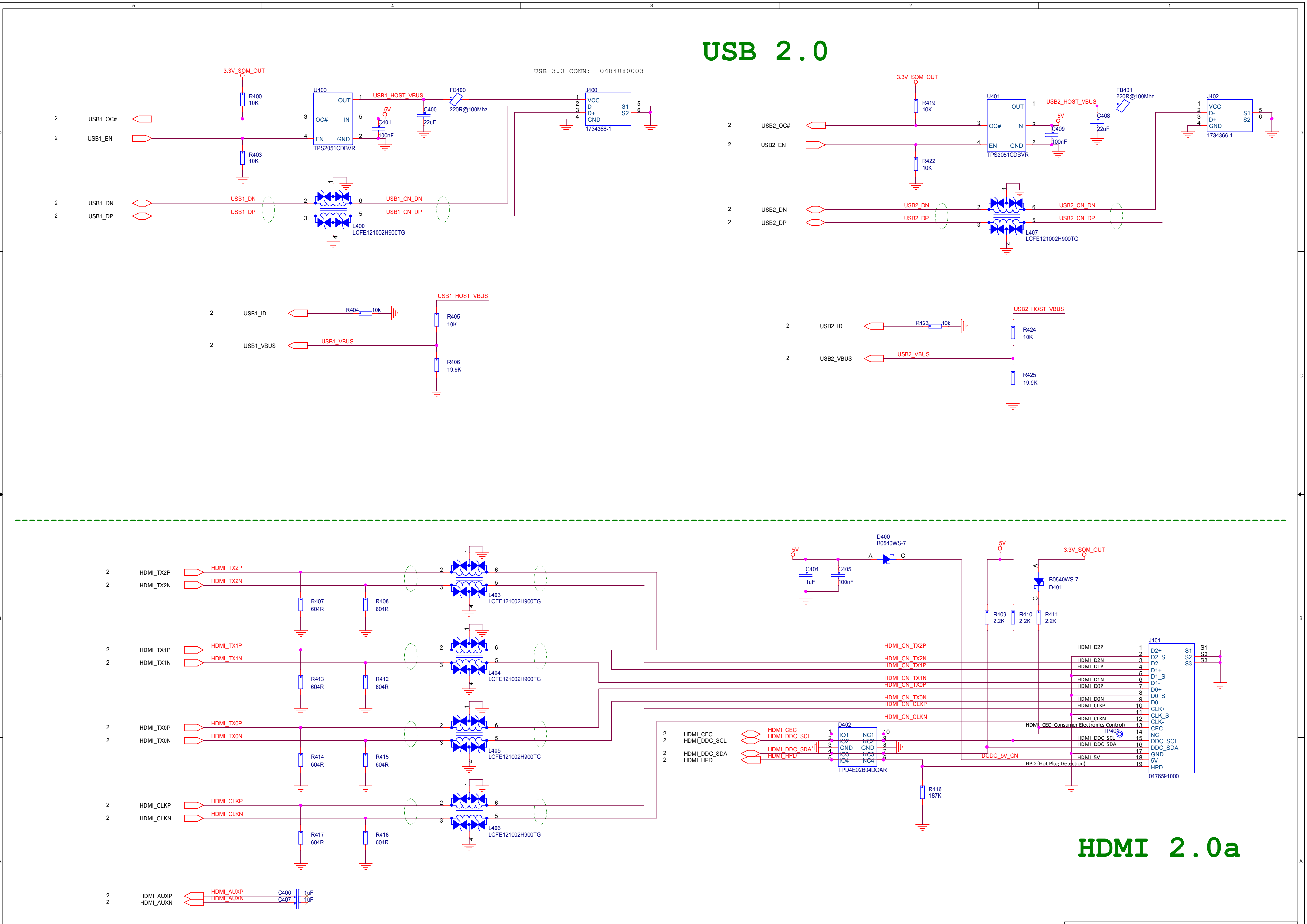
I2C1: PMIC+RTC BQ24735, PMM240,BD71837MWV, DS1339U
I2C2: AIR FLOW SENSOR SFM3000
I2C3: OXY FLOW SENSOR SFM3000
I2C4: ANALOG SENSOR ADS7828
UART1+3: DEBUG CP2105
UART4: PROXIMAL FLOW SFM3300
SAI1: BOOT
SAI2: AUDIO NAU8820YG
SPI1: MOTOR DRIVER TMC4361

Place all the standoffs and connectors according the SOM layout (Sa717.001a)

Title	NewVue2018		
Size C	Document Number CPU		Rev 1.0
Date: Wednesday, January 02, 2019	Sheet 2	of 9	

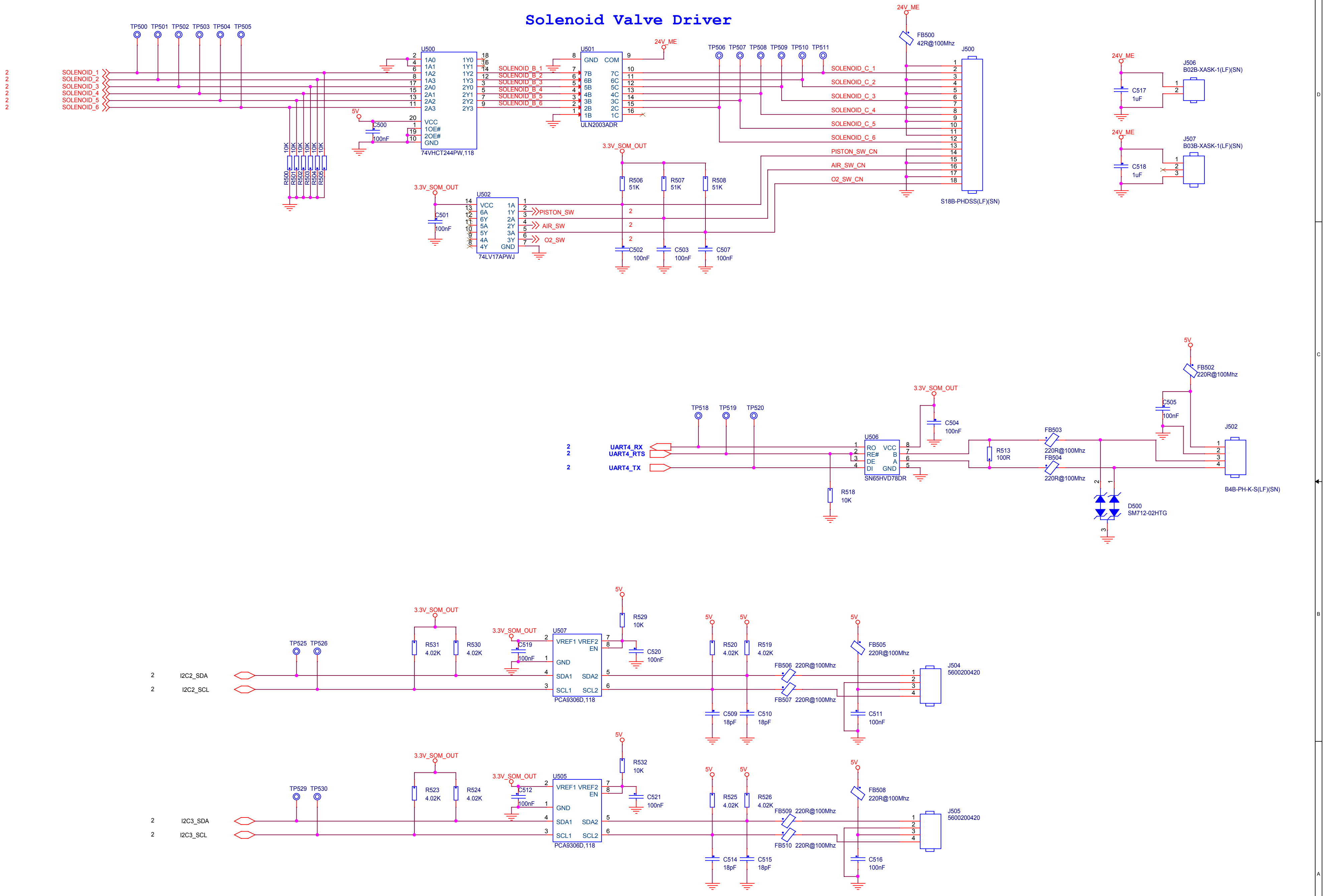


Title NewVueLPC		
Size C	Document Number Sensor	Rev 1.0
Date: Wednesday, January 02, 2019	Sheet 3 of 9	

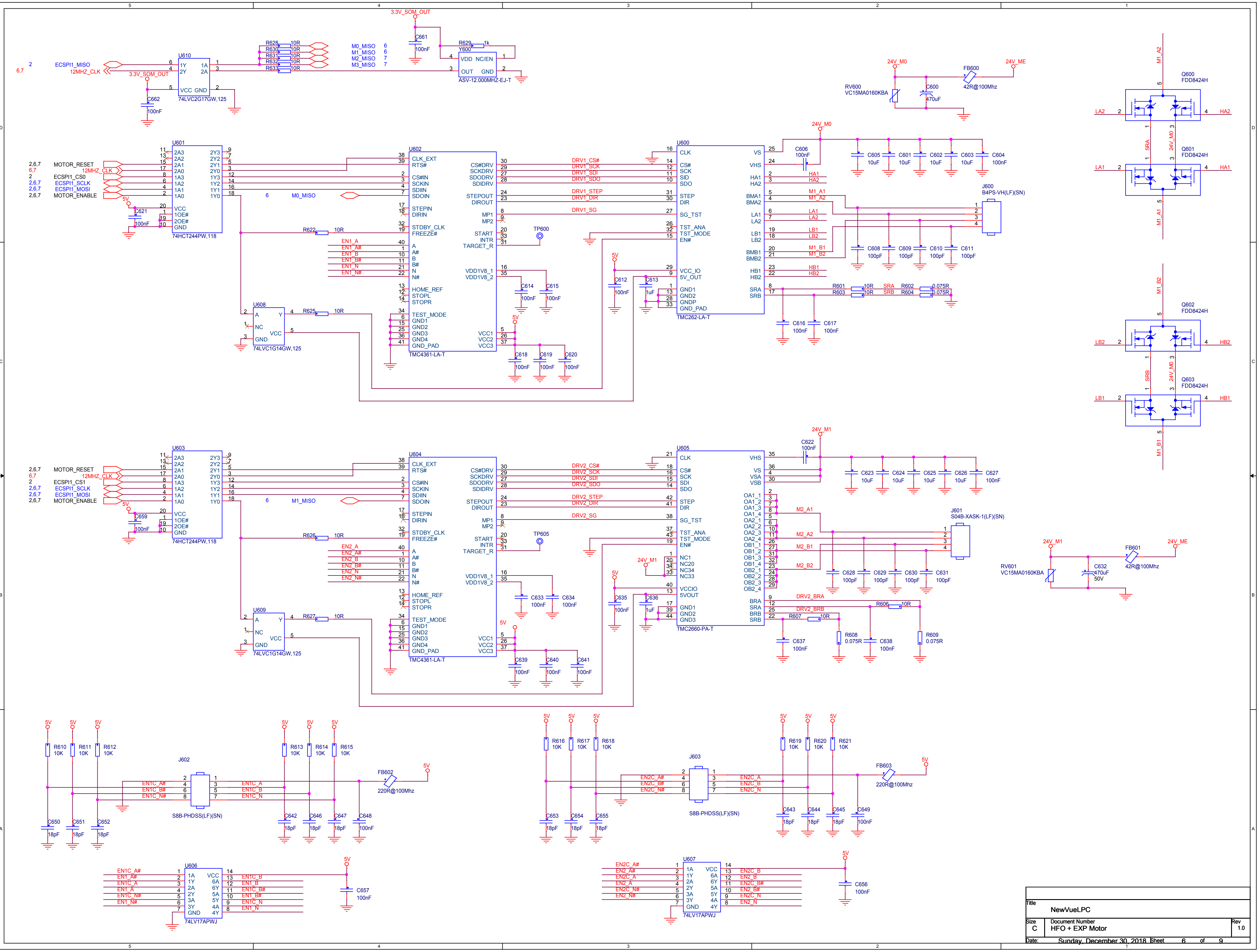


Title NewVueLPC		
Size C	Document Number USB	Rev 1.0
Date: Saturday, December 29, 2018	Sheet 4 of 9	

Solenoid Valve Driver



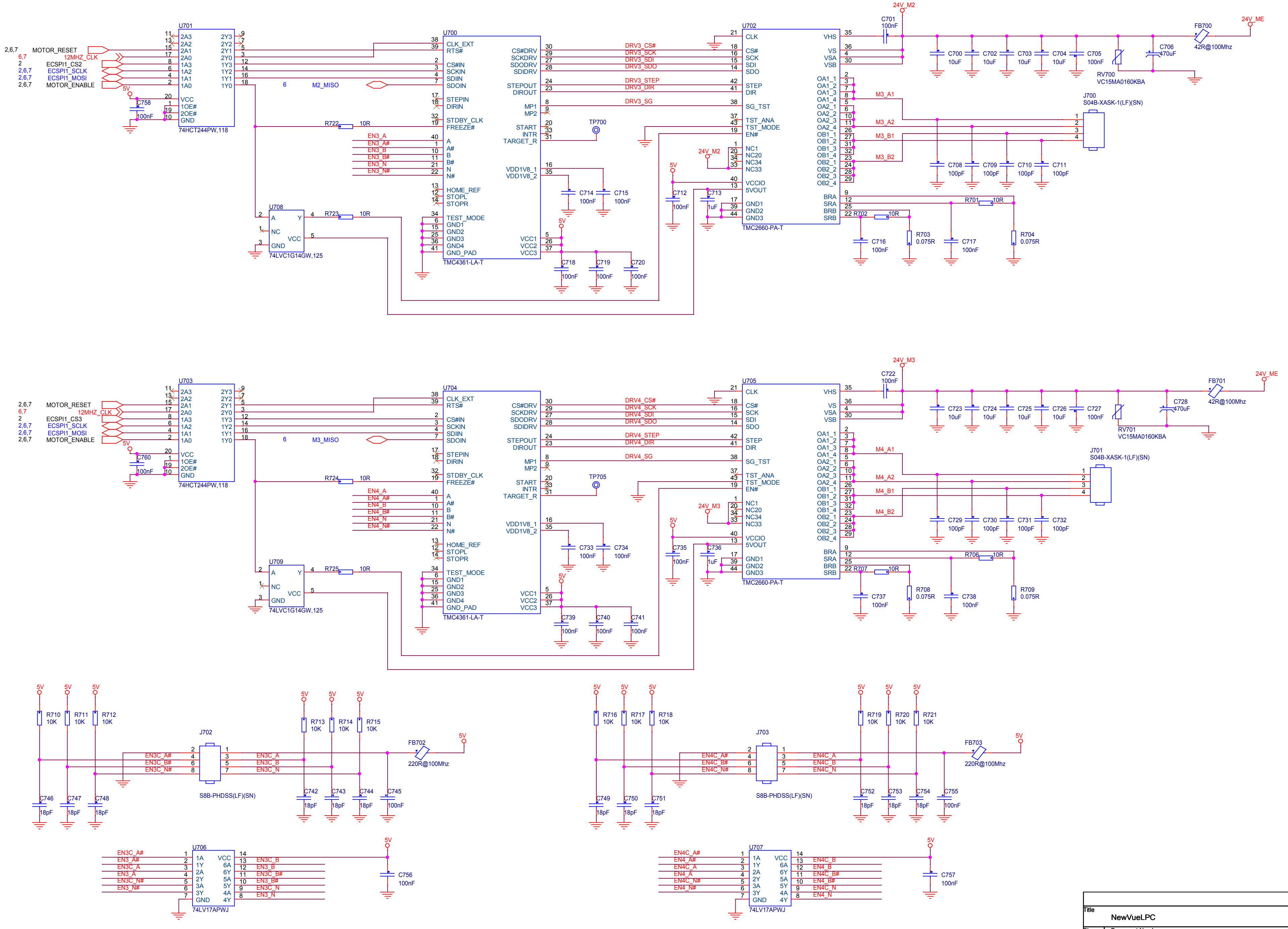
Title	NewVueLPC	
Size C	Document Number Devices	Rev 1.0
Date: Sunday, December 30, 2018	Sheet 5 of 9	



Title
NewVueLPC

Size	Document Number	Rev
C	HFO + EXP Motor	1.0

Date: Sunday, December 30, 2018 Sheet 6 of 9



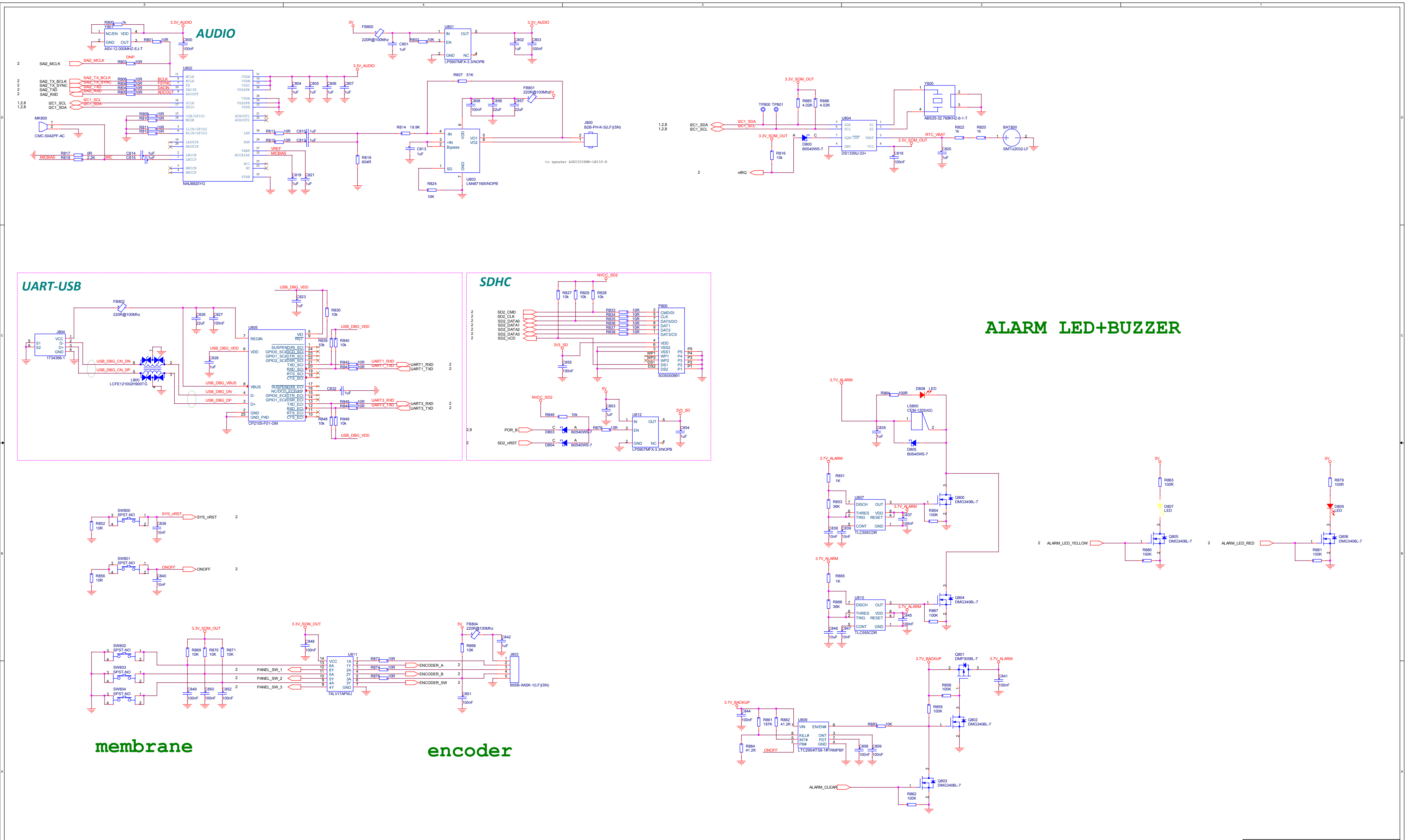
Title
NewVueLPC

Size C

Document Number
Air + O2 Motor

Rev 1.0

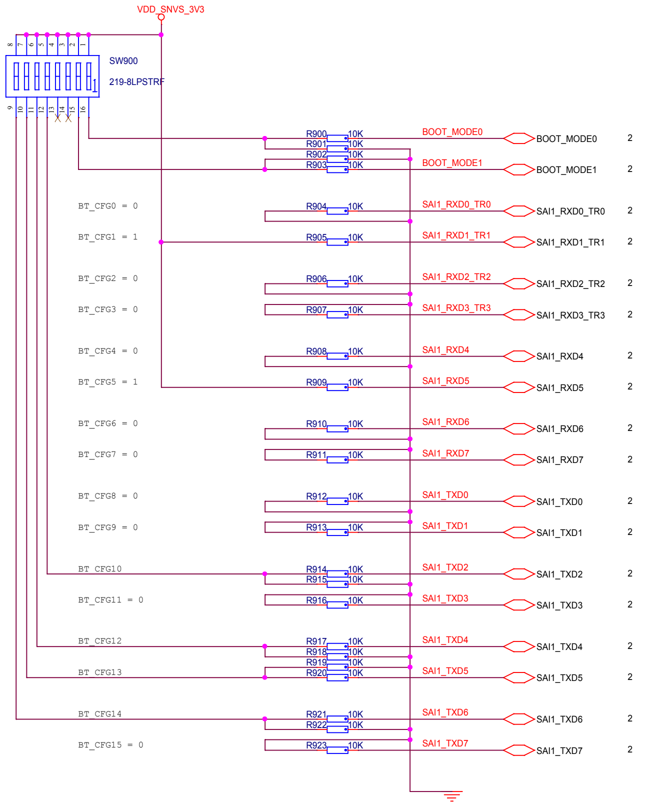
Date: Sunday, December 30, 2018 Sheet 7 of 9



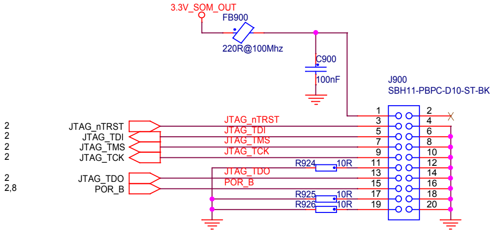
Title		
NewVueLPC		
Size D	Document Number <Doc>	Rev 1.0
Date: Sunday, December 30, 2018	Sheet 8 of 9	

iMX8M Boot Configs

	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	**BOOT_CFG[15]**	**BOOT_CFG[14]**	**BOOT_CFG[13]**	**BOOT_CFG[12]**	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**
	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - eSDHC1 01 - eSDHC2		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			QSPI Instance 0 - QuadSPI0 1 - Reserved	SDR SMP: "000" : Default "001-111"		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC1 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	USDHC2 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.				Reserved
QSPI	0x470[7:0]	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0 : one clock delay 1: two clock delay	Reserved	Reserved	Reserved	Reserved
SPINOR	0x470[7:0]	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved



NOTE:
1. Place tables BOOT TYPE and BOOT CFG on the bottom silkscreen layer
2. It is possible to reorder the nets with purpose to simplify layout
In case of reorder, please provide the schematic for review



JTAG

BOOT TYPE	**SW1**	**SW2**
Boot From Fuses	0	0
Serial Downloader	0	1
Internal Boot (Development)	1	0
Reserved	1	1

BOOT CFG	**SW5**	**SW6**	**SW7**	**SW8**
EMMC	0	0	1	0
SD	1	1	0	0