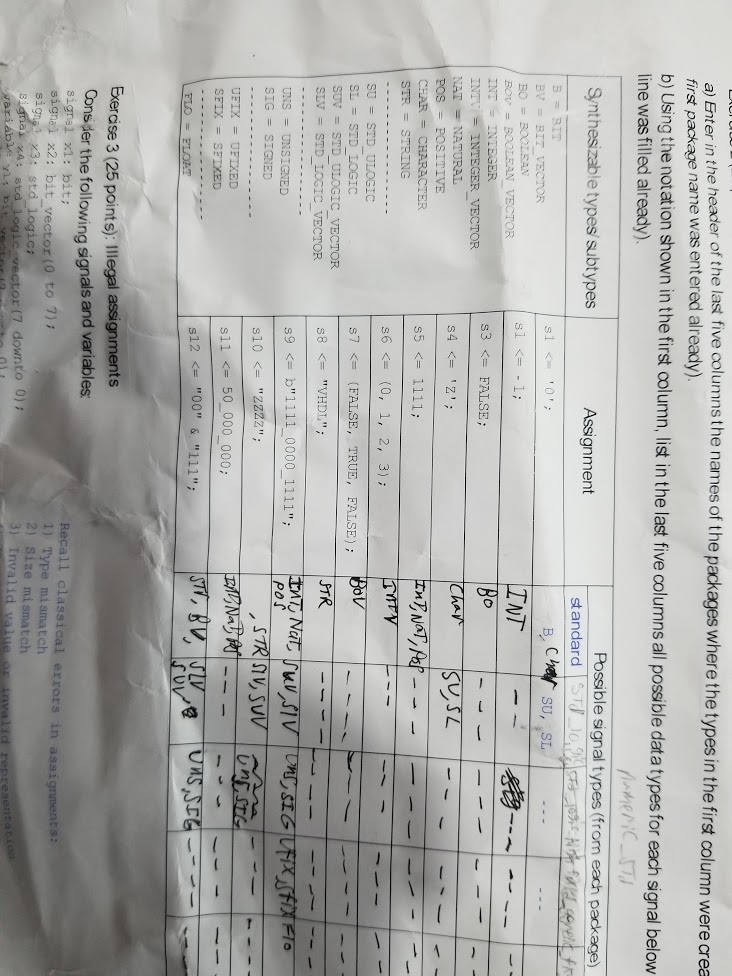
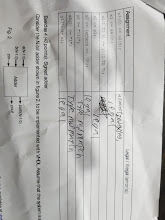
**Exercise 1: attributes of arrays**

1. **31**
2. **0**
3. **0**
4. **31**
5. **31 DOWNTO 0**
6. **0 TO 31**
7. **32**
8. **FALSE**

**Exercise 2:**



**Exercise 3: illegal assignments`**

****

**Exercise 4: Signed Adder**

b) VHDL code  
**library** ieee;

**use** ieee.std\_logic\_1164.**all**;

**use** ieee.numeric\_std.**all**;

**entity** adder **is**

**port**(

a, b, cin : **in** std\_logic;

sum, cout : **out** std\_logic

);

**end** **entity** adder;

**architecture** RTL **of** adder **is**

**begin**

sum <= a **XOR** b **XOR** cin;

cout <= (a **and** b) **or** (cin **and** a) **or** (cin **and** b);

**end** **architecture** RTL;

--------------------------------------------

**library** ieee;

**use** ieee.std\_logic\_1164.**all**;

**use** ieee.numeric\_std.**all**;

**use** work.**all**;

**entity** generic\_ripple **is**

**generic**(

*N* : integer := 8);

**port**(

a, b : **in** std\_logic\_vector(*N* - 1 **downto** 0);

cin : **in** std\_logic;

sum : **out** std\_logic\_vector(*N* - 1 **downto** 0);

cout : **out** std\_logic

);

**end** **entity** generic\_ripple;

**architecture** RTL **of** generic\_ripple **is**

**signal** temp : std\_logic\_vector(*N* **downto** 0);

**begin**

temp(0) <= cin;

cout <= temp(*N*);

signed\_adder : **for** i **in** 0 **to** *N* - 1 **generate**

full\_adder\_i : **entity** work.adder

**PORT** **MAP**(

temp(i), a(i), b(i), sum(i), temp(i + 1)

);

**end** **generate**;

**end** **architecture** RTL;

d) Simulation results (N = 8)

