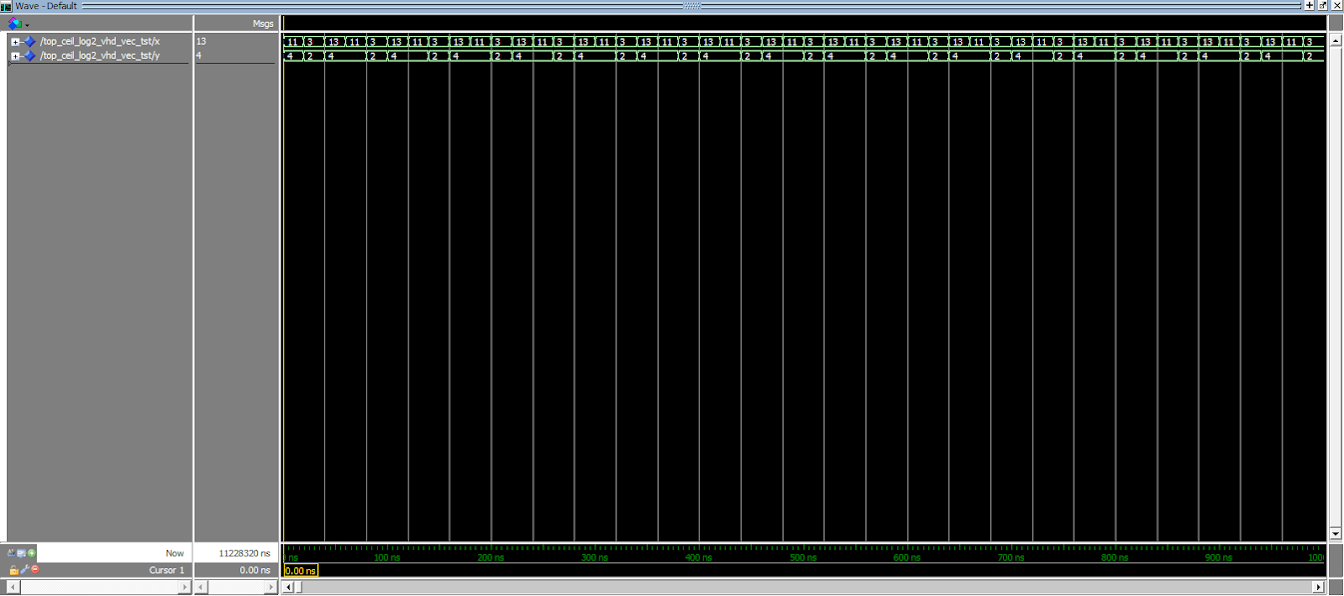
Exercise 1: ceil\_log2 function

1. VHDL code
   1. LIBRARY ieee;
   2. USE ieee.std\_logic\_1164.all;
   3. USE ieee.numeric\_std.all;
   4. use ieee.math\_real.all;
   5. PACKAGE lab4 IS
   6. FUNCTION count\_leading\_zeros(*x* : UNSIGNED) return UNSIGNED;
   7. FUNCTION ceil\_log2(*x* : UNSIGNED) return UNSIGNED;
   8. END PACKAGE lab4;
   9. package body lab4 is
   10. FUNCTION count\_leading\_zeros(*x* : UNSIGNED) return UNSIGNED IS
   11. VARIABLE count : UNSIGNED(*x*'*RANGE*) := to\_unsigned(0, *x*'*LENGTH*);
   12. BEGIN
   13. FOR i IN *x*'*RANGE* LOOP
   14. CASE *x*(i) IS
   15. WHEN *'0'* => count := count + 1;
   16. WHEN OTHERS => EXIT;
   17. END CASE;
   18. END LOOP;
   19. RETURN count;
   20. END FUNCTION count\_leading\_zeros;
   21. FUNCTION ceil\_log2(*x* : UNSIGNED) return UNSIGNED IS
   22. -- as it turns out this can be done with a count leading zeros procedure which is
   23. -- very close to our count leading ones procedure
   24. VARIABLE temp : UNSIGNED(*x*'*RANGE*) := to\_unsigned(0, *x*'*LENGTH*);
   25. begin
   26. IF *x* = to\_unsigned(0, *x*'*LENGTH*) THEN
   27. return to\_unsigned(0, *x*'*LENGTH*);
   28. ELSE
   29. temp := count\_leading\_zeros(*x* - to\_unsigned(1, *x*'*LENGTH*));
   30. return to\_unsigned(*x*'*HIGH*, *x*'*LENGTH*) - temp + to\_unsigned(1, *x*'*LENGTH*);
   31. END IF;
   32. end FUNCTION ceil\_log2;
   33. end lab4;
2. Simulation results

Exercise 2: natural\_to\_thermometer converter

1. VHDL code

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.numeric\_std.ALL;

USE ieee.math\_real.ALL;

PACKAGE lab4 IS

FUNCTION natural\_to\_thermometer (*x*: UNSIGNED) RETURN BIT\_VECTOR;

END PACKAGE lab4;

PACKAGE BODY lab4 IS

FUNCTION natural\_to\_thermometer(*x*: UNSIGNED) RETURN BIT\_VECTOR IS

VARIABLE temp: BIT\_VECTOR((2\*\**x*'*LENGTH* - 1) DOWNTO 0) := (OTHERS => *'0'*);

BEGIN

FOR i IN 0 TO temp'*left* LOOP

IF i < *x* THEN

temp(i) := *'1'*;

ELSE

EXIT;

END IF;

END LOOP;

RETURN temp;

END FUNCTION natural\_to\_thermometer;

END PACKAGE BODY lab4;

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.numeric\_std.ALL;

USE ieee.math\_real.ALL;

USE work.lab4.all;

ENTITY top\_natural\_to\_thermometer IS

GENERIC(

-- number of input bits

*BITS* : INTEGER := 7

);

PORT(

-- input in stl format

x : IN STD\_LOGIC\_VECTOR(*BITS* - 1 DOWNTO 0) := (OTHERS => *'0'*);

--num of bits, take the log base 2, then convert to an int.

y : OUT STD\_LOGIC\_VECTOR((2 \*\* *BITS*) - 1 DOWNTO 0) := (OTHERS => *'0'*)

);

END ENTITY top\_natural\_to\_thermometer;

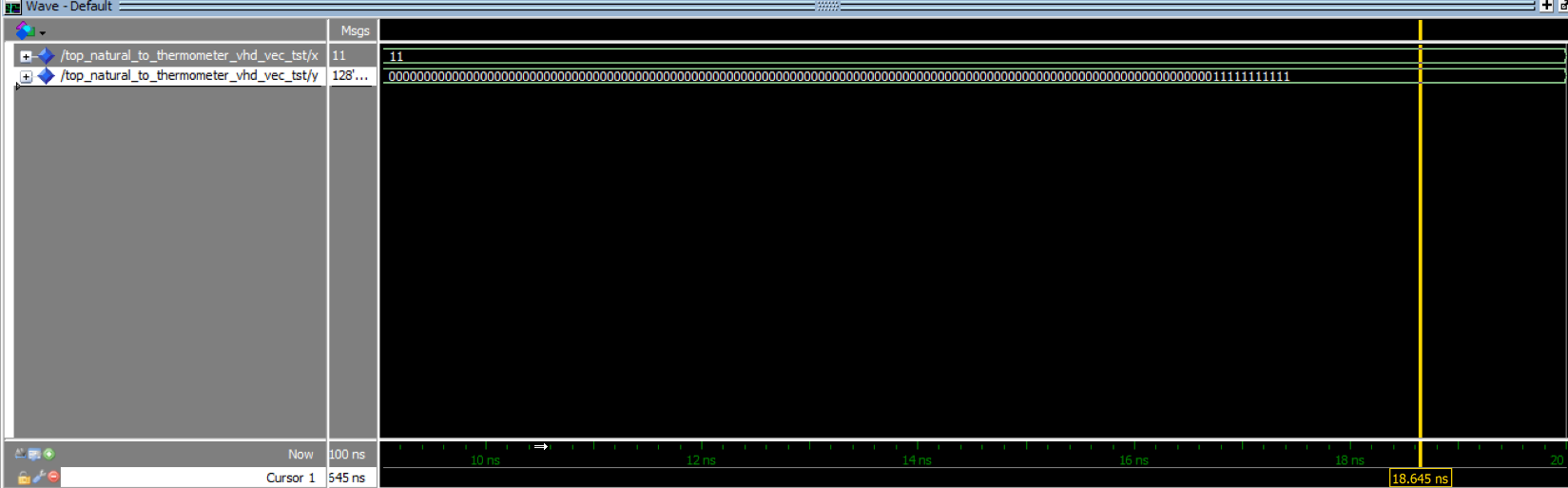
ARCHITECTURE arch OF top\_natural\_to\_thermometer IS

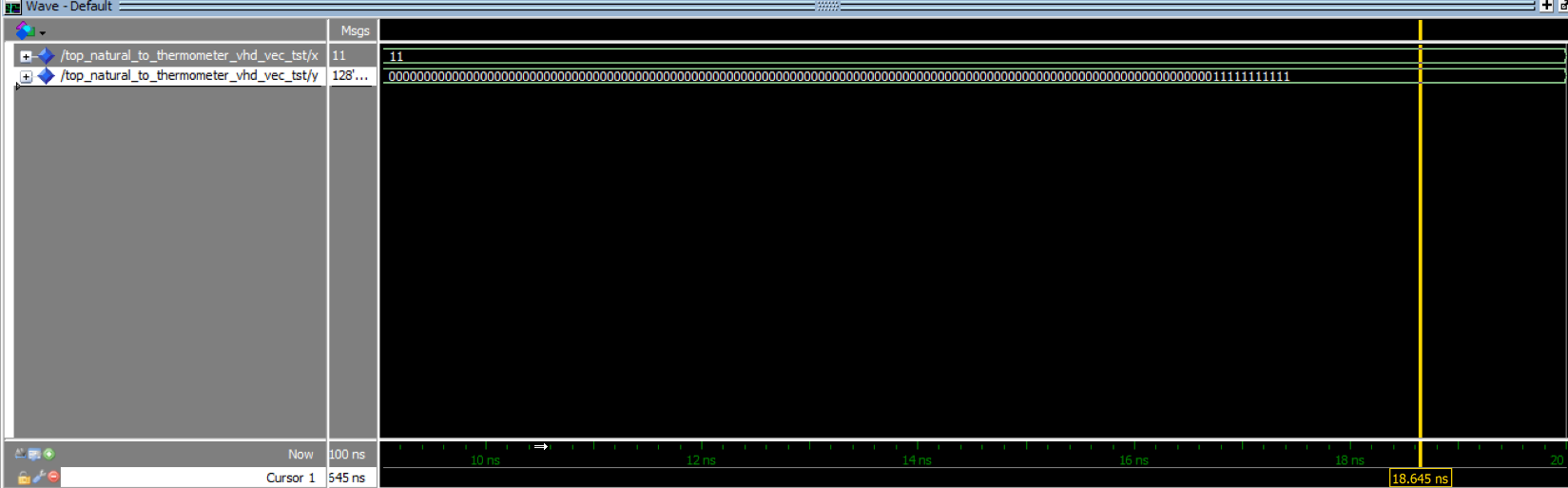
BEGIN

y <= to\_stdlogicvector(natural\_to\_thermometer(UNSIGNED(x)));

END ARCHITECTURE arch;

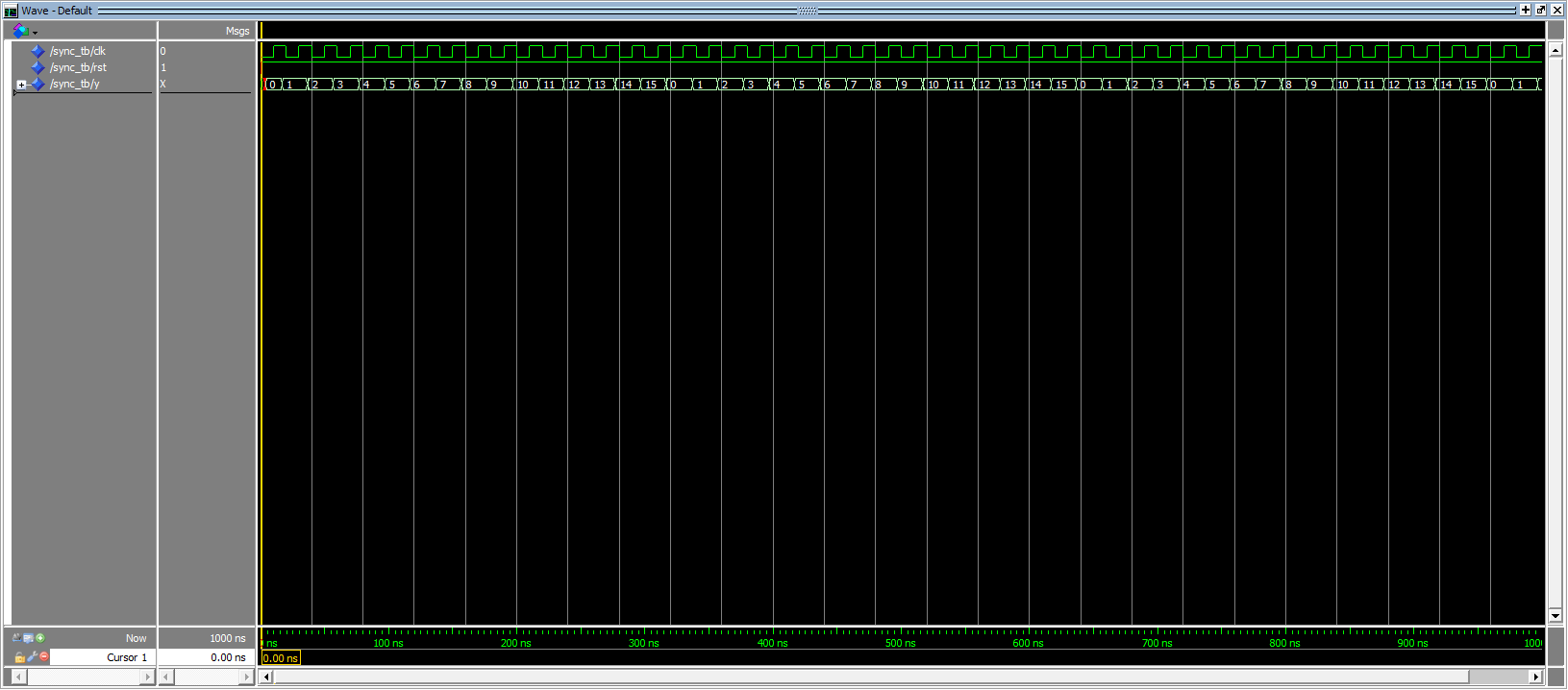
1. Simulation results





Exercise 3: Synchronous Counter

1. VHDL code
2. Simulation Results



Exercise 4: Pulse Width Modulator

1. VHDL code

d) Simulation results (N = 8)