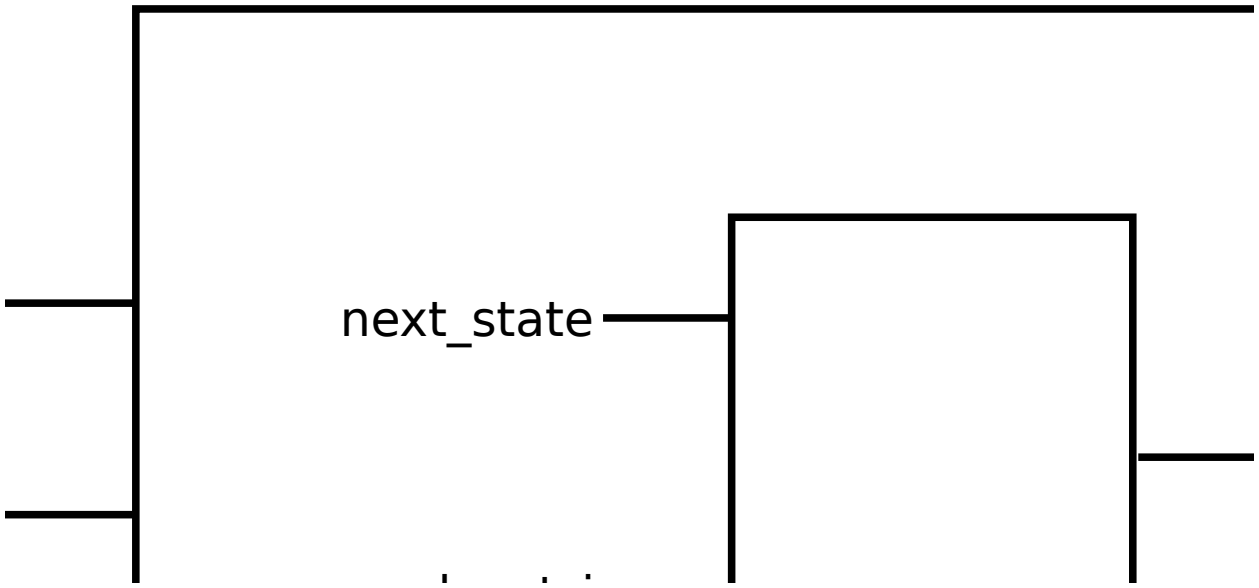
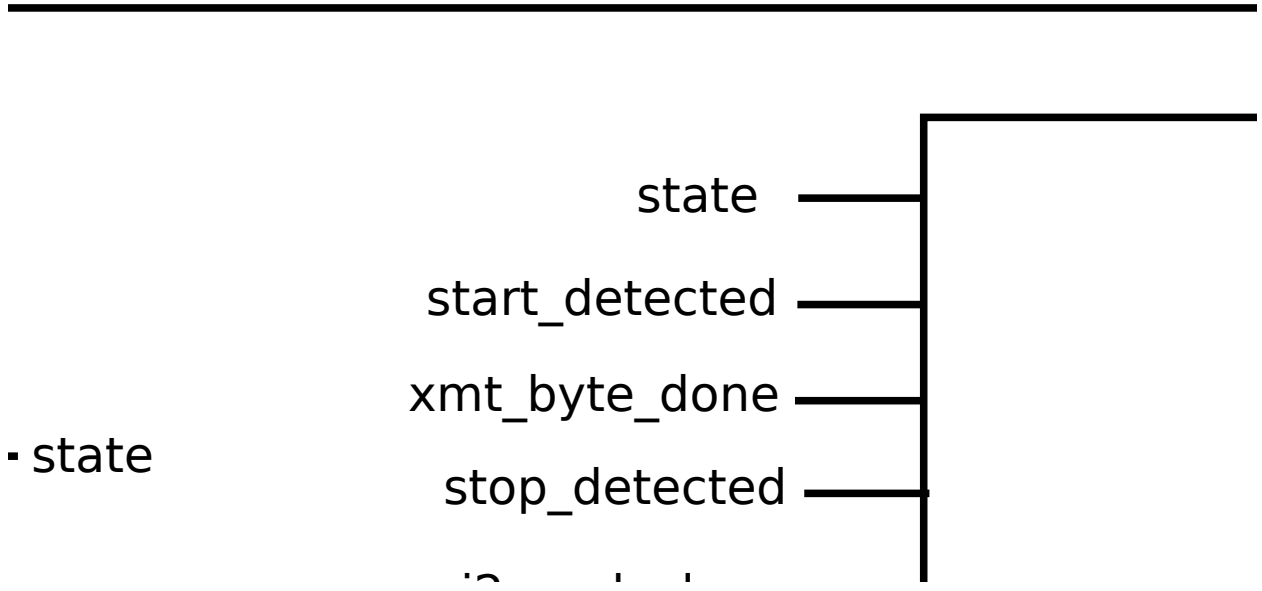
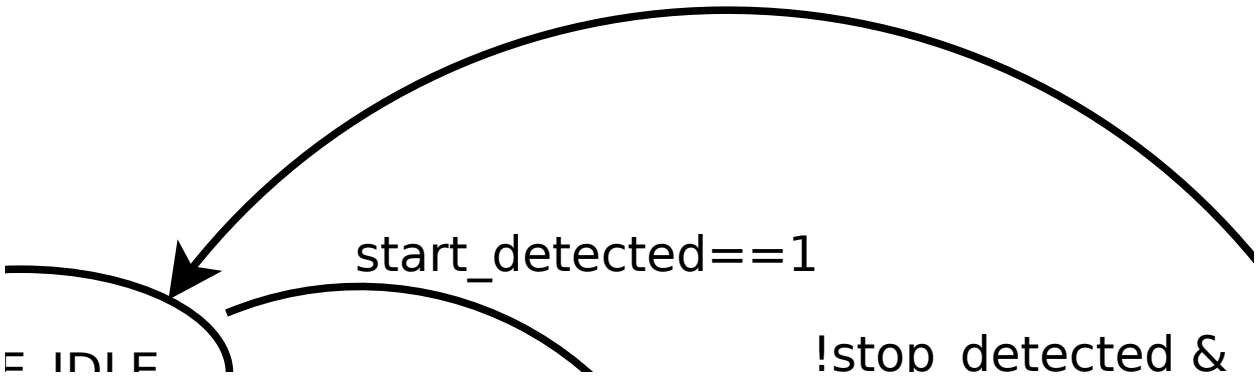
i2c_data -

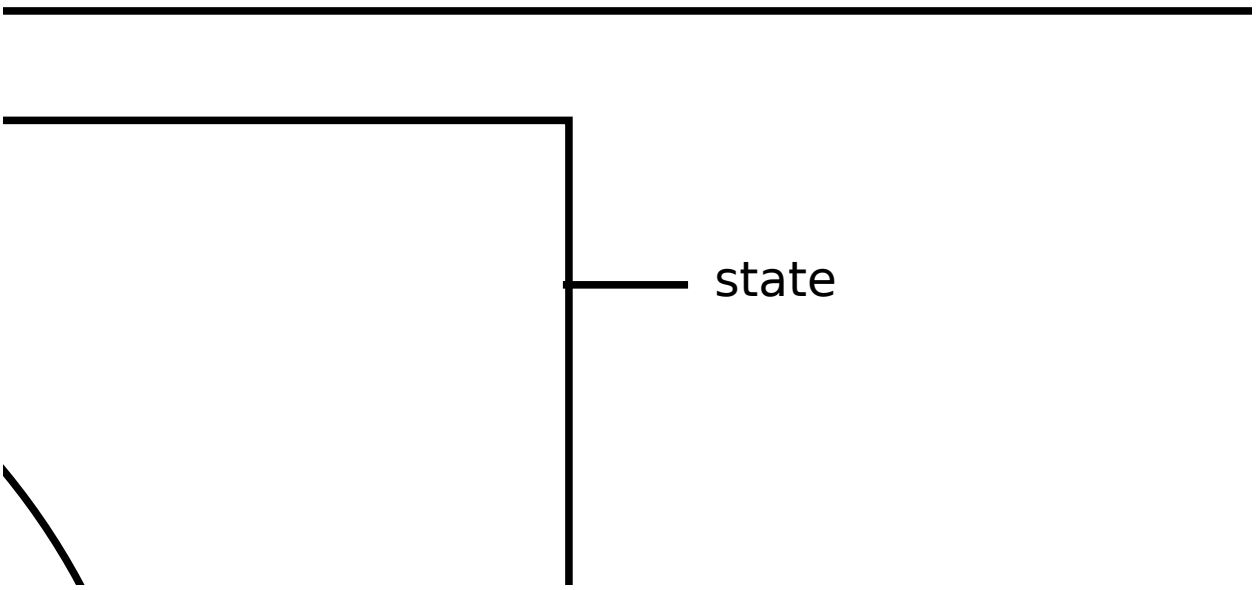
i2c_data_rise -

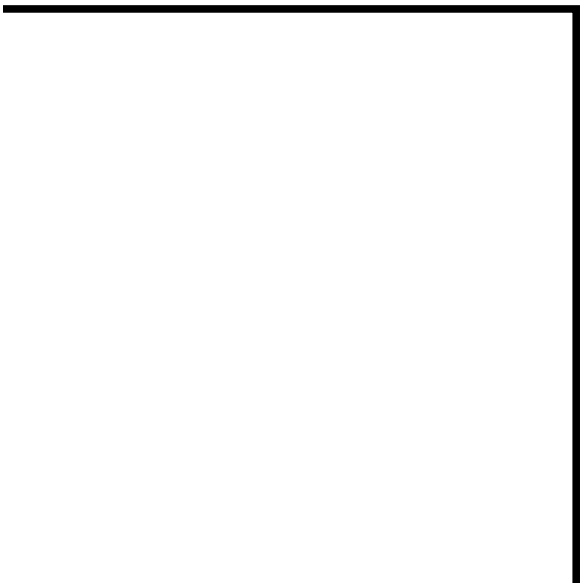

next_state


state
start_detected
xmt_byte_done
state
stop_detected


STATI


start_detected==1
!stop_detected &


state



i2c_data_fall -

i2c_clk -

i2c_clk_rise -

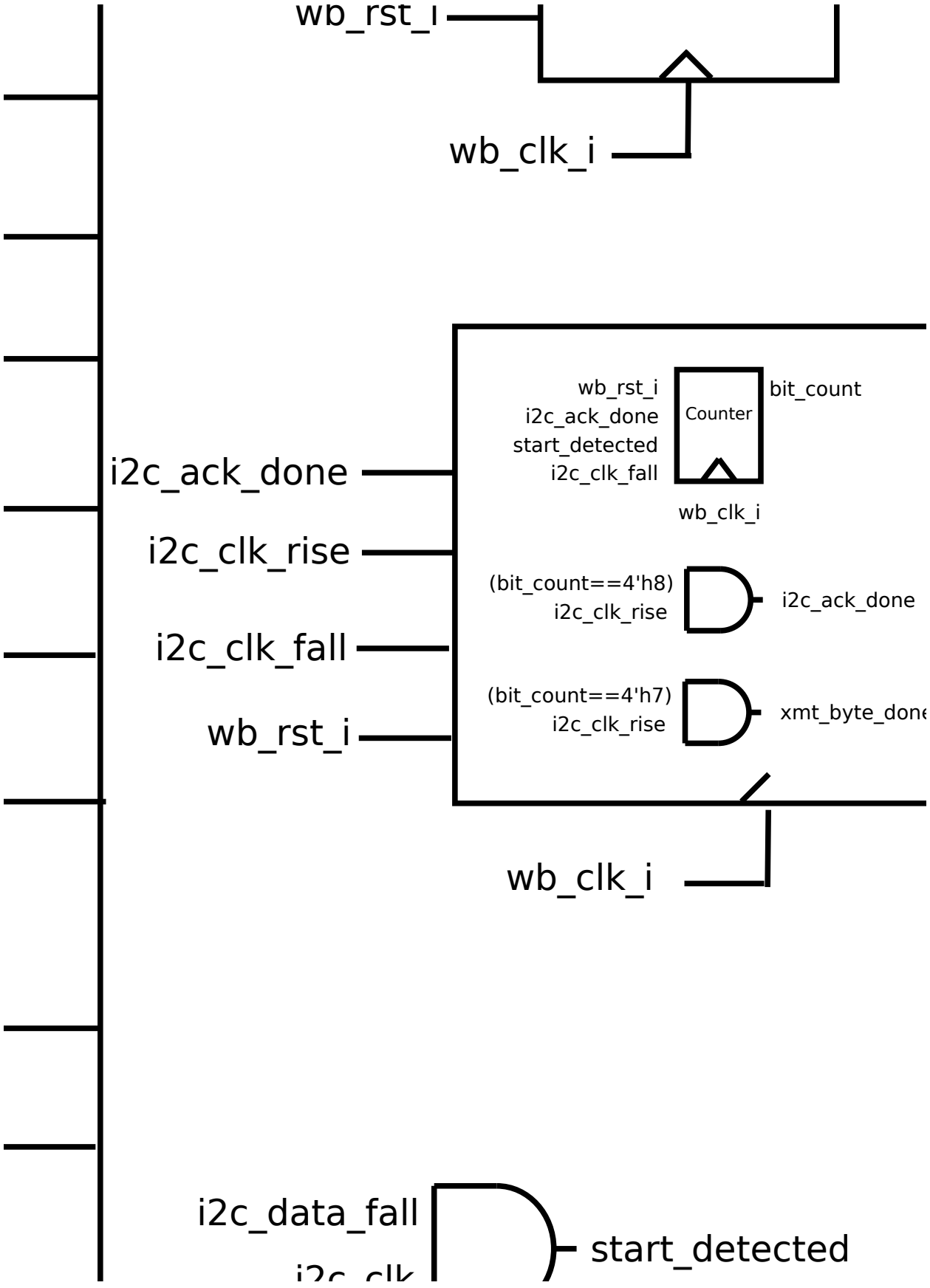
i2c_clk_fall -

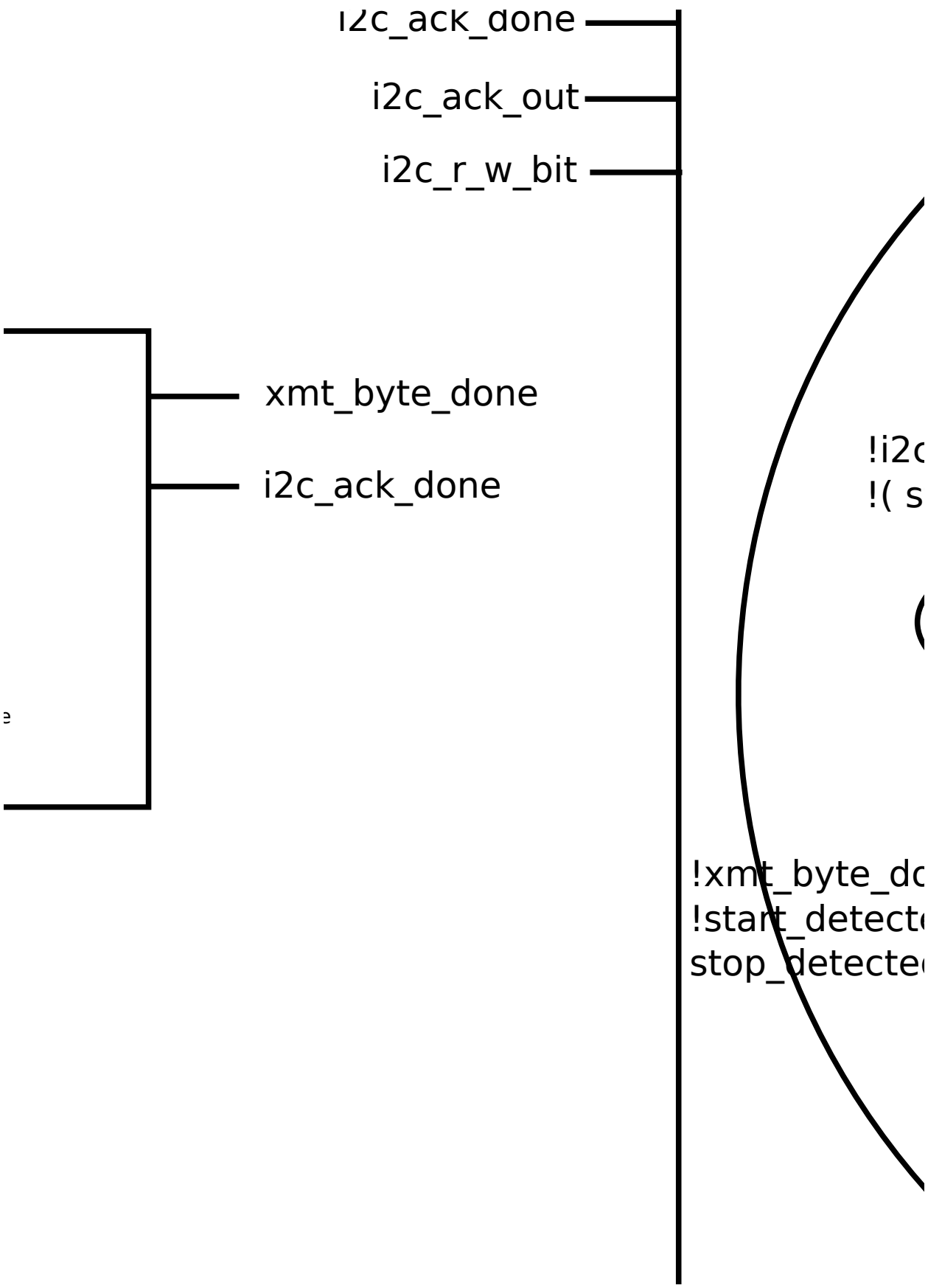
i2c_r_w_bit -

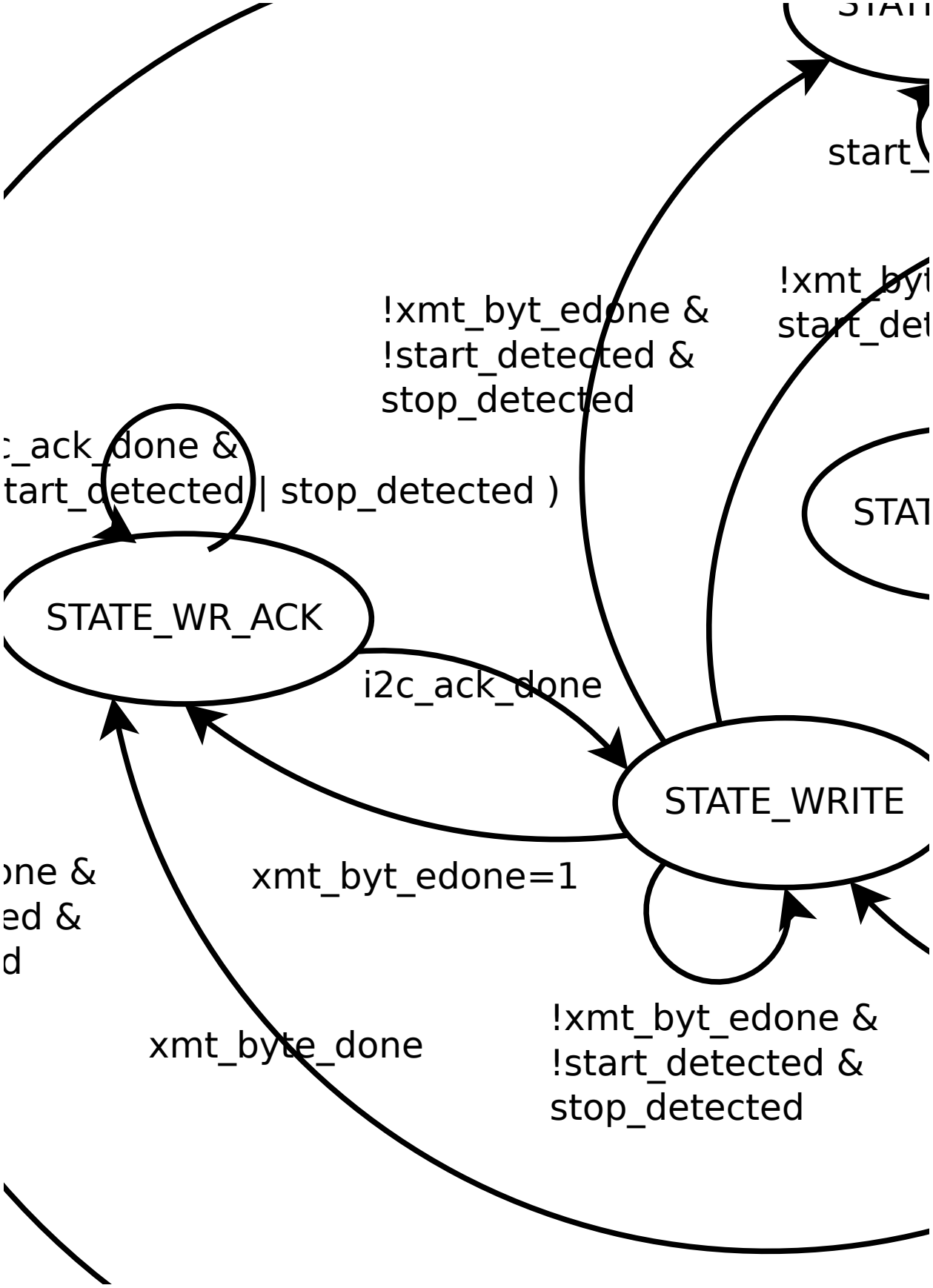
i2c_ack_out -

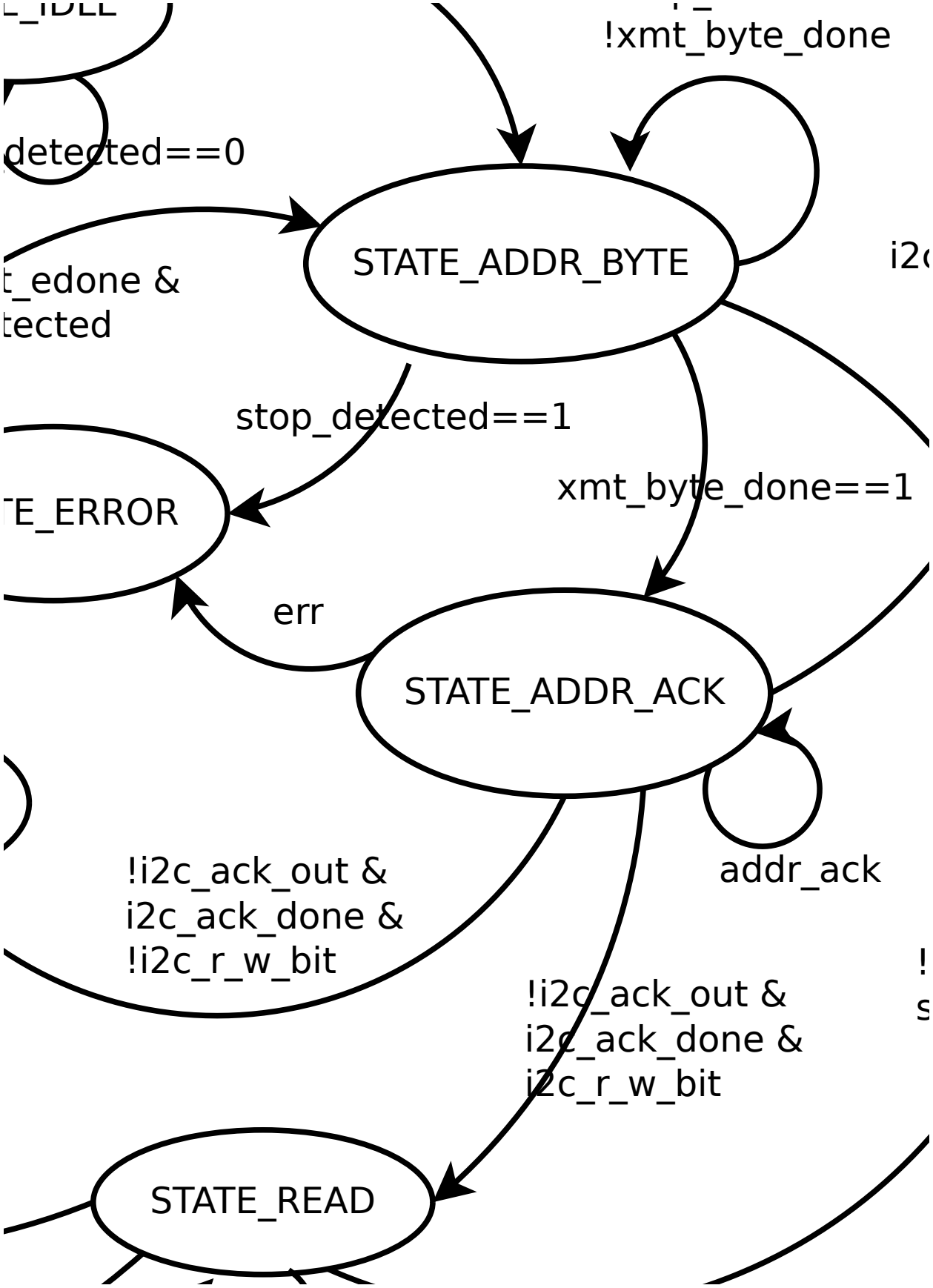
wb_clk_i -

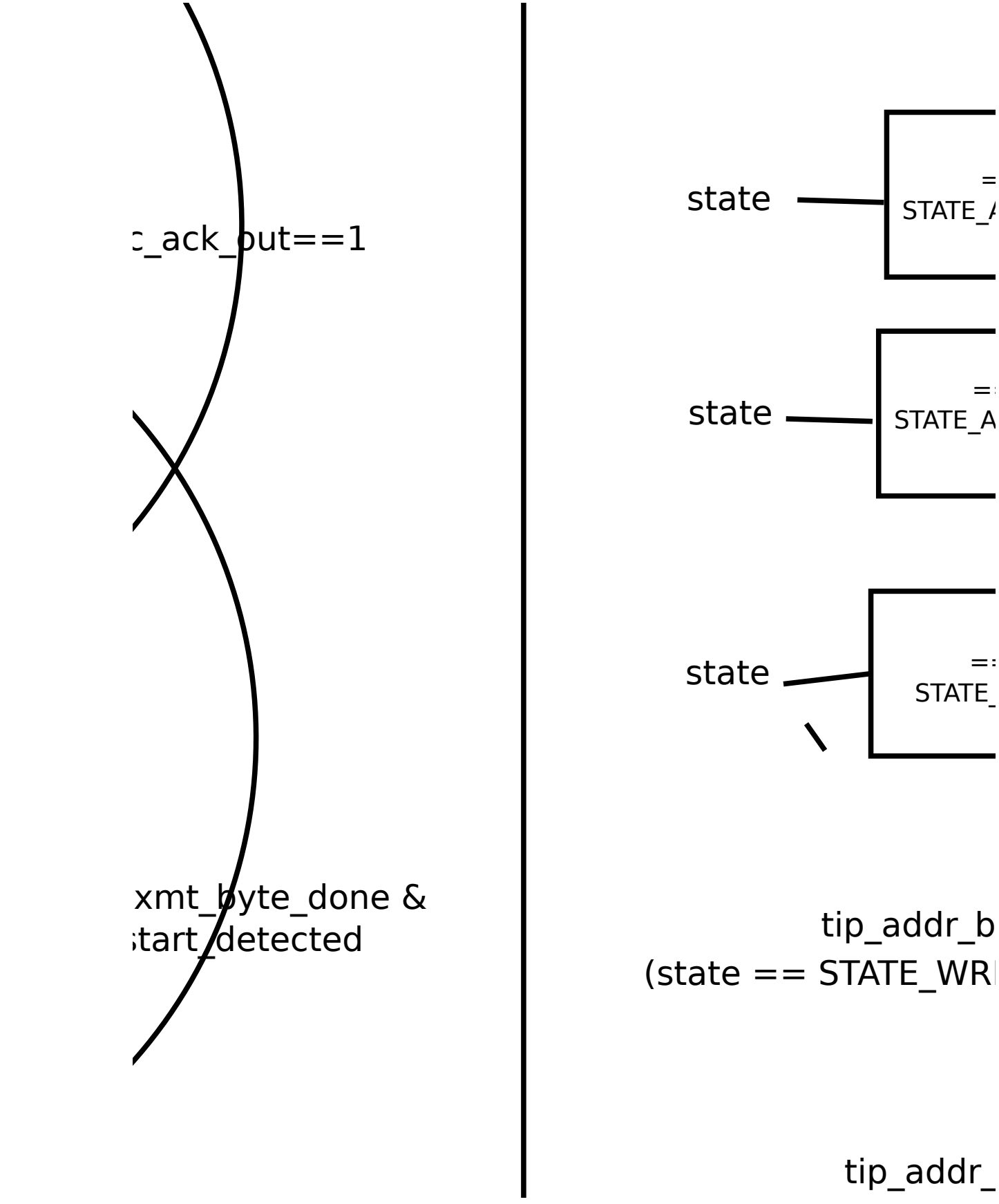
wb_rst_i -

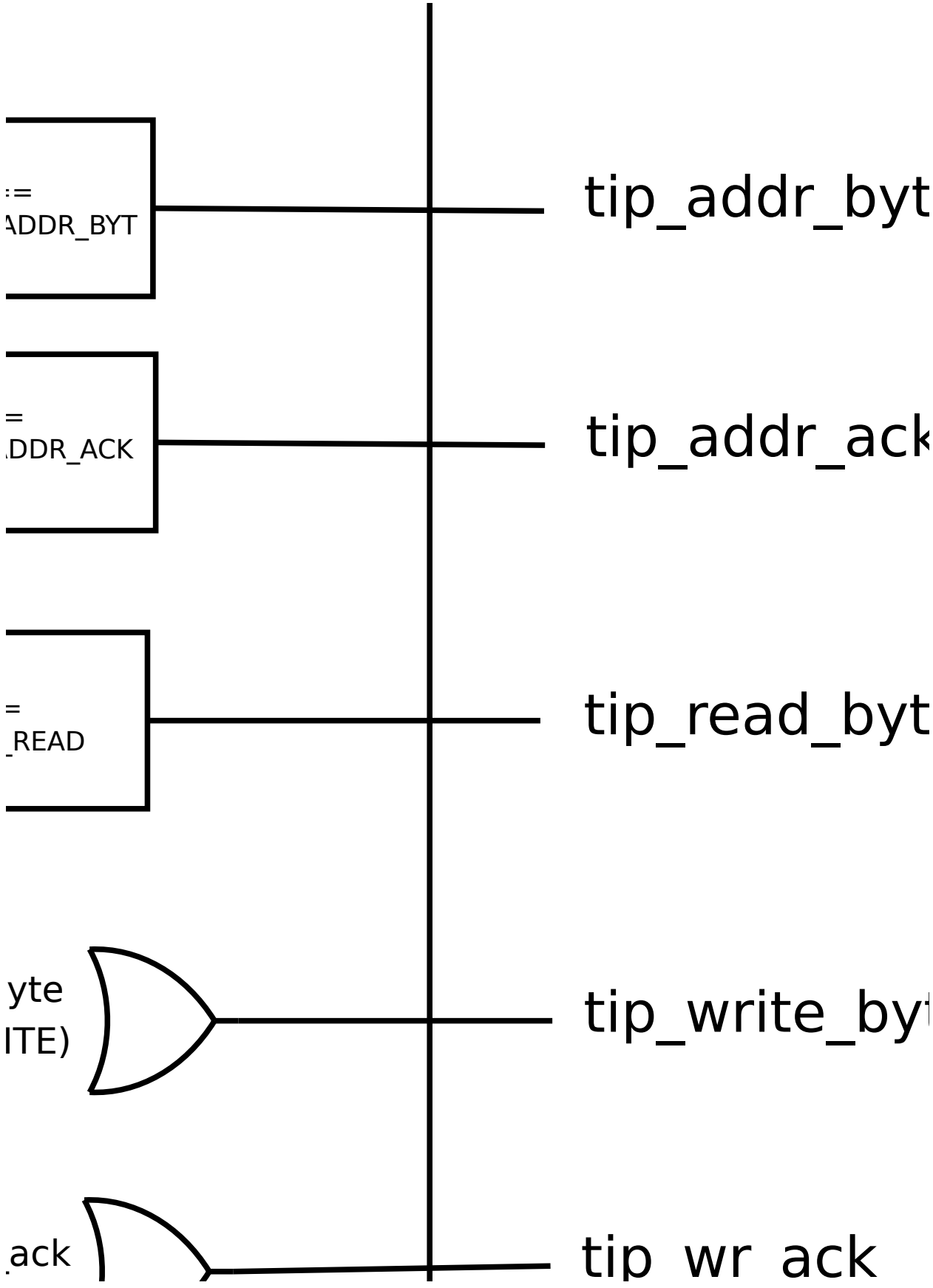

wb_rst_i
wb_clk_i
i2c_ack_done
i2c_clk_rise
i2c_clk_fall
wb_rst_i
wb_rst_i
i2c_ack_done
start_detected
i2c_clk_fall
Counter
bit_count
wb_clk_i
(bit_count==4'h8)
i2c_clk_rise
i2c_ack_done
(bit_count==4'h7)
i2c_clk_rise
xmt_byte_done
wb_clk_i
i2c_data_fall
start_detected


i2c_ack_done
i2c_ack_out
i2c_r_w_bit
xmt_byte_done
i2c_ack_done
!i2c
!( s
!xmt_byte_do
!start_detecte
stop_detecte


!xmt_byt_edone &
!start_detected &
stop_detected
_ack_done &
tart_detected || stop_detected )
STATE_WR_ACK
i2c_ack_done
STATE_WRITE
xmt_byt_edone=1
xmt_byte_done
!xmt_byt_edone &
!start_detected &
stop_detected


!xmt_byte_done
detected==0
STATE_ADDR_BYTE
stop_detected==1
xmt_byte_done==1
err
STATE_ADDR_ACK
addr_ack
!i2c_ack_out &
i2c_ack_done &
!i2c_r_w_bit
!i2c_ack_out &
i2c_ack_done &
i2c_r_w_bit
STATE_READ


c_ack_out==1
xmt_byte_done &
start_detected
state
=
STATE_A
state
=
STATE_A
state
=
STATE_
tip_addr_b
(state == STATE_WR
tip_addr_

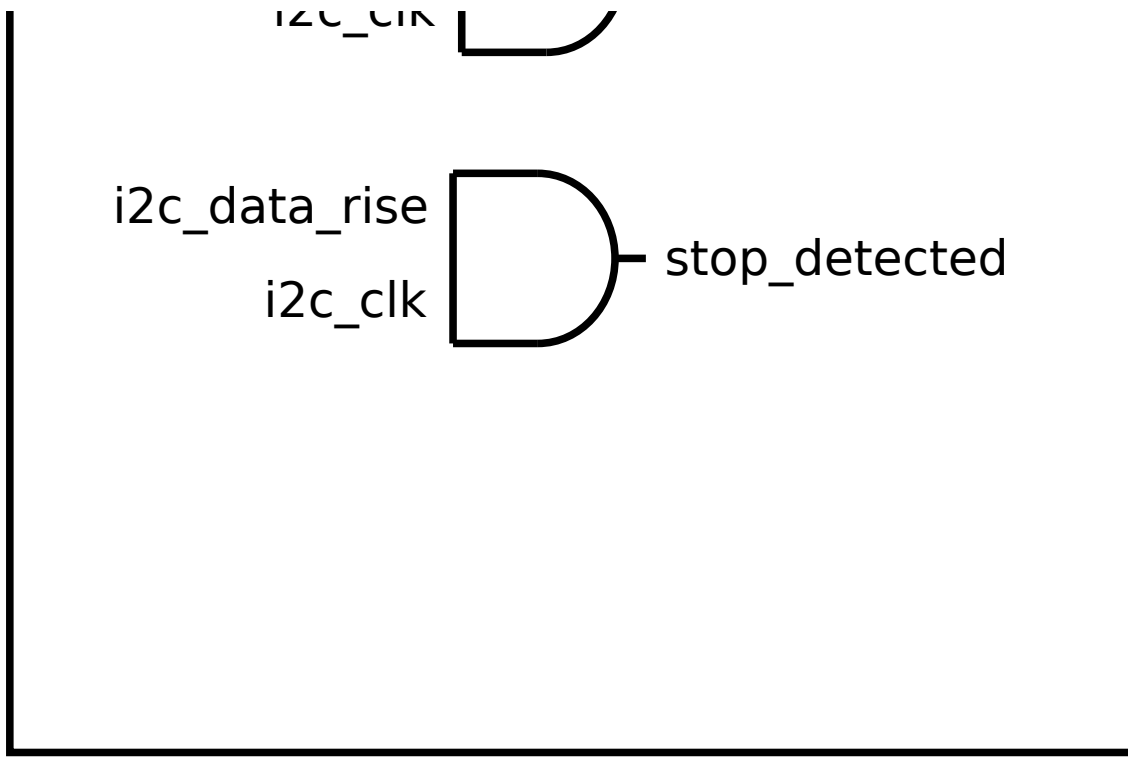

:=
ADDR_BYT
tip_addr_byt
=
DDR_ACK
tip_addr_ack
=
_READ
tip_read_byt
yte
ITE)
tip_write_byt
_ack
tip_wr_ack

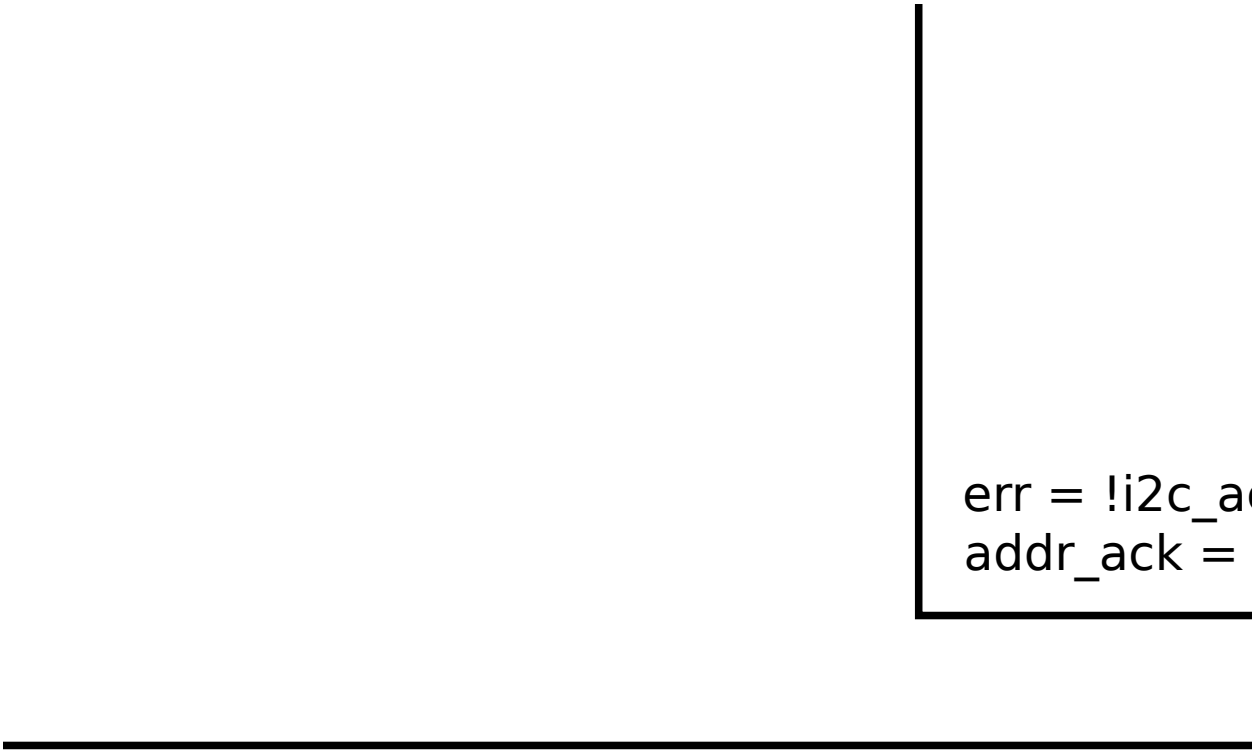
:e

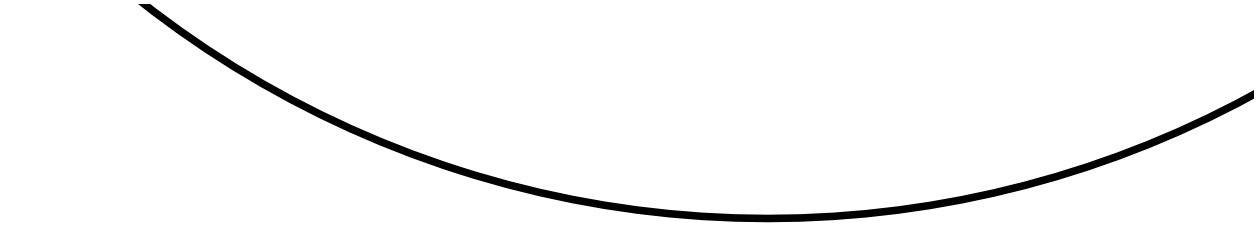
<

:e

te


i2c_clk
i2c_data_rise
i2c_clk
stop_detected

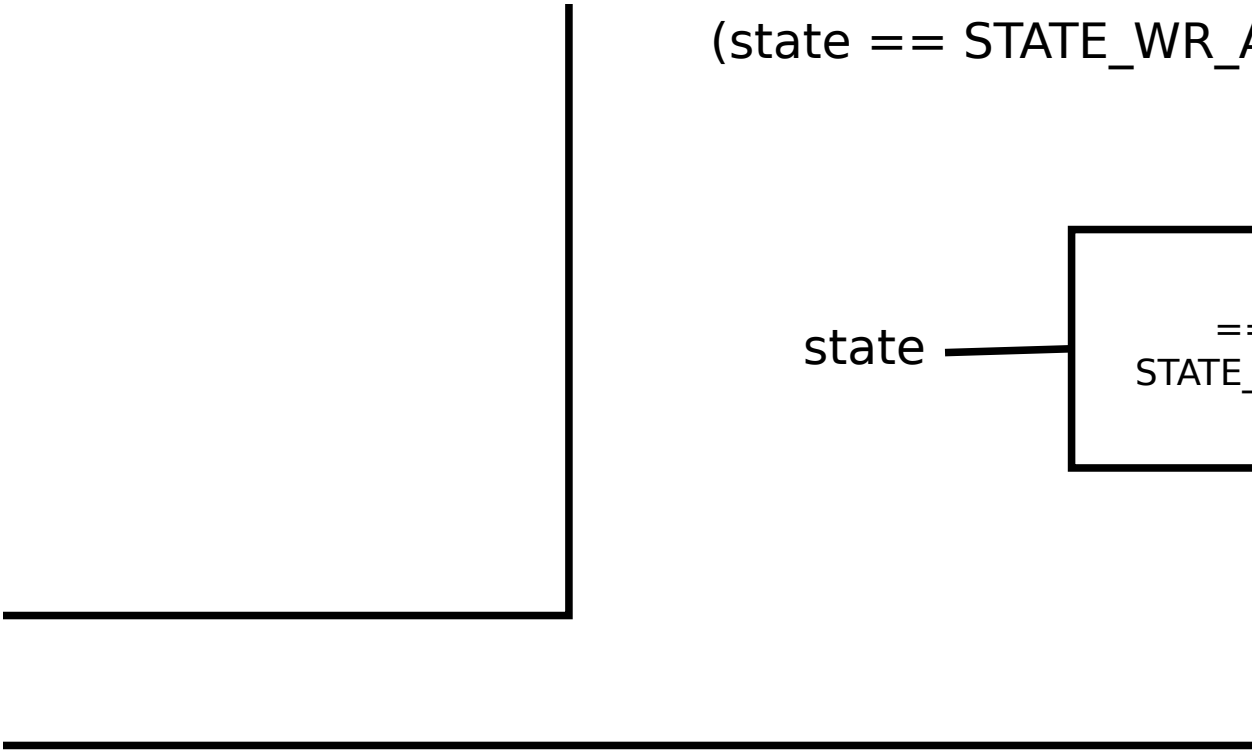

err = !i2c_a
addr_ack =

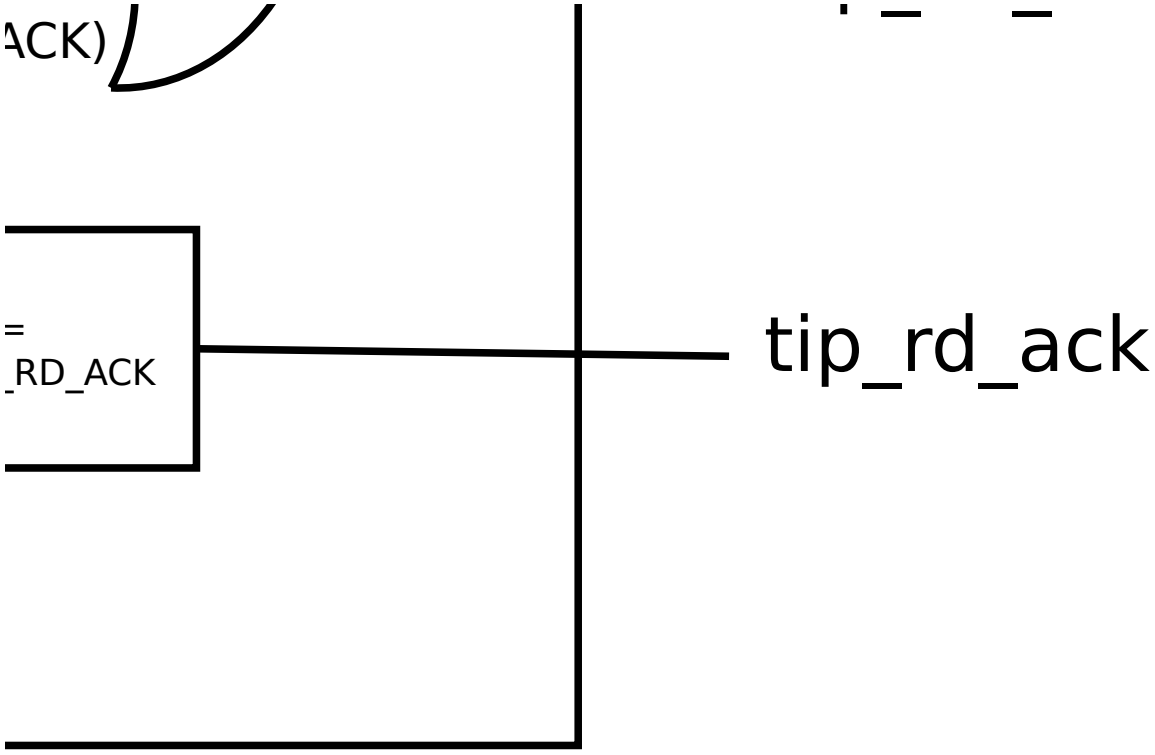


ck_out & !i2c_ack_done & ( start_detected | stop_de
!i2c_ack_out & !i2c_ack_done & !( start_detected | s

!xmt_byte_done &
!start_detected &
!stop_detected

tected )
stop_detected )


(state == STATE_WR_A
state
=
STATE_


ACK)
=
_RD_ACK
tip_rd_ack