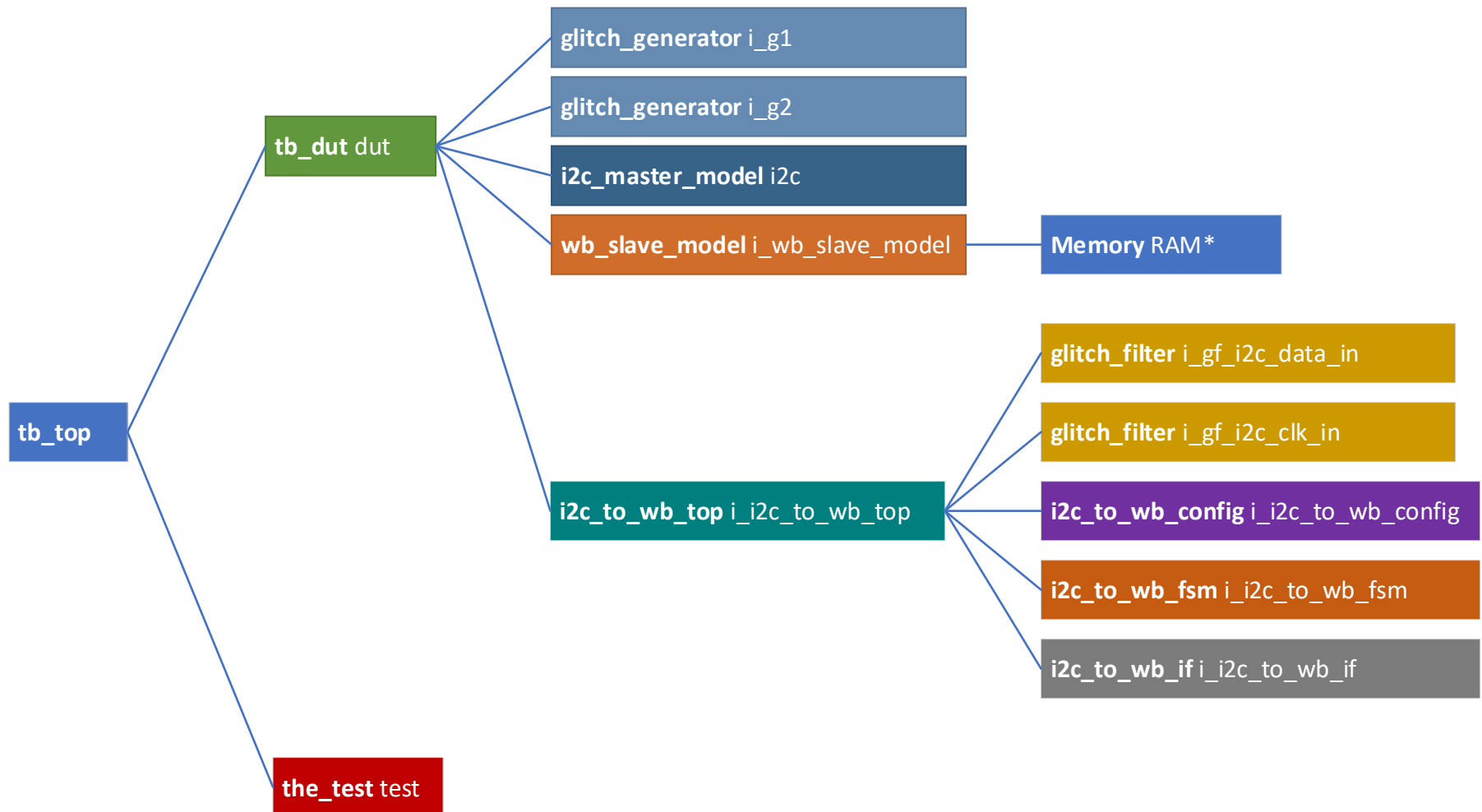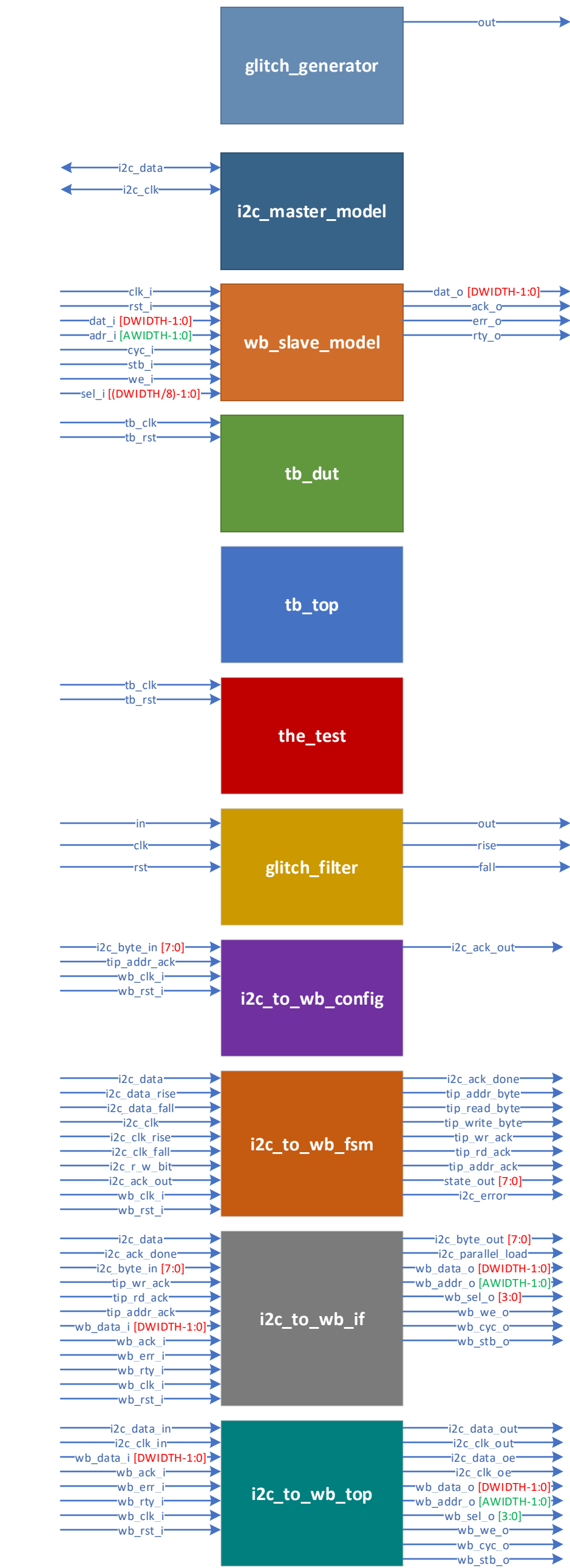# Module Hierarchy

DWIDTH = Data_Width
AWIDTH = Address_Width
wb = WishBone

Module Hierarchy

glitch_generator
out

i2c_master_model
i2c_data
i2c_clk

wb_slave_model
clk_i · dat_o [DWIDTH-1:0]
rst_i · ack_o
dat_i [DWIDTH-1:0] · err_o
adr_i [AWIDTH-1:0] · rty_o
cyc_i
stb_i
we_i
sel_i [(DWIDTH/8)-1:0]

tb_dut
tb_clk
tb_rst

tb_top

the_test
tb_clk
tb_rst

glitch_filter
in · out
clk · rise
rst · fall

i2c_to_wb_config
i2c_byte_in [7:0] · i2c_ack_out
tip_addr_ack
wb_clk_i
wb_rst_i

i2c_to_wb_fsm
i2c_data · i2c_ack_done
i2c_data_rise · tip_addr_byte
i2c_data_fall · tip_read_byte
i2c_clk · tip_write_byte
i2c_clk_rise · tip_wr_ack
i2c_clk_fall · tip_rd_ack
i2c_r_w_bit · tip_addr_ack
i2c_ack_out · state_out [7:0]
wb_clk_i · i2c_error
wb_rst_i

i2c_to_wb_if
i2c_data · i2c_byte_out [7:0]
i2c_ack_done · i2c_parallel_load
i2c_byte_in [7:0] · wb_data_o [DWIDTH-1:0]
tip_wr_ack · wb_addr_o [AWIDTH-1:0]
tip_rd_ack · wb_sel_o [3:0]
tip_addr_ack · wb_we_o
wb_data_i [DWIDTH-1:0] · wb_cyc_o
wb_ack_i · wb_stb_o
wb_err_i
wb_rty_i
wb_clk_i
wb_rst_i

i2c_to_wb_top
i2c_data_in · i2c_data_out
i2c_clk_in · i2c_clk_out
wb_data_i [DWIDTH-1:0] · i2c_data_oe
wb_ack_i · i2c_clk_oe
wb_err_i · wb_data_o [DWIDTH-1:0]
wb_rty_i · wb_addr_o [AWIDTH-1:0]
wb_clk_i · wb_sel_o [3:0]
wb_rst_i · wb_we_o
· wb_cyc_o
· wb_stb_o

Hierarchy tree:

tb_top
├─ tb_dut dut
│ ├─ glitch_generator i_g1
│ ├─ glitch_generator i_g2
│ ├─ i2c_master_model i2c
│ ├─ wb_slave_model i_wb_slave_model ─ Memory RAM*
│ └─ i2c_to_wb_top i_i2c_to_wb_top
│   ├─ glitch_filter i_gf_i2c_data_in
│   ├─ glitch_filter i_gf_i2c_clk_in
│   ├─ i2c_to_wb_config i_i2c_to_wb_config
│   ├─ i2c_to_wb_fsm i_i2c_to_wb_fsm
│   └─ i2c_to_wb_if i_i2c_to_wb_if
└─ the_test test