Training instructions

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Objectives

- Get familiar with Kactus2 tool
- Create different IP-XACT top-level elements:
  - Component from Verilog source
  - Structural Design for a component
  - Bus/Abstraction definition for communication
- Generate
  - Documentation for IPs
  - Structural HDL from IP-XACT design

Component creation

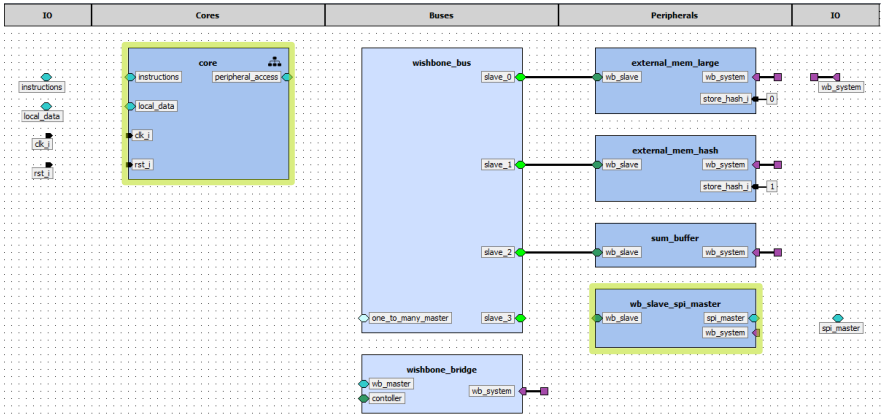
- Create new component *wb_slave_spi_master* for Wishbone-SPI communication
  - Import source files in: tut.fi/communication.bridge/wb_slave_spi_master/1.0
- Fill in component details:
  - Registers (4)
  - Bus interfaces (3)
    - Wishbone interface
    - Clk/reset interface
    - SPI, see next page for details

Bus/Abstraction Definition

- Create new bus definition for Serial Peripheral Interface (SPI) communication
  - Kactus2 creates an empty abstraction definition automatically
- Define 4 wire signals:
  - Slave clock, SCKL
  - Data line, MISO
  - Data line, MOSI
  - Chip-select, CS
- Use the created definitions and create port maps in
  - your wb_slave_spi_master component, SPI bus interface
  - component tut.fi:cpu.structure:cpu_example:1.0, *spi_master* bus interface

Design creation

- Open HW design for tut.fi:cpu.structure:cpu_example:1.0 and instantiate *wb_slave_spi_master* in it
- Connect *wb_slave_spi_master* and *core* instances to correct bus interfaces and/or ad-hoc ports
  - Why *peripheral_access* cannot be connected to *one_to_many_master*?
- Double-click instance *core and* complete the structural HW design for it. Use the following components in library cpu.logic:
  - clock
  - memory_controller
  - instruction_decoder
  - alu



HW design for tut.fi:cpu.structure:cpu_example:1.0

Generation

- Open the top-level HW design (tut.fi:cpu.structure:cpu_example:1.0)
- Select  to generate documentation
- Check the generated file(s)
  - Which component(s) and/or design(s) are included in the documentation?
- Select  to generate Verilog, or  to generate VHDL
- Now open component tut.fi:cpu.logic:alu:1.0 and select Verilog or VHDL generation again
  - What is the difference between the two generation runs (Design vs. Component)?