Training instructions

Esko Pekkarinen
esko.pekkarinen@tut.fi
29th October 2018

Objectives

- Get familiar with Kactus2 tool
- Create different IP-XACT top-level elements:
  - Component from Verilog source
  - Structural Design for a component
  - Bus/Abstraction definition for communication
- Generate
  - Documentation for IPs
  - Structural HDL from IP-XACT design

Component creation

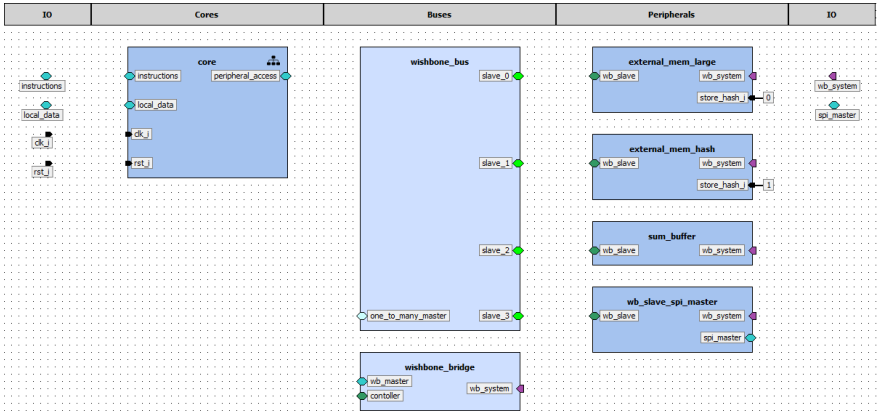
- Create new component *wb_master_cpu_slave* for core-to-Wishbone communication
  - Import source files in: tut.fi/communication.bridge/wb_master_cpu_slave/1.0
- Fill in component details:
  - Bus interfaces:
    - Wishbone master interface
    - Wishbone clk/reset system interface
    - Core slave interface (tut.fi:interface:peripheral_control:1.0)
  - Add transparent bridge from core to wishbone bus interfaces

Bus/Abstraction Definition

- Create new bus definition for Serial Peripheral Interface (SPI) communication
  - Kactus2 creates an empty abstraction definition automatically
- Define master and slave modes for 4 wire signals:
  - Slave clock, SCKL
  - Data line, MISO
  - Data line, MOSI
  - Chip-select, CS
- Use the created definitions and create port maps in
  - component wb_slave_spi_master, *spi_master* bus interface
  - component tut.fi:cpu.structure:cpu_example:1.0, *spi_master* bus interface

Design creation

- Open HW design for tut.fi:cpu.structure:cpu_example:1.0
- Instantiate components core_example, *wb_master_cpu_slave* and the following peripherals:
  - 2x wb_external_mem
  - sum_buffer
  - *wb_slave_spi_master*
- Connect the instances
  - Why *peripheral_access* cannot be connected to *one_to_many_master*?



HW design for tut.fi:cpu.structure:cpu_example:1.0

Generation

- Open the top-level HW design (tut.fi:cpu.structure:cpu_example:1.0)
- Select  to generate documentation
- Check the generated file(s)
  - Which component(s) and/or design(s) are included in the documentation?
- Select  to generate Verilog, or  to generate VHDL
- Now open component tut.fi:cpu.logic:alu:1.0 and select Verilog or VHDL generation again
  - What is the difference between the two generation runs (Design vs. Component)?