405GP Evaluation Board Switch Settings

The 405GP Evaluation Board has four sets of switches: U52, U53, U54 and U79. These switches control settings for internal clock ratios, PLL divisors, PLL tuning bits, boot options, PCI modes and ECC mode. The default switch settings are printed on the evaluation board and provided in the board schematics. Table 1 lists the default switch settings for the evaluation boards containing the pass 1 405GP.

The default clock ratios shipped on the evaluation board are for 133 MHz operation. For 200 MHz operation the switch setting must be modified as indicated in Table 2. (For assistance, contact ppcsupp@us.ibm.com)

Switch	#	Setting	Description (configuration)
U52	S1	CLOSED(ON)	PLL Forward Divide Ratio (3)
	S2	OPEN(OFF)	
	S3	CLOSED(ON)	PLL Feedback Divide Ration (2)
	S4	OPEN(OFF)	
	S5	CLOSED(ON)	PLL Control Tuning bits (4)
	S6	OPEN(OFF)	
	S7	OPEN(OFF)	
	S8	CLOSED(ON)	PLB Divide Ratio from CPU (2)
U53	S1	OPEN(OFF)	
	S2	CLOSED(ON)	OPB Divide Ratio from PLB (2)
	S3	OPEN(OFF)	
	S4	CLOSED(ON)	PCI Divide Ratio from PLB (2)
	S5	OPEN(OFF)	
	S6	CLOSED(ON)	Peripheral Bus Divide Ratio from PLB (2)
	S7	CLOSED(ON)	Note: The printed settings on the 405GP evaluation board incorrectly show U53 S7 set to the OPEN(OFF) position.
	S8	CLOSED(ON)	ROM Width (8 bits)
U54	S1	CLOSED(ON)	
	S2	CLOSED(ON)	ROM Location (Peripheral Attach)
	S3	OPEN(OFF)	Reserved
	S4	CLOSED(ON)	PCI Synchronous Mode (Enabled)
	S5	CLOSED(ON)	ECC Mode Disabled
	S6	OPEN(OFF)	Internal PCI Arbiter Disable (Enabled)
	S7	CLOSED(ON)	405GP Ref Clk Source (Internal) Note: OFF – Ref Clk source from J23
	S8	OPEN(OFF)	PCI Clk Source (Internal) Note: ON – PCI Clk source from J21
U79	S1	OPEN(OFF)	PCI Clk Divisor (12)
	S2	OPEN(OFF)	Note: Divisor used only if U54 S4 is OFF – PCI Synchronous Mode is disabled.
	S3	OPEN(OFF)	SDRAM Clk Divisor (6)
	S4	CLOSED(ON)	Note: Divisor used only if U79 S7 set to OFF – SDRAM Clk source from an alternate on-board clk)
	S5	CLOSED(ON)	On Board Flash
	S6	CLOSED(ON)	Flash at Address (0xFFF8 0000 and SRAM at Address 0xFFF0 0000) Note: OFF – SRAM at Address 0xFFF8 0000 and Flash at Address 0xFFF0 0000
	S7	CLOSED(ON)	SDRAM Clk Source (405GP) Note: OFF – SDRAM Clk source from an alternate on-board clock
	S8	CLOSED(ON)	Unused

Table 1 Default Settings
(133 MHz CPU/ 66 MHz PLB/ 33 MHz OPB/ 33 MHz Peripheral Bus/ 33 MHz PCI)

405GP Evaluation Board Switch Settings

Switch	#	Setting	Modified Switches	Description (configuration)
U52	S1	OPEN(OFF)	Modify	PLL Forward Divide Ratio (4)
	S2	CLOSED(ON)	Modify	
	S3	OPEN(OFF)	Modify	PLL Feedback Divide Ratio (3)
	S4	CLOSED(ON)	Modify	
	S5	CLOSED(ON)		Default
	S6	OPEN(OFF)		
	S7	OPEN(OFF)		
	S8	CLOSED(ON)		Default
U53	S1	OPEN(OFF)		
	S2	CLOSED(ON)		Default
	S3	OPEN(OFF)		
	S4	OPEN(OFF)	Modify	PCI Divide Ratio from PLB (3)
	S5	CLOSED(ON)	Modify	
	S6	CLOSED(ON)		Peripheral Bus Divide Ratio from PLB (3)
	S7	OPEN(OFF)	Modify	
	S8	CLOSED(ON)		Default
U54	S1	CLOSED(ON)		
	S2	CLOSED(ON)		Default
	S3	OPEN(OFF)		Default
	S4	CLOSED(ON)		Default
	S5	CLOSED(ON)		Default
	S6	CLOSED(ON)	Modify	Internal PCI Arbiter Disable (Disabled)
	S7	CLOSED(ON)		Default
	S8	OPEN(OFF)		Default
U79	S1	OPEN(OFF)		Default
	S2	OPEN(OFF)		
	S3	OPEN(OFF)		Default
	S4	CLOSED(ON)		
	S5	CLOSED(ON)		Default
	S6	CLOSED(ON)		Default
	S7	CLOSED(ON)		Default
	S8	CLOSED(ON)		Default

Table 2 Modified Settings
(200 MHz CPU/ 100 MHz PLB/ 50 MHz OPB/ 33 MHz Peripheral Bus/ 33 MHz PCI)