The ARC ISA

• The ARC ISA is a subset of the SPARC ISA.

Mnemonic	Meaning
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Memory	ld	Load a register from memory						
	st	Store a register into memory						
	sethi	Load the 22 most significant bits of a register						
	andcc	Bitwise logical AND						
Logic	orcc	Bitwise logical OR						
	orncc	Bitwise logical NOR						
	srl	Shift right (logical)						
Arithmetic	addcc Add							
	call	Call subroutine						
	jmpl	Jump and link (return from subroutine call)						
	be	Branch if equal						
Control	bneg	Branch if negative						
	bcs	Branch on carry						
	bvs	Branch on overflow						
	Branch always							

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ARC Instruction and PSR Formats

	op 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
SETHI Format	0 0 rd op2 imm22
Branch Format	0 0 0 cond op2 disp22
CALL format	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 0 1
Arithmetic Formats	11 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 1 0 rd op3 rs1 0 0 0 0 0 0 0 0 0 rs2
	1 0 rd op3 rs1 1 simm13 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 1 1 rd op3 rs1 0 0 0 0 0 0 0 0 0 rs2
Memory Formats	

op	Format	op2	Inst.	op3 (op=10)		op3 (op=11)		cond	branch	
0.0	SETHI/Branch	010	branch	010000	addcc		000000 ld		0001	be
01	CALL	100	sethi	010001	andcc		000100 st		0101	bcs
10	Arithmetic			010010	orcc	'			0110	bneg
11	Memory			010110	orncc				0111	bvs
ш				100110	srl				1000	ba
				111000	impl					

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

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