ECE 273: Introduction to Digital Logic

Lab <7> : < Counters >

By

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Today
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Honor Code:

I have neither given nor received unauthorized assistance on this graded report.

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Objective

The purpose of this lab is to design a 4-bit counter using a JK FF.

Theory

Truth tables, state tables and k-maps were used in the design of this lab.

Equipment Used

- Software: Xilinx, PlanAhead.
- Hardware: BASYS Board

Procedure

First, I will start with a two-bit counter that follows this state diagram:

A	B	A+	B+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

Table 1: Two-bit state table

From this table and using the JK excitation table:

Q	Q+	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Table 2: JK Excitation Table

Now I can generate a state excitation table:

Q1	Q2	J1	K1	J2	K2
0	0	0	X	1	X
0	1	1	X	X	1
1	0	X	0	X	0
1	1	X	1	X	1

Table 3:State Excitation Table

Q2 \ Q1	0	1
0		x
1	1	x

Table 4: J1 k-map

Q2 \ Q1	0	1
0	x	
1	x	1

Table 5: K1 k-map

Q2 \ Q1	0	1
0	1	1
1	x	x

Table 6: J2 k-map

Q2 \ Q1	0	1
0	x	x
1	1	1

Table 7: K2 k-map

J1= Q2;
K1= Q2
J2= 1;
K2= 1;

Here FF 2 goes first since it will give the most significant bit. And now that I figured out the formulas I can draw the schematic as such:

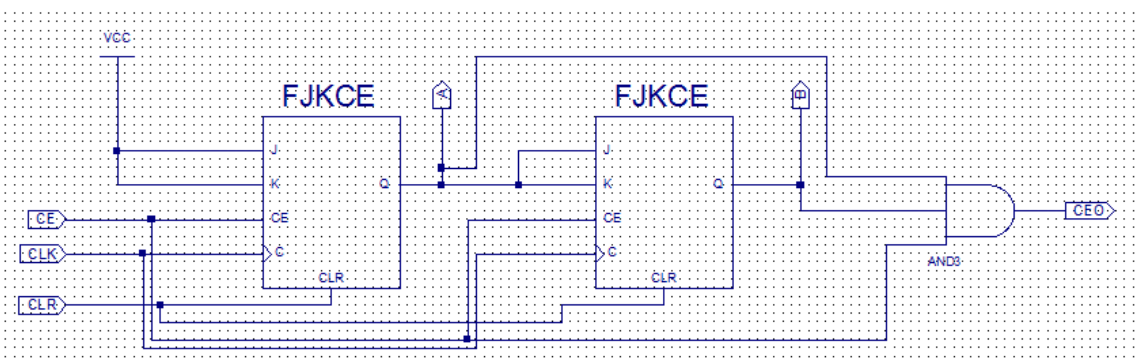

Figure 1: Two-Bit Schematic

CE is clock enable (Q can change only if CLR LO and CE HI). That's why the CEO is the AND-ing of A,B, and CE.

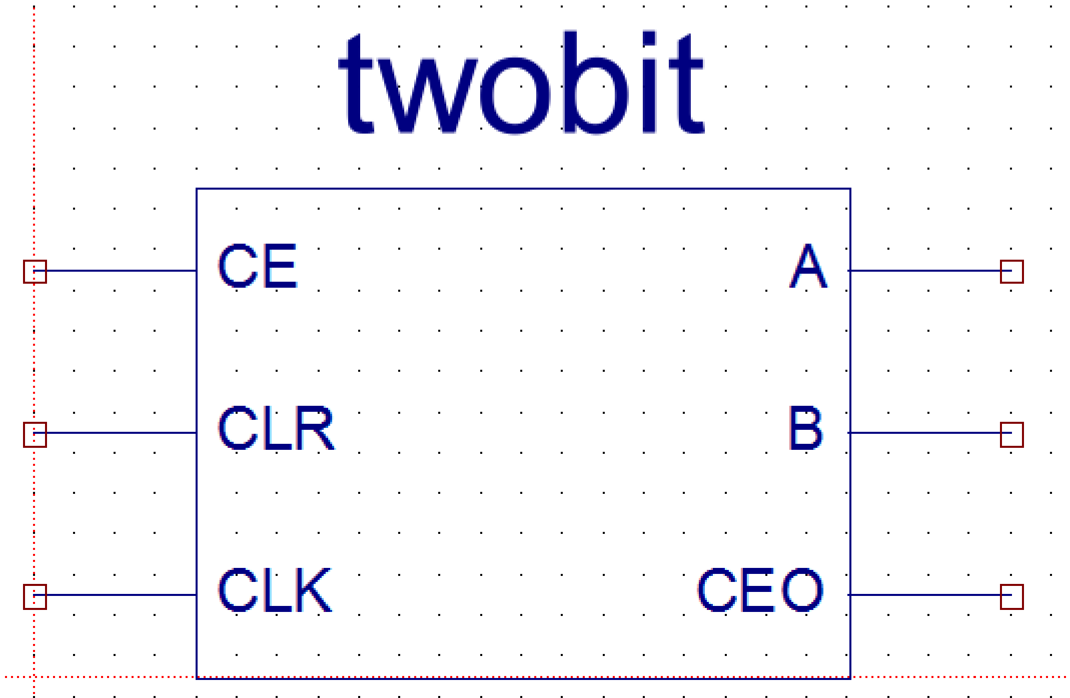

Figure 2: Two-bit Symbol

I cascade two Two-but adders according to the following schematic bearing in mind our most significant bit assignment and setting up a proper clock divider.

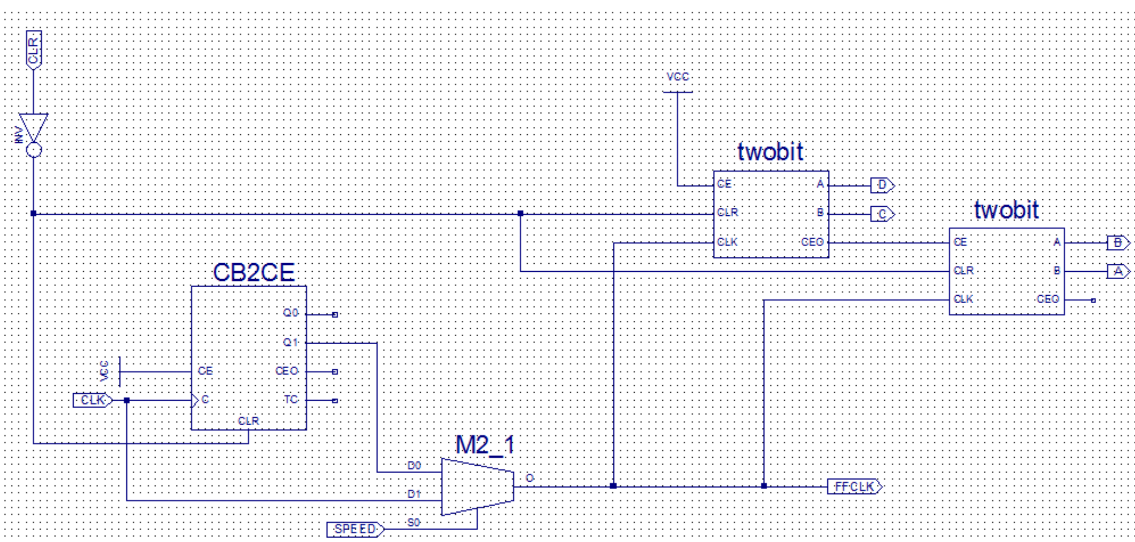

Figure 3: Four Bit Adder

Speed here determines the speed of the clock.

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Now for the test bench which is slightly different in this lab since I have to simulate more than one processes.

```
RESET : PROCESS
   BEGIN
      CLR <= '0';
             WAIT FOR 10ns;
             CLR <= '1';
             WAIT;
   END PROCESS;
CLOCK :PROCESS
       BEGIN
             CLK <= '0';
             WAIT FOR 100ns;
             CLK <= '1';
             WAIT FOR 100ns;
       END PROCESS;
SPD :PROCESS
       BEGIN
             SPEED <= '1';
             WAIT;
       END PROCESS;
```

Having the test bench enables us to generate the waveforms:

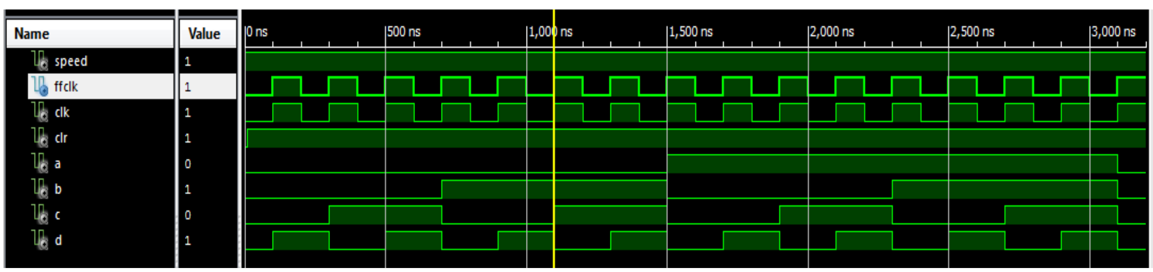

Figure 4: Waveforms

Now to implement this on hardware using the PlanAhead software to assign pins according to these physical constraints:

```
# PlanAhead Generated
physical constraints
NET "D" LOC = M5;
NET "C" LOC = M11;
NET "B" LOC = P7;
NET "A" LOC = P6;
NET "FFCLK" LOC = G1;
NET "CLK" LOC = C8;
NET "SPEED" LOC = E2;
NET "CLR" LOC = N3;
```

A, B, C, D, and FFCLK are all LED bulbs that turn on in sequence to indicate a decimal digit for example in the waveform I see 0101 which is five this means P6 is off, P7 is on, M11 is off and m is on.

Results

I see that the board coincides with the waveforms displaying all decimal numbers between 0 and 15 in binary (0 and 1) such that 0 means the bulb is off and 1 means the bulb is on. The speed, and CLR are switches such that switching the Speed (E2) up increases the rate at which the counters increments the count and switching CLR(N3) up clears everything.

Conclusion

I conclude that counters are very simple yet very important components. They are used in several different field and can be utilized for several tasks.