

# Hema C. P. Movva

hemacp@utexas.edu

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<b>Education</b>	Ph.D., Electrical Engineering, The University of Texas at Austin	Expected 2018
	M.S.E., Electrical Engineering, The University of Texas at Austin	2012
	B.Tech., Electrical Engineering, Indian Institute of Technology Bombay	2009
<b>Publications</b>	HCP Movva et al., Tunable $\Gamma - K$ Valley Populations in Hole-Doped Trilayer WSe <sub>2</sub> , <i>Phys. Rev. Lett.</i> <b>120</b> , 107703 (2018)	
	HCP Movva et al., Density-Dependent Quantum Hall States and Zeeman Splitting in Monolayer and Bilayer WSe <sub>2</sub> , <i>Phys. Rev. Lett.</i> <b>118</b> , 247701 (2017)	
	HCP Movva et al., High-Mobility Holes in Dual-Gated WSe <sub>2</sub> Field-Effect Transistors, <i>ACS Nano</i> <b>9</b> , 10402 (2015)	
<b>Experience</b>	<b>Research Assistant</b> , The University of Texas at Austin	
	Ongoing	
	<ul style="list-style-type: none"><li>• Ph.D. advisors: Emanuel Tutuc, Sanjay Banerjee</li><li>• Electrical transport in transition metal dichalcogenide (TMD) heterostructures</li><li>• Fabrication of FETs using atomically thin TMDs such as WSe<sub>2</sub>, MoS<sub>2</sub>, etc.</li><li>• Magnetotransport measurements in high-mobility TMD FETs</li><li>• Tunneling phenomena in TMD heterostructure FETs</li></ul>	
	<b>Research Assistant</b> , The University of Texas at Austin	
	Aug '10 - May '12	
	<ul style="list-style-type: none"><li>• M.S.E. advisor: Sanjay Banerjee</li><li>• Surface charge transfer doping of graphene for use in self-aligned FETs</li><li>• Fabricated graphene FETs with chemically doped source/drain access regions</li></ul>	
	<b>Engineer R&amp;D</b> , Solar Semiconductor Inc., Hyderabad, India	
	Jun '09 - Aug '10	
	<ul style="list-style-type: none"><li>• Modeled wattage losses in c-Si photovoltaic modules</li><li>• Developed distributed circuit models for c-Si solar cells and modules</li><li>• Managed sun simulators for solar cell and module characterization</li></ul>	
	<b>Circuit Design Intern</b> , Texas Instruments, Bangalore, India	
	May '08 - Aug '08	
	<ul style="list-style-type: none"><li>• Designed a high-speed dynamic latch based voltage comparator</li><li>• Designed a 250 MSPS 6-bit SAR analog-to-digital convertor</li></ul>	
<b>Honors</b>	Best Paper Award, 74 <sup>th</sup> IEEE Device Research Conference	2016
	Best Poster Award, 73 <sup>rd</sup> IEEE Device Research Conference	2015
	Best Poster Award, 9 <sup>th</sup> International Nanotechnology Conference (INC9)	2013
	Silver Medal, 37 <sup>th</sup> International Physics Olympiad	2005
	National Talent Search scholarship, India	2003
<b>Service</b>	<b>Reviewer</b> , IEEE Trans. Electron Dev., ACS Appl. Mater. Interfaces, Nanoscale	
	<b>Mentor</b> , Research Experience for High School Young Scholars	Sum. '17
	<b>President</b> , Japan Karate Association of Austin	May '13 - May '15
<b>Skills</b>	<u>Fabrication:</u> Electron-beam lithography, standard cleanroom processing	
	<u>Electrical:</u> Semiconductor parameter analyzers, probe stations, He cryostats	
	<u>Metrology:</u> Atomic force microscopy, scanning electron microscopy	
	<u>Software:</u> MATLAB, LabVIEW, C	