

Cascaded H-bridge Multilevel Inverter

A report submitted in partial fulfillment of the requirements for the
Course EE449 - Major Project
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APRIL 2023

DECLARATION

We hereby declare that the Report of the Major Project titled “**CASCADED H-BRIDGE MULTILEVEL INVERTER**” which is being submitted to the **National Institute of Technology Karnataka, Surathkal**, in fulfilment of the requirements for the award of the Degree of **Bachelor of Technology** in **Electrical and Electronics Engineering** is a *bonafide report of the work carried out by us*. The material contained in this report has not been submitted to any University or Institution for the award of any Degree.

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CERTIFICATE

This is to certify that the Major Project Work Report titled “**CASCADED H-BRIDGE MULTILEVEL INVERTER**” submitted by **HEMADARSHINI GOPAL** (Roll No.: **191EE217**), **KURUBA SAILASREE** (Roll No.: **191EE220**), **NEHA SAYYAD** (Roll No.: **191EE246**) and **VADEEPOGU RUPAN PRAKASH** (Roll No.: **191EE159**) as the record of the work carried out by them, is *accepted as the Major Project Work Report submission in partial fulfilment of the requirements for the award of degree of Bachelor of Technology in Materials Engineering* in the Department of **Metallurgical and Materials Engineering**.

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ACKNOWLEDGEMENT

We would like to take this opportunity to express our deepest appreciation and gratitude to all those who have helped us toward the successful completion of our major project. We would like to thank our guide, Dr. Yellasiri Suresh for his continued guidance, suggestions, encouragement, and support throughout the course of this project. His presence has helped us learn and understand various new technologies in the field of Power Electronics, making it easier for us to complete this project.

Additionally, we thank our department for letting us choose the project of our interest and for providing us with the relevant resources and support when needed. We also express our heartfelt gratitude to our friends and family who have continuously supported and encouraged us in every possible way.

ABSTRACT

In this report a brief review on multilevel inverters and different multilevel inverter topologies are discussed. Inverter is a power electronic device that converts DC power into AC power at desired output voltage and frequency. Multilevel inverters nowadays have become an interesting area in the field of industrial applications. This Project mainly involves analysis of Cascaded H-bridge topology, conduction loss and switching loss calculations, LC filter design and different SPWM modulation techniques. It also involves implementing 3-level CHB MLI with and without SPWM on the Arduino UNO board.

Key Words: Inverter, Multilevel inverters, Cascaded H-bridge, 3-level CHB MLI, 5-level CHB MLI, SPWM.

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1. INTRODUCTION

1.1 Inverter

Inverters are power electronic devices that regulate the flow of electrical power. An inverter converts the DC voltage to an AC voltage. The batteries in the inverter store energy in the form of direct current and the home appliances we use need alternating current. The inverter can be utilized to power our appliances during such emergencies as power outages.

1.2 Working of an inverter

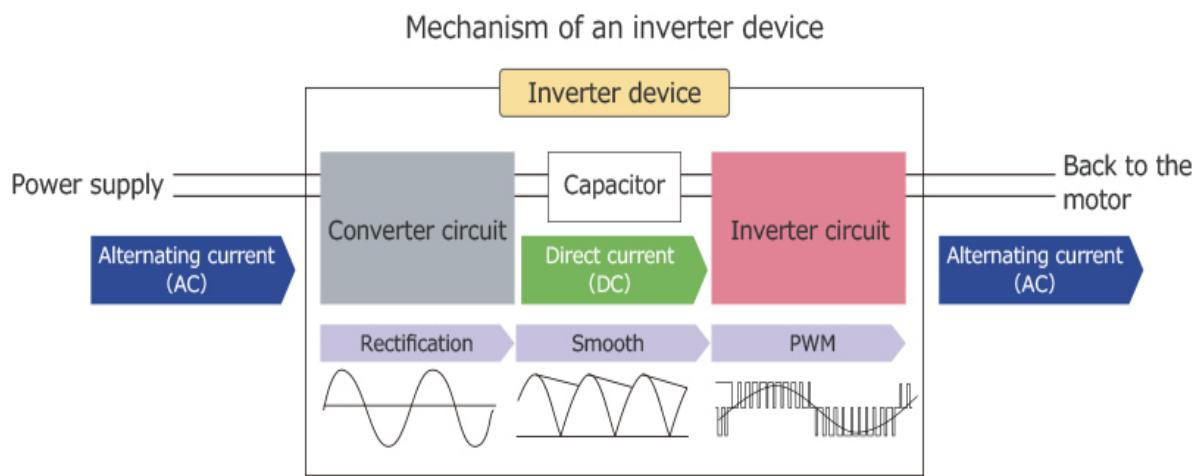


Fig 1: Inverter

Converter circuit used in the front part constantly converts alternating current to direct current. This process is called rectification. Diode is used to pass electricity in a forward direction to convert it into direct current, but not in the reverse direction.

Diode's structure is shaped like a bridge so that it can pass the negative peak in a forward direction. This is called full-wave rectification due to the fact that it transforms both the forward and negative wave peaks. Ripple voltage fluctuations will remain, in order to clean this up the capacitor is repeatedly charged and discharged, gently smoothing and changing the waveform close to that of direct current.

The inverter circuit then outputs alternating current with varying voltage and frequency. The DC/AC conversion mechanism switches power transistors such as "IGBT (Insulated Gate Bipolar Transistor) and changes the ON/OFF intervals to create pulse waves with different widths. This is called Pulse Width Modulation (PWM).

Pulse width control image

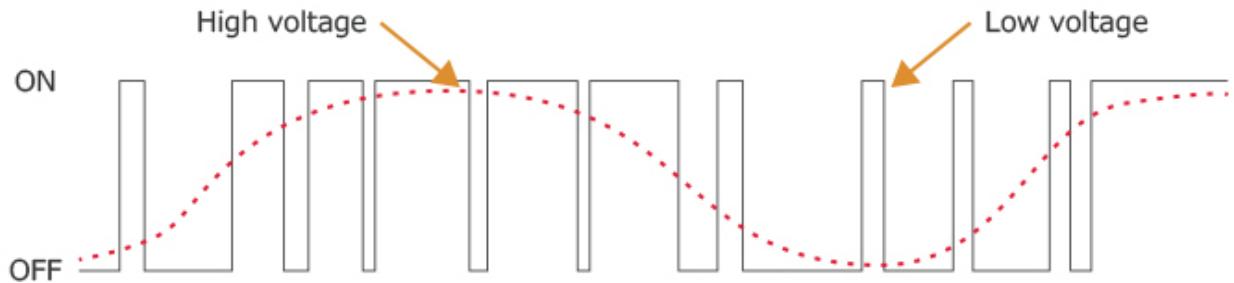


Fig 2: Pulse width control image

1.3 Difference between UPS and Inverter

- The primary purpose of a UPS is to store electrical power, whereas an inverter transforms AC power into DC power.
- In the event of a power failure, the UPS will switch from mains to battery immediately, but the inverter will be delayed for a time.
- UPS connects directly to the appliance, while the inverter is first connected to the battery and then to the appliance circuit.

1.4 Types of inverters

The Single-phase inverters are divided into two types:

- Half-bridge inverter
- Full-bridge inverter.

Half Bridge Inverter:

It consists of two switches, voltage sources of voltage equal to $V_{dc}/2$. The switches are balanced with each other so that when one switch is activated, another switch is automatically deactivated.

Full Bridge Inverter:

A full-bridge inverter circuit converts direct current to alternating current. The components required for conversion are two times more than that used in single phase Half bridge inverters. The output will be equal to the given input i.e. V_{dc} .

1.5 Applications of an inverter

The inverter is used for emergency backup in case of power failure. It turns on electrical appliances when the main power is turned off. They are used in many applications such as:

- Small car adapters for offices, home applications, large grid systems, solar power

systems.

- UPS-Uninterruptible power supplies
- An inverter is the basic building block of an SMPS- switched mode power supply.
- These can be used in Centrifugal fans, pumps, mixers, extruders, test stands, conveyors, metering pumps and Web-handling equipment.

2. MULTILEVEL INVERTER

2.1 Definition

Some devices in industries require medium or low power to operate. Using a high power source for all industrial loads can be beneficial for some high power motors, while it can be detrimental to others. The multi-level inverter is like an inverter that provides high output power from a medium voltage source such as batteries, super capacitors, and solar panels.

The multi-level inverter (MLI) is an improved form of a two-stage inverter. In a multi-level inverter we do not process two-level voltage instead in order to create a smoother stepped output waveform, more than two voltage levels are combined together. The smoothness of the waveform is proportional to the voltage levels, as we increase the voltage level the waveform will be smoother but the circuit complexity will increase.

2.2 Difference between inverter and multilevel inverter

In recent years, more attention has been paid to high power multistage converters. Better power quality, smaller output filter, lower output d_v/d_t stress, increased modularity and reliability, and use of low voltage semiconductors in high voltage applications These are just a few of the advantages of these converters over conventional two- or three-level converters.

Sl. No	Conventional Inverter	Multilevel Inverter
1.	THD is high in the output waveform	THD is low in the output waveform
2.	High Switching stresses	Low Switching stresses
3.	Not used for high Voltage applications	Used for High voltage applications
4.	High voltage levels cannot be produced	Low voltage levels cannot be produced
5.	High d_v/d_t and EMI	Low d_v/d_t and EMI
6.	High switching frequency, increased switching losses	Lower switching frequency, reduced switching losses

2.3 Different structures of multilevel inverter

A. Diode Clamped Multilevel Inverter:

The main concept of this inverter is to use diodes and provide the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage. It is the main drawback of the diode clamped multilevel inverter.

This problem can be solved by increasing the switches, diodes, and capacitors. Due to the capacitor balancing issues, these are limited to the three levels.

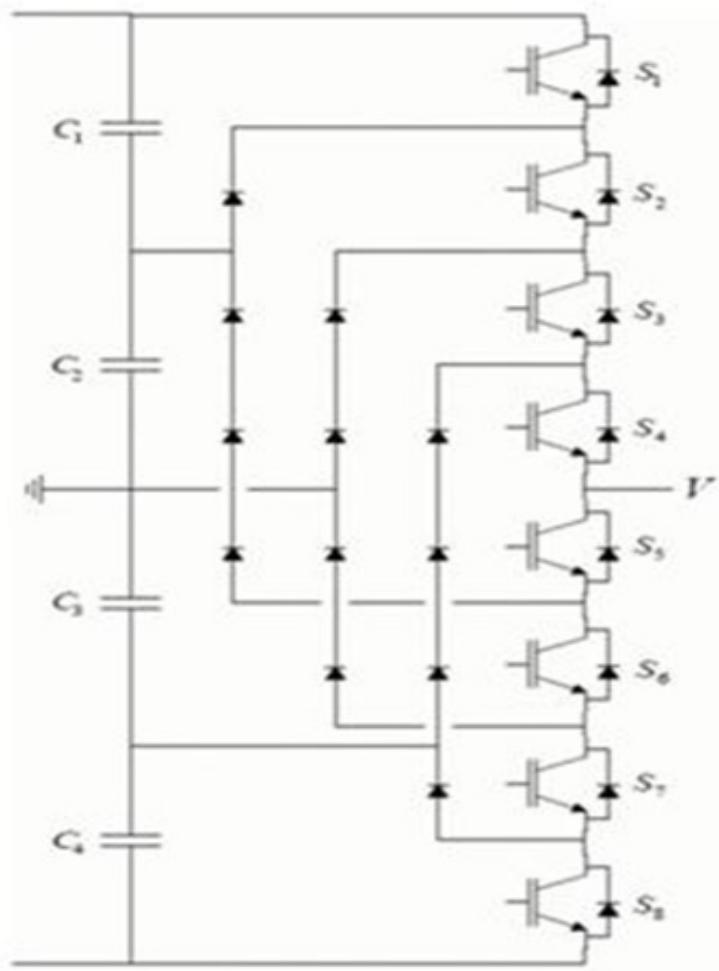


Fig 3: 5-level diode clamped

B. Flying Capacitors Multilevel Inverter:

The main concept of this inverter is to use capacitors. It is of a series connection of capacitor clamped switching cells. The capacitors transfer the limited amount of voltage to electrical devices. In this inverter switching states are like in the diode clamped inverter. Clamping diodes are not required in this type of multilevel inverters. The output is half of the input DC voltage. It is a drawback of the flying capacitors multilevel inverter. It also has the switching redundancy within the phase to balance the flying capacitors. It can control both the active and reactive power flow. But due to the high-frequency switching, switching losses will take place.

EX: 5-level flying capacitors multilevel inverter

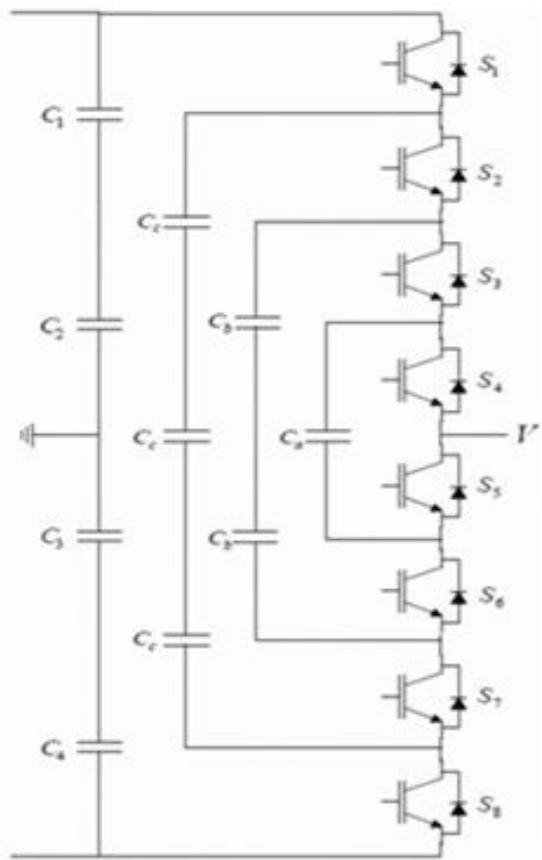


Fig 4: 5-level Flying capacitor

3. CASCADeD H- BRIDGE INVERTER

3.1 Structure

One of the basic and well-known topologies among all multilevel inverters is Cascaded H-Bridge Multilevel Inverter. It can be used for both single and three phase conversion. It uses H-Bridge including switches and diodes.

The modulation technique that applies to each cell of the inverter may be the same or different. It varies from fundamental switching frequency PWM, carrier based PWM or combination of the two different PWM methods (known as mixed / hybrid PWM method). In this project we are using Level Shifted PWM. Level Shifted PWM uses some carrier signals, which are arranged in different levels among the carriers.

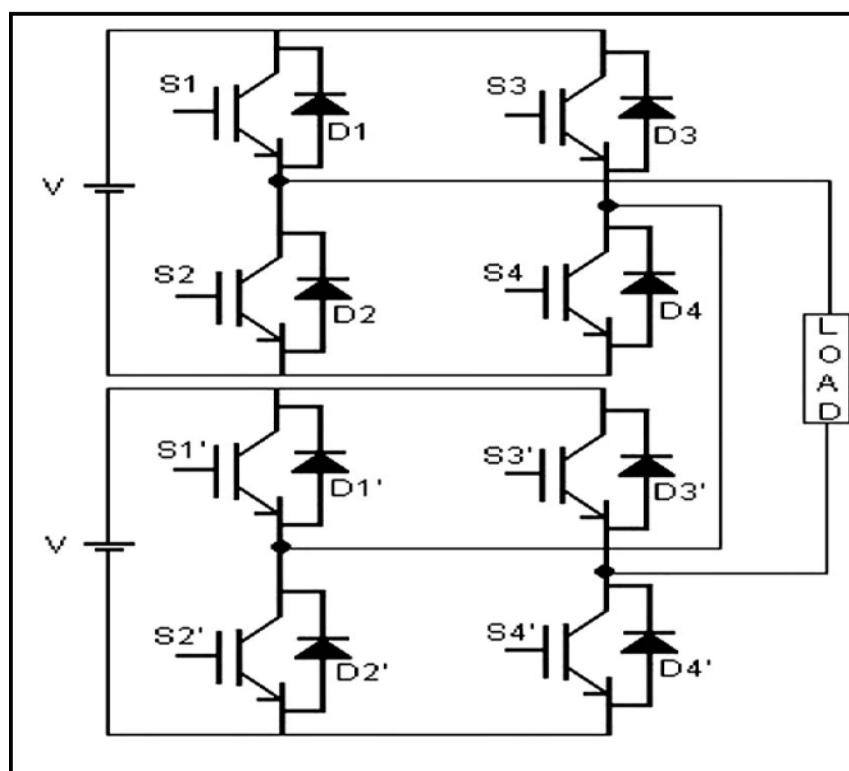


Fig 5: 5 level cascaded H-bridge

Each H-Bridge Cell consists of four switches and four diodes as shown in the Fig 5.

- Like every H-Bridge, different combinations of switch positions determine different voltages such as $V+$, $V-$ and 0.
- Two switching combinations are present for 0 volts.
- S_1 and S_3 are connected to positive voltage and S_2 and S_4 are connected to negative voltage.

3.2 Working of 3- level H-bridge inverter

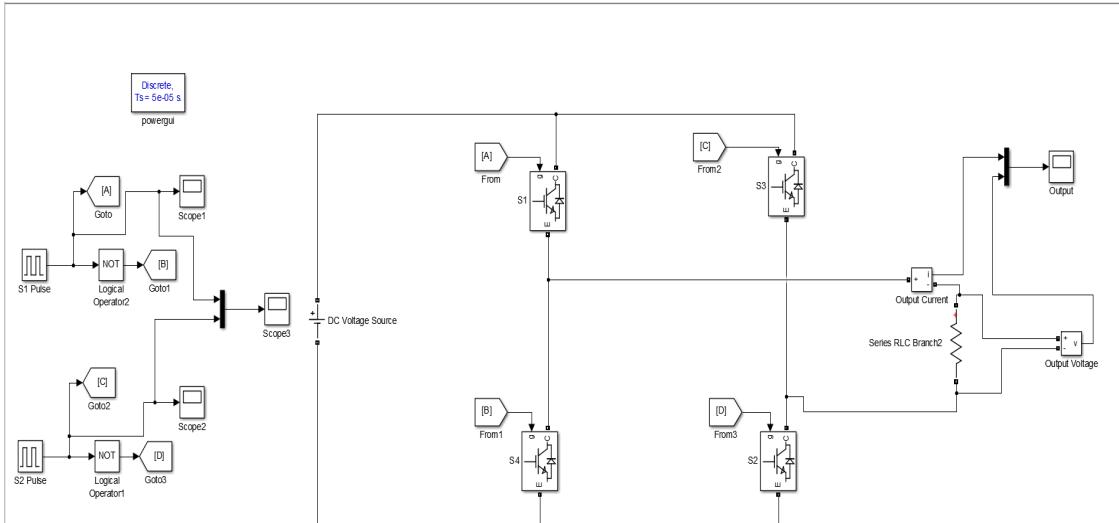


Fig 6: Circuit of 3-level H-bridge

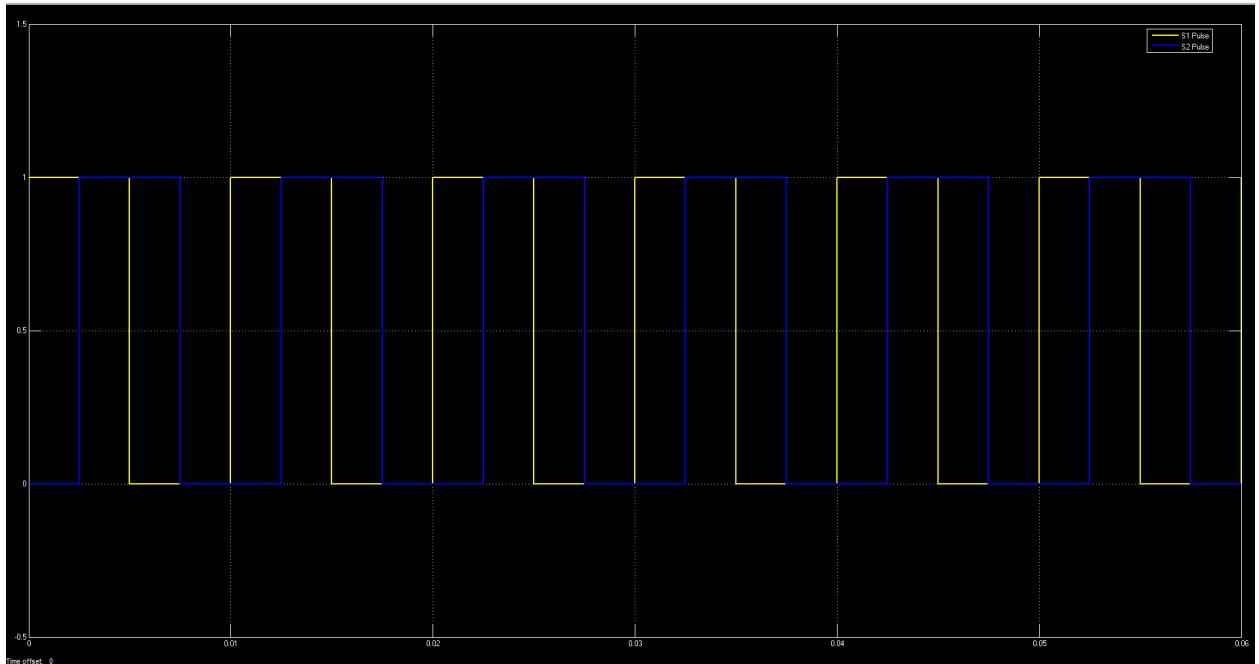


Fig 7: Switching pattern pulse

Pulse given to the switch S2 is delayed by $T/4$ sec when compared to switch S1. And the switches in the same branch have inverted pulses so that there won't be any short circuit.

The switching pattern and the output voltage is given in the below table.

Table 1: Switching pattern and output voltages

Switches States				Output Voltage
S1	S2	S3	S4	
ON	OFF	ON	OFF	0
ON	ON	OFF	OFF	V_{dc}
OFF	OFF	ON	ON	$-V_{dc}$
OFF	ON	OFF	ON	0

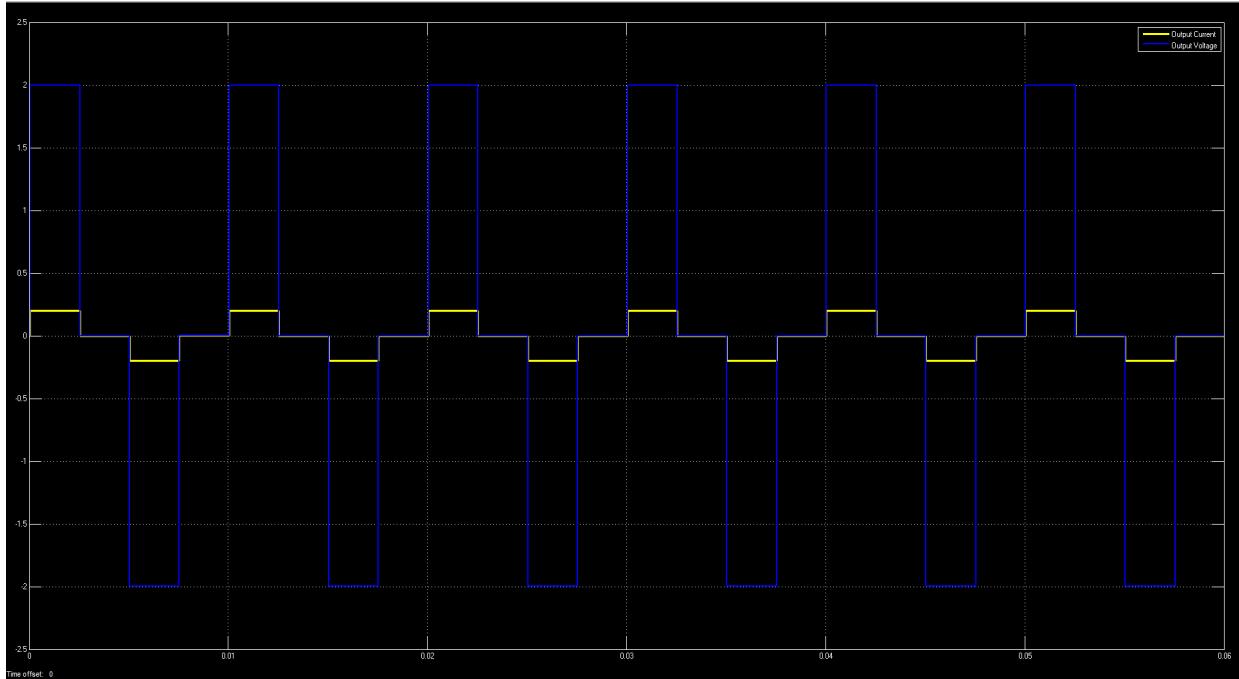


Fig 8: Output waveform of 3 level cascaded H-bridge

3.3 Advantages of Cascaded H-Bridge Multilevel Inverter

- It needs less number of components compared with diode clamped and flying capacitor inverters. Soft-switching is possible by some of the new switching methods.
- They are used to eliminate the bulky transformer required in case of conventional multi-phase inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. But these require a large number of isolated voltages to supply each cell.
- The total number of output voltage levels is more than twice that of the number of DC sources available.
- The use of separate DC sources provides isolation of between sources of each module.
- Since the outputs of all the modules gets added, the voltage rating of individual modules is low and hence stress on individual devices also gets reduced.

4. SIMULATIONS AND OBSERVATIONS

4.1 Half Bridge Inverter

Input Parameters:

T = 0.01s

V₁ = 2V

V₂ = 2V

Duty Cycle = 50%

R = 10 ohm

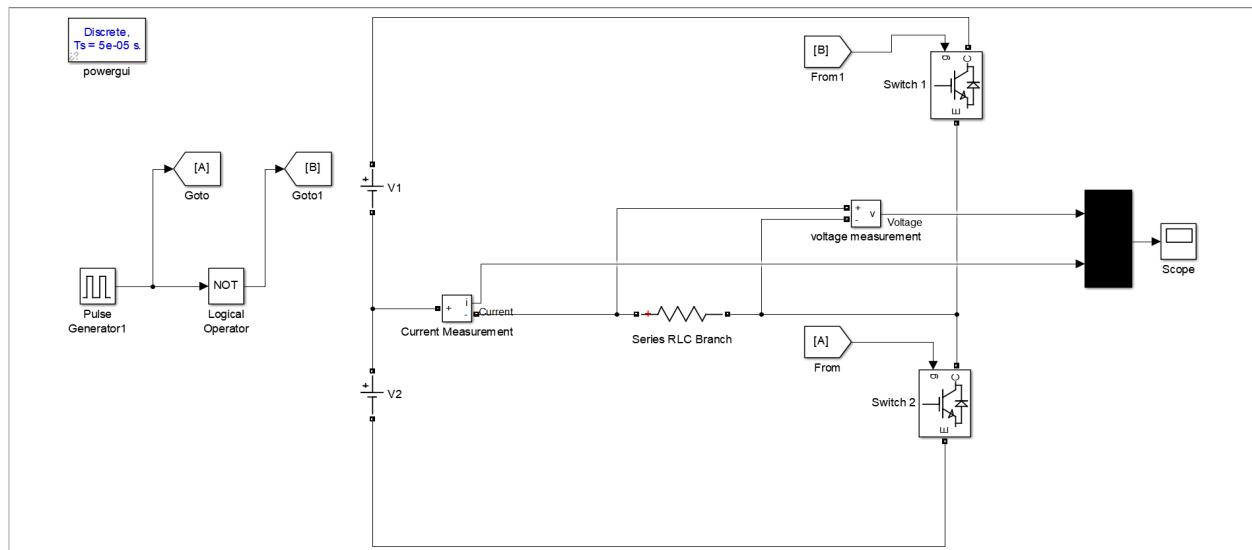


Fig 9: Circuit of Half bridge inverter

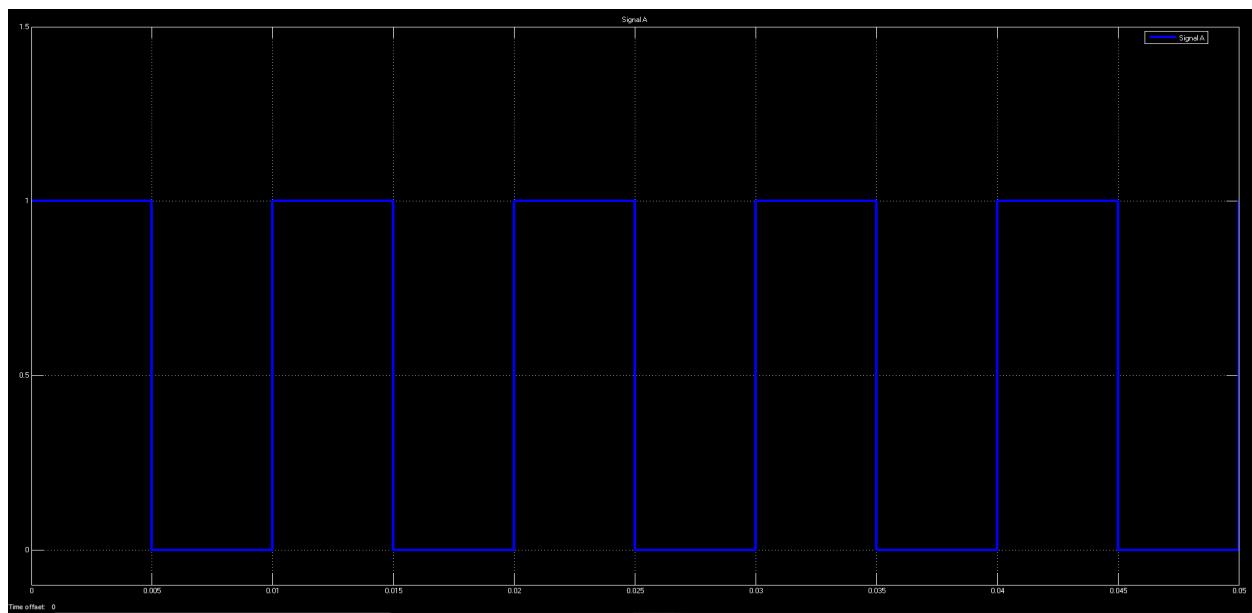


Fig 10: Input signal to S2

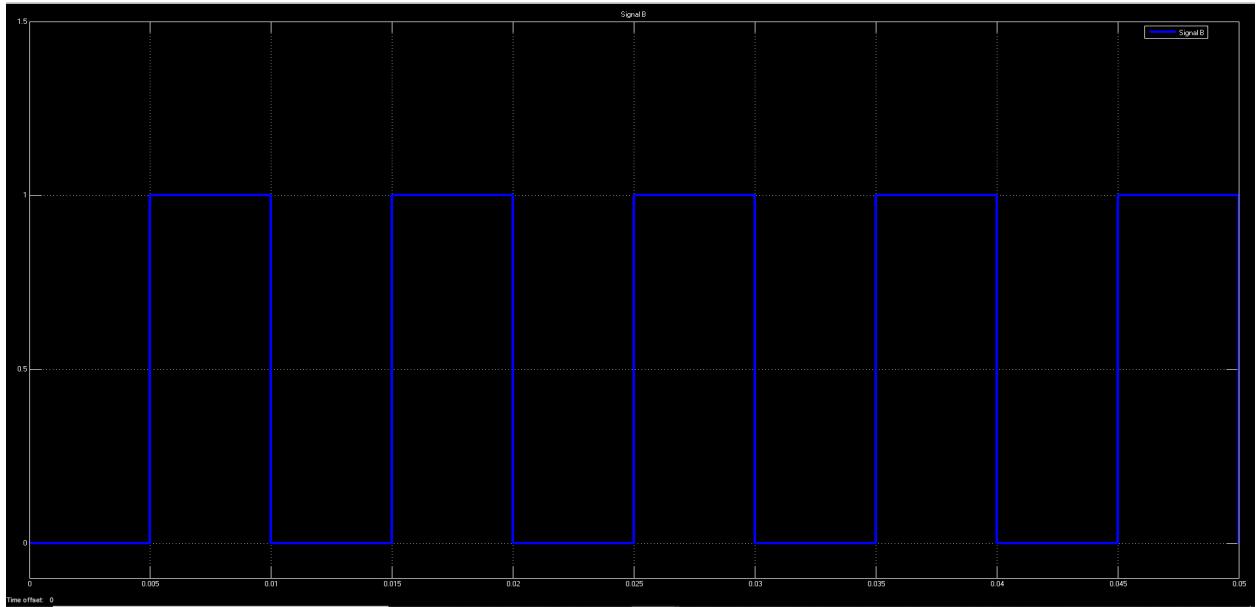


Fig 11: Input signal to S1

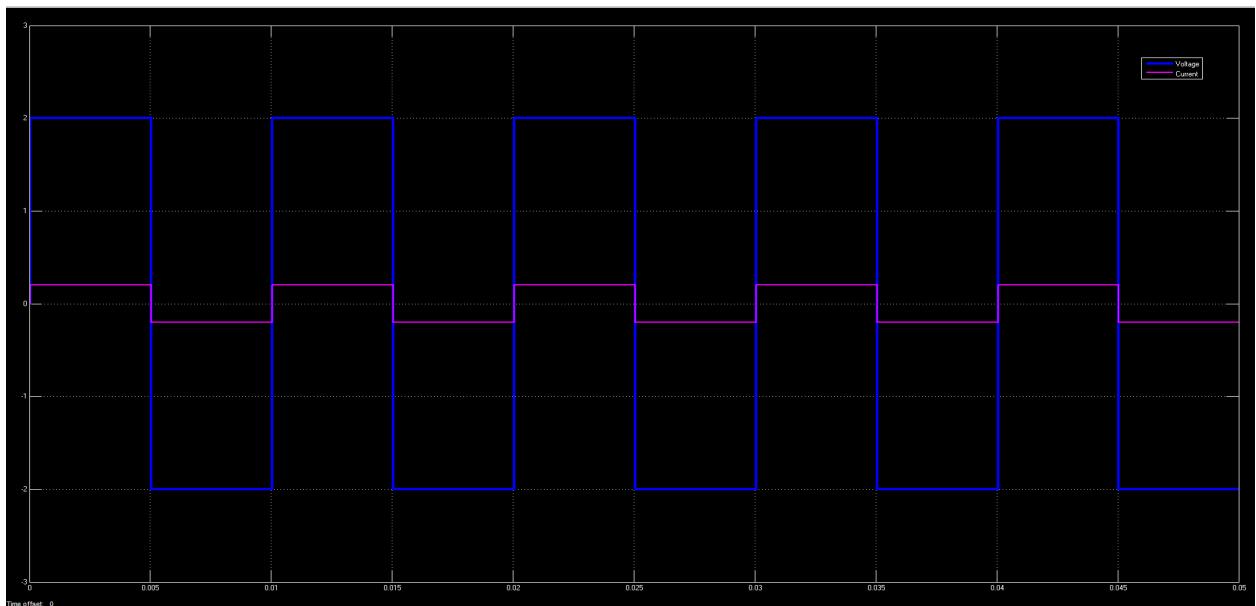


Fig 12: Output of Full bridge inverter

4.2 Full Bridge Inverter

Input Parameters:

T = 0.01s

V₁ = 2V

Duty Cycle = 50%

R = 10 ohm

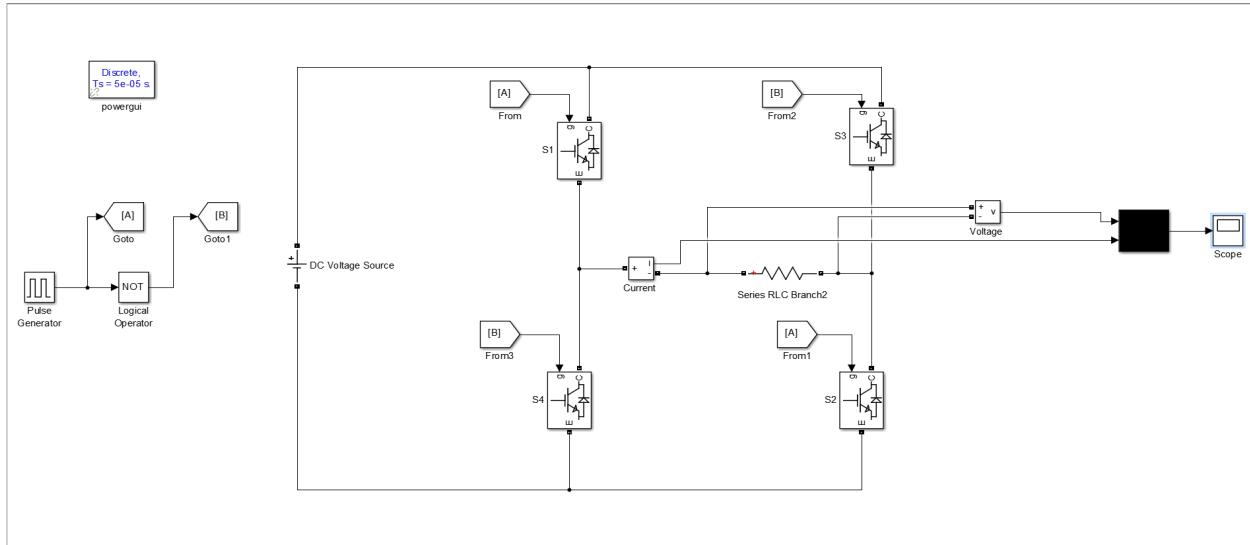


Fig 13: Circuit of Full bridge inverter

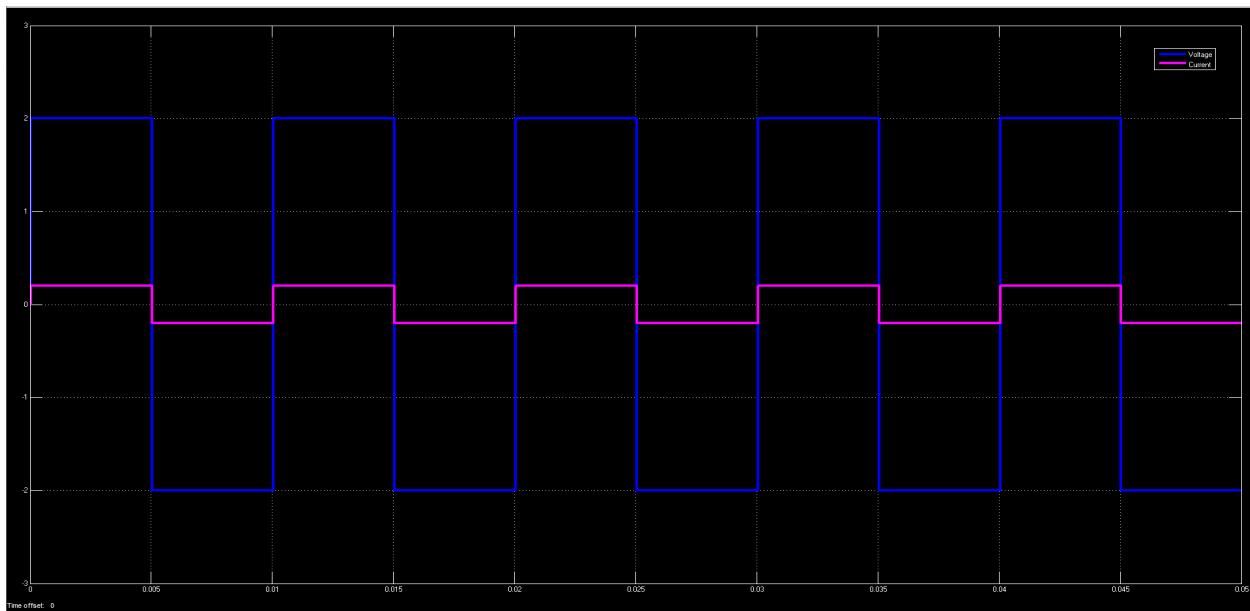


Fig 14: Output waveform of full bridge inverter

4.3 5-level Inverter

Input Parameters:

T= 0.02s

V_i=2V

R=10 ohm

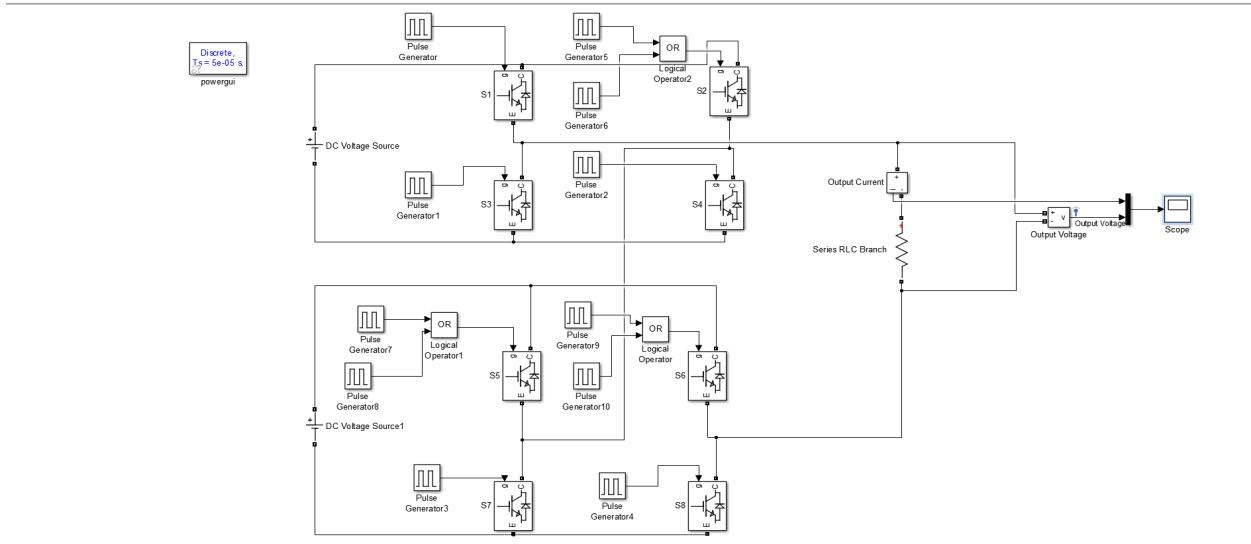


Fig 15: Circuit of 5-level inverter

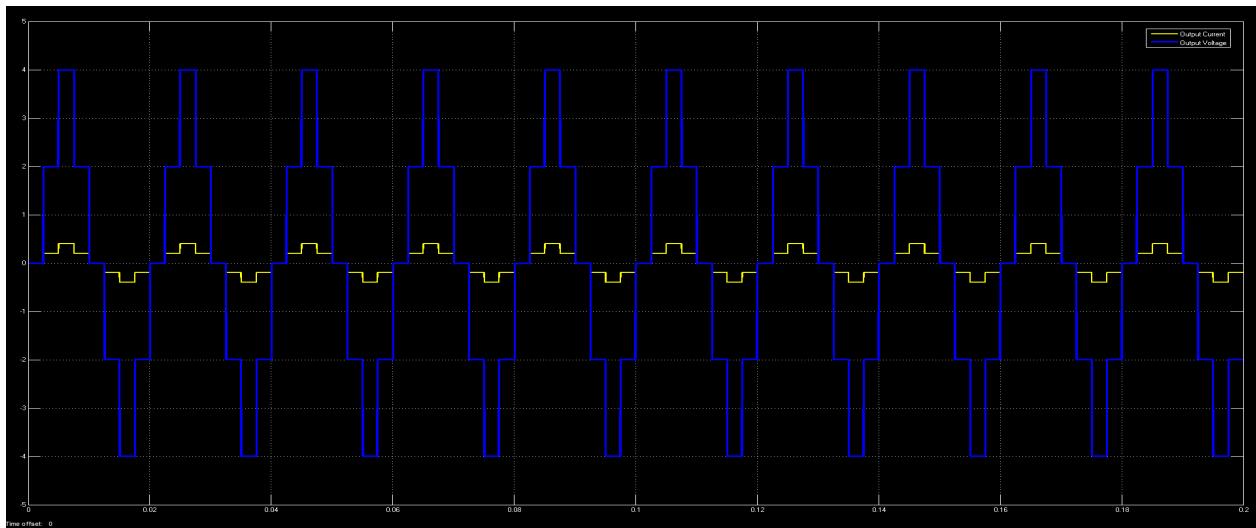


Fig 16: Output waveform of 5-level inverter

4.4 5-level SPWM inverter

Input Parameters:

T= 0.02s

V₁ = 2V

V₂ = 2V

R=10 ohm

Pulse width modulation type: Level Shifted

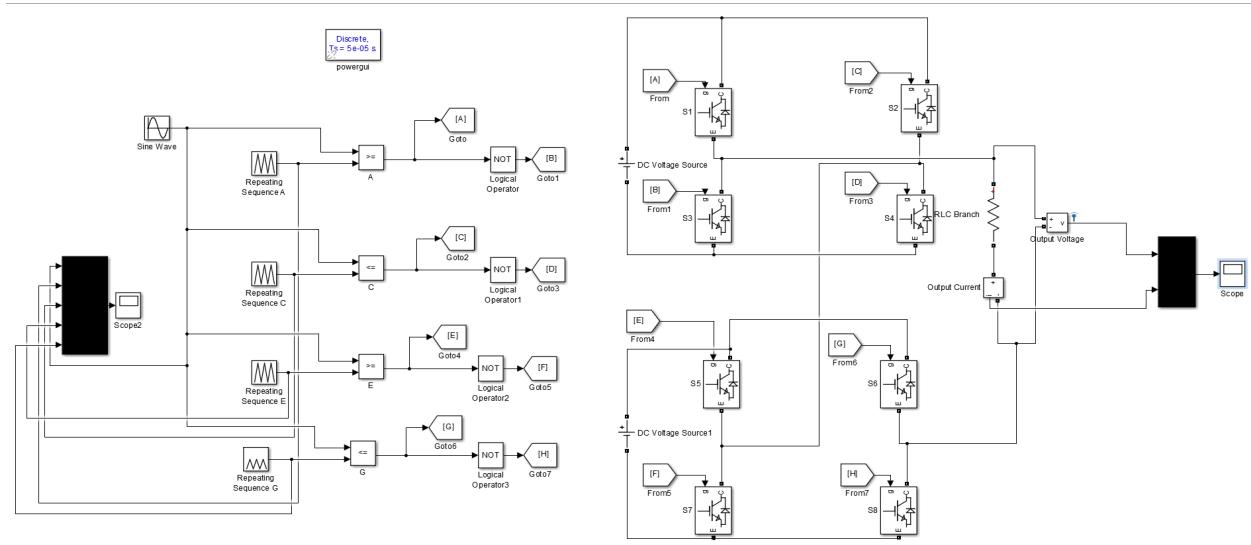


Fig 17: Circuit of 5-level SPWM inverter

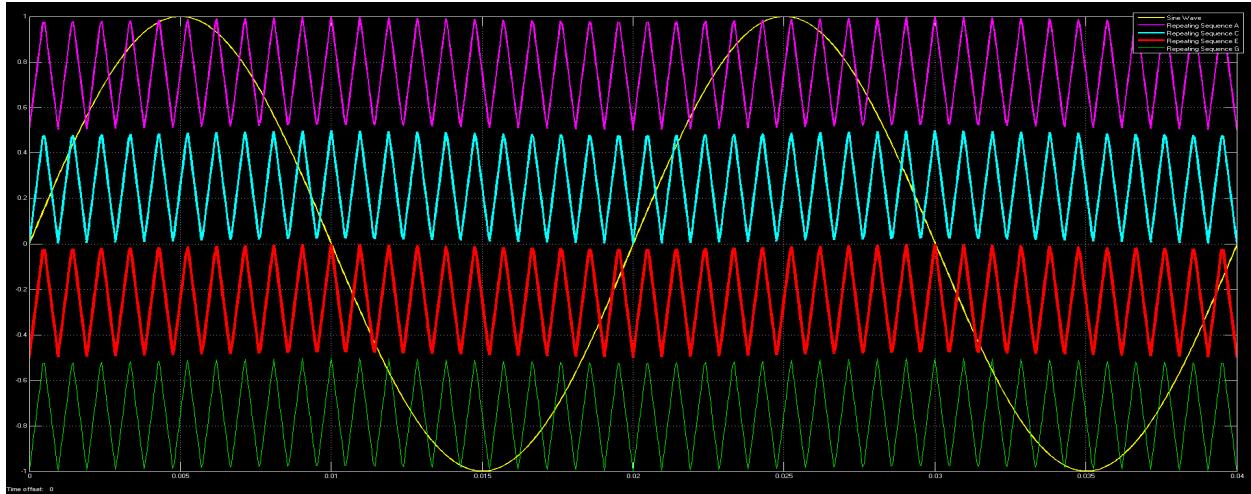


Fig 18: Switching pattern

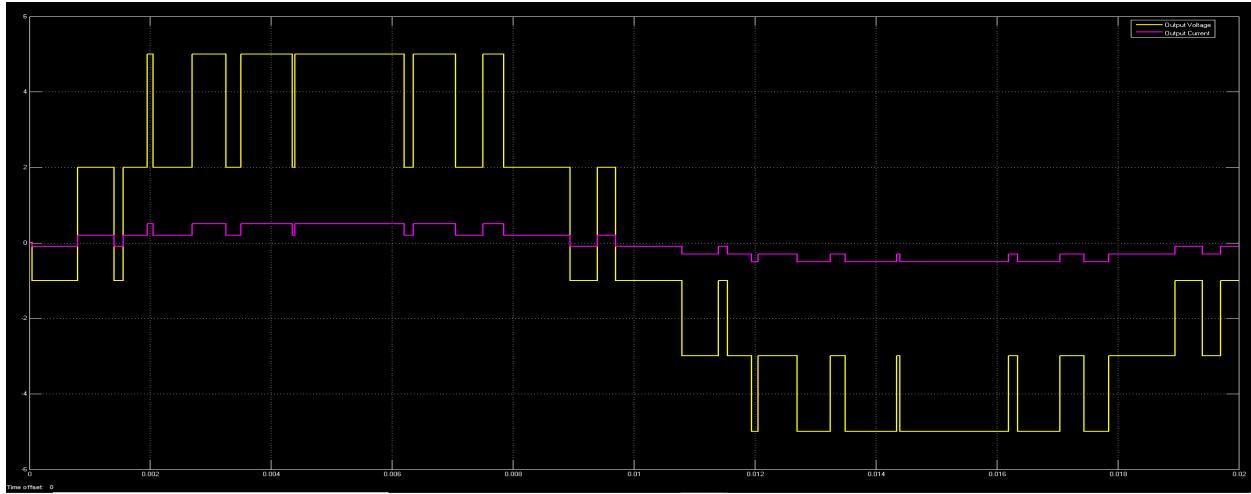


Fig 19: Output waveform of 5-level SPWM inverter

Table 2: Comparison table of Carrier wave frequency vs. THD(%)

Carrier frequency (Hz)	3-Level	5-Level
19*50	51.91	26.61
20*50	55.07	27.43
21*50	50.8	26.87
22*50	53.36	27.5
23*50	53.46	26.99
24*50	50.42	26.28
25*50	54.94	27.41

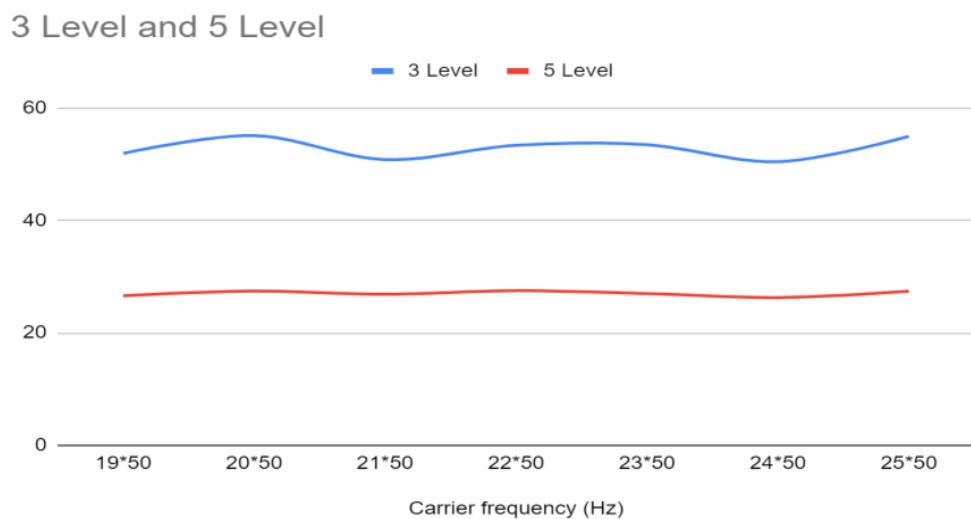


Fig 20: THD comparison graph of 3-level and 5-level

THD Calculations:

Table 2: Comparison table of modulation index and THD

Modulation Index	Bridge 1		Bridge 2		Total THD	
	THD	Amplitude	THD	Amplitude	THD	Amplitude
0.1	236.33%	3.856e-05	236.33%	0.1928	236.33%	0.1928
0.2	149.28%	8.138e-05	149.28%	0.407	149.28%	0.4069
0.3	108.53%	0.001177	108.53%	0.5887	108.53%	0.5886
0.4	76.81%	0.0001597	76.81%	0.7988	76.81%	0.7987
0.5	51.28%	0.0002024	51.28%	1.012	51.28%	1.012
0.6	312.72%	0.09628	41.24%	1.103	44.47%	1.2
0.7	178.36%	0.254	38.31%	1.157	42.14%	1.411
0.8	126.73%	0.4154	36.36%	1.183	38.48%	1.598
0.9	91.89%	0.598	35.73%	1.204	33.58%	1.802
1	64.96%	0.7841	35.89%	1.214	27.11%	1.988

MODULATION INDEX vs THD

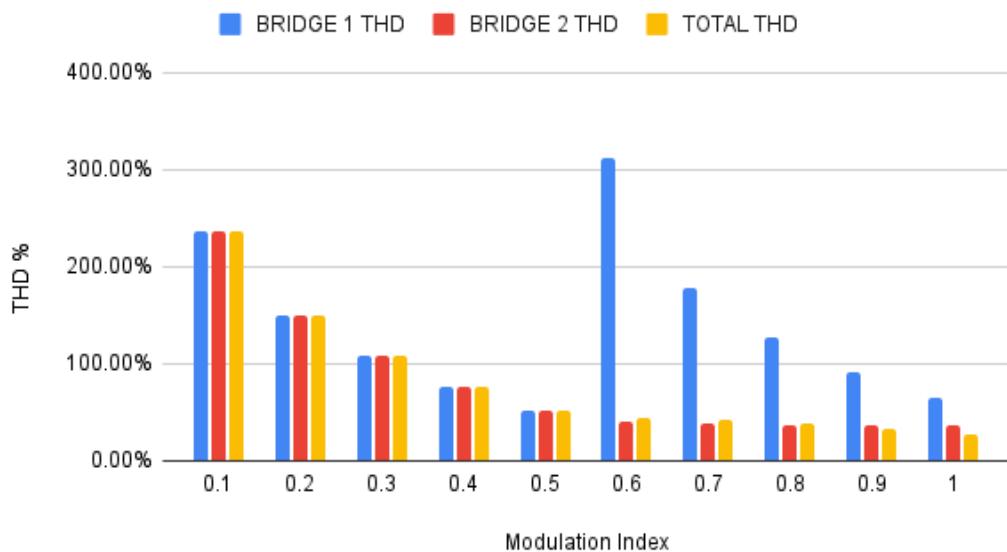


Fig 21: Modulation index vs THD

4.5 Modulation index and how it affects the output:

$$\text{Amplitude modulation index } (m_a) = V_{\text{ref}} / V_c,$$

where V_c and V_{ref} are carrier and reference voltages respectively.

$$\text{Frequency modulation index } (m_f) = f_c / f_{\text{ref}},$$

where f_c and f_{ref} are carrier and reference frequencies respectively.

Both, the modulation index and the carrier frequency are affecting the harmonic contents of the inverter output voltage waveform. The frequency spectrums of the unwanted harmonics are shifted towards higher frequency by increasing the carrier frequency. The total harmonic distortion (THD) factor of the inverter output voltage decreases as the modulation index increases. For carrier frequencies, greater than a certain value, the THD factor doesn't change much by further increasing the frequency of the carrier signal.

$$\text{THD} = \sqrt{\sum_{n=1,2,3..}^r \frac{V_n^2 - V_1^2}{V_1^2}}$$

V_n is the rms value of nth harmonic, V_1 is the value of the fundamental component, n is the low-order harmonics and r is the maximum harmonic included in the THD calculation.

4.6 Different Modulation Techniques

4.6.1 Phase Disposition

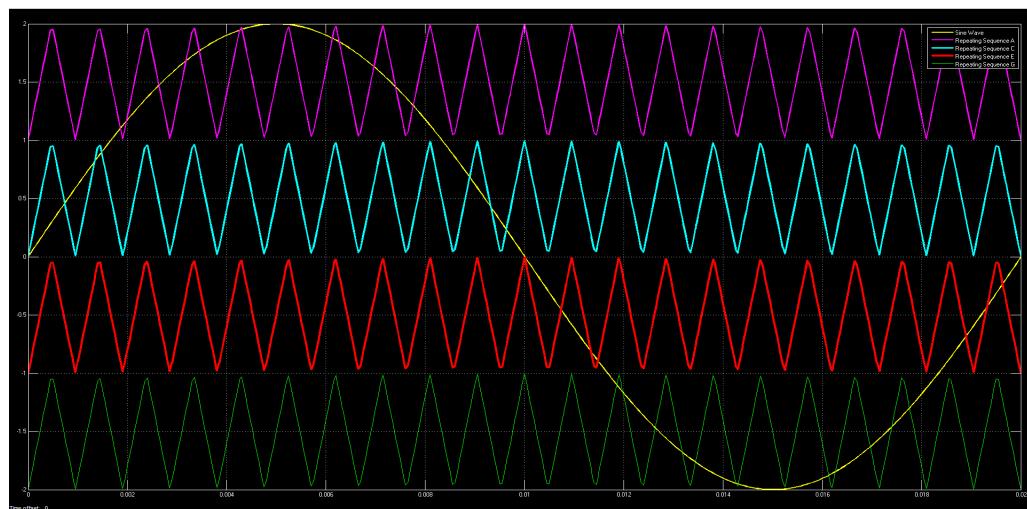


Fig 22: Phase disposition Input

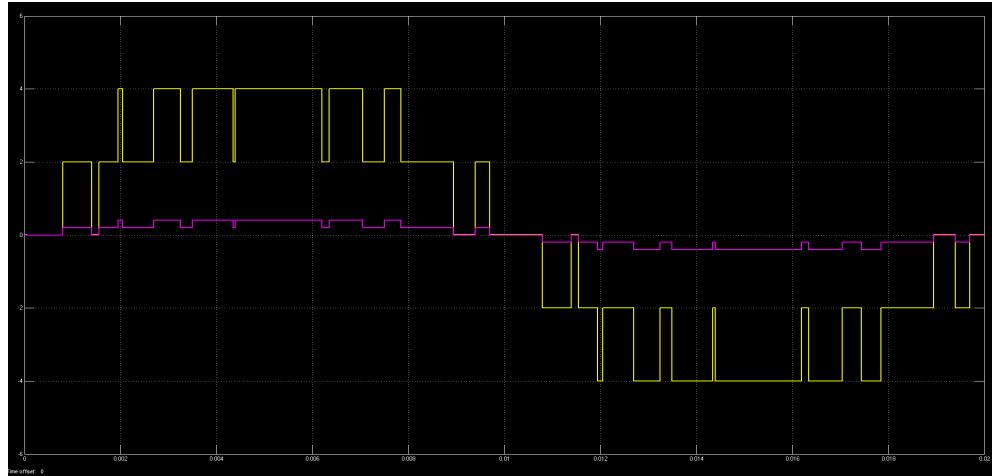


Fig 23: Phase disposition output

Fig 22 demonstrates the sine-triangle method for a five-level inverter where in modulation or sinusoidal reference signal is compared with four ($m-1$ in general) triangle waveform when the number of output voltage level is 5 ($= m$), 4 ($m-1$) carrier waveforms are arranged so that every carrier is in phase.

- The carriers are in phase across all the bands.
- The frequency modulation index $m_f = f_c / f_m$.
- The amplitude modulation index $m_a = 2A_m / A_z(m-1)$.

4.6.2 Phase Opposition and Disposition

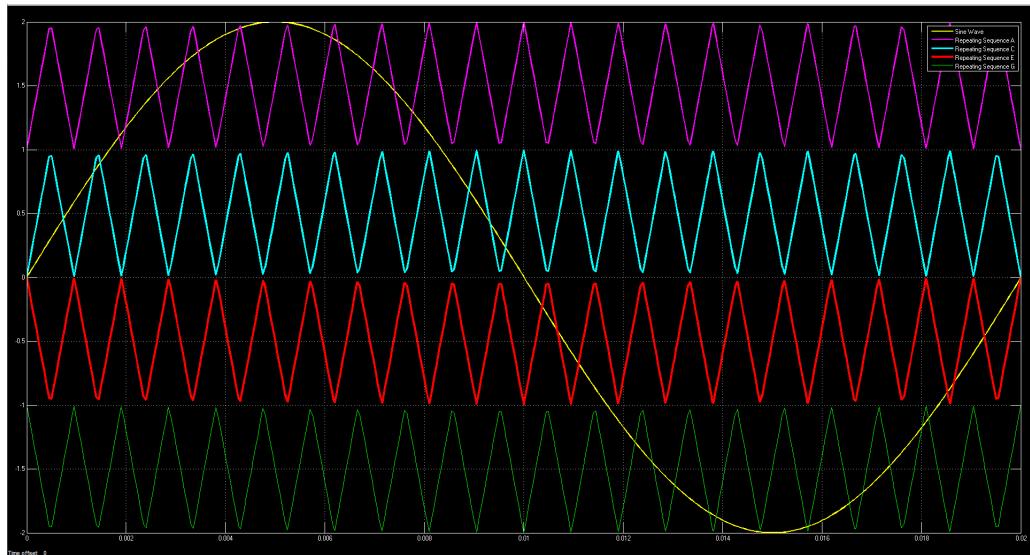


Fig 24: Phase opposition and disposition input

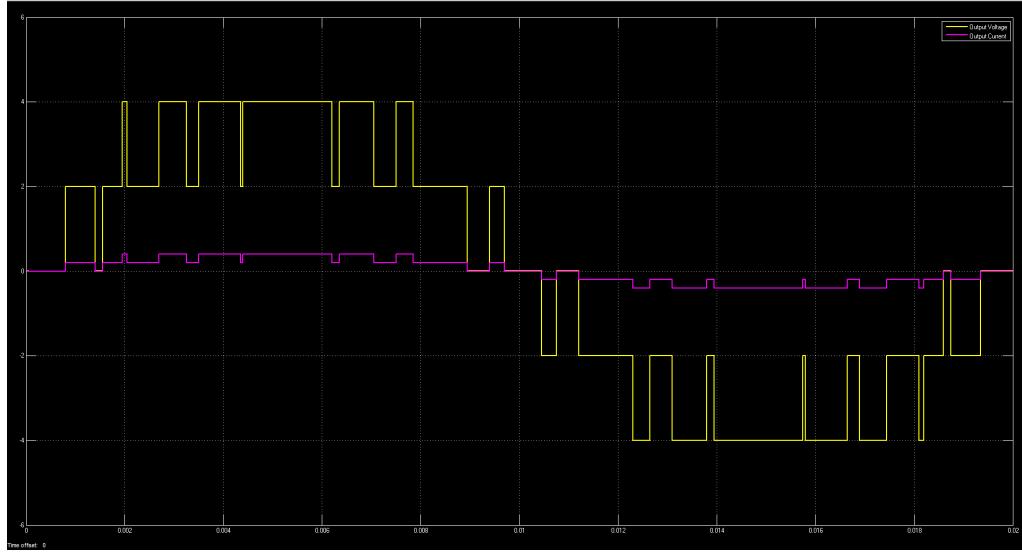


Fig 25: Phase opposition and disposition output

For POD modulation all carrier waveforms above zero reference are in phase and they are 180 degrees out of phase with those below zero. When the number of levels is m ($= 5$), $m - 1$ ($= 4$) carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180° out of phase with those below zero. The significant harmonics are located around the carrier frequency for both the phase and line-to-line voltage. Formula for m_a and m_f are the same as that of PD PWM technique.

4.6.3 Alternative Phase Opposition and Disposition

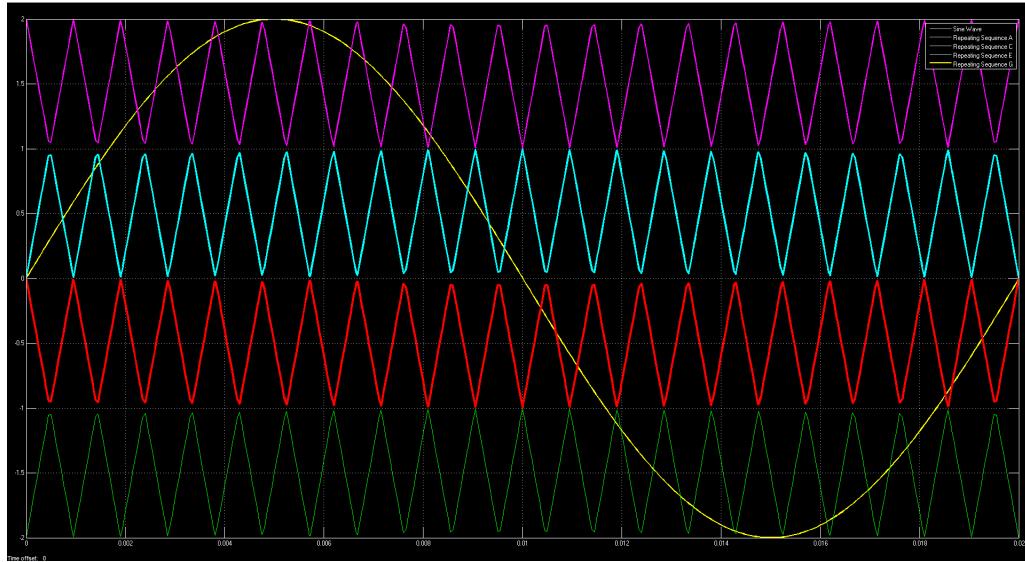


Fig 26: Alternative phase opposition and disposition input

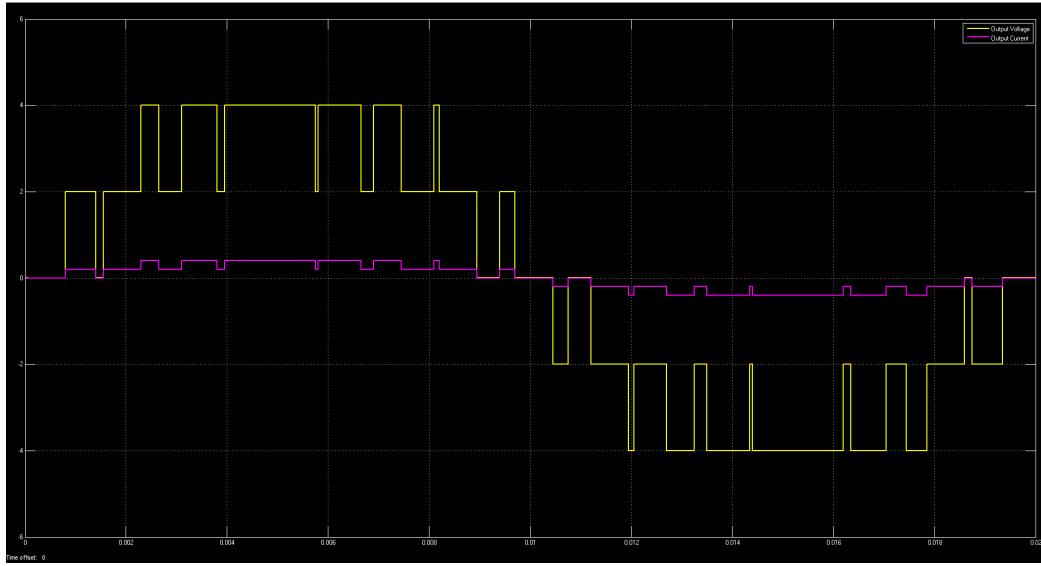


Fig 27: Alternative phase opposition and disposition output

In case of APOD modulation, every carrier wave is out of phase with its neighbor carrier by 180° . Since APOD and POD schemes in case of three level inverters are the same, a five level inverter is considered to discuss the APOD scheme. When the number of levels $m (= 5)$, $m - 1 = 4$ carrier waveforms are arranged so that every carrier waveform is out of phase with its neighbor carrier by 180° . Carriers in adjacent bands are phase displaced by 180° . With this method, the most significant harmonics are centered as sidebands around the carrier. Formulas for m_a and m_f are the same as that of the PDPWM strategy.

4.6.4 Carrier Overlapping PWM – A

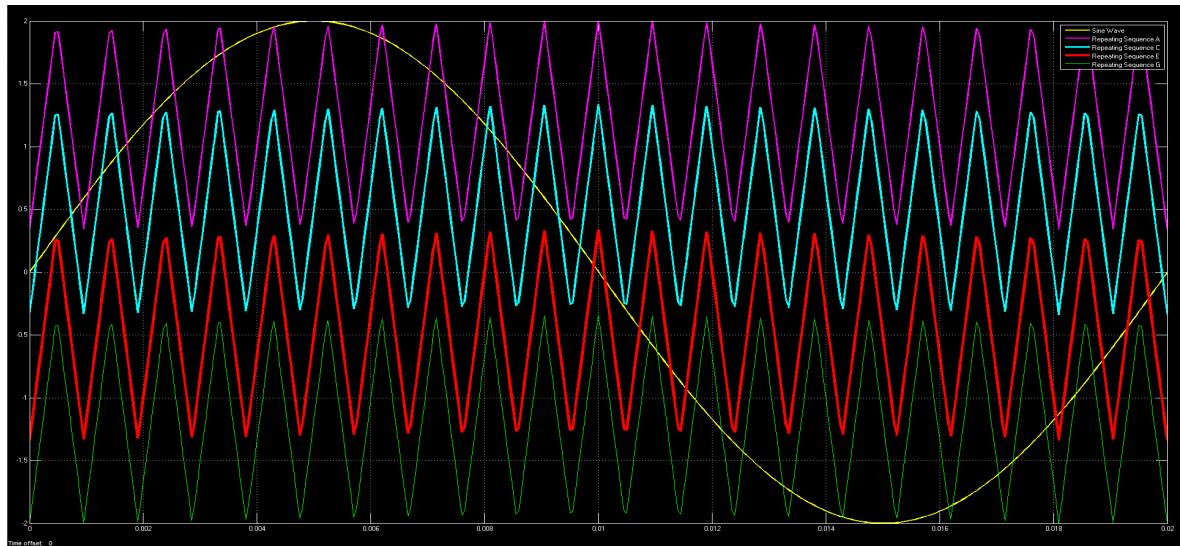


Fig 28: carrier overlapping PWM- A input

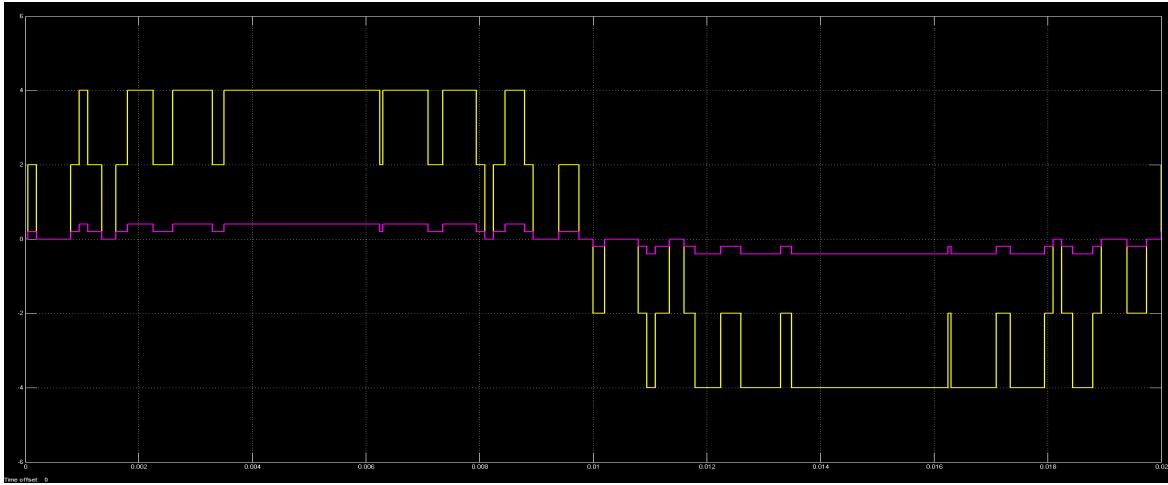


Fig 29: carrier overlapping PWM-B output

In this case it can be seen that the four carriers are overlapped with each other and the reference sine wave is placed at the middle of the four carriers. The carrier waves are in same phase.

4.6.5 Carrier Overlapping PWM – B

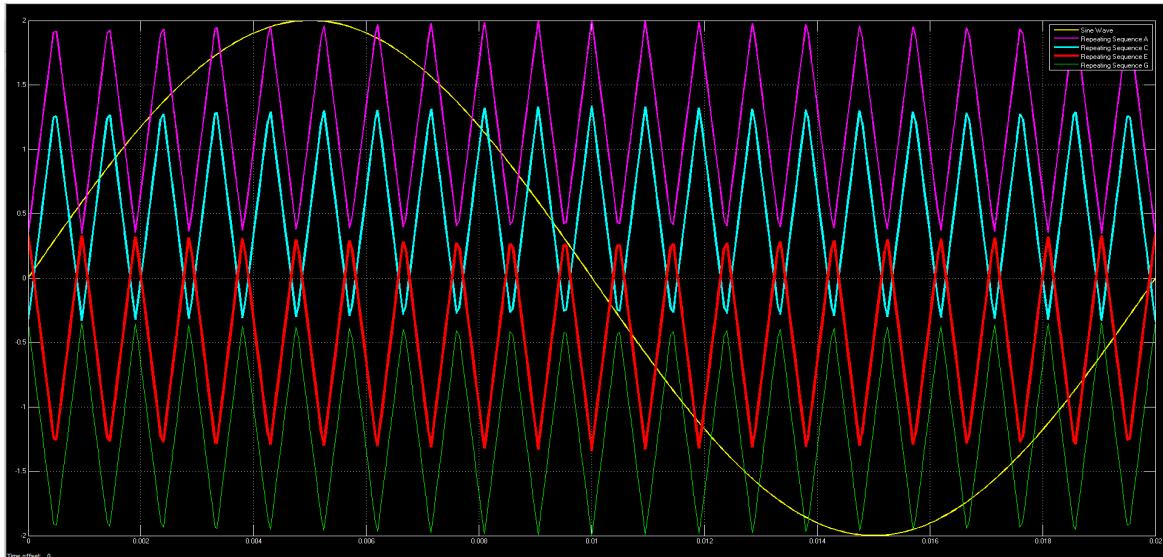


Fig 30: carrier overlapping pwm-B input

In this case it can be seen that they are divided equally into two groups according to the positive/negative average levels. In this strategy, the two groups are opposite in phase with each other while keeping in phase within the group.

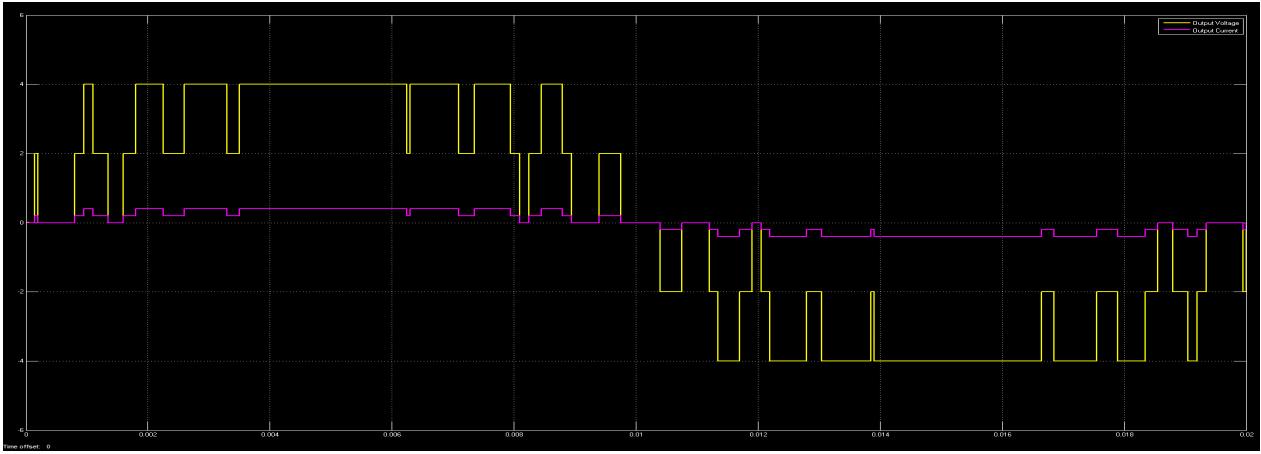


Fig 31: carrier overlapping pwm-B output

4.6.6 Carrier Overlapping PWM - C

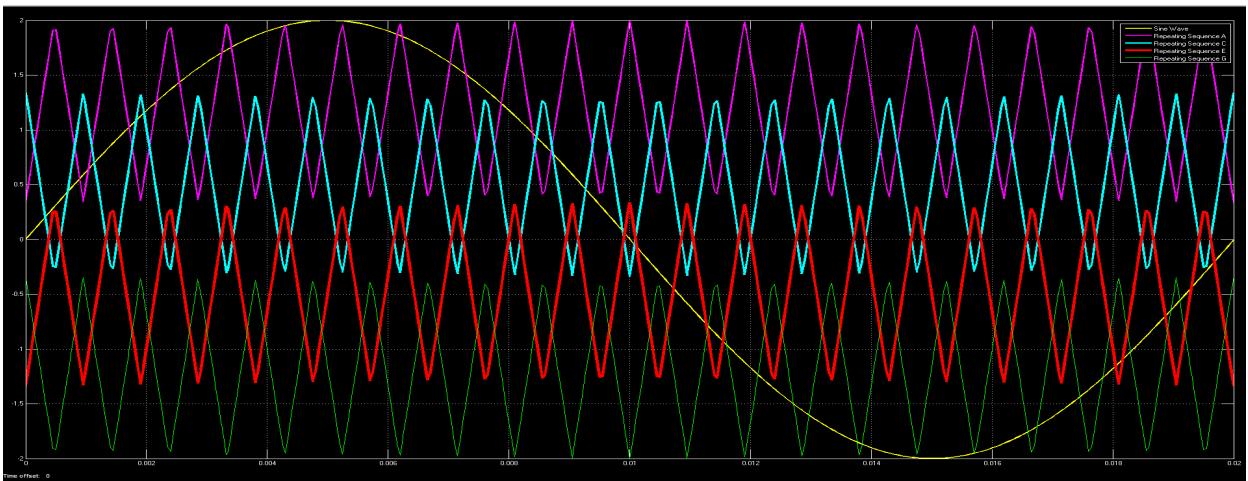


Fig 32: carrier overlapping pwm-c input

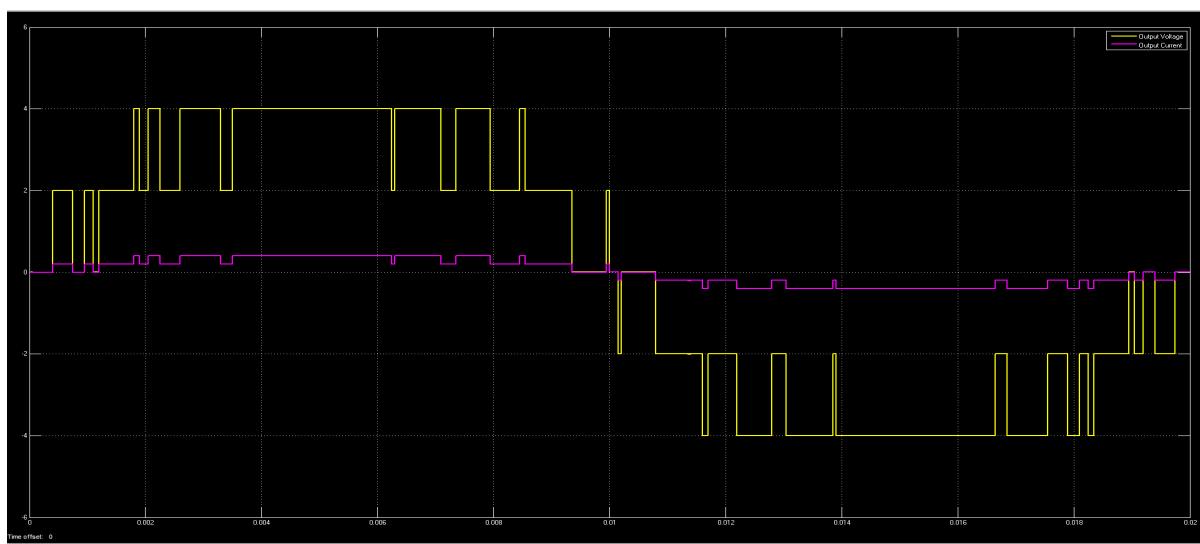


Fig 33: carrier overlapping pwm-c output

In this strategy, carriers invert their phase in turns from the previous one. It may be identified as PWM with amplitude overlapped and neighboring phase interleaved carriers.

4.6.7 Variable Frequency PWM

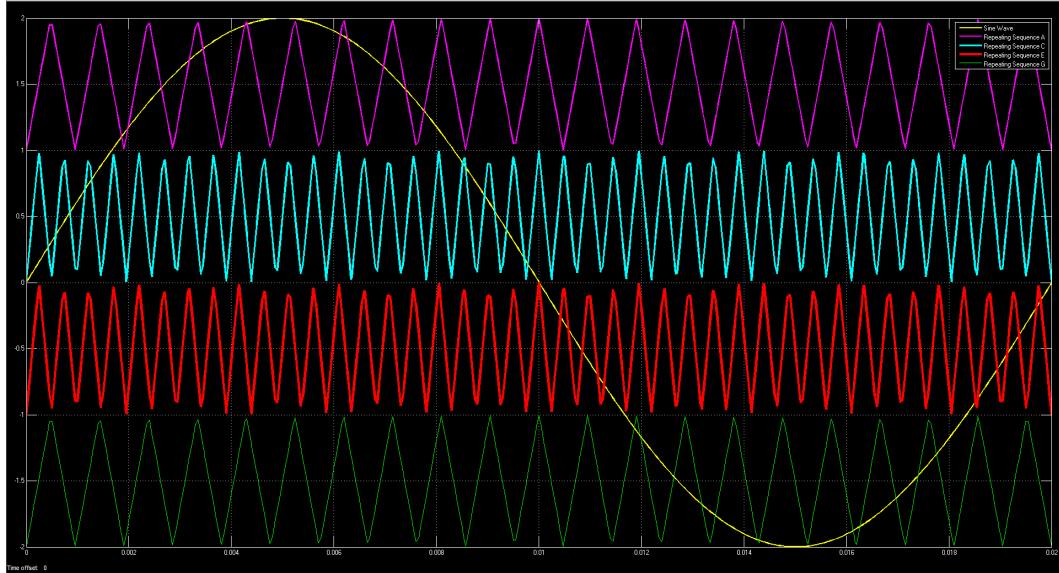


Fig 34: variable frequency input

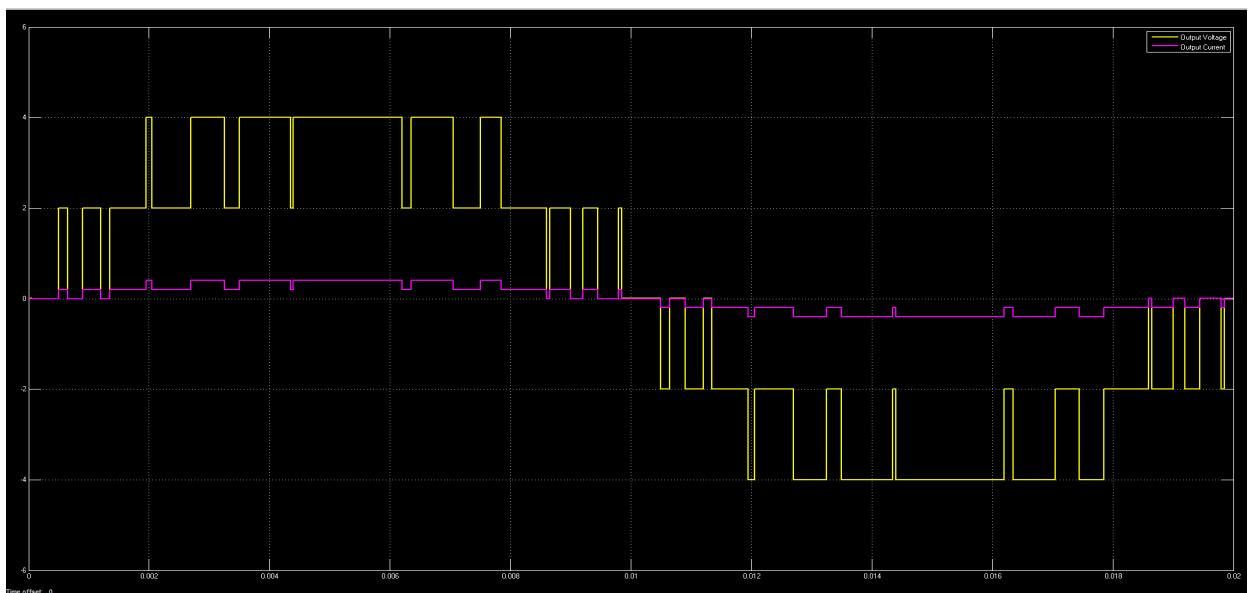


Fig 35: variable frequency output

The number of switching for upper and lower devices of chosen MLI is much more than that of intermediate switches in above PWM strategies using constant frequency carriers. In order to equalize the number of switching's for all the switches, VFPWM strategy is used in which the carrier frequency of the intermediate switches is properly increased to balance the numbers of switching for all the switches. In fig 34, the frequencies of carrier wave and sine wave are 41 and 21 respectively. The amplitude modulation index for VFPWM strategy is:

$$m_a = 2A_m / A_c(m-1).$$

Modulation technique	Total Loss	Conduction Loss	Switching Loss	THD
Phase Disposition	0.03424	2.009 e-5	0.03422	26.87%
Phase Opposition and Disposition	0.03412	2.004 e-5	0.0341	26.91%
Alternative Phase Opposition and Disposition:	0.03424	2.009 e-5	0.03422	26.88%
Carrier Overlapping PWM - A:	0.04103	2.28 e-5	0.04101	33.96%
Carrier Overlapping PWM - B:	0.04083	2.272 e-5	0.04081	33.17%
Carrier Overlapping PWM - C:	0.03908	2.202 e-5	0.03905	24.95%
Variable Frequency PWM:	0.03432	2.012 e-5	0.0343	26.71%

Table 3: Comparison of different modulation techniques

4.7 Relation between THD and Power Factor

The total power factor is calculated as follows:

$$PF_{TOTAL} = PF \times PF_{THD}$$

$$PF = \cos(\theta)$$

Where PF = displacement power factor

θ = Difference between the phase of the voltage and the phase of the current (phase displacement) in degrees.

The displacement power factor is the ratio of true power to apparent power due to the phase displacement between the current and voltage

$$PF_{THD} = \sqrt{1/(1+THD^2)}$$

Where PF_{THD} = distortion power factor, THD = Total harmonic distortion

The presence of harmonics complicates the discussion of the power factor. The distortion power factor is the ratio of true power to apparent power due to THD. Hence, Lower THD in power systems means higher power factor.

5. DESIGN AND CALCULATIONS

5.1 Switch Loss Calculations

Total losses = conduction loss + switching loss

Losses of 5 level SPWM:

Conduction loss = 2.009 e-5

Switching loss = 0.03422

Total loss = 0.03424

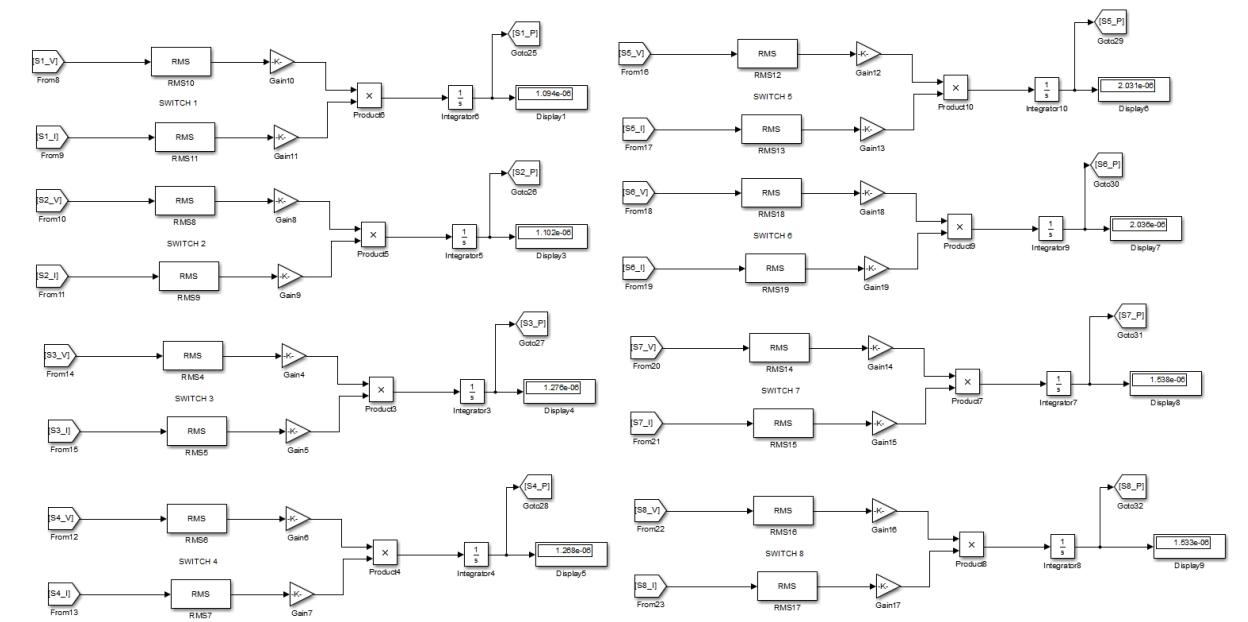


Fig 36: Conduction losses

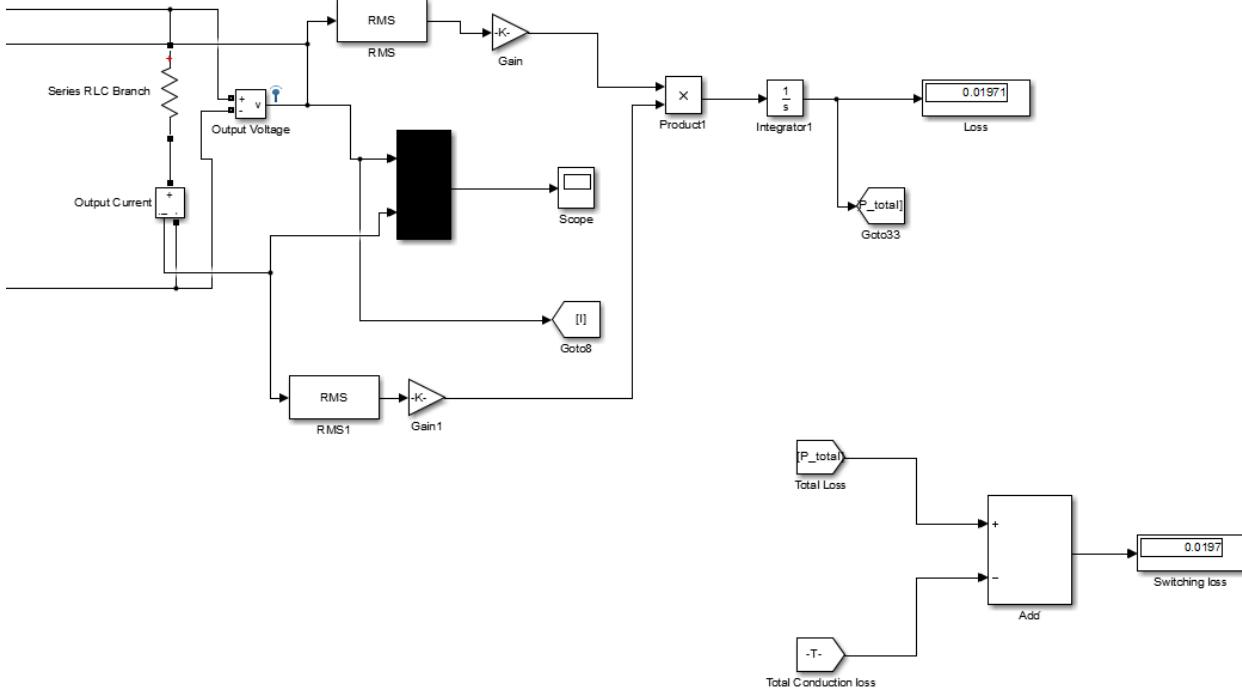


Fig 37: Total losses

5.2 Filter Design and Calculations

LC Filter Design

$$V_{in} = 100\text{v}$$

$$R = 10\Omega$$

$$V_{out}(\text{rms}) = V_{dc} = 100\text{v}$$

$$V_o = 100\sqrt{2} \sin \omega t$$

$$I_{out}(\text{rms}) = 10 \text{ A}$$

$$P_{out} = 1000 \text{ watt}$$

Inductor design

$$\Delta I_{peak} = 20\% \text{ of rated current} = 2\text{A}$$

$$\Delta I_{peak_ax} = V_{dc} / (4XL FSW)$$

$$L = V_{dc} / (4 \times \Delta I_{peak_ax} \times Fsw) = 100 / (4 \times 2 \times \sqrt{2} \times 1000)$$

$$= 8.83\text{mH}$$

Capacitance design

$$F_c = 1 / (2 \times \pi \times V \times C)$$

$$F_c \leq F_{crossover} / 10$$

$$C = (10/2*\pi*F_{crossover})^2 * (1/L)$$

$$= (10/2*\pi*1000)^2 * (1/8.83*10^{-3})$$

$$= 0.286\text{mF}$$

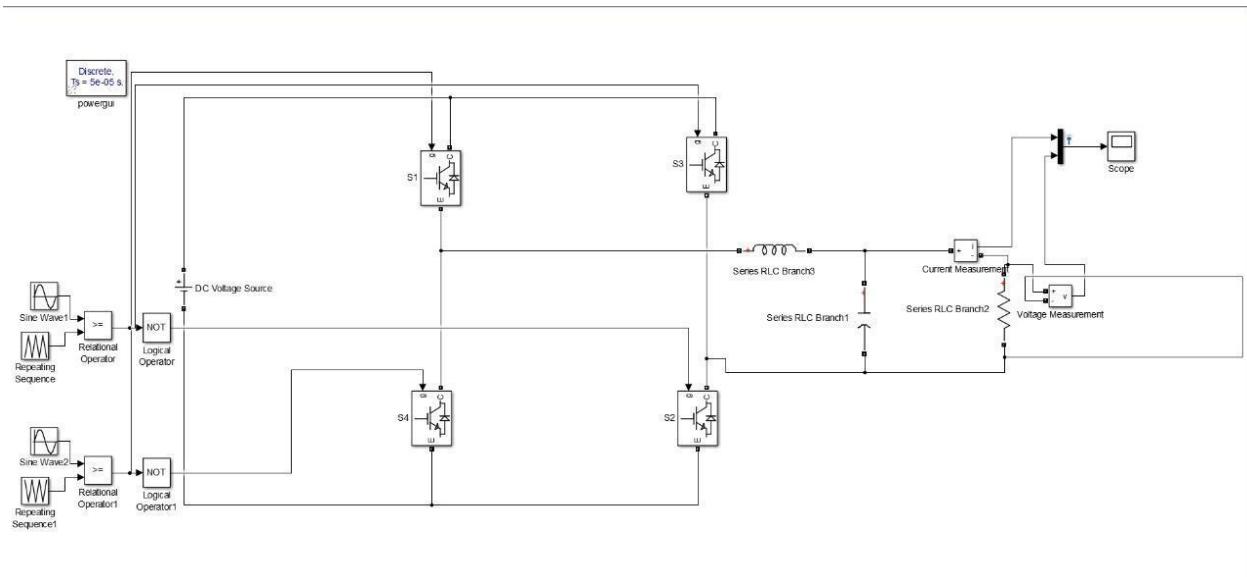


Fig 38: First order filter circuit

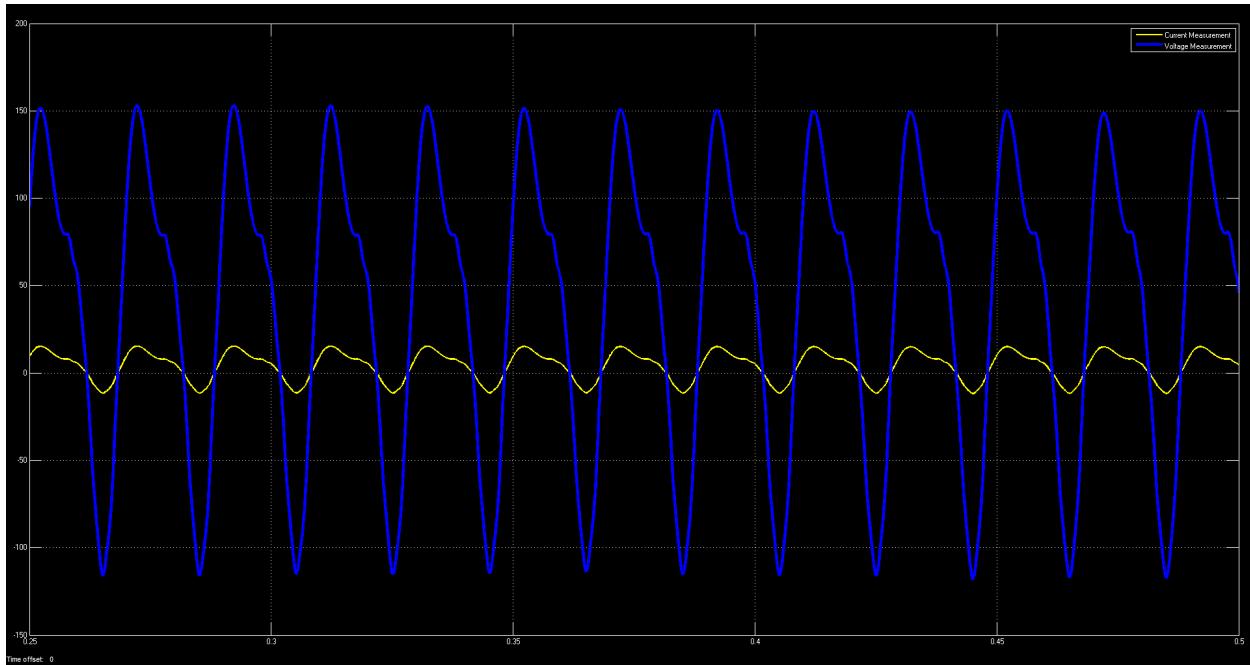


Fig 39: Output of first order LC filter

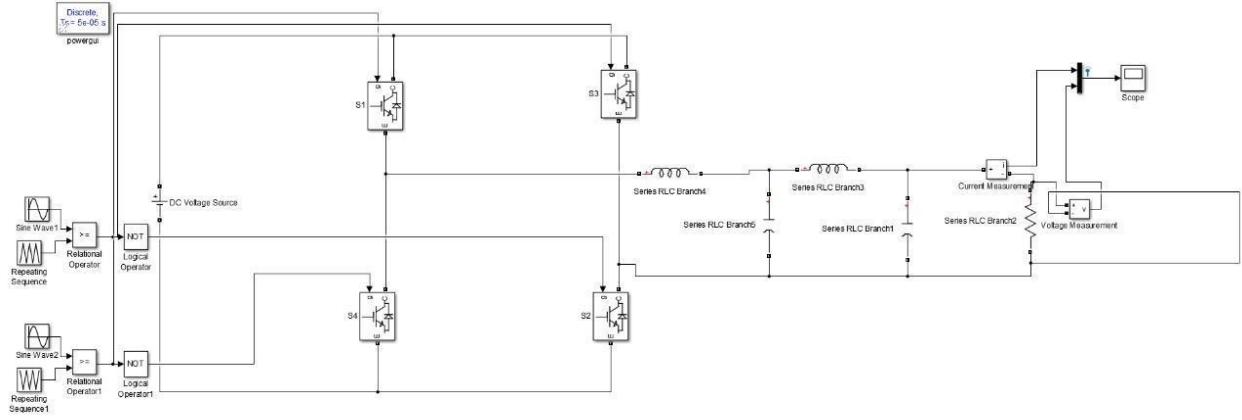


Fig 40: Second order filter circuit

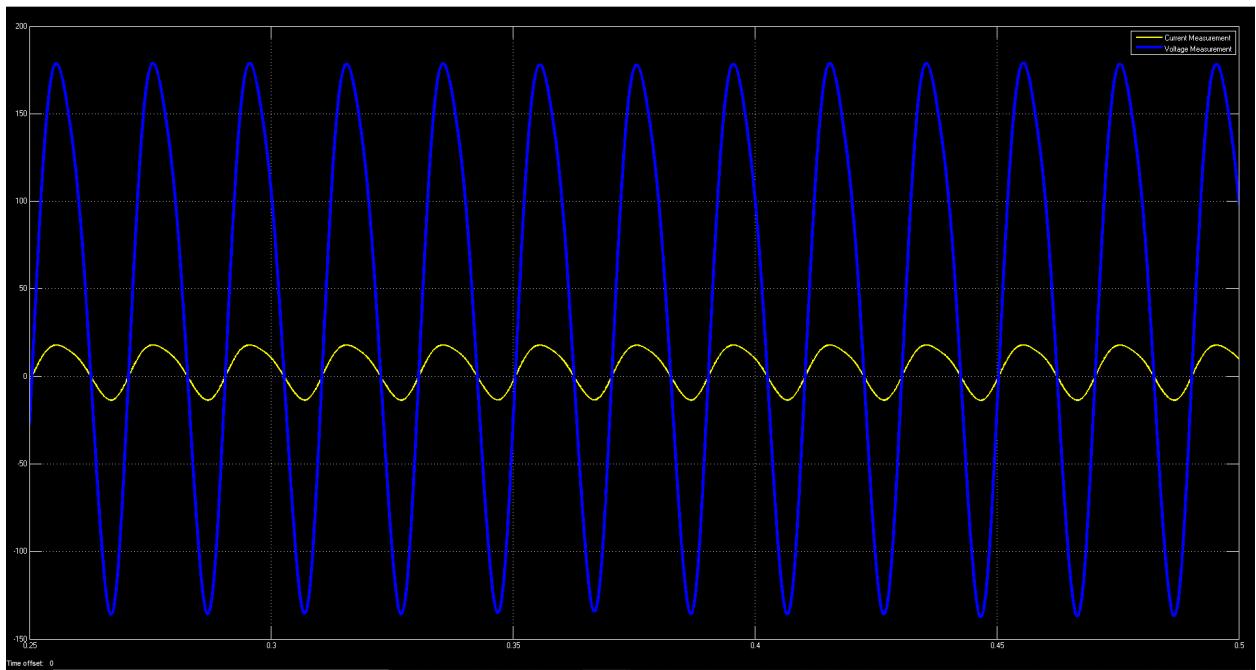


Fig 41: Output of second order LC filter

6. HARDWARE IMPLEMENTATION

6.1 Components used

Arduino UNO, MOSFETs -700N65P, H-bridges, pulse generator, DC Supply, Oscilloscope, Multimeter, Breadboard, Connecting wires.

6.2 Testing Arduino UNO Output pins

Out of 13 signal output pins of Arduino UNO 6 pins (pin nos 3, 5, 6, 9, 10, 11) are used for SPWM output. To test the output pins, a rectangular pulse and SPWM pulse is given as input to Arduino.

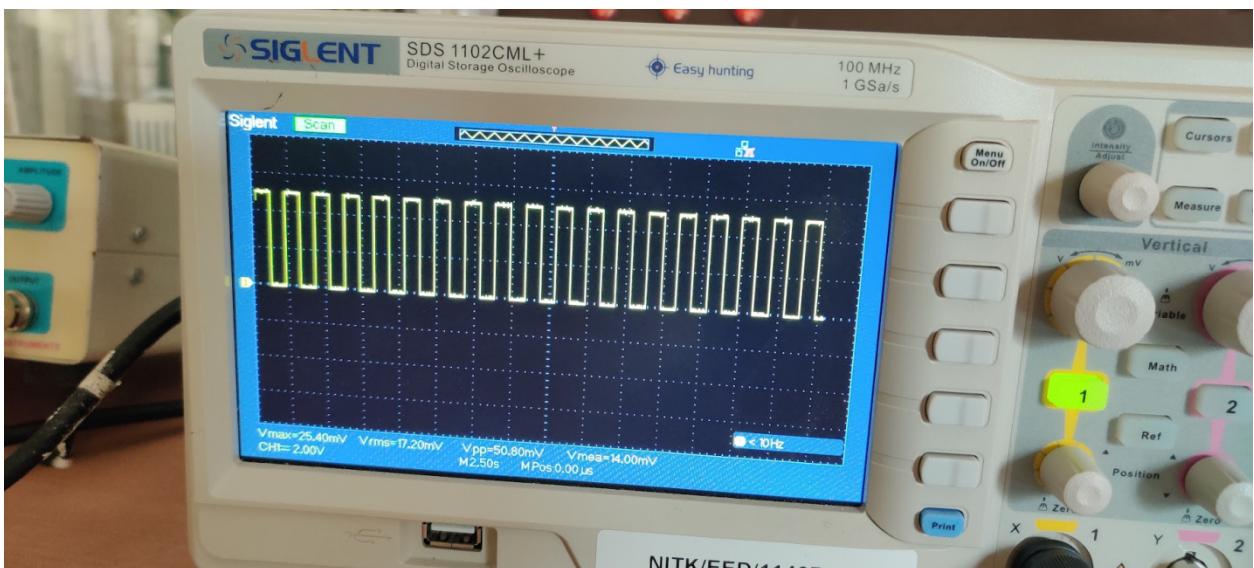


Fig 42: Rectangular Pulse generated using arduino uno

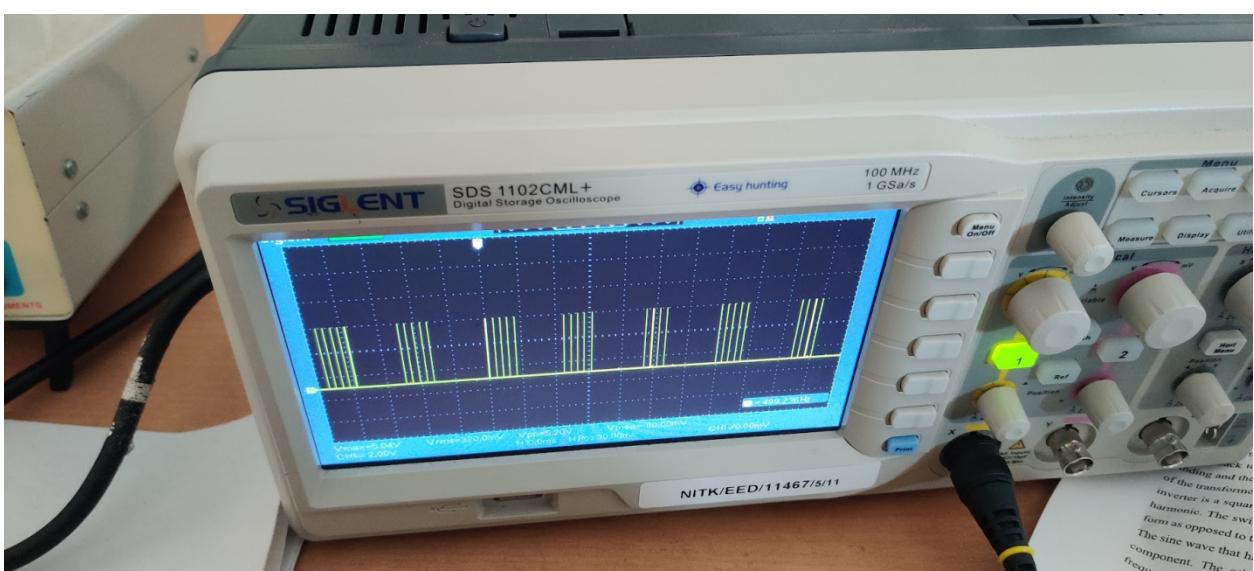


Fig 43: SPWM Pulse generated using arduino uno

6.3 Circuit diagram

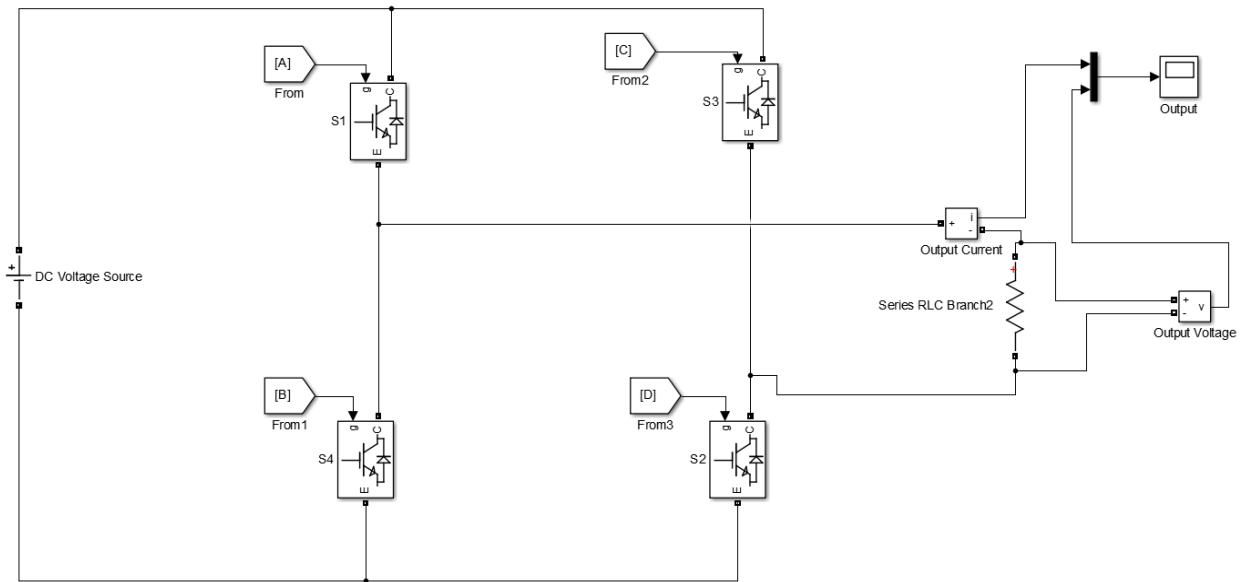


Fig 44: Circuit diagram of 3-level CHB MLI

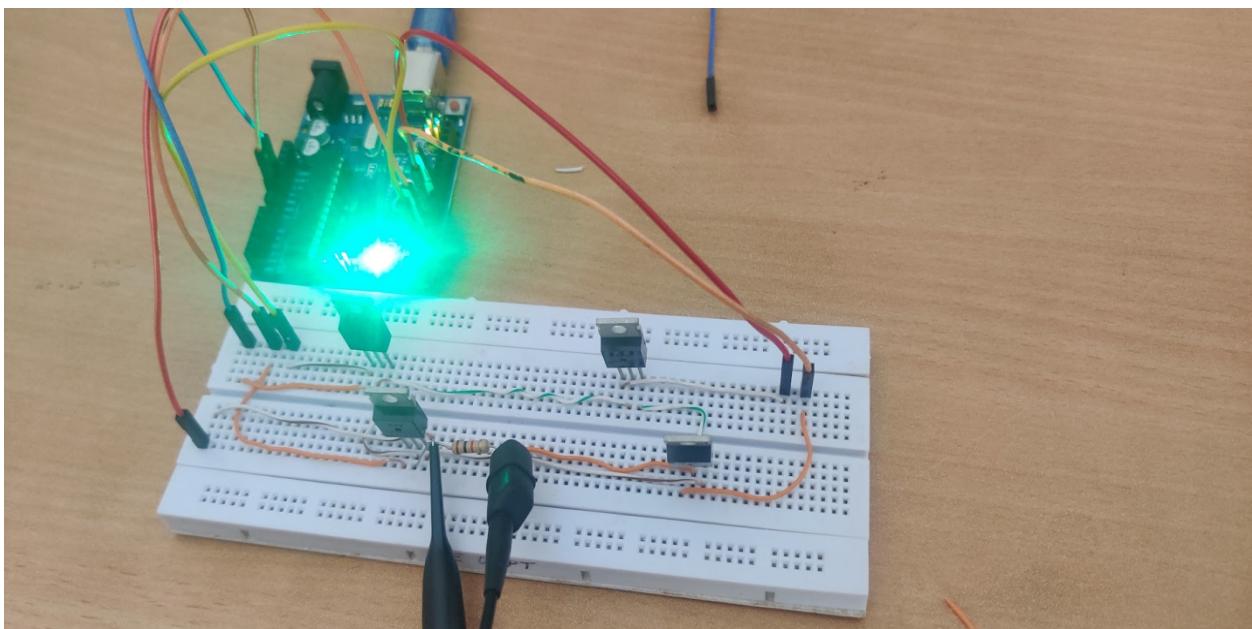


Fig 45: Circuit of 3-level CHB MLI using mosfets

A 3 level CHB MLI is built using 4 Mosfets, breadboard and the connections are made according to Figure 28. The Mosfet gate triggering pulses are generated using MATLAB simulink and are loaded into Arduino UNO.

6.4 Input and output images

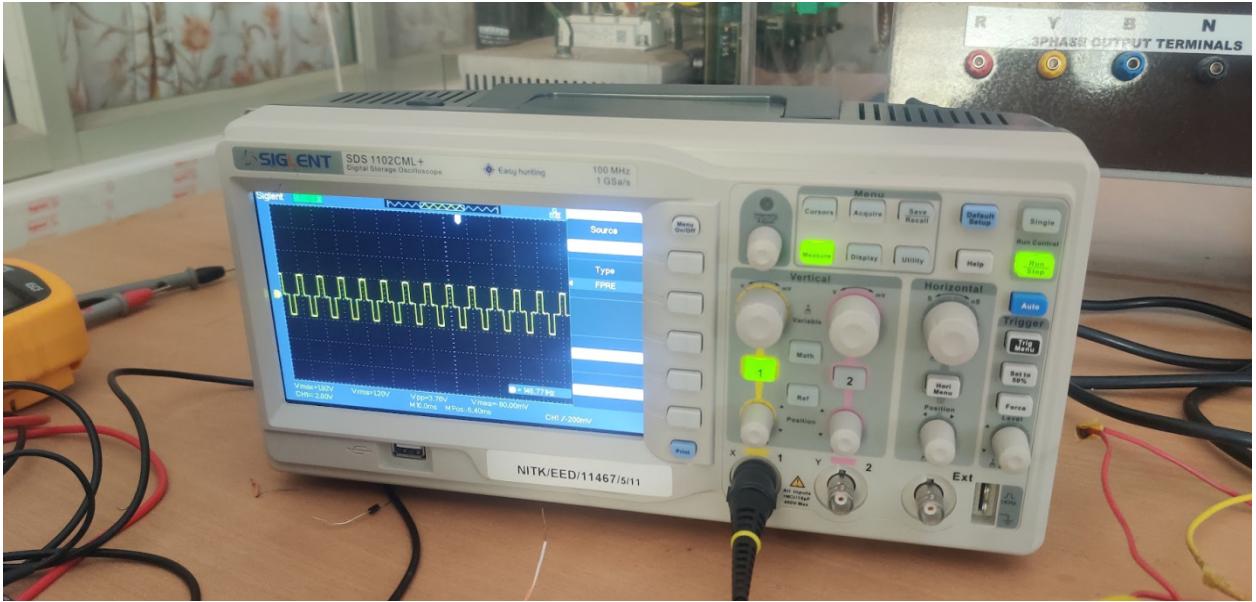


Fig 46: Output of 3-level MLI

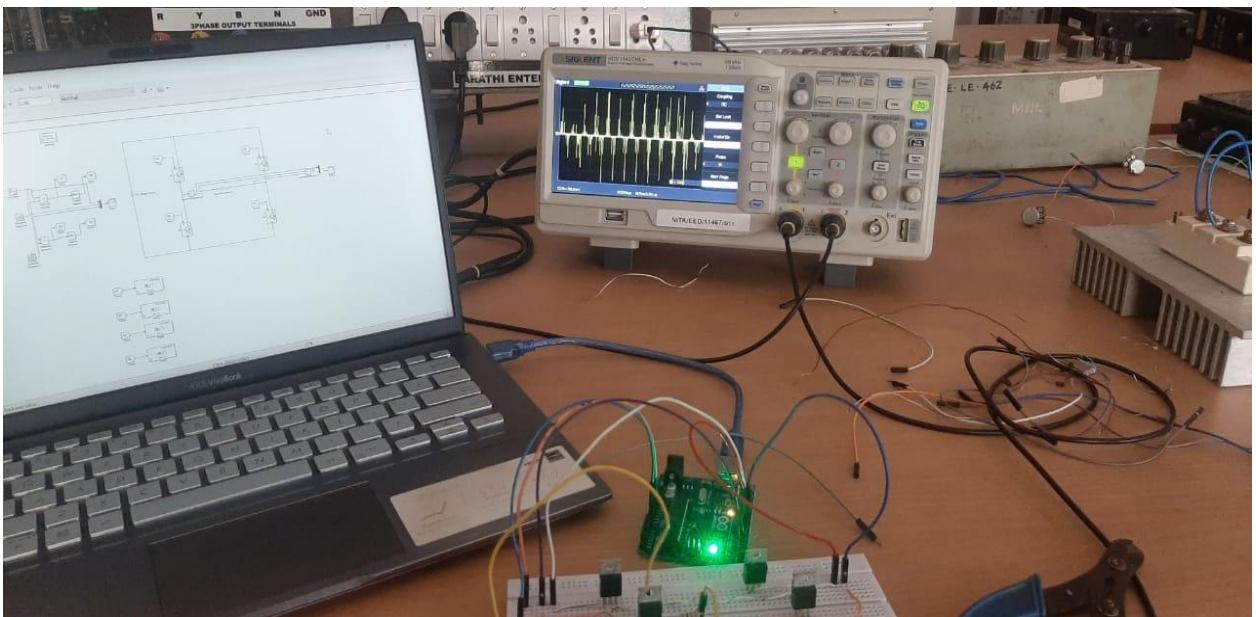


Fig 47: Output of SPWM 3-level MLI

7. CONCLUSION

In this project, different topologies of inverters such as full bridge, half bridge, cascaded h-bridge have been analyzed. 3 level and 5 level inverters have been analyzed with SPWM technique and different SPWM techniques have also been executed. After analysis we find that the THD values of SPWM inverters are less than the normal multilevel inverters. It has been observed that with increase in levels in multilevel inverters and with increase in modulation index THD decreases till a certain point. As the THD decreases, the power factor is improved. The above output variations have been demonstrated. Simultaneously, 3-level CHB MLI with and without SPWM has been implemented on the Arduino UNO board.

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