ANNA UNIVERSITY QUESTIONS

COMBINATIONAL LOGIC

PART-A

1. What are half and full adders? **(April 2003)**

2. State the condition for $B = I_2$ in the Boolean expression

$$B = I_0 \overline{S}_0 \overline{S}_1 + I_1 \overline{S}_0 S_1 + I_2 S_0 \overline{S}_1 + I_3 S_0 S_1$$ **(April 2003)**

What is the combinational logic circuit realised by the above boolean expression.

3. State the condition to check the equality of two n-bit binary numbers A and B. **(April 2003)**

4. Distinguish between combinational and sequential logic circuits. **(April 2003, April 2004)**

5. Using a single 7485 IC, draw the logic diagram of a 4 bit comparator. **(April 2003)**

6. Write down the truth table of a full adder. **(April 2004)**

7. Write down the truth table of a full subtractor. **(Nov. 2004)**

8. Describe the truth table of a half subtractor and write the Boolean expression corresponding to the difference and the borrow. **(April 2005)**

9. What is a combinational circuit? Give an example. **(April 2005)**

10. Draw the circuit of a half-adder. **(Dec. 2005)**

11. Write the truth table for a half-subtractor. **(Dec. 2005)**

12. Draw the flow diagram of gray to binary conversion. **(Dec. 2005)**

13. Draw a combinational logic circuit which can compare whether two bit binary numbers are same or not. **(Dec. 2005)**

14. Draw a parity checker circuit for 3 bit binary word $x_1 x_2 x_3$. **(May 2006)**

15. Represent a half adder in block diagram from and also its logic implementation. **(May 2006)**

16. Construct a 4-bit binary to gray code converter circuit and discuss its operation. **(May 2006)**

17. Mention any two uses of HDL. **(May 2006)**

18. What is logic synthesis? **(Dec. 2006)**

19. List the important features of HDL. **(Dec. 2006)**

20. Design a half adder. **(May 2007)**

21. What is a full adder? **(May 2007)**

22. What are the modeling techniques available to build HDL module? **(May 2007)**

23. Draw the circuit diagram for 3 bit parity generator. **(Dec. 2007)**

24. Define combinational circuit. **(May 2009)**

25. What is the need for code conversion? Give two commonly used codes. **(May 2009)**

PART-B

1. Design a parity generator to generate an odd parity bit for a 4-bit word. Use EX-OR and EX-NOR gates. **(8) (April 2003)**

2. Design a combinational circuit that compares two 4-bit numbers A and B to check if they are equal or not. **(8) (April 2003)**

3. (i) Design a full adder and a full subtractor. **(14)**

(ii) Draw the block diagram of a 2's complement adder/subtractor. **(2) (April 2003)**

4. Using a single 7483, draw the logic diagram of a 4 bit adder/subtractor.

5. Draw the Logic diagram of a 4 bit parallel adder/subtractor using full adders and explain. **(8) (Nov. 2003)**

6. Draw a full adder circuit using only NOR gates. **(8) (Nov. 2003)**

7. Design and explain the following circuits: (i) Full adder, (ii) Comparator. **(16) (Nov. 2003)**

8. (i) Explain how a full adder can be built using two half adders and an OR gate. **(6)**

(ii) Design a half adder using atmost three NOR gates. **(10) (April 2004)**

9. Design a look ahead carry generator. **(16) (April 2004)**

10. Design a circuit that converts 8421 BCD Code to excess 3 code. **(16) (April 2004)**

11. Implement the logic function $Y(A, B, C) = \sum m(1, 2, 7)$ using 74151A and 74153. **(8) (Nov. 04)**

12. Design a Binary to Gray Converter. **(16) (Nov. 2004)**

13. Design a BCD to Gray Code Converter. Use don't cares. **(16) (Nov. 2004)**

14. Explain carry look ahead adder circuit. **(16) (Nov. 2004)**

15. Explain with truth table and gate level circuit diagram for a full adder. **(12) (April 2005)**

16. Design a combinational circuit which accepts 3 bit binary number and converts its equivalent excess 3 code. **(10) (April 2005)**

17. Design and explain the working of Gray to BCD converter. **(16) (April 2005)**

18. Design a BCD adder to add two BCD digits. **(16) (Dec. 2005)**

19. (i) Design a 4-bit binary to BCD code converter. **(10) (Dec. 2005)**

(ii) Design a 4-bit binary to gray code converter. **(6) (Dec. 2005)**

20. Design and implement a binary to gray code converter. **(16) (Dec. 2005)**

21. Design a combinational circuit whose input is 4 bit binary number and whose output is 2's complement of input number. **(4) (Dec. 2005)**

22. Design a combinational logic circuit that will generate the square of all the combinations of a 3 bit binary number. **(8) (Dec. 2005)**

23. Design and explain: (i) 4 bit magnitude comparator. **(16) (May 2006)**

24. Design a BCD to 7 segment code converter. **(16) (May 2006)**

25. **(i)** Design a binary multiplexer, using half adders and/or full adders, to multiply two 2-bit numbers. **(8)**

(ii) Design a combinational logic circuit to compare two 2-bit binary numbers A and B and to generate the outputs A < B, A = B and A > B. Is there a way to derive the third output from the first two outputs? **(8) (May 2006)**

26. Design a 4 bit magnitude comparator to compare two 4 bit numbers. **(16) (Dec. 2006)**

27. Construct a combinational circuit to convert given binary coded decimal number into an Excess-3 code. For example when the input to the gate is 0110 then the circuit should generate output as 1001. **(16) (Dec. 2006)**

28. Design a 4 bit comparator using logic gates. **(16) (May 2007)**

29. Design a 4 bit adder/subtractor using logic gates and explain its operation. **(16) (May 2007)**

30. Draw the block diagram of a BCD adder and explain its operation. **(10) (May 2007)**

31. (i) Design a combinational circuit to convert BCD to gray code. **(12) (May 2007)**

(ii) Design a 4 bit subtractor. **(4) (May 2007)**

32. (i) Design a combinational circuit to convert Excess-3 code to BCD code. **(10) (May 2007)**

(ii) Design a 2 bit x 2 bit multiplier. **(6) (May 2007)**

33. (i) Design a combinational circuit to convert gray code to BCD. **(12) (Dec. 2007)**

(ii) Design a Full adder circuit with a Decoder. **(4) (Dec. 2007)**

34. Design a 4 bit magnitude comparator to compare two 4 bit numbers. **(Dec. 2007)**

35. (i) Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is less than three. The output is 0 otherwise. **(6) (Dec. 2008)**

(ii) Design a code converter that converts a decimal digit from 8,–4,–2,–1 code to BCD. **(10) (Dec. 2008)**

36. (i) Design a 4 bit combinational circuit incrementer – A circuit that adds one to a 4-bit binary number? Use half-adders for this problem. **(8) (Dec. 2008)**

(ii) Design a combinational circuit that generates the 9's complement of a BCD digit. **(8) (Dec. 2008)**

37. Design a BCD to 7 segment decoder. **(16) (May 2009)**

38. With a suitable block diagram explain the operation of BCD adder. **(16) (May 2009)**

COMBINATIONAL LOGIC

PART-A

1. Distinguish between a decoder and a multiplexer. **(Nov 2003, April 2004)**

2. Draw a 1 to 2 demultiplexer circuit. **(Nov 2003)**

3. Draw a 1 to 2 multiplexer circuit. **(Nov 2003)**

4. What is a demux? **(April 2004)**

5. What is a decoder and obtain the relation between the number of inputs *'n'* and outputs *'m'* of a decoder? **(April 2005)**

6. Implement the logic function f = AB + A'.B' using a suitable multiplexer. **(Dec 2005)**

7. How can a decoder be converted into a demultiplexer? **(Dec 2005)**

8. Distinguish between decoder and multiplexer. **(Dec 2005)**

9. Implement the logic function f = $\sum$ *m* (0,2,3,6) using a decoder. **(May 2006)**

10. How can a multiplexer used to convert 8-bit parallel data into serial form? **(May 2006)**

11. What are functions of encoders and decoders? **(Dec. 2006)**

12. What is a Multiplexer? **(Dec. 2006)**

13. Design a 2 input NAND gate using 2:1 multiplexer. **(May 2007)**

14. Implement the given function in 4:1 multiplexer f = $\sum$ *m* (0,1,3,5, 6). **(May 2007)**

15. What is a priority encoder? **(May 2007)**

16. Mention any two applications of multiplexers. **(May 2007)**

17. What is logic syntheses in HDL? **(Dec. 2007)**

18. Construct a 16x1 multiplexer with two 8x1 multiplexer and 2x1 multiplexer. **(Dec. 2008)**

19. Draw the logic diagram of 4 bit even parity checker. **(Dec. 2008)**

20. What is decoder? Draw the block diagram and truth table for 2 to 4 decoder. **(May 2009)**

21. Give some applications of multiplexer. **(May 2009)**

22. Compare the serial and parallel adder. **(Dec 2010)**

23. Define look ahead carry addition. **(Dec 2010)**

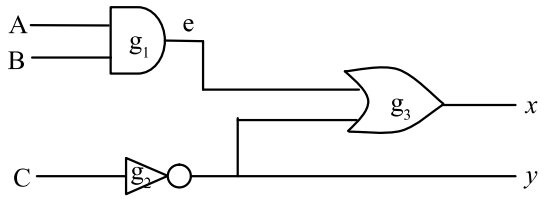
24. Define priority encoder **(Dec 2010)**

25. Write a dadflow description of a 2-to-1 line Mux uisng a condiitonal operator **(Dec 2010)**

24. Draw the schematic of half-adder logic. **(May 2011)**

25. Determine the size and number of multiplexers required to implement a full adder. **(May 2011)**

26. Write the HDL description of the following circuit. **(May 2011)**



27. With a block diagram show how a full adder can be designed using two half address and one OR gate. **(Dec 2011)**

28. List the modelling techniques available in HDL. **(Dec 2011)**

29. Define decoder. Draw the block diagram and truth table for 2 to 4 decoder. **(Dec 2011)**

30. Define Tri-state gates. **(May 2012)**

31. Define Logic Synthesis and Simulation. **(May 2012)**

32. Write the stimulus for 2-to-1 line multiplexer. **(May 2012)**

33. Implement a Full adder with two half adders. **(Dec 2012)**

34. Implement a 4-bit even parity checker. **(Dec 2012)**

35. Construct a 4 × 16 decoder using 3 × 8 decoders. **(Dec 2012)**

36. Write down the truth table of a full subtrator. **(May 2013)**

37. What is meant by Test Bench? **(May 2013)**

38. Distinguish between a decoder and a demultiplexer. **(May 2013)**

PART – B

1. Implement the function $F(X_1,X_2,X_3,X_4) = \sum (0,1,3,4,8,9,15)$ with an 8x1 multiplexer where the following variables are connected in the specified order to selection lines S_2S_1 and S_0 respectively (i) X_1,X_2,X_3 (ii) X_2,X_3,X_4 **(8) (April 2003)**

2. Design and explain the working of a 1 to 8 demultiplexer. **(10) (April 2003)**

3. Explain how you will build a 64 input MUX using nine 8 input MUXs. **(8) (April 2003)**

4. Implement the following Boolean function using an 8 to 1 multiplexer and 4 to 1 multiplexer. $F(A,B,C) = \sum (0,1, 5,7)$. **(12) (Nov 2003)**

5. Design and explain the working of a 4 to 1 multiplexer. **(8) (Nov 2003)**

6. Realize $F(w,x,y,z) = \sum (1,4,6,7,8,9,10,11,15)$ using 4 to 1 MUX. **(16) (April 2004)**

7. **(i)** Implement a 3 to 8 line decoder. **(8)**

(ii) Implement the logic function Y(A,B,C) = $\sum$ m (1,2,7) using 74151A and 74153.

(8) (Nov 2004)

8. Design a seven segment decoder circuit to display the numbers 0 to 3. **(16) (Nov 2004)**

9. Implement the switching function F= $\sum$ (3, 6-8, 10, 13-15) using an 8 input multiplexer.

(10) (Nov 2004)

10. Show that when two 2 input multiplexers drive another 2 input MUX, the result is a 4 input multiplexer. **(6) (Nov 2004)**

11. Show that when a 3 line to 8 line DEMUX drives eight 3 line to 8 line DEMUXs, the result is a 6 line to 64 line DEMUX. **(6) (Nov 2004)**

12. Implement the following function with a multiplexer, f (a,b,c,d) = $\sum$ (0,1, 3,4,8,9,15).

(10) (April 2005)

13. Implement the following Boolean expression using an 4:1 MUX F= $\sum$(0,1, 2,4,6,9,12,14).

(8) (April 2005)

14. Design and explain the working of full adder and a decoder. **(12) (April 2005)**

15. What is the simplest logic circuit for a decoder that produces a 1 output when the BCD input is 0000 ? **(8) (Dec 2005)**

16. Implement the following function with a multiplexer, f (A,B,C,D) = $\sum$ (0,1, 3,4,8,9,15).

(6) (Dec 2005)

17. Write the structural VHDL description for a 2 to 4 decoder and explain it in detail.

(16) (Dec 2005)

18. Implement the following Boolean function using an 8:1 MUX f (a,b,c,d) = a'bd' + acd +b'cd+a'c'd **(8) (Dec 2005)**

19. Design and explain the priority encoder. **(8) (May 2006)**

20. Describe the structural verilog description of 4 to 1 multiplexer. Also draw the internal diagram of the multiplexer. **(16) (May 2006)**

21. Construct a full adder circuit and write a HDL program module for the same.

(16) (Dec. 2006)

22. (i) Implement the following with a multiplexer

$F(A,B,C) = \sum(1,2,4,5)$ **(8) (Dec. 2006)**

23. Implement the Boolean function using 8:1 multiplexer.

$F(A,B,C,D) = A'BD+ACD+B'CD+A'C'D.$ **(8) (May 2007)**

24. Construct a full adder circuit and write a HDL program module for the same.

(16) (May 2007)

25. Implement the Boolean function using 8:1 multiplexer.

$F(A,B,C,D) = AB'D + A'C'D + B'CD' + AC'D$. **(16) (Dec. 2007)**

26. **(i)** A 8x1 multiplexer has inputs A,B and C connected to the selection inputs S2, S1 and S0 respectively. The data inputs 10 to 17 are as follows 11=12=17=0; 13=15=15=1; 10=14=D and 16=D′. Determine the Boolean function that the multiplexer implements. **(10) (Dec. 2008)**

(ii) Write the HDL dataflow description of a quadrupul –2 to –1 line multiplexers with enable. **(6) (Dec. 2008)**

27. **(i)** using the conditional operator (?;), write a HDL, dataflow description of a 4-bit adder subtractor of unsigned numbers. **(8) (Dec. 2008)**

(ii) Implement the Boolean function $F = \sum(0,1,3,4,8,9,15)$ using a multiplexer.

(8) (Dec. 2008)

28. Define decoder. Design a 3 to 8 decoder. With suitable block diagram explain how a 4 to 16 decoder can be formed by using the same. **(16) (May 2009)**

29. Relative a BCD to Excess-3 code conversion circuit starting from its truth table.

(16) (Dec 2010)

30. Design a full adder and subtractor using NAND and NOR gates respectively.

16 (Dec. 2010)

31. **(i)** Define multiplexer

(ii) Implemment the following Boolean function using 8 : 1 MUX.

F(A, B, C, D) = ABC + ACD + BCD + ACD **16 (Dec. 2010)**

32. **(i)** Design a combinational circuit that comprises only of NOR gates for the following expression giving the input output relation. **(10)**

(ii) Draw the schematic of a full adder circuit and give its truth table. **(6) (May 2011)**

33. **(i)** Design a BCD to Excess - 3 code converter using truth table and K-Map simplification **(10) (May 2011)**

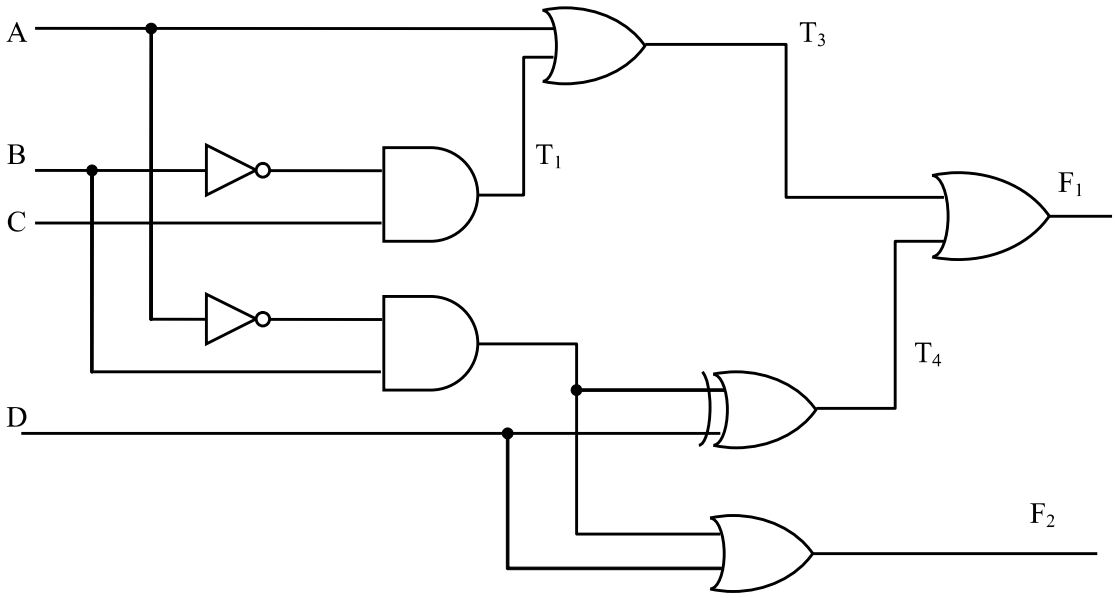
(ii) Draw the schematic of a magnitude comparator and give its truth table.

(6) (May 2011)

34. **(i)** Design a combinational logic using a suitable multiplexer to realize the following Boolean expression. **(10)**

(ii) Compare and contrast between encoders and multiplexers. **(6) (May 2011)**

35. Consider the combinational circuit shown in figure.



(i) Derive the Boolean expressions for T_1 through T_4. Evaluate the outputs F_1 and F_2 as a function of the four inputs. **(4)**

(ii) List the truth table with 16 binary combinations of the four input variables. Then list the binary values for T_1 through T_4 and outputs F_1 and F_2 in the table. **(4)**

(iii) Plot the output Boolean function obtained in part (ii) on maps and show that simplified Boolean expressions are equivalent to the ones obtained in Part (i) **(8) (Dec. 2011)**

36. **(i)** With suitable block diagram explain Binary multiplier. **(8)**

(ii) Write a detailed note on carry-propagation. **(8) (Dec. 2011)**

37. Construct a 5 to 32 line decoder with four 3 to 8 line decoders with enable and a 2 to 4 line decoder. Use block diagrams for components. **(16) (Dec. 2011)**

38. **(i)** Implement the following Boolean function with 16 x 1 multiplexer : **(6)**

$$F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$$

Use block diagram representation.

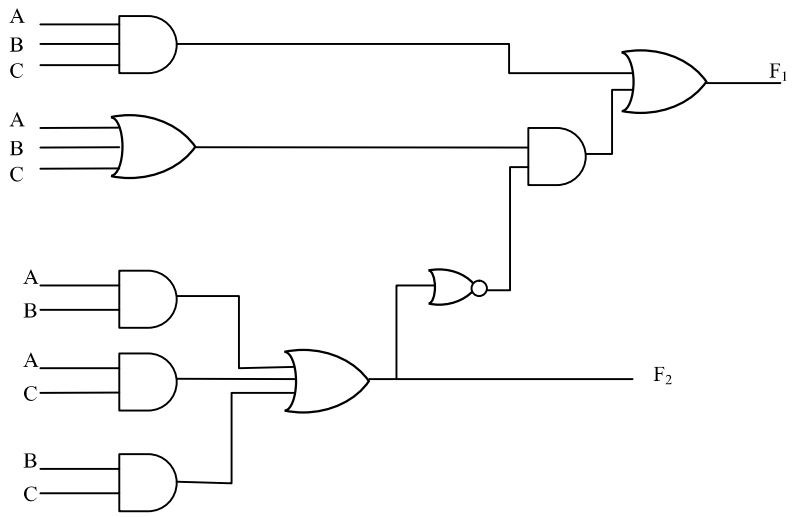
(ii) Write HDL gate level description for 3 to 8 line decoder. **(4) (Dec. 2011)**

39. Design Half and Full Substractor circuits. **(16) (May 2012)**

40. Design a circuit that converts 8421 BCD code to Excess-3 code. **(16) (May 2012)**

41. Implement a full adder with two 4×1 multiplexers. **(16) (May 2012)**

42. i) Analyse the combinational circuit shown in figure, determine the truth table and the Boolean expressions governing the outputs of the circuit. **(10)**



ii) Explain BCD adder with a neat block diagram. **(6) (Dec 2012)**

43 i) Design a BCD to excess-3 code converter using logic gates. **(12)**

ii) Draw the diagram of a 4-bit adder subtractor using full adder. **(4) (Dec 2012)**

44. Implement F(A, B, C, D) = ∑(1, 3, 4, 11, 12, 13, 14, 15) using 8 × 1 multiplexer. **(8) (Dec 2012)**

45. Design a 4-input priority encoder. **(6) (Dec 2012)**

46. Design a full adder using 2 half adders. **(16) (May 2013)**

47. Design a combinational circuit to convert binary to gray code. **(16) (May 2013)**

48. Implement the switching function F = ∑m(0, 1, 3, 4, 12, 14, 15) using an 8 input MUX. **(16) (May 2013)**