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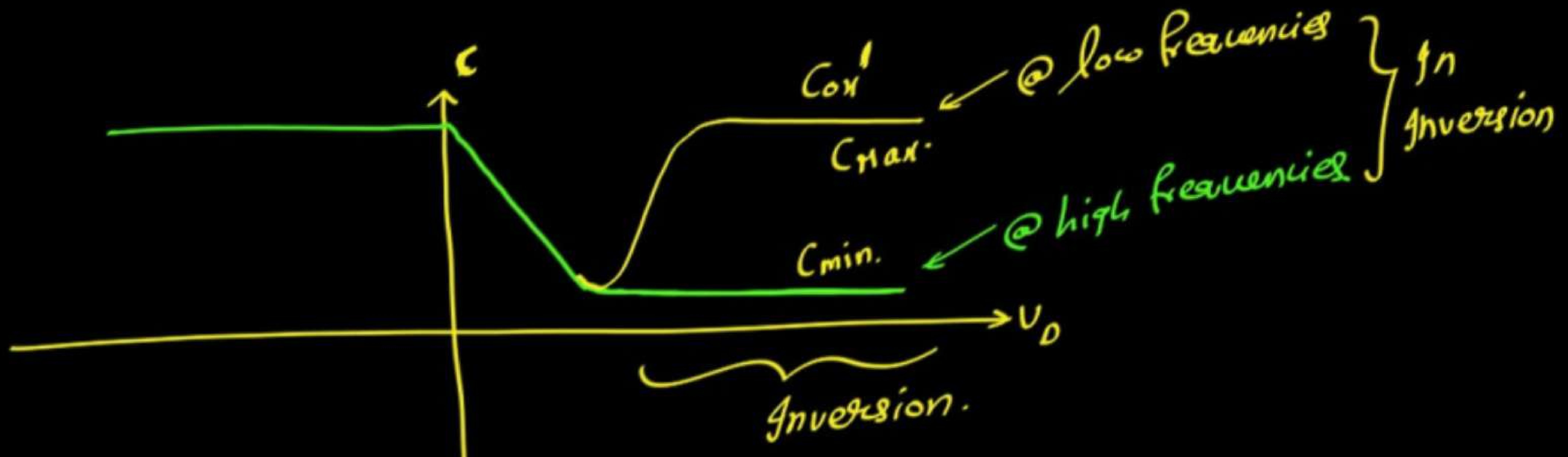


$$\boxed{C_{min}' = \frac{\epsilon_{ox}}{t_{ox} + \left[\frac{\epsilon_{ox}}{\epsilon_{si}}\right] x_d}}$$

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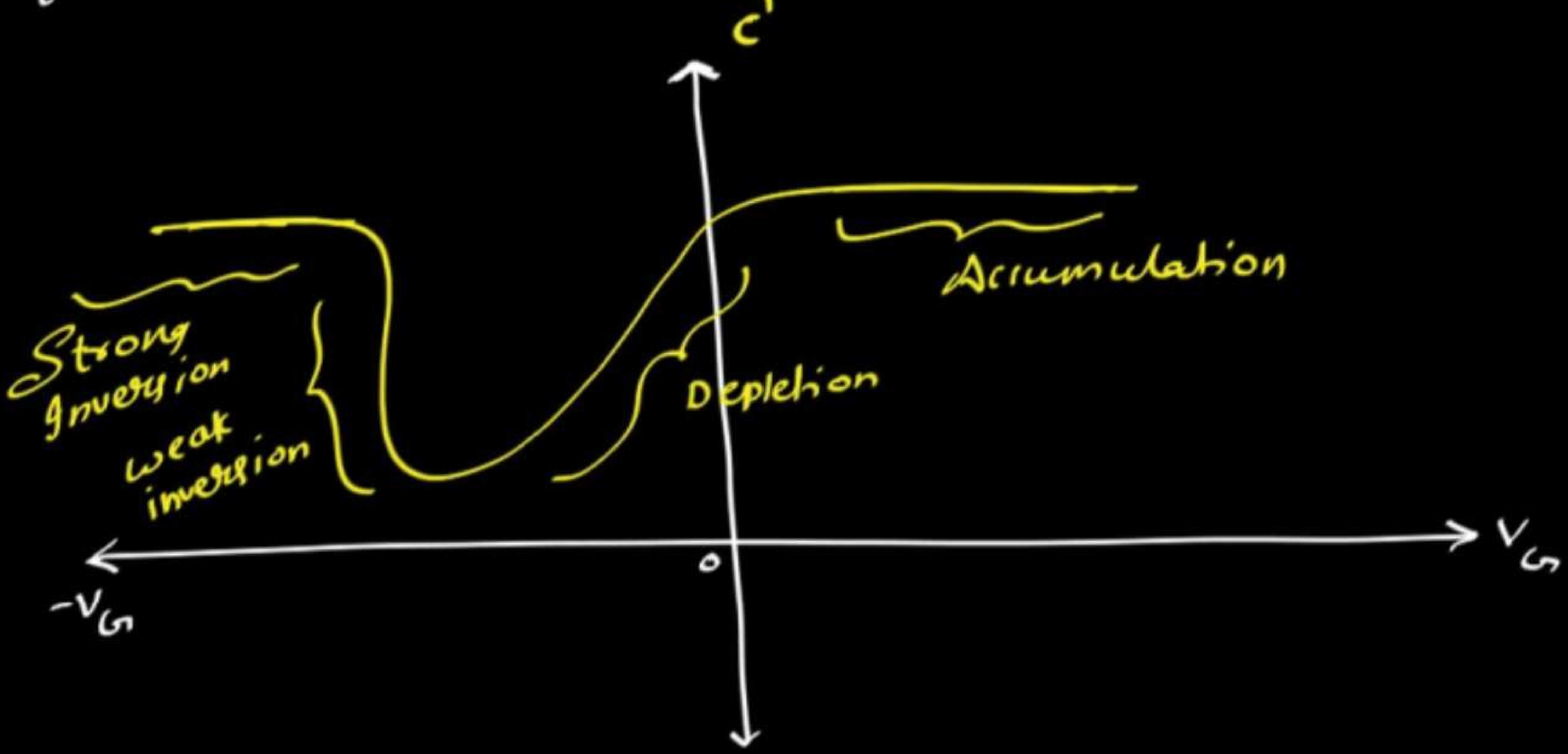
In Inversion Mode,

@ low frequency → Cap., is $\underline{C_{max}}$.

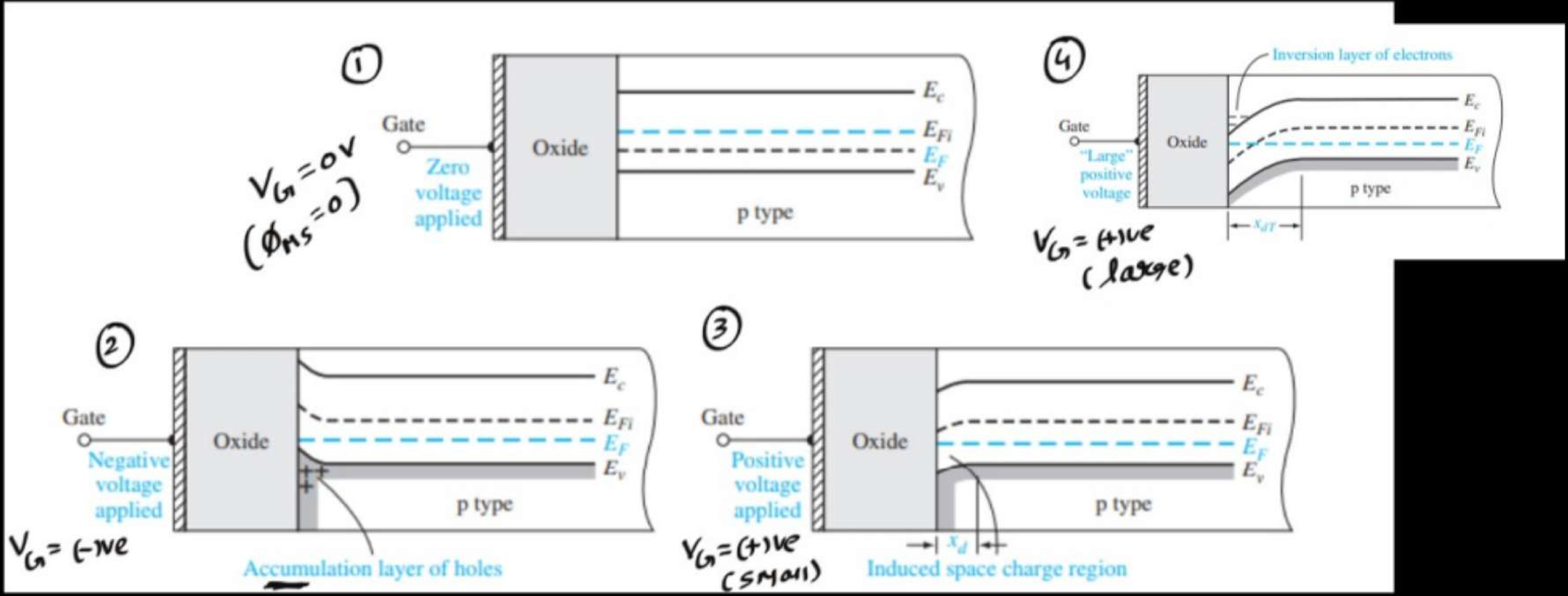
@ high frequency → Cap., is $\underline{C_{min}}$.

Similarly for n-type substrate → $\boxed{\text{PMOS}}$

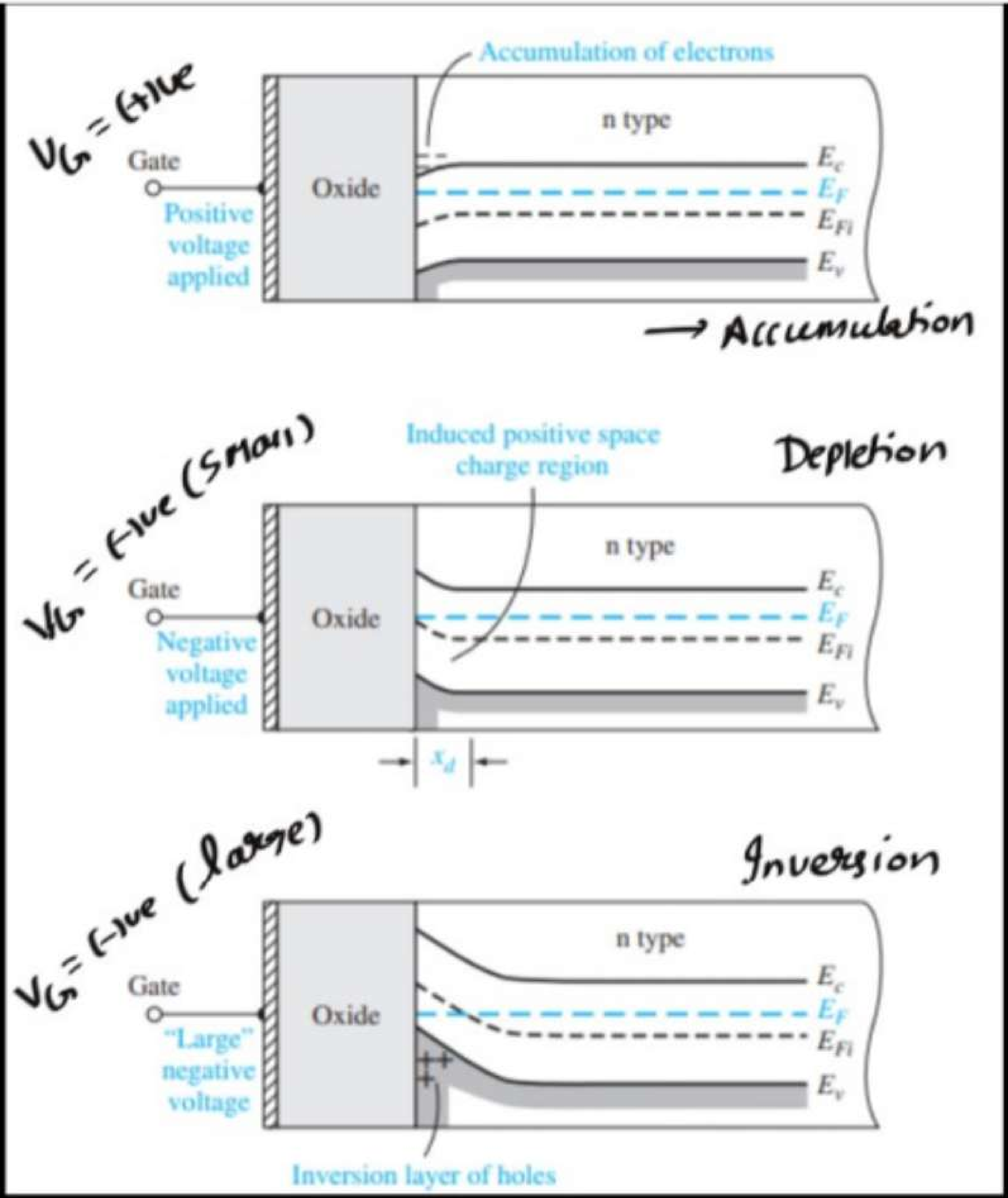


Till Now we have Seen →

NMos ( P-substrate)




$$\phi_{fp} = \frac{kT}{q} \log_e \left| \frac{N_A}{n_i} \right| \quad \& \; x_{d_{Max}} = x_{p_{Max}} = \sqrt{\frac{2\epsilon}{q} \cdot \frac{1}{N_A} \cdot \psi_{si}} = \sqrt{\frac{2\epsilon}{q} \cdot \frac{1}{N_A} \cdot 2\phi_{fp}} = x_{d_{Max}}$$




Similarly →

PMOS
(n-type Substrate)

$$\phi_{f_n} = \frac{KT}{q} \log_e \left| \frac{N_D}{n_i} \right|$$

$$(x_n)_{max} = \sqrt{\frac{2\epsilon}{q} \cdot \frac{1}{N_D} \cdot \psi_{si}}$$

$$= \sqrt{\frac{2\epsilon}{q} \cdot \frac{1}{N_D} \cdot 2\phi_{f_n}}$$

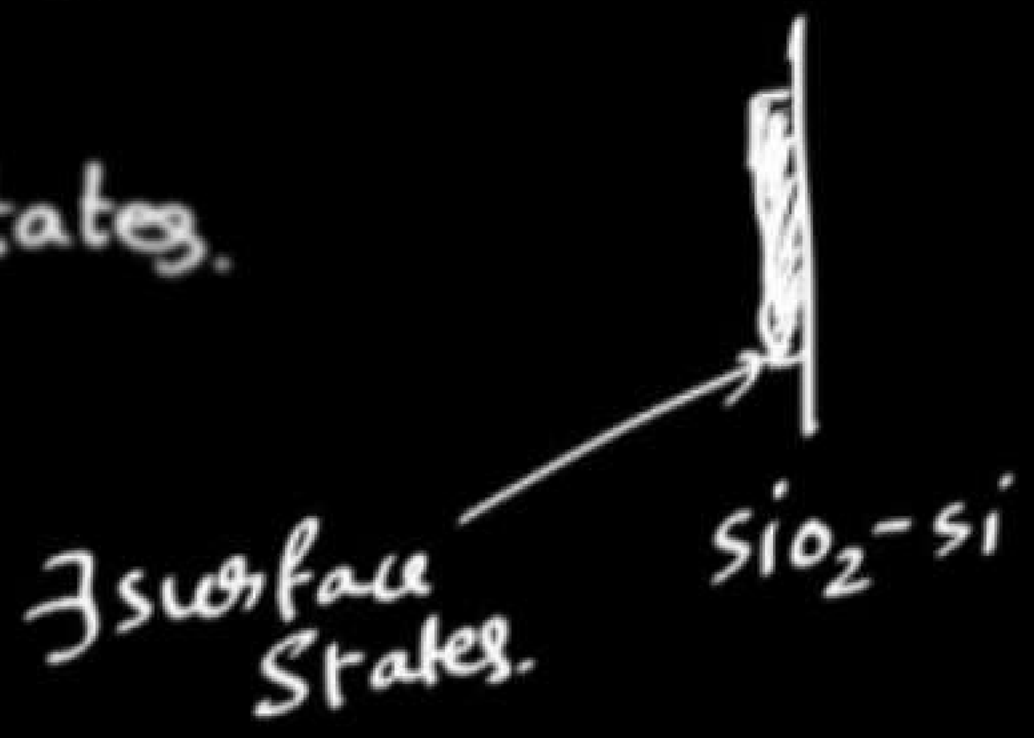
$$= x_{d_{max}}$$

**Ideal Mos-cap**

1. $\phi_M = \phi_S$.
2. Oxide has No charge.
3. Oxide has infinite Resistance $\Rightarrow R_G = \infty$ & $I_G = 0$.
4. No Surface States @ $SiO_2$-$Si$ Interface.

**Practical Moscap**

1. $\phi_M \neq \phi_S$ [once Metal is fixed, $\phi_M$ = const., but if S.C., doping changes $\phi_S$ changes]
2. ∃ Some Trap charges in Oxide.
3. $R_G \cong 100\,T\Omega$.
4. ∃ Surface States.



($SiO_2$)

Practically a Net Fixed charge (Usually Positive) May Exist in Insulator.

The Positive charge has been identified with "broken Covalent bonds (or) dangling Covalent bonds" Near the Oxide-Semiconductor Interface.

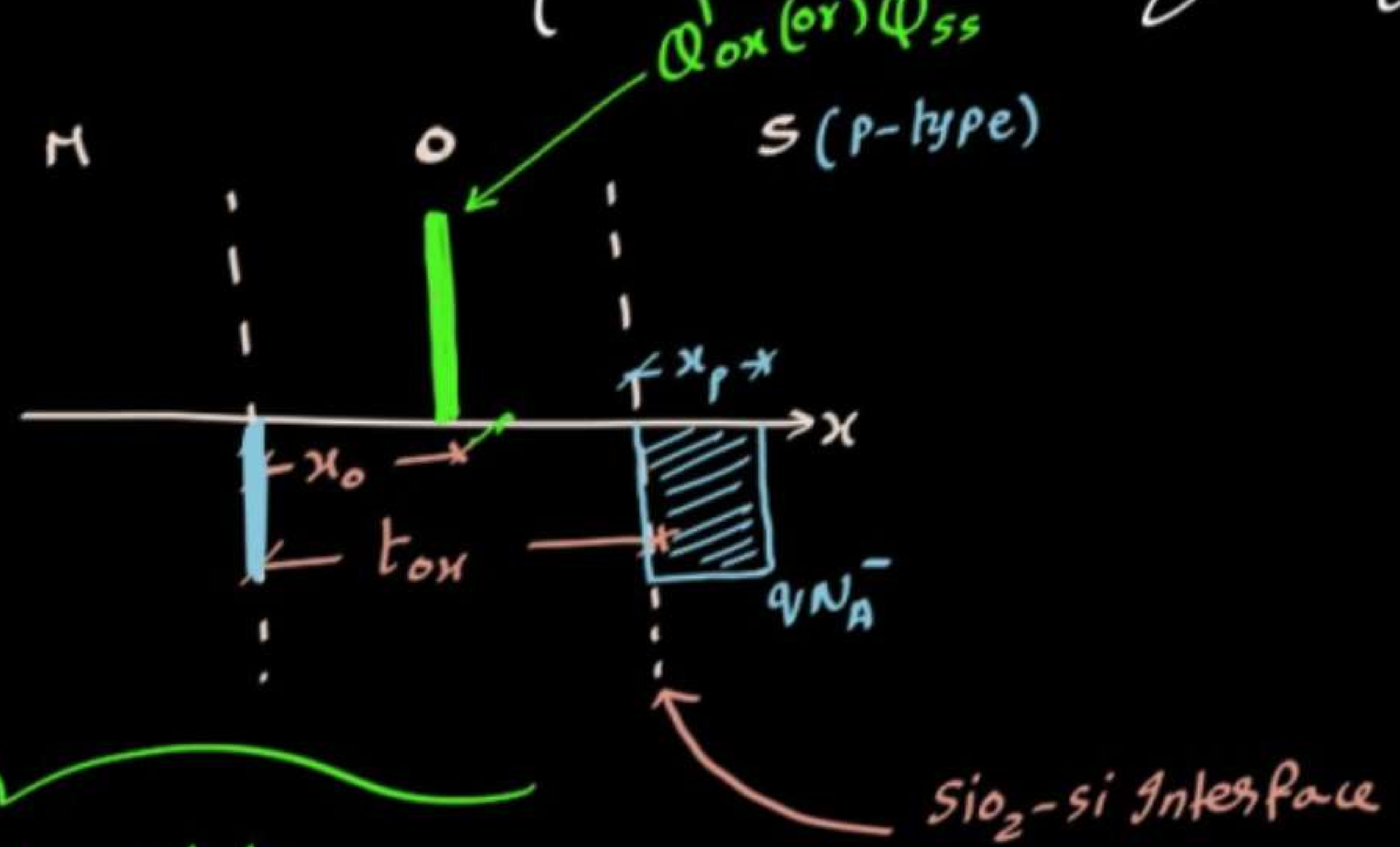
During thermal formation of $SiO_2$, Oxygen diffuses through the Oxide & reacts Near $Si$-$SiO_2$ interface to form $SiO_2$. "Si Atoms May also break away from the Si Material Just Prior to reaching to form $SiO_2$".

When Oxydation Process is terminated, Excess si may Exist in the Oxide Near the Interface, Resulting in Dangling Bonds.

$\int_V \rightarrow$

$\Rightarrow$

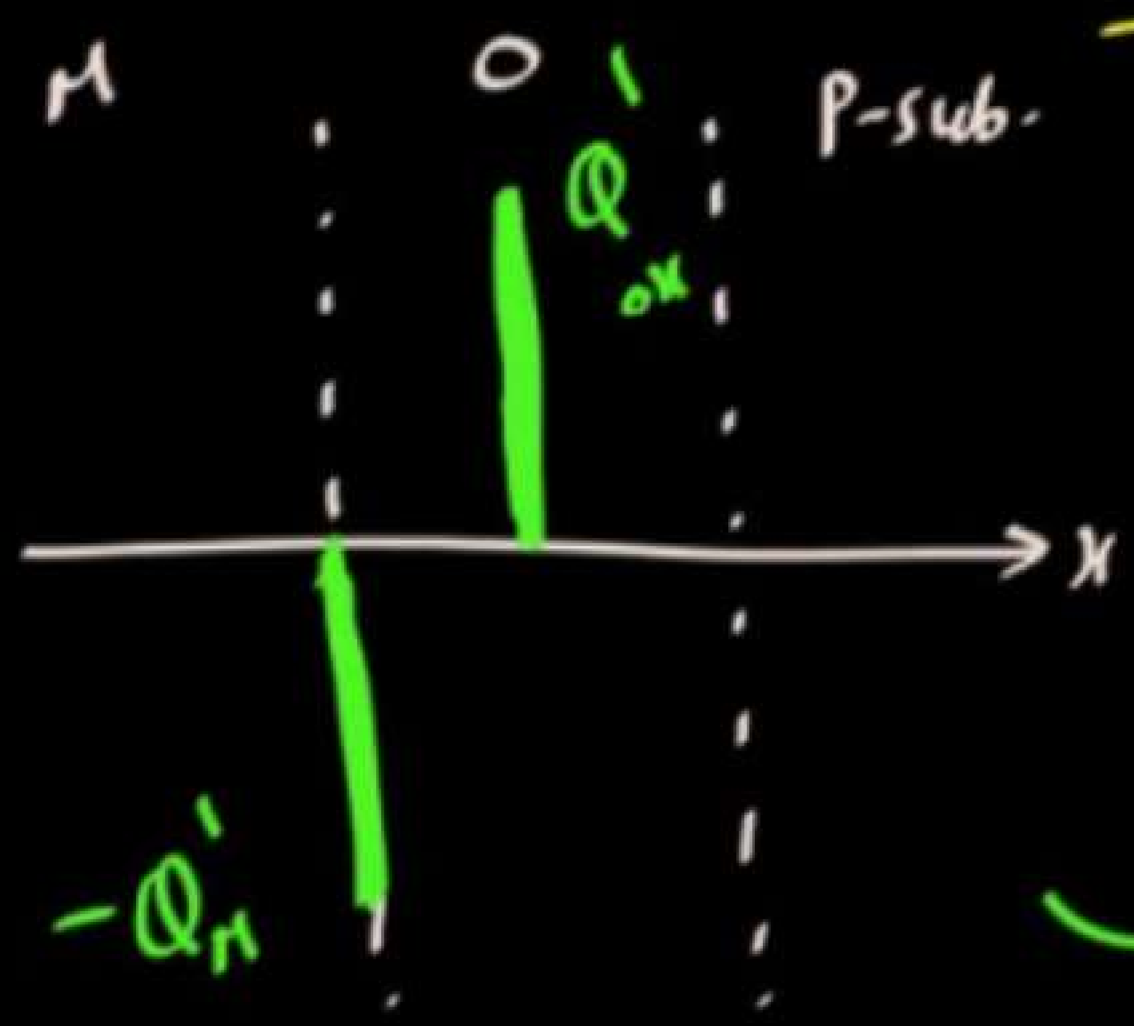
$\boxed{\text{Even @ } V_G = 0V}$




Even @ $V_G = 0V$, MOS Diode is in Depletion Mode $\rightarrow$ $\exists$ dep. region in substrate.

Since Even @ $V_G = 0V \longrightarrow \exists\ x_d$ in substrate $\Rightarrow$ Our Task is to make $x_d = 0$.

This Can be done by providing (−)ve Voltage @ GATE (Externally)



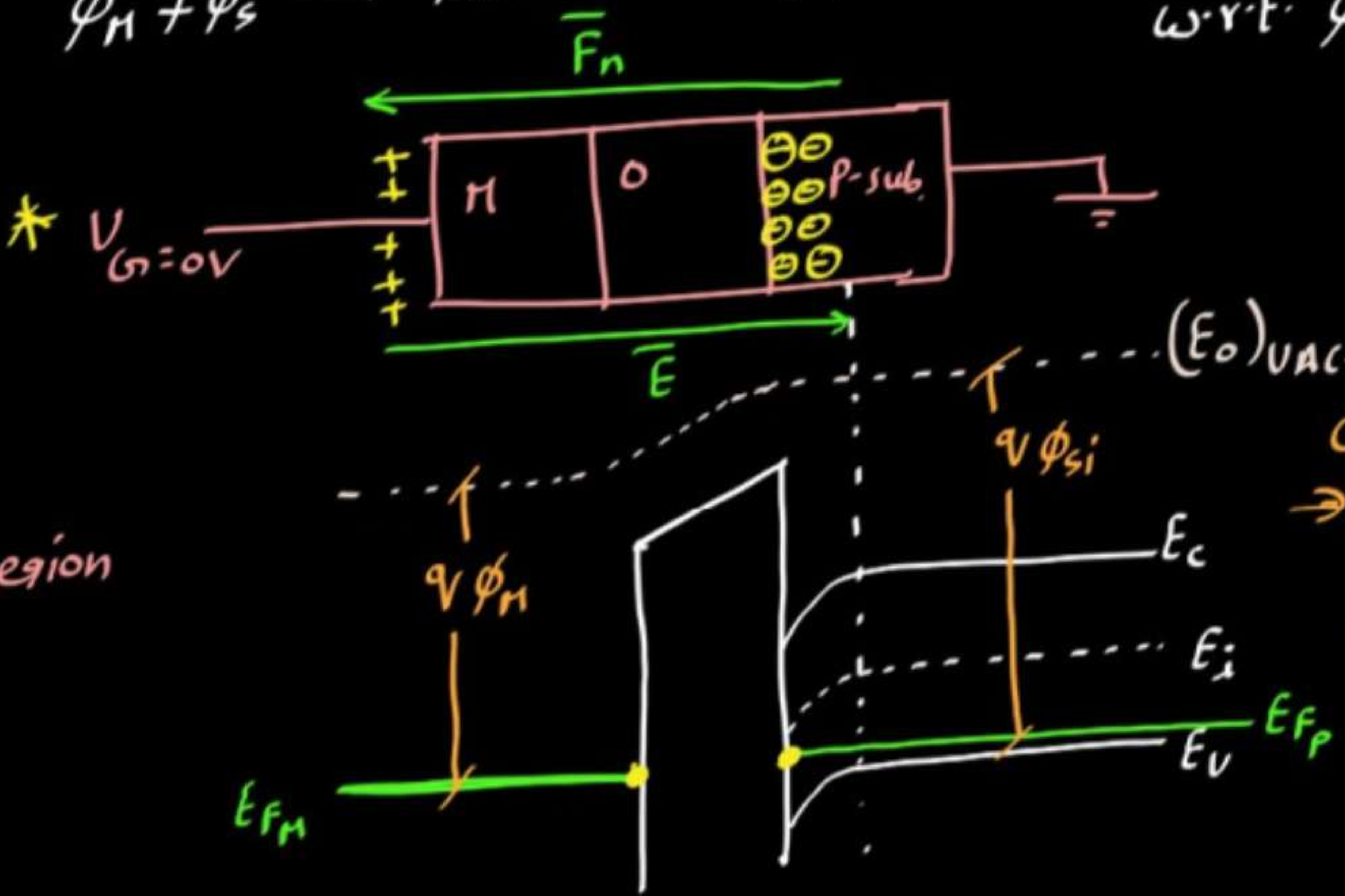

$\Rightarrow$ Charges ($Q'_{ox}$) Can be balanced by Charges in Metal ($Q'_M$)

$\Rightarrow Q'_{sc} = Q'_{si} = 0.$

It will Change Threshold Voltage.

∴ Surface states/Traps Problem Resolved.

→ Now $\phi_M \neq \phi_S$ → Then which $\phi_M$ should be choosed w.r.t. $\phi_S$?



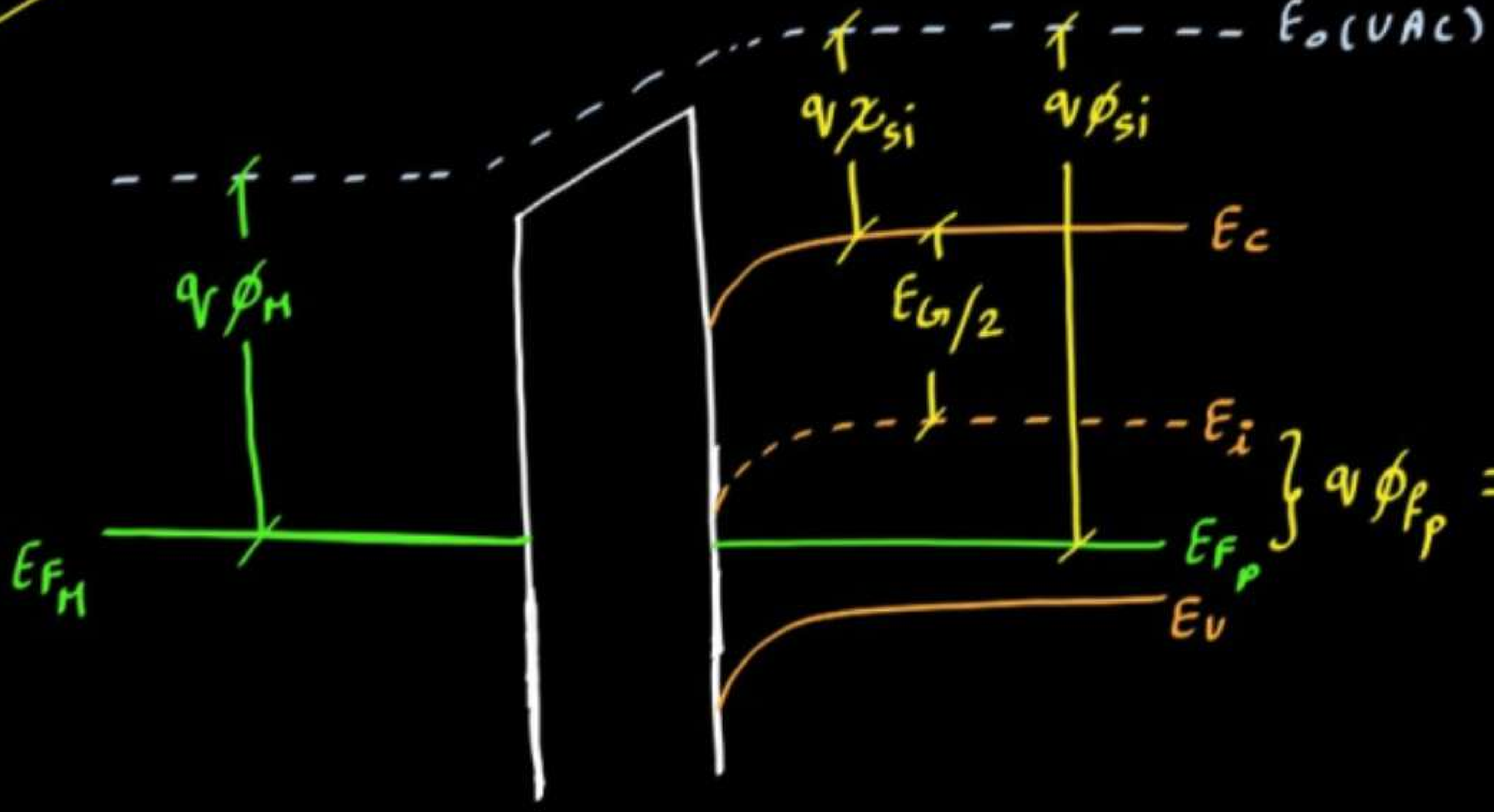

As @ $V_G = 0V$, Already device is Under dep. region

Choose Metal

$\Rightarrow \phi_M < \phi_{si}$.

$\therefore \phi_{MS} = \phi_M - \phi_S$
$= (-)ve.$

$\boxed{@\ V_G = 0V}$

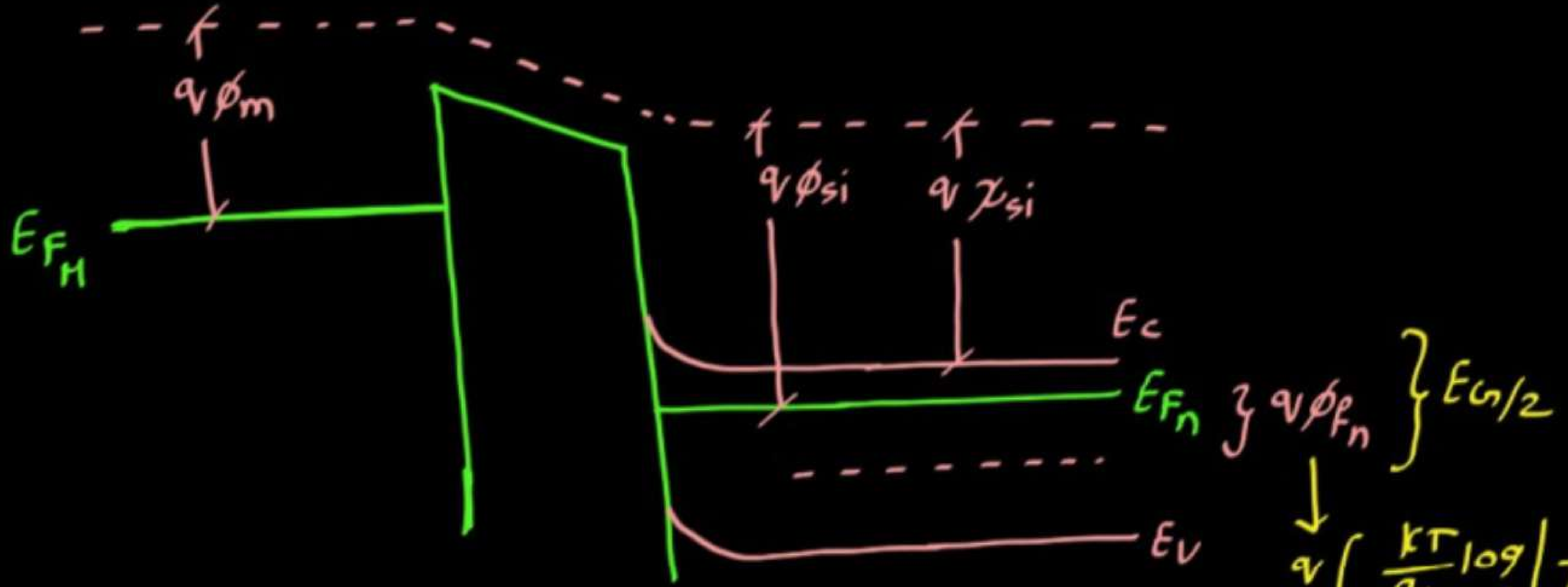



P-substrate.

$$q\phi_{f_p} = q\left(\frac{kT}{q}\log_e\left|\frac{N_A}{n_i}\right|\right).$$

$$\therefore\ \phi_{MS} = \left[\phi_M - \left(\chi_{si} + \frac{E_G}{2} + \phi_{f_p}\right)\right]$$

Similarly for PMOS $\longrightarrow$ Substrate is n-type $\longrightarrow$

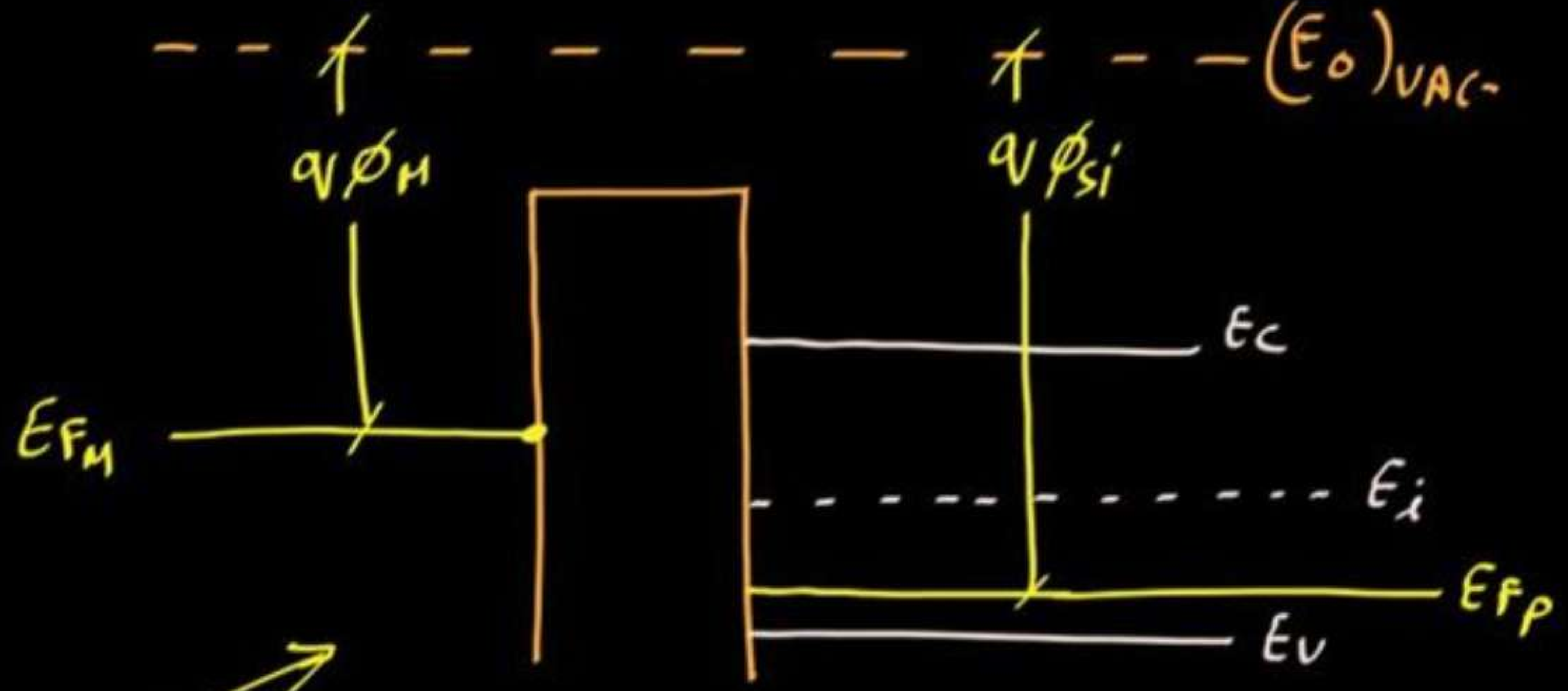



$$q\phi_{F_n} \rightarrow q\left[\frac{kT}{q}\log_e\left|\frac{N_D}{n_i}\right|\right].$$

$$\phi_{MS} = \phi_m - \left[\chi_{si} + \frac{E_G}{2q} - \phi_{F_n}\right].$$

NMOS

Do Some thing Externally we Need ⇒ band diagram




→ Flat Band Condition.

$\therefore \phi_{MS} = V_{FB_1}$

$\therefore V_{FB_1} = \phi_M - \phi_s$

[Our Target to acheive this → flat band].

Ideally for MOS diode @ $V_{G}=0V$, Bands in S.C. are Flat $\Rightarrow$ Called $\boxed{\text{Flat band Condition.}}$

But Practical MOS diode,

Bands are Not Flat.

So practically to Make Bands Flat, We must Apply some External Voltage $\longrightarrow$ Called, $\boxed{\text{Flat Band Voltage } (V_{FB}).}$

$\downarrow$

Applied Gate voltage such that there is No Band bending in Semiconductor & as a result, Zero Net Space charge in this region.

For NMOS $\Rightarrow$ P- Substrate $\longrightarrow$

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$$V_G = V_{FB_1} = \phi_M - \phi_{SC} = \phi_{MS}.$$

In Above Case, $\phi_{MS} = (-)ve$

$\Rightarrow V_{FB} = (-)ve$

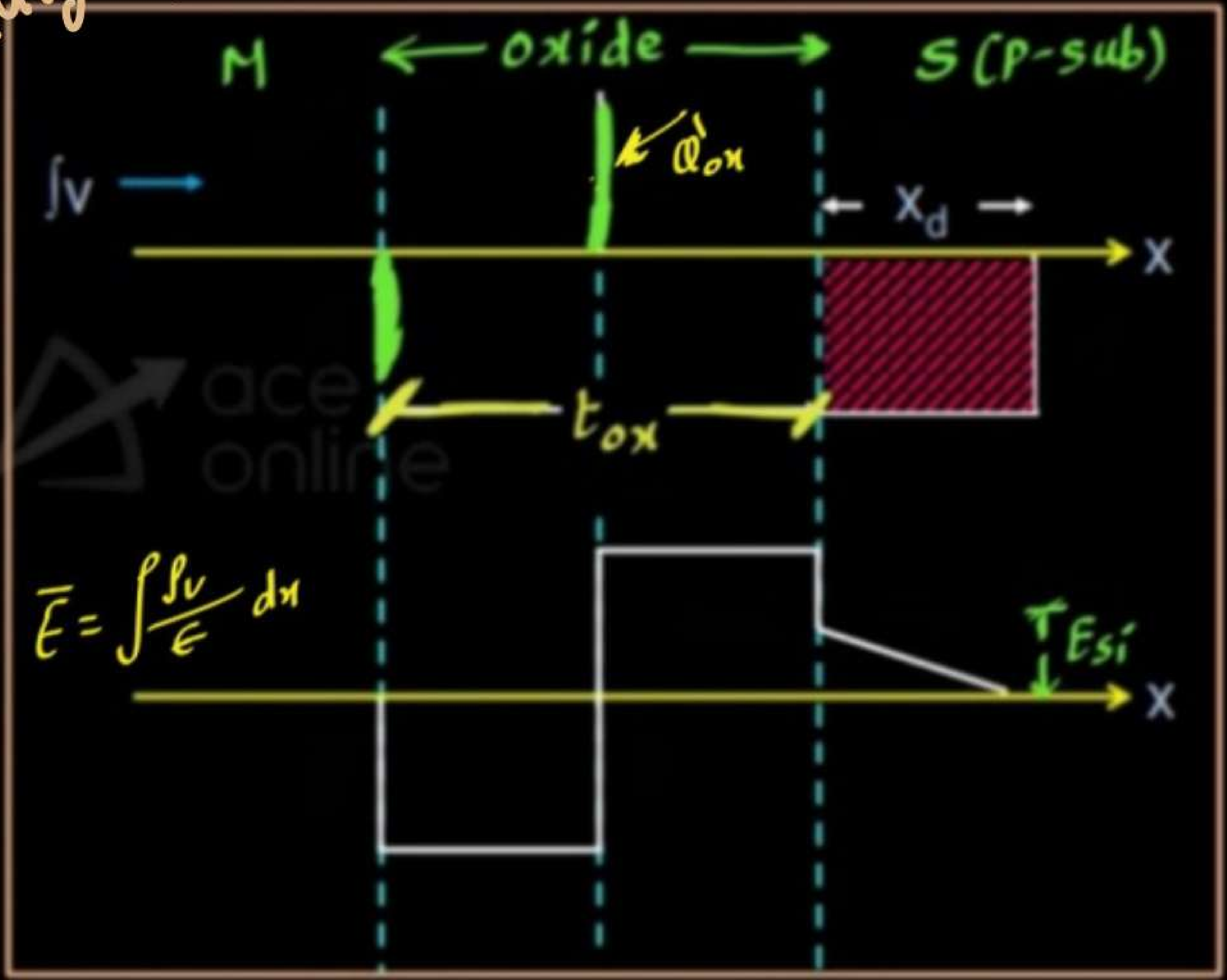
$\Rightarrow V_G = (-)ve$

Now to make bands flat, we should Apply $V_G = (-)ve$.

So, If $V_G = (-)ve \Rightarrow E_F$ moves up in Metal $\Rightarrow$ bands could be flat.

$\Rightarrow$ Due to $V_{FB}$, Threshold Voltage will be Modified.

2nd Non Ideality →




@ $V_G = 0V$ itself

@ Equilibrium itself we get depletion region in p-side.

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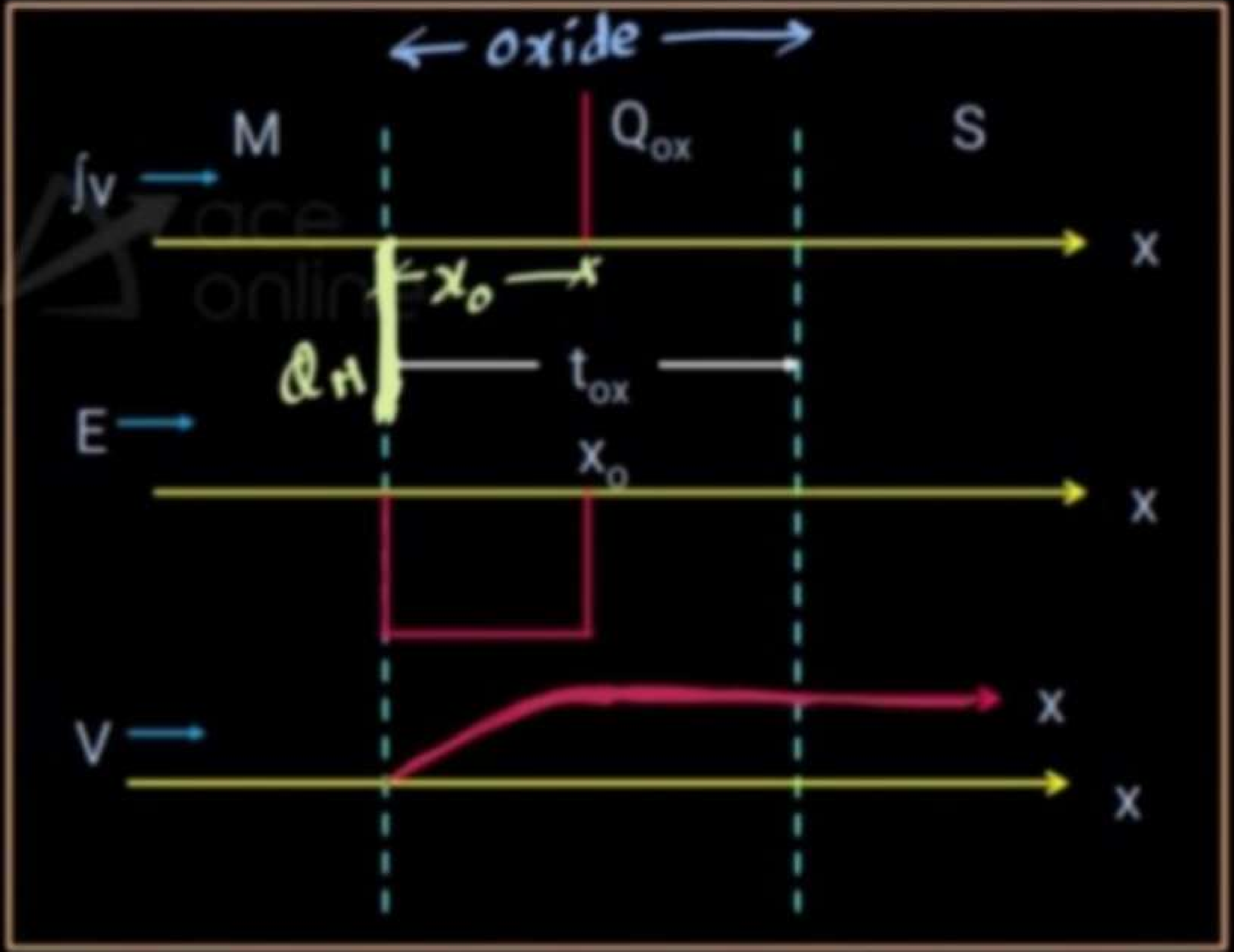
Now to make flat band, and understand that there is No depletion in s.c. i.e., (-ve) charges in metal ↑↑ ⇒ (-)ve charges in Metal ↑↑↑

⇒ Must provide $V_G = (-)ve$, which is Flat Band Voltage.




$\because Q = CV \Rightarrow V = \frac{Q}{C} = \frac{Q}{\frac{\epsilon}{d}}$

$\Rightarrow V = \frac{Q}{\epsilon} d$

Here
$V \longrightarrow V_{FB}$
$d \longrightarrow x_0$
$\epsilon \longrightarrow \epsilon_{ox}$
$Q \longrightarrow Q'_{ox}$

As $Q'_M + Q'_{ox} = 0$

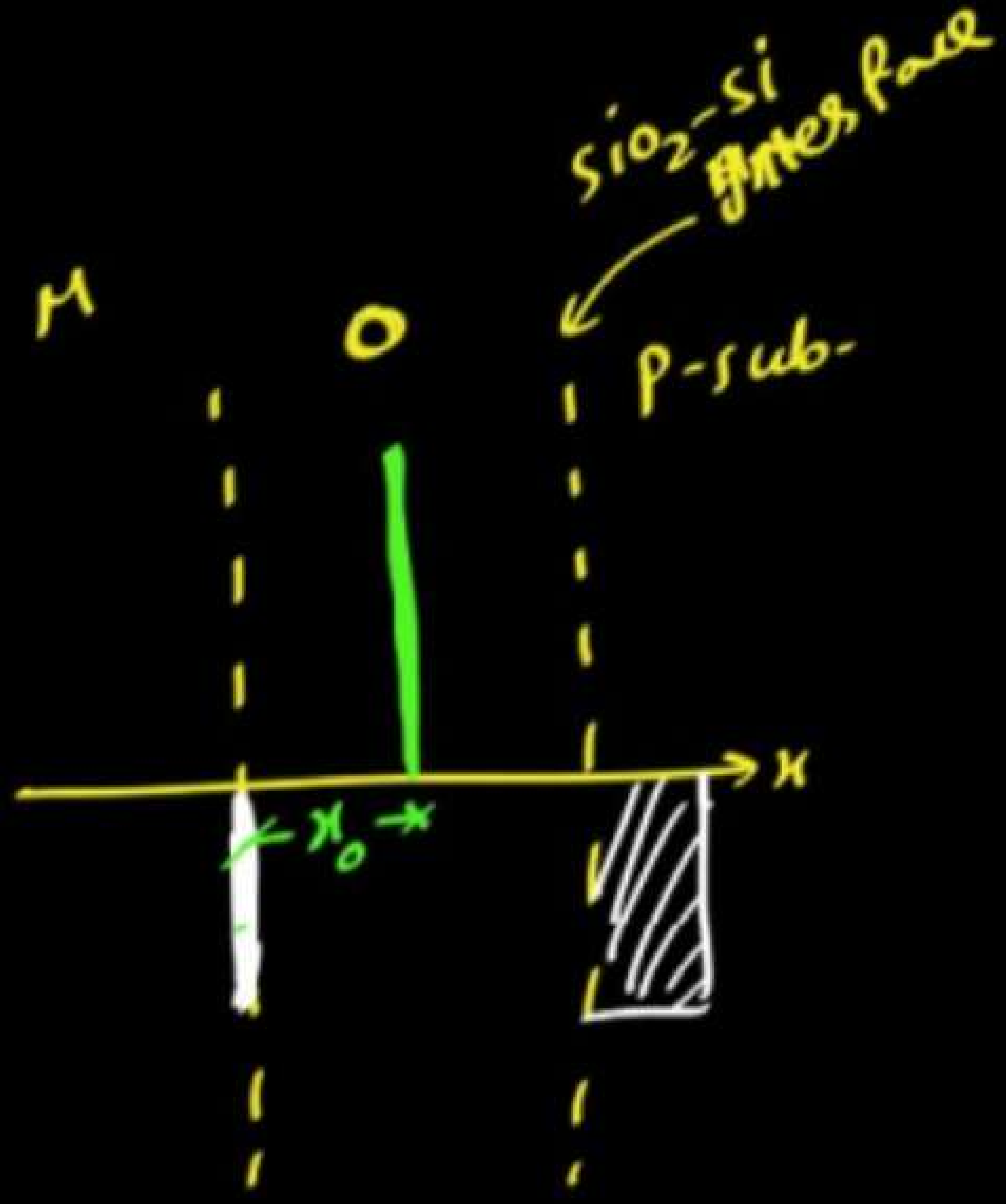
$\Rightarrow Q'_M = -Q'_{ox}$.

To Find $V_{FB_2} \longrightarrow$ (To Maintain Zero charge in Substrate).

$\downarrow$

Logic $\longrightarrow$ $Q' = C'V \Rightarrow V = \dfrac{Q'}{C'} = \dfrac{Q'}{\frac{\epsilon}{d}}$

$\therefore V = \dfrac{Q'}{\epsilon} d$




Now here $V \rightarrow V_{FB_2}$

$d \rightarrow x_0$

$\epsilon = \epsilon_{ox}$

$Q' = Q'_{ox}$

Target to Make $Q'_{dep} = 0$.

$\therefore Q'_M + Q'_{ox} = 0$.

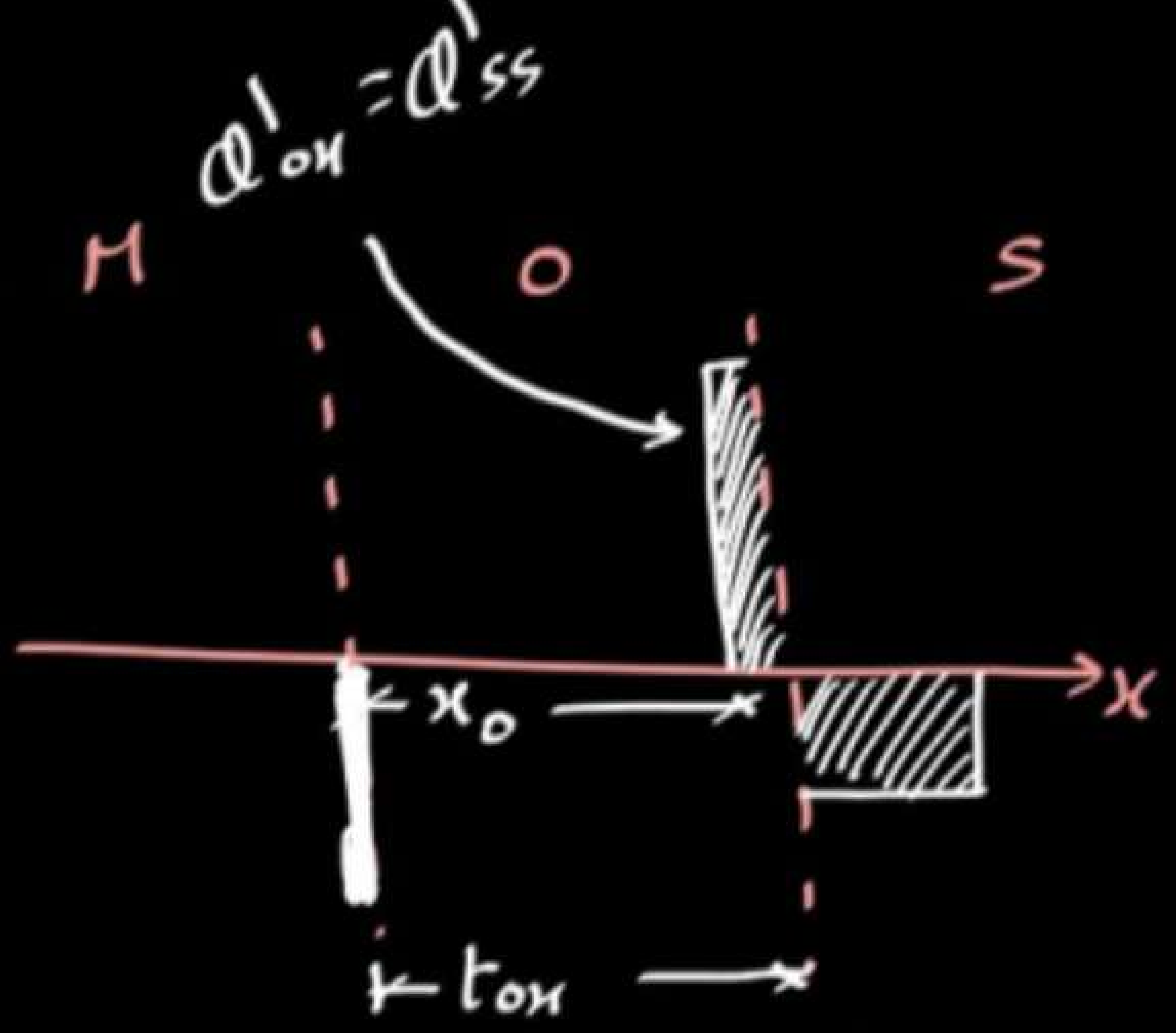
[$Q'_{oxide}$ Must to be balanced by $Q'_{Metal}$].

$$\therefore \boxed{V_{FB_2} = \frac{-Q'_{ox}}{\epsilon_{ox}} \cdot x_o}$$

$$V_{FB_2} = \frac{-Q'_{ox}}{\epsilon_{ox}} \cdot x_o \cdot \frac{t_{ox}}{t_{ox}}$$

Since, $C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

$$\Rightarrow \boxed{V_{FB_2} = \frac{-Q'_{ox}}{C'_{ox}} \cdot \frac{x_o}{t_{ox}}}$$




$\Rightarrow x_o = t_{ox}$.

In GATE Exam $\longrightarrow$ If $Q'_{ox}$ is given @ Surface of $Si$ - $SiO_2$

$$\therefore \boxed{V_{FB_2} = \frac{-Q'_{ox}}{C'_{ox}}}$$

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$$\Rightarrow V_{FB_2} = \frac{-Q'_{ox}}{\epsilon_{ox}} x_0$$

$$= \frac{-Q'_{ox}}{\epsilon_{ox}} \cdot x_0 \cdot \frac{t_{ox}}{t_{ox}}$$

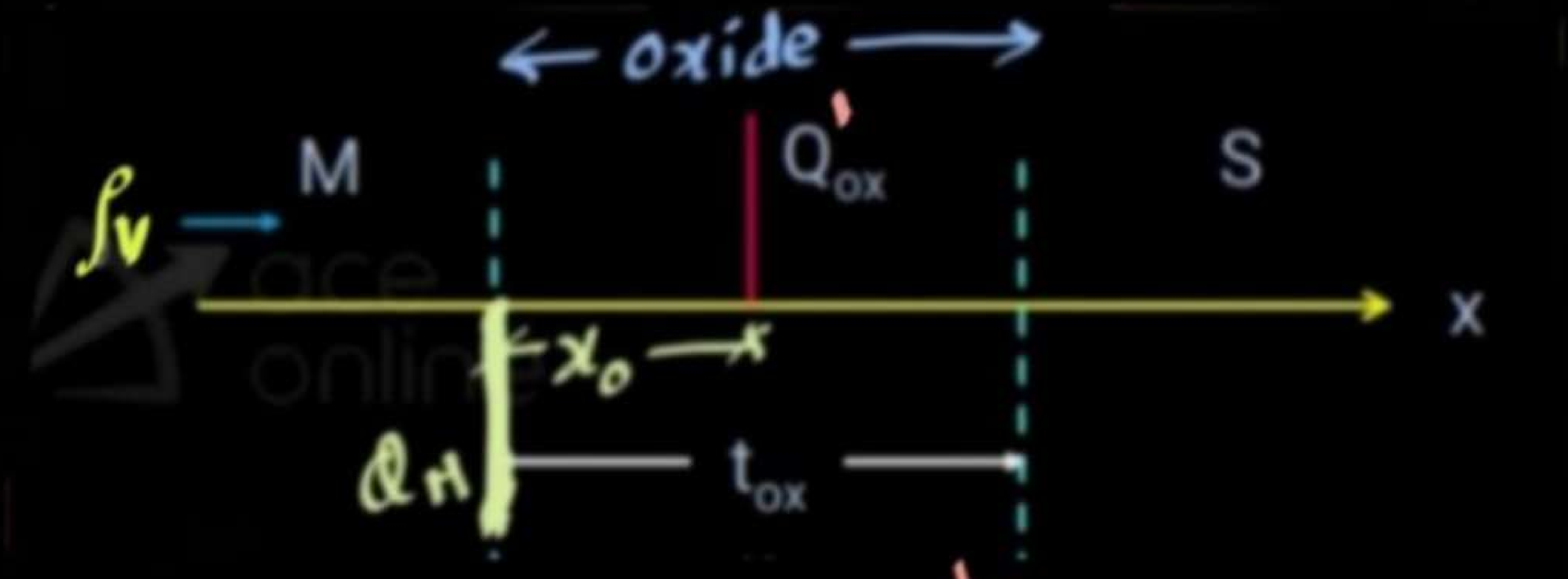
$$\Rightarrow \boxed{V_{FB_2} = \frac{-Q'_{ox}}{C'_{ox}} \cdot \frac{x_0}{t_{ox}}.}$$

[$Q'_{ox}$ = charge in oxide/unit Area];

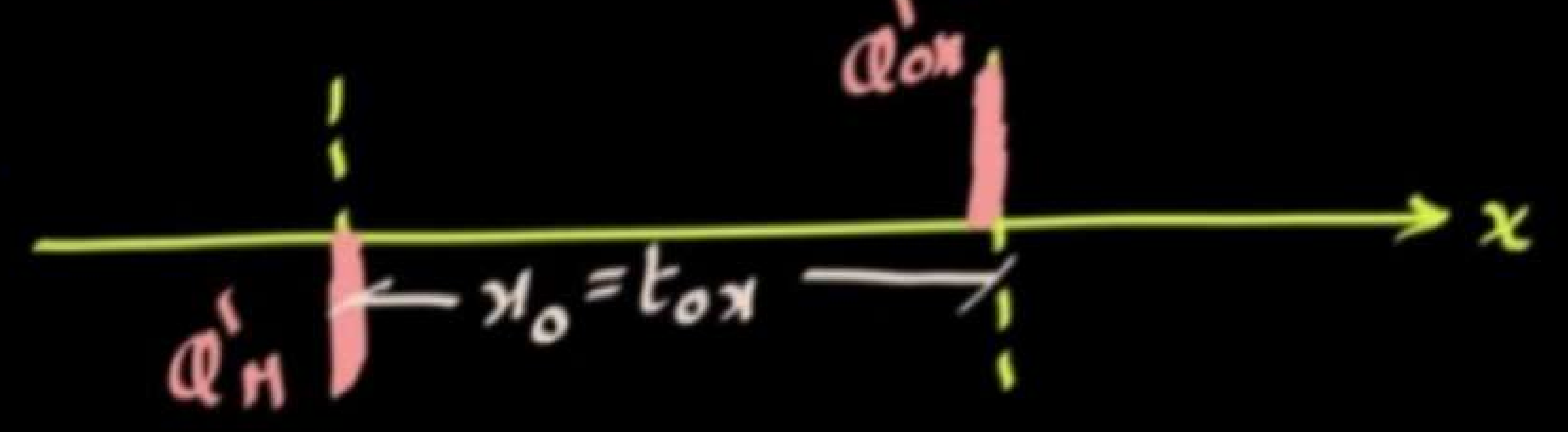
This is $V_{FB}$ due to 2nd Non Ideality.

In GATE Exam, If $x_o$ given $= t_{ox}$,

then →




Now $\rho_V$ →



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Then $V_{FB} = \frac{-Q'_{ox}}{C_{ox}'} \cdot \frac{x_o}{t_{ox}}$

$= \frac{-Q'_{ox}}{C_{ox}'}$.

Hence Overall Flat Band Voltage,

$$V_{FB} = \underbrace{(V_{FB})}_{\text{due to 1st Non Ideality}} + \underbrace{(V_{FB})}_{\text{due to 2nd Non Ideality}}$$

$$\Rightarrow V_{FB} = \phi_{MS} + \left[\frac{-Q_{ox}'}{C_{ox}'}\left[\frac{x_0}{t_{ox}}\right]\right]$$

$$\Rightarrow \text{Practical,} \quad \boxed{V_{Th} = \frac{\sqrt{2q\epsilon_{si}N_A(2\phi_F)}}{C_{ox}'} + 2\phi_F + V_{FB}.}$$

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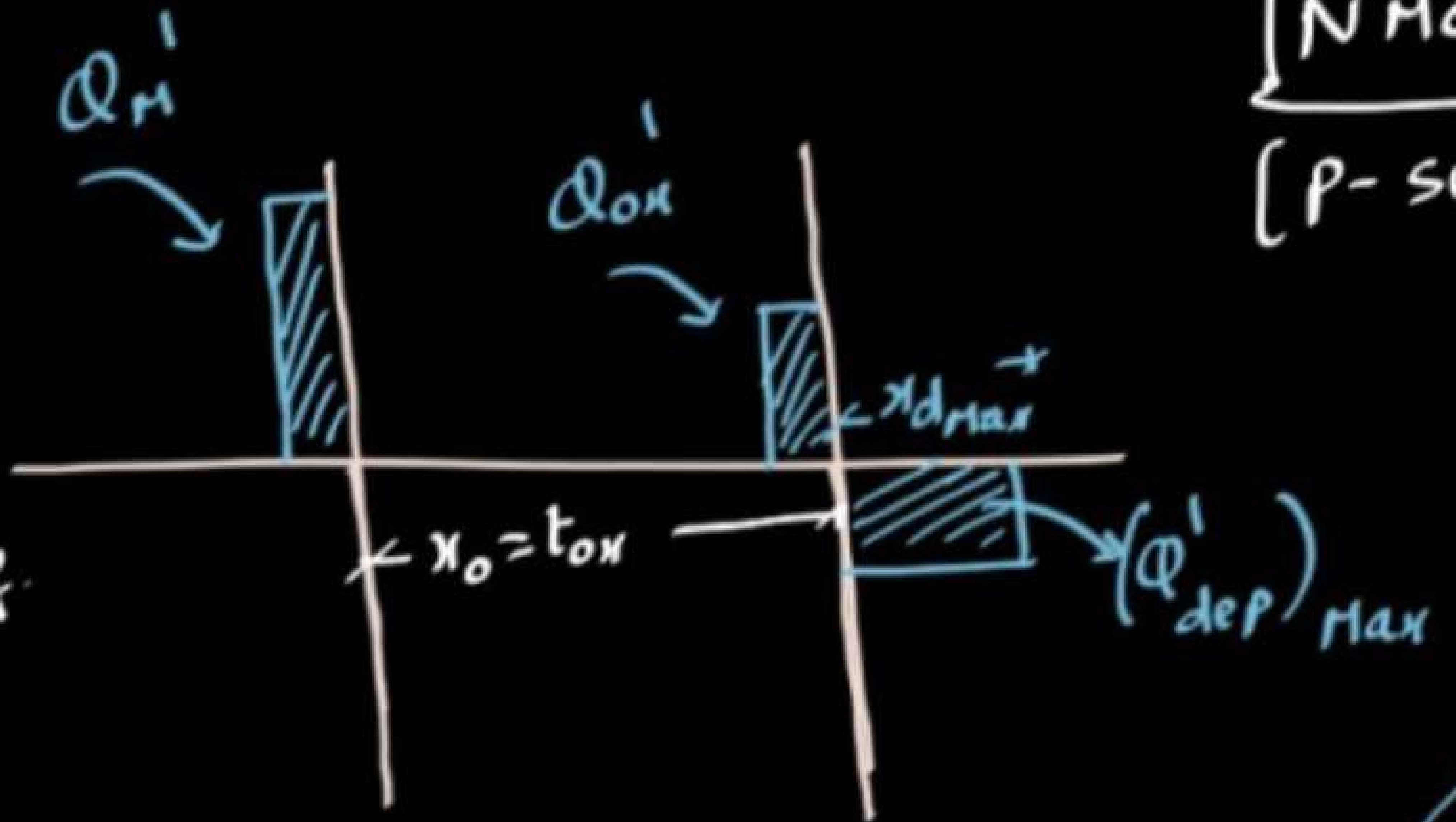
$$\therefore \boxed{V_{Th} = V_{Th_0} + V_{FB}}$$

$V_{Th_0}$ → Threshold voltage for Ideal MOS Diode.

Note →

$\boxed{\text{NMOS}}$

[p- substrate].




@ $V_G = V_{Th}$, $\psi_{si} = 2\phi_f$.

$$V_{Th} = \frac{|Q'_{dep}|_{Max}}{C_{ox}'} - \frac{Q'_{ox}}{C_{ox}'} + \phi_{MS} + 2\phi_f$$

[Taken as (-)ve]

If $Q'_{dep_{Max}} = -qN_A x_{d_{Max}}$

Then take $\left[\frac{-Q'_{dep_{Max}}}{C_{ox}'}\right]$ in $V_{Th}$ formulae.

If $Q'_{dep_{Max}} = qN_A x_{d_{Max}}$

Then take $\left[\frac{Q'_{dep_{Max}}}{C_{ox}'}\right]$ in $V_{Th}$ formulae.

If $Q'_{dep} = -q(x_{dep})_{Max} N_A$

VFB2 VFB1

$$\Rightarrow V_{Th} = \frac{-(Q'_{dep})_{Max}}{C_{ox}'} - \frac{Q'_{ox}}{C_{ox}'} + \phi_{MS} + 2\phi_f.$$

Also $\rightarrow$ $V_{Th} = \left[ \left| Q'_{dep} \right|_{Max} - Q'_{ox} \right] \left[ \dfrac{t_{ox}}{\epsilon_{ox}} \right] + \phi_{MS} + 2\phi_{fp}$

Also $\rightarrow$ $V_{Th} = \dfrac{\left| Q'_{dep} \right|_{Max}}{C'_{ox}} + V_{FB} + 2\phi_{fp}$.

Negative $V_{Th}$ for p-type Substrate $\Rightarrow$ Depletion Mode device, An (-)ve Vol. Must be Applied to GATE in order to Make Inversion layer charge to Zero.

where (+)ve Gate voltage will Induce a layer "Inversion layer charge".

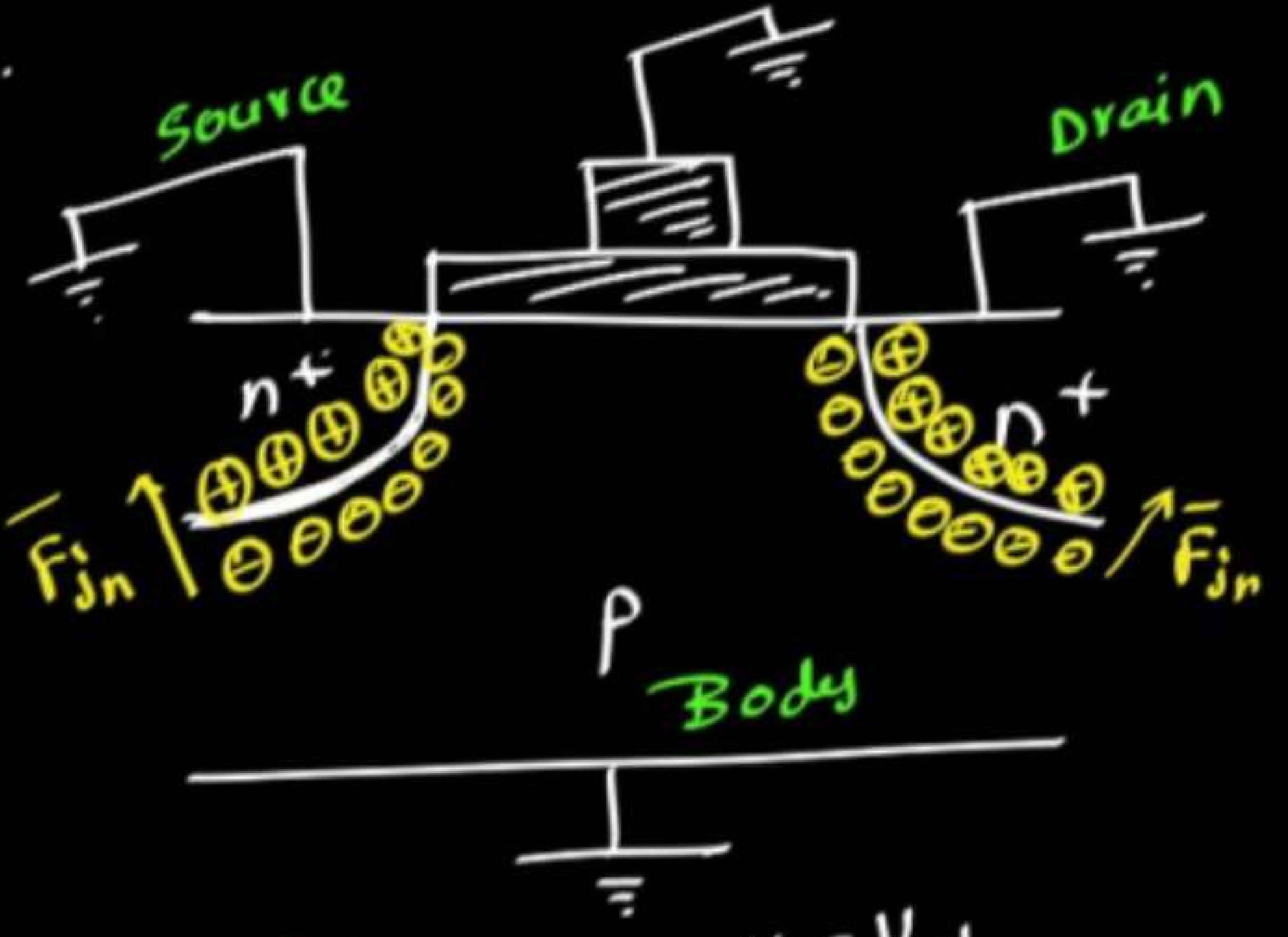
Similarly $\longrightarrow$ n-type Substrate $\rightarrow$

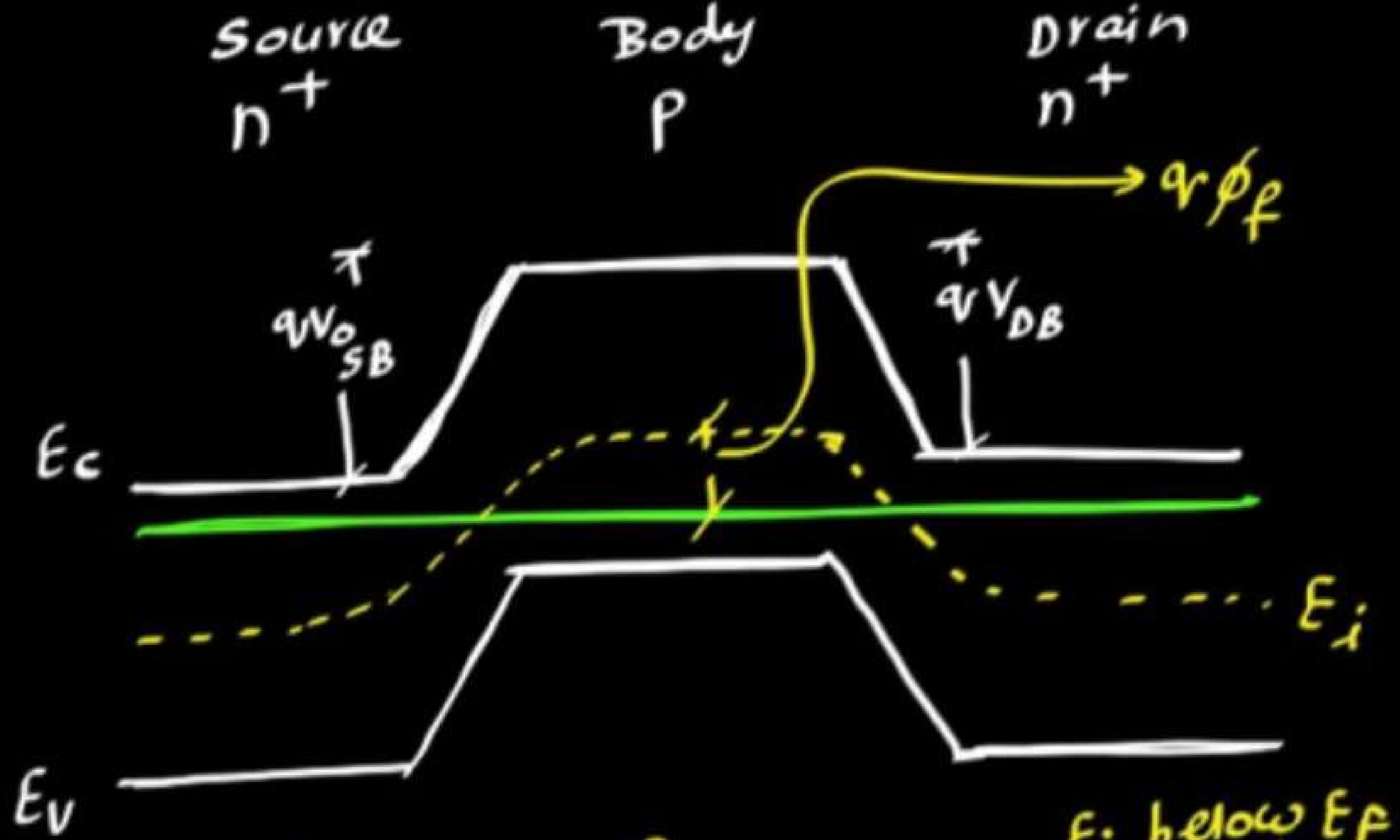
$$V_{TP} = \left[-|Q'_{dep}|_{max} - Q'_{ox}\right]\left[\frac{t_{ox}}{\epsilon_{ox}}\right] + \phi_{ms} - 2\phi_{fn}.$$

where $|Q'_{dep}|_{max} = qN_D x_{d_{max}}$.

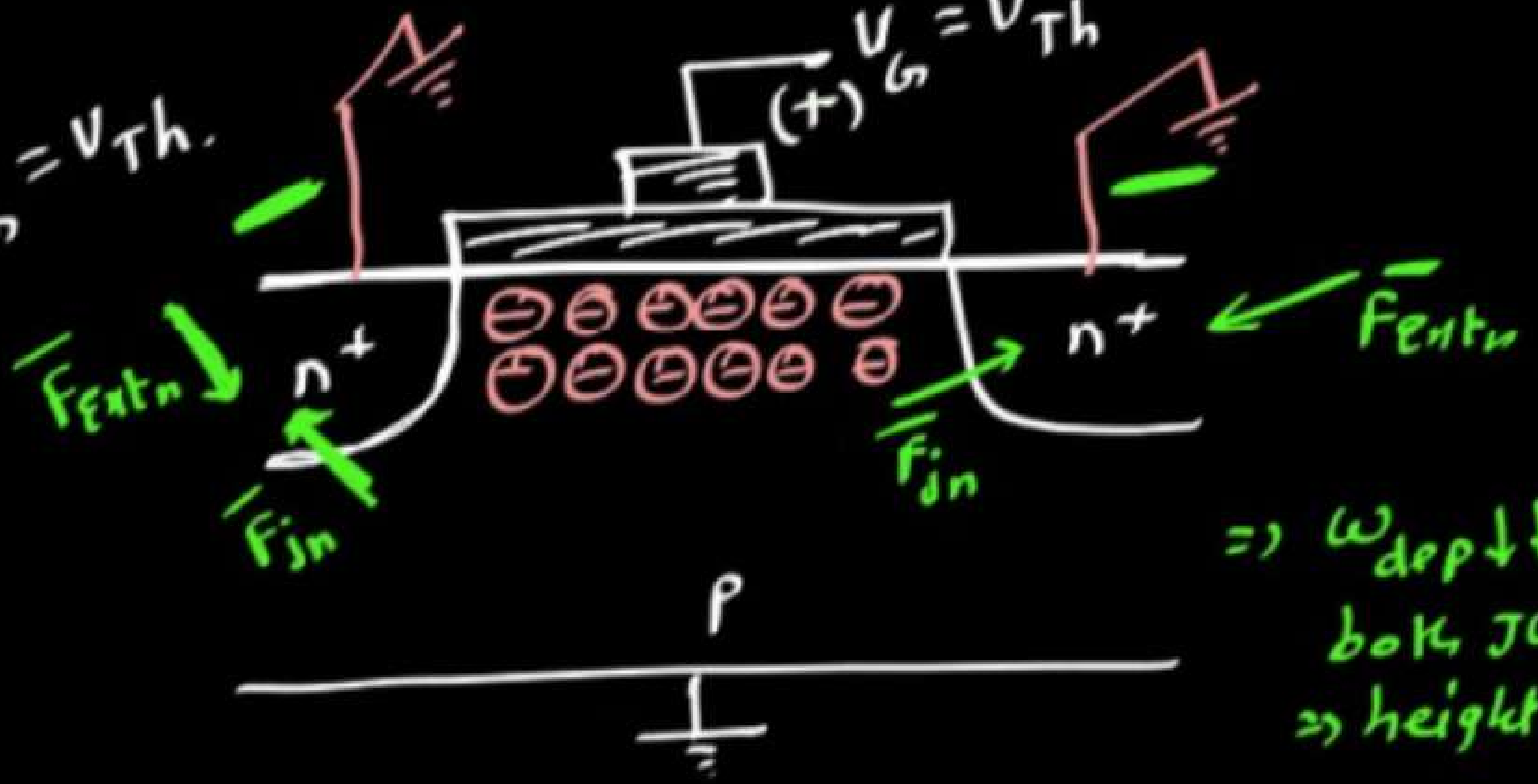
Body Effect →

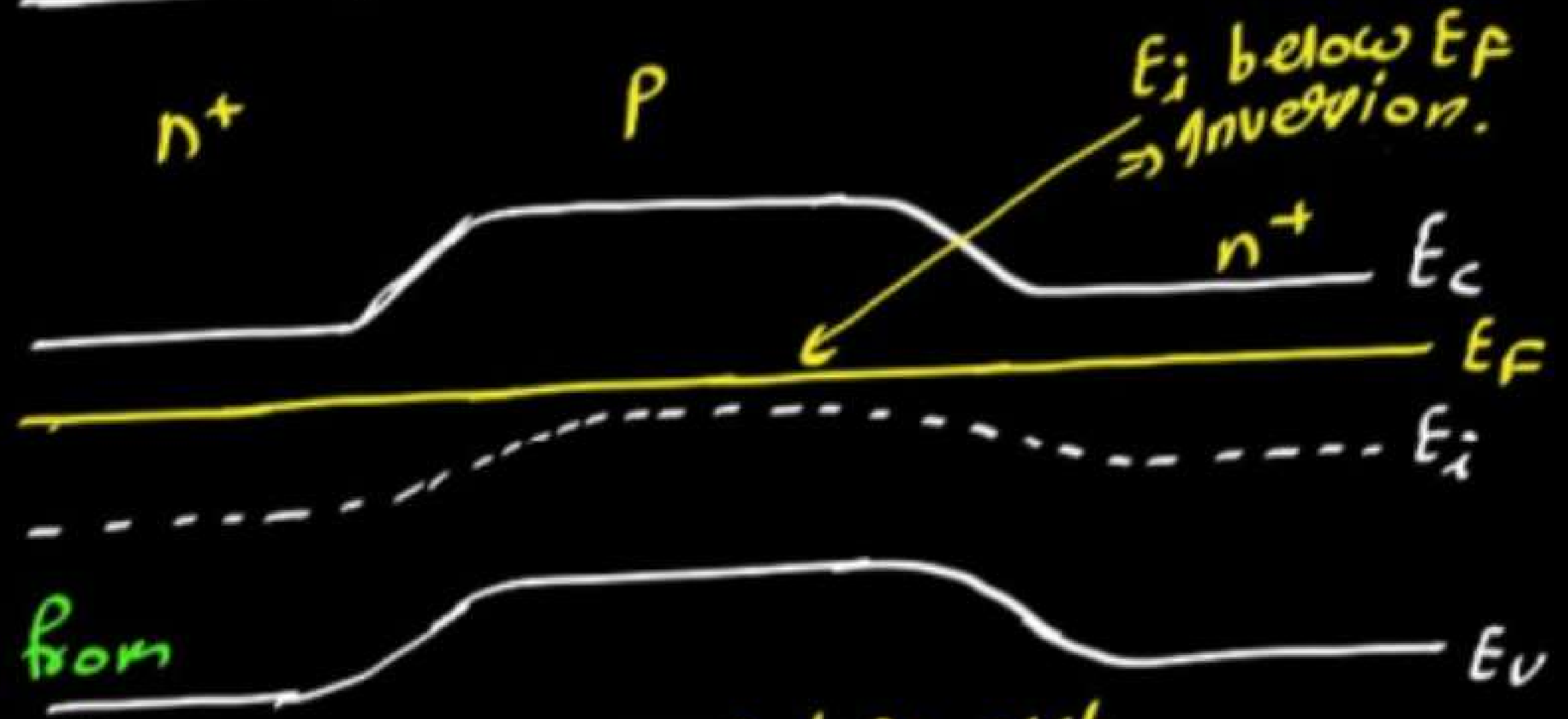
@$V_G = 0V$.



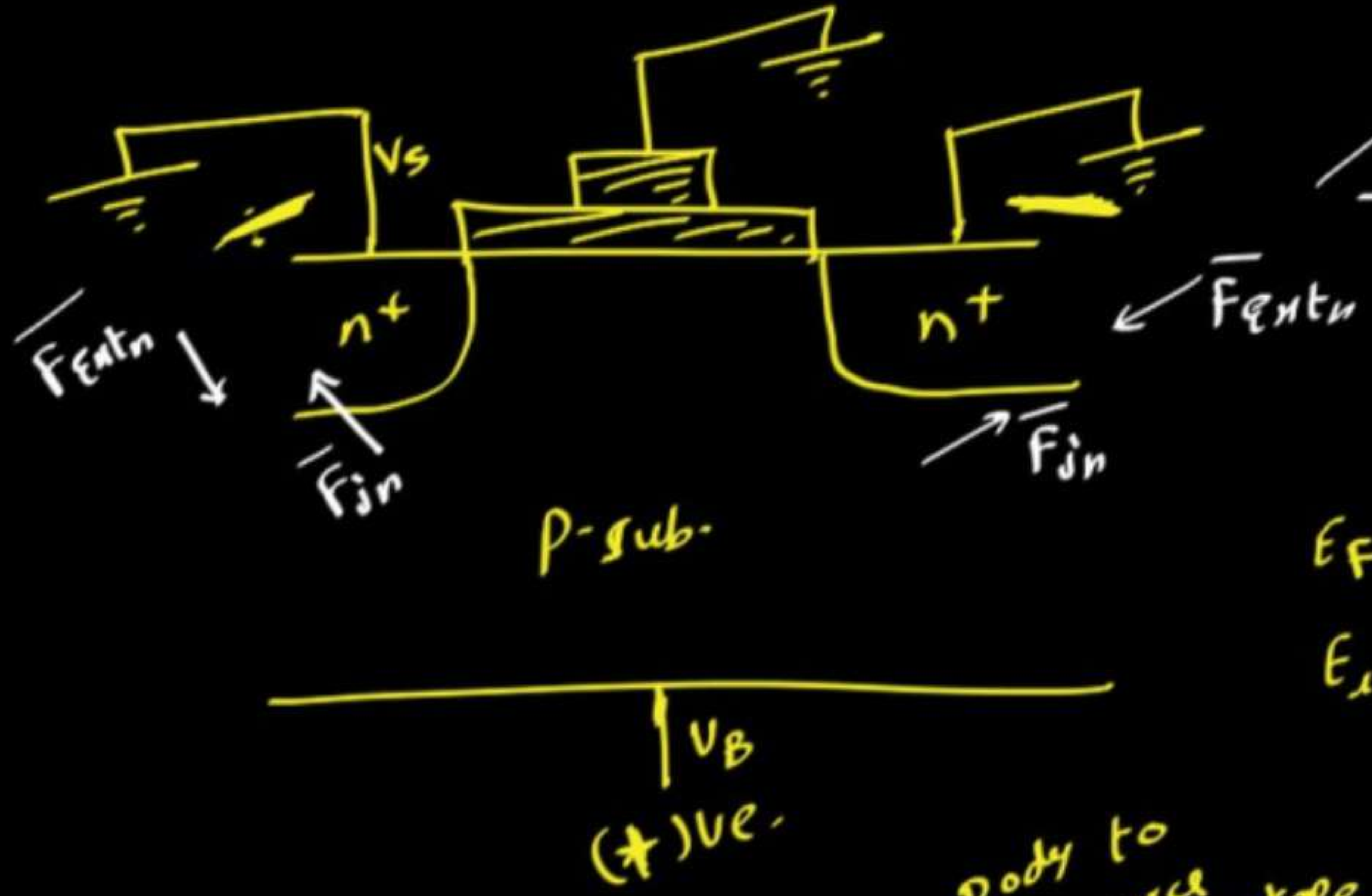

@$V_G = V_{Th}$.




⇒ $\omega_{dep}\downarrow\downarrow$ from both junction
⇒ height of slope $\downarrow\downarrow$.

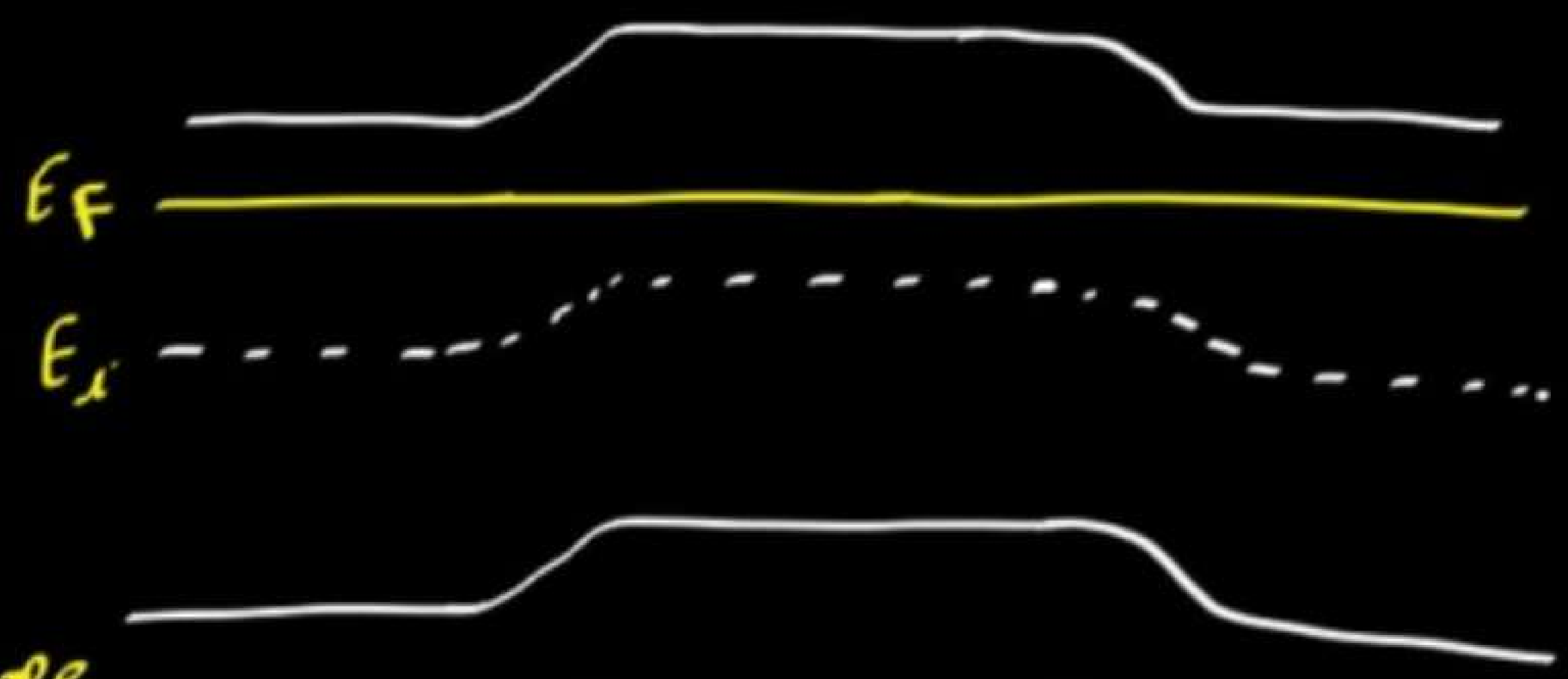
⇒ p-type act as n-type.




$\rightarrow w_{dep}\downarrow$

$\rightarrow$ Slope $\downarrow$

Even Now ∃ Channel.




Body to source voltage

Here In this case,

$V_{BS} = (+)ve$

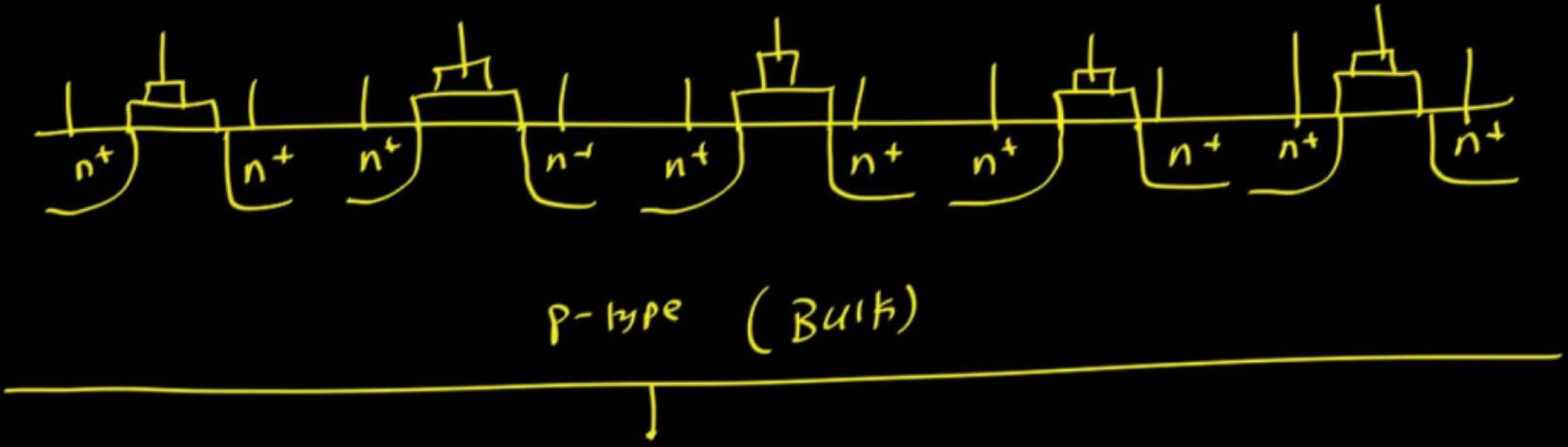
(or) $V_{SB} = (-)ve$

Body Effect

(or) Back Effect

(or) Bulk Effect.

IN IC's $\longrightarrow$



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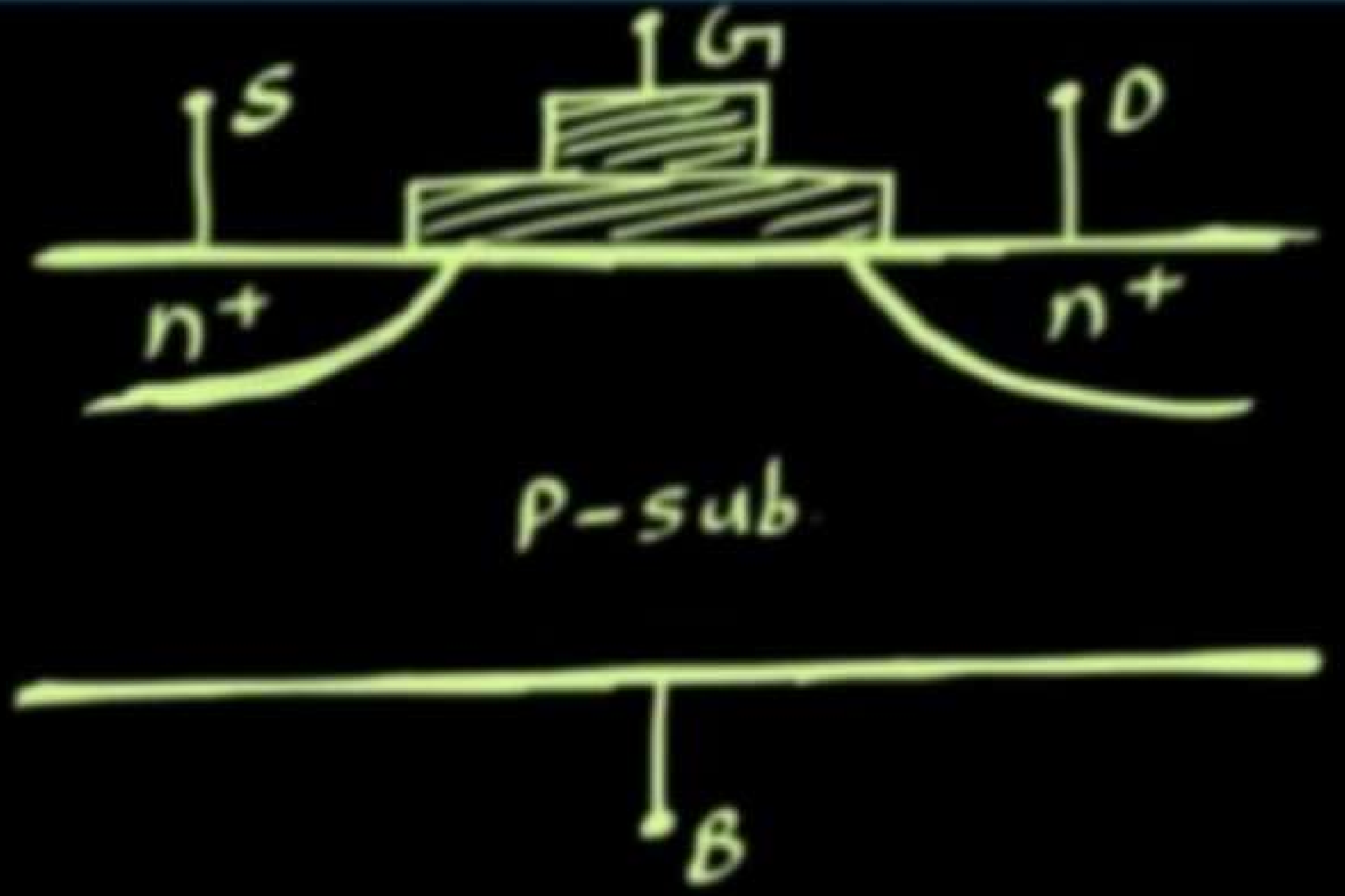
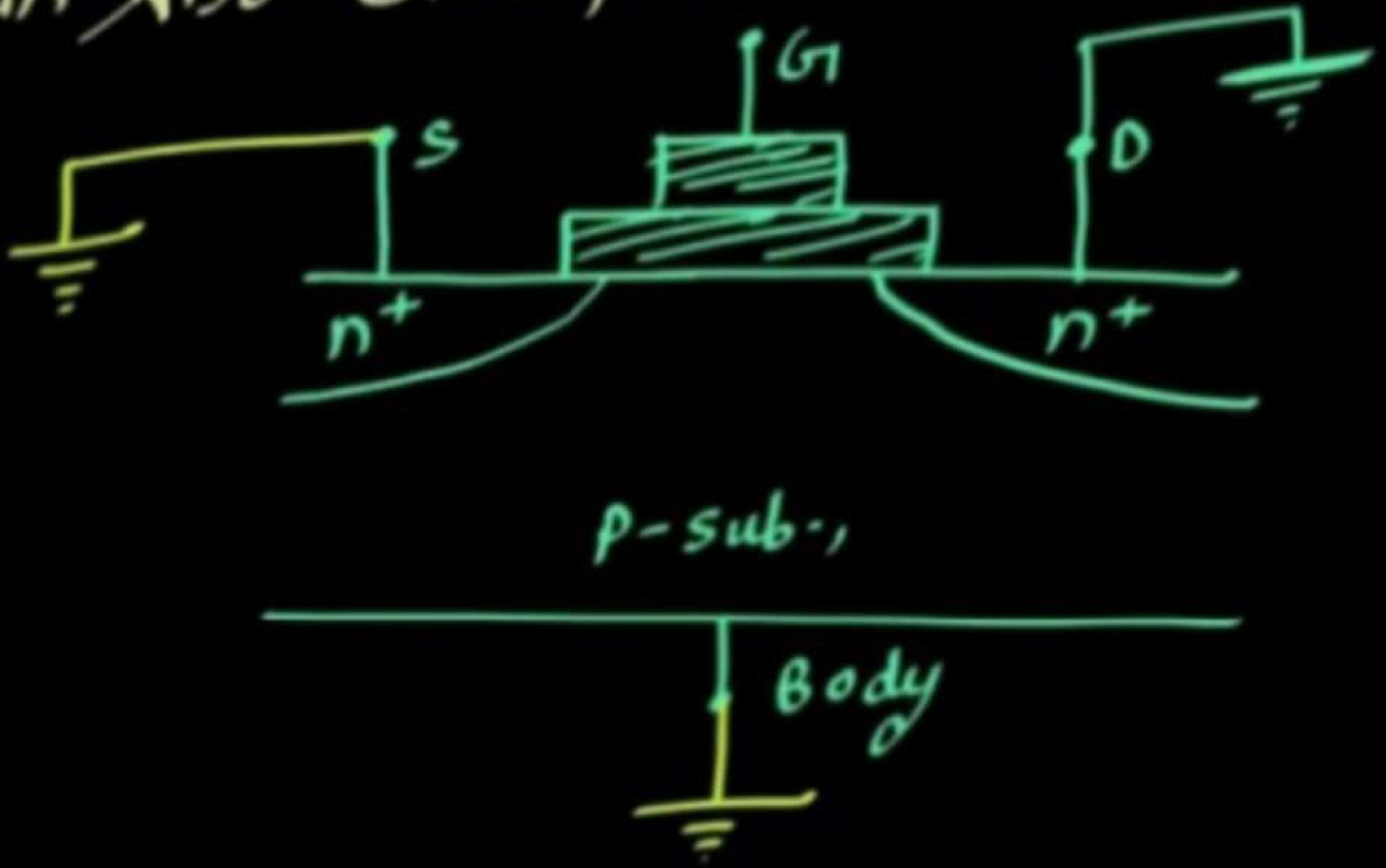
If pottentials of Body and Source are Not Same → ? Body/Back/Bulk Effect.

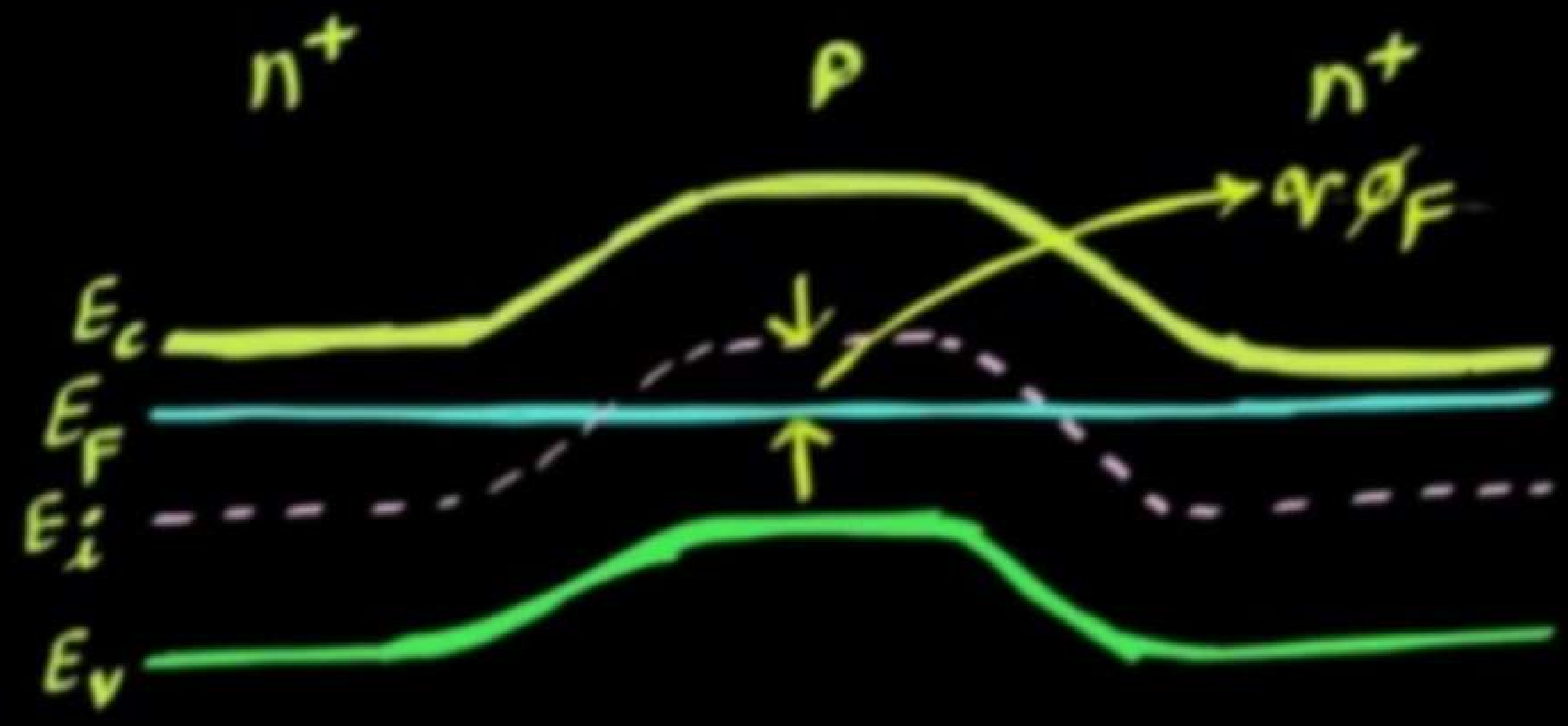



Initially Assume Pottentials @ Bulk & Source are Same, Let Initially source is GND.

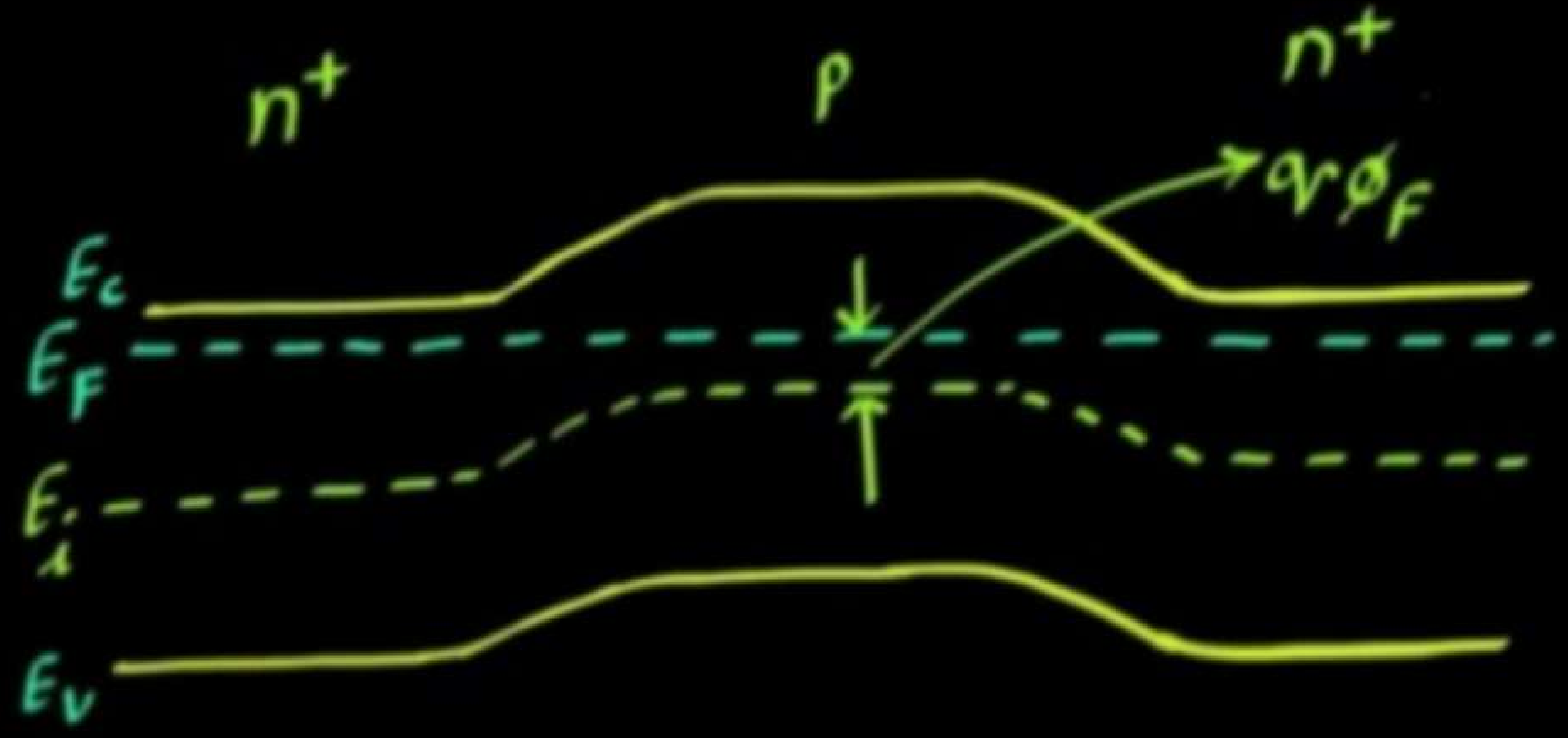
To Understand in More detailed →

As we don't Need Any Current Now (for testing) Let Drain Also Grounded.

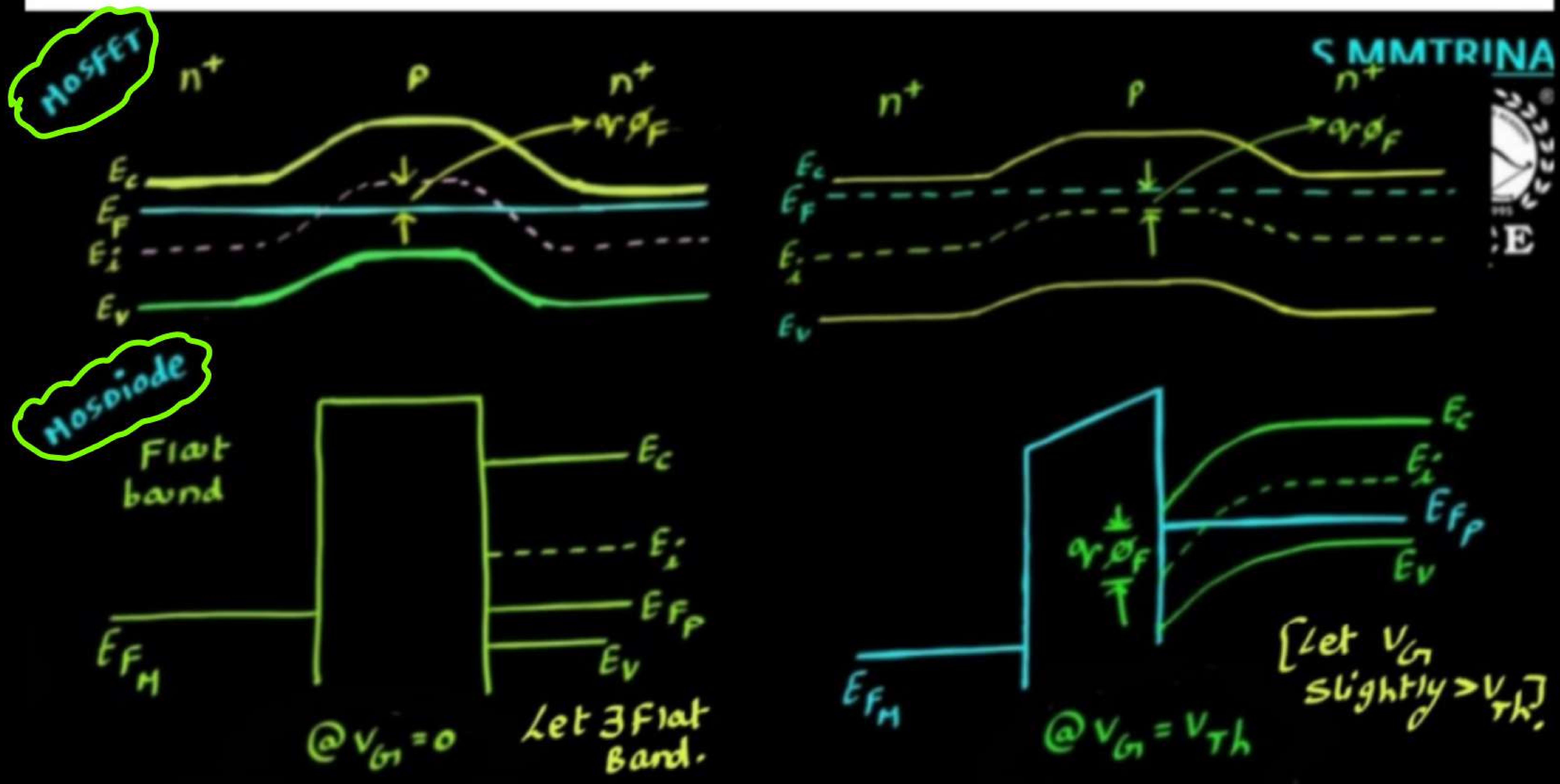





→ Energy band diagram for MOSFET @ $V_G = 0$.




→ Energy band Diagram of MOSFET @ $V_G = V_{Th}$.


MOSFET
n+
p
n+
$q\phi_F$
$E_c$
$E_F$
$E_i$
$E_v$
n+
p
n+
$q\phi_F$
$E_c$
$E_F$
$E_i$
$E_v$
Mosdiode
Flat band
$E_c$
$E_i$
$E_{F_p}$
$E_v$
$E_{F_M}$
@$V_G=0$
Let ∃ Flat Band.
$E_c$
$E_i$
$E_{F_p}$
$E_v$
$q\phi_F$
$E_{F_M}$
@$V_G = V_{Th}$
[Let $V_G$ slightly $> V_{Th}$]

Now

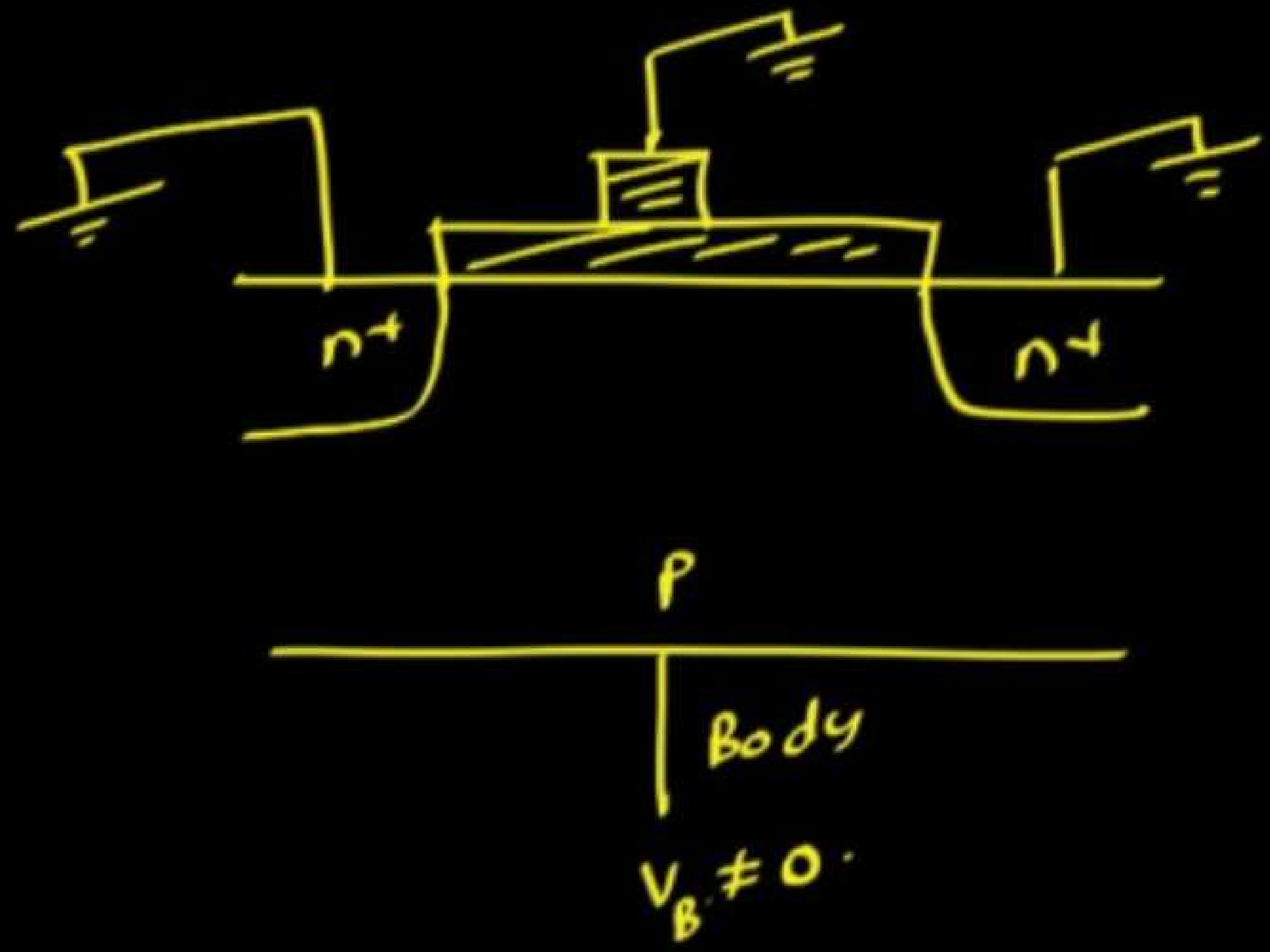
Let →

$V_G = 0$

$V_S = 0$

$V_D = 0$

$V_B \neq 0$



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Now let $V_{SB} = (-)ve \Rightarrow V_S - V_B = (-)ve \Rightarrow V_B$ Must be positive.

① $V_B = (+)ve \Rightarrow$ P-sub. is (+)ve $\Rightarrow$ F-bias $\Rightarrow qV_{bi}\downarrow\downarrow\downarrow$

$\Rightarrow$ @ $V_G = 0V \longrightarrow$


③ Barrier pottential decreased by $qV_{SB}$.

④ @ $V_G = 0V$ in previous case slope is large, so to invert channel we have given large $V_{Th}$.

⑤ But Now as slope$\downarrow\downarrow\downarrow$ $\Rightarrow$ to get $\psi_s = 2\phi_F$ we get this @ lesser $V_G$ to get a Threshold point $\Rightarrow V_{Th}\downarrow\downarrow \Rightarrow V_B$ decides the surface charge.

Now let $V_{SB} = (+)ve \Rightarrow V_S - V_B = (+)ve \Rightarrow V_B = (-)ve.$

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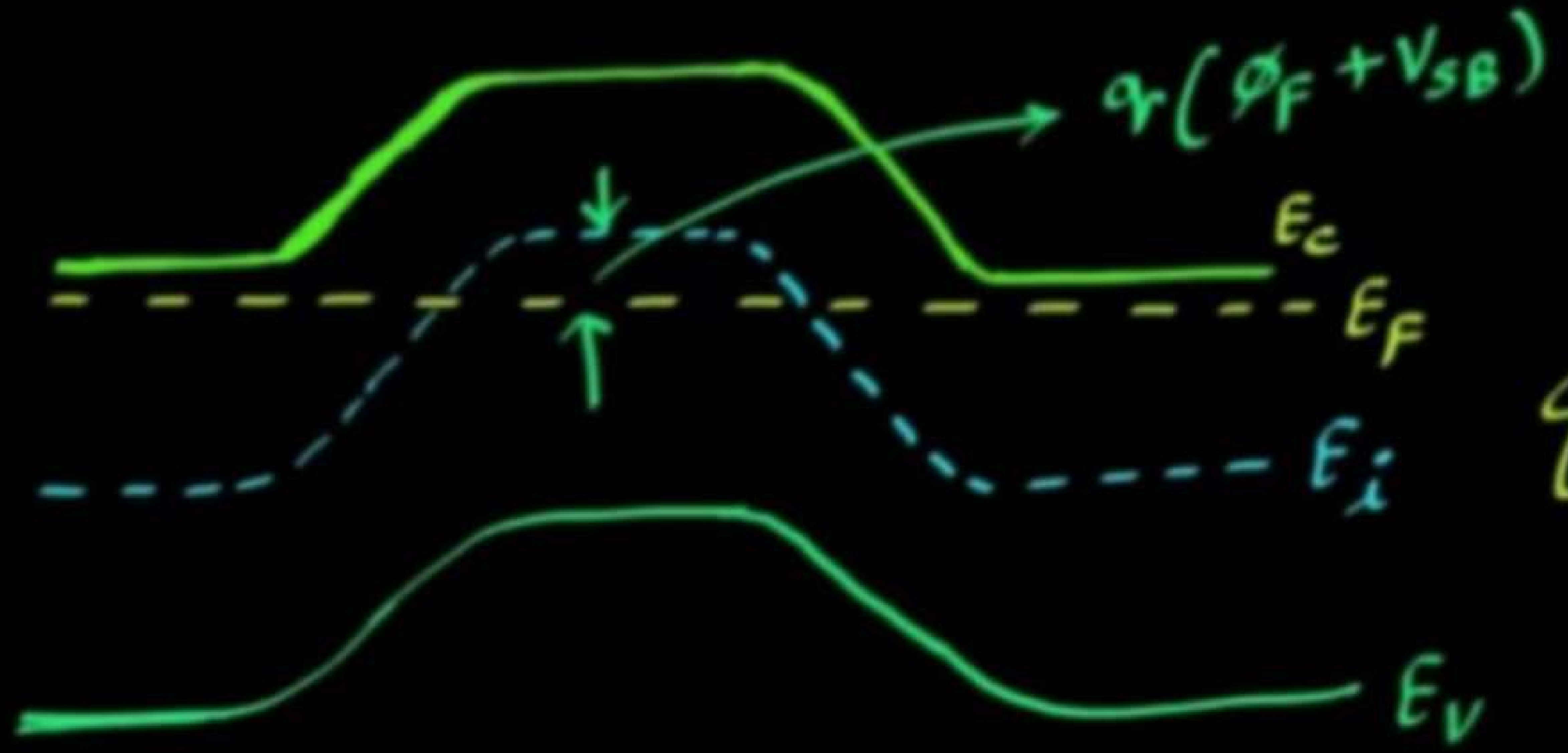
$\Rightarrow$




Now Barrier potential Slope ↑↑↑ by $qV_{SB}$,

Now to get $\psi_s = 2\phi_F$,

$V_{Th}$ ↑↑↑.

To do this we must Apply large $V_G$.

This Effect is Called

Body Effect (or) Bulk Effect

(or) Back Effect.

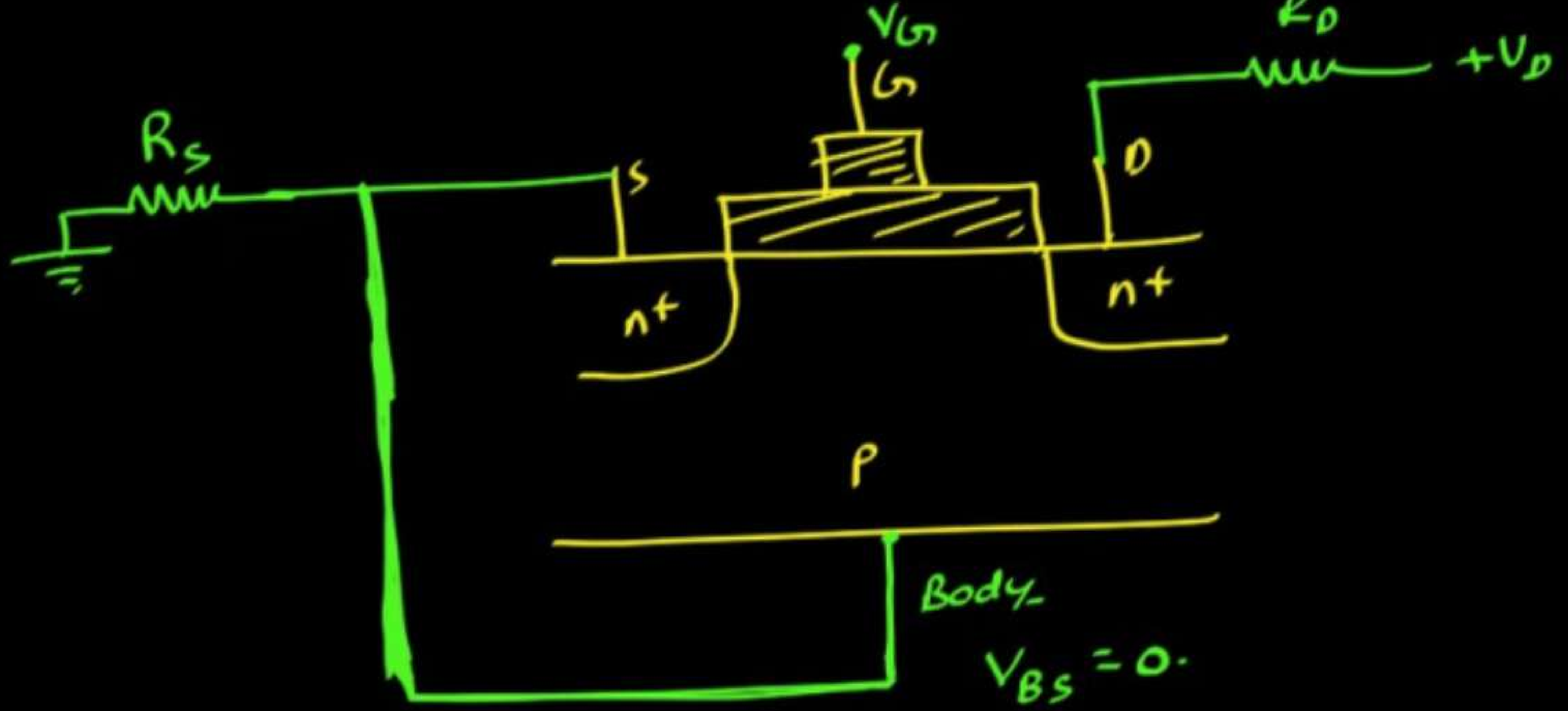
Hence By Including Body Effect,

$$V_{Th} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_{si} N_A (2\phi_F + V_{SB})}}{C_{ox}'}.$$

Responsible for Body Effect.

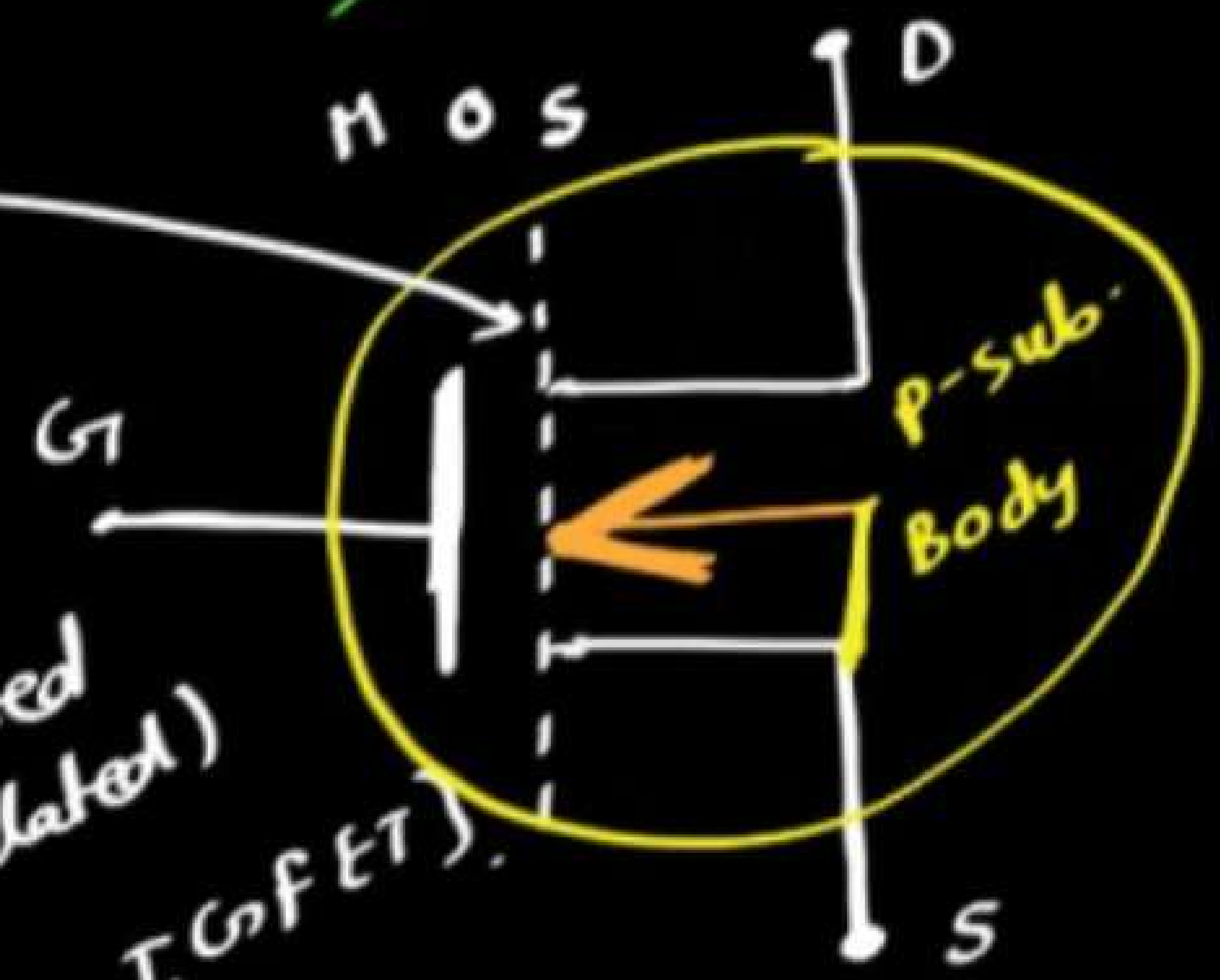
$\therefore$ To Avoid Body Effect,

we must make $V_{SB} = 0$.

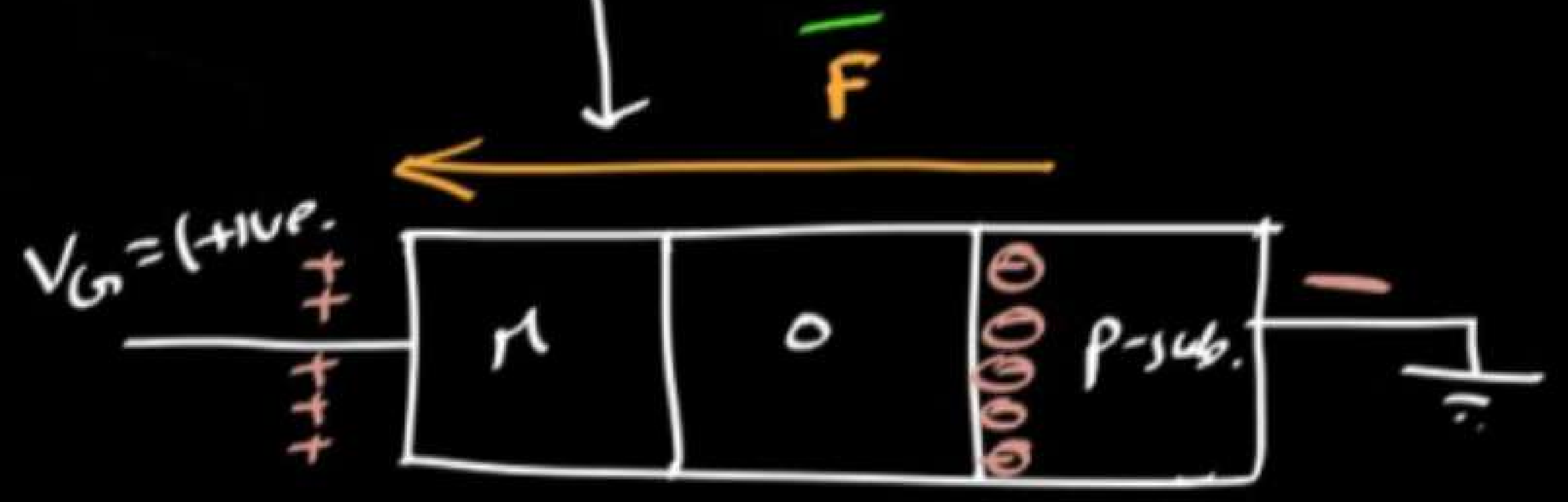


From Above Analysis →

Channel is Temporary.



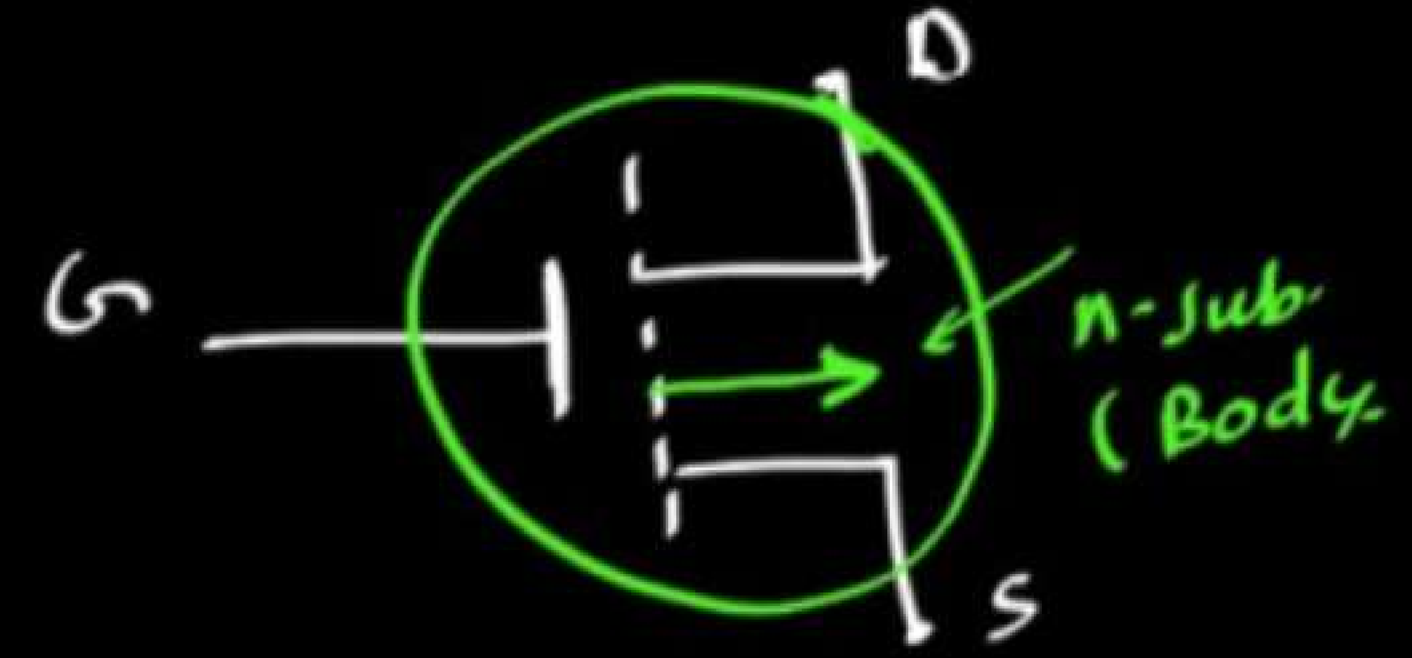

Let NMOS

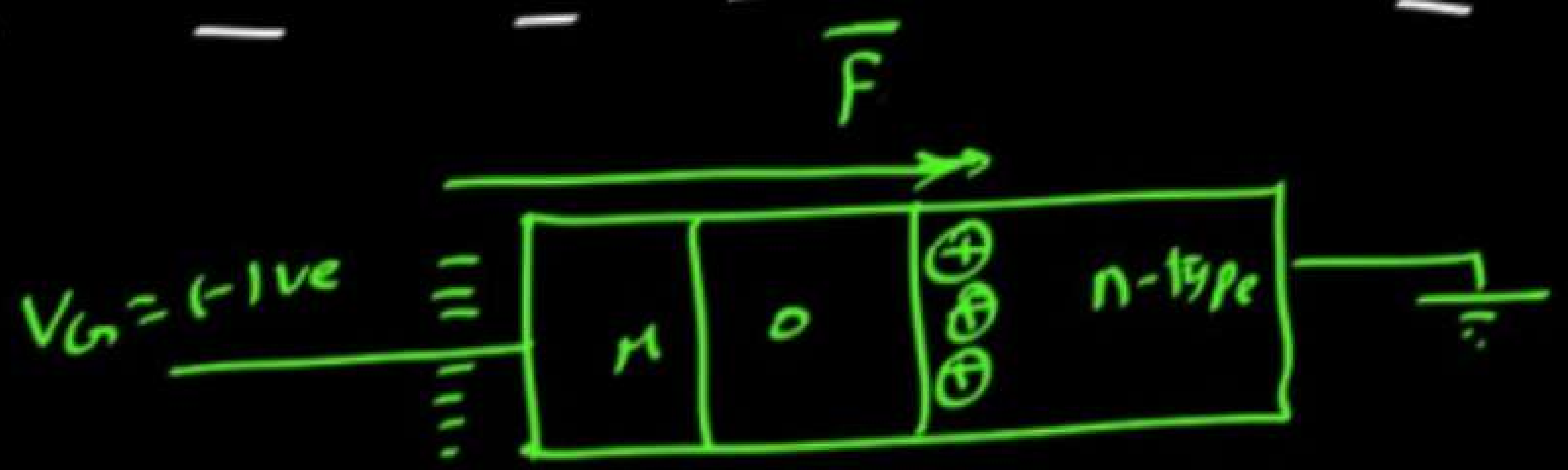


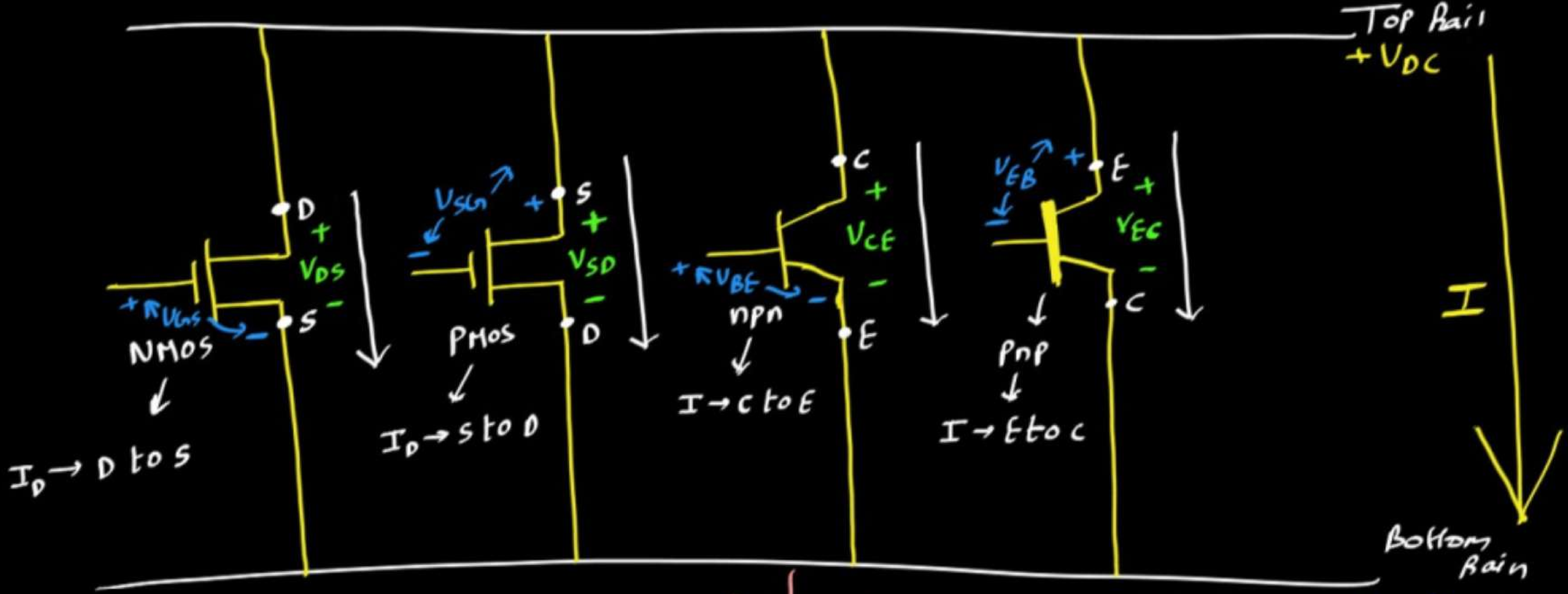

G → Isolated
(Insulated)

(MOSFET ↔ IGFET)

PMOS →



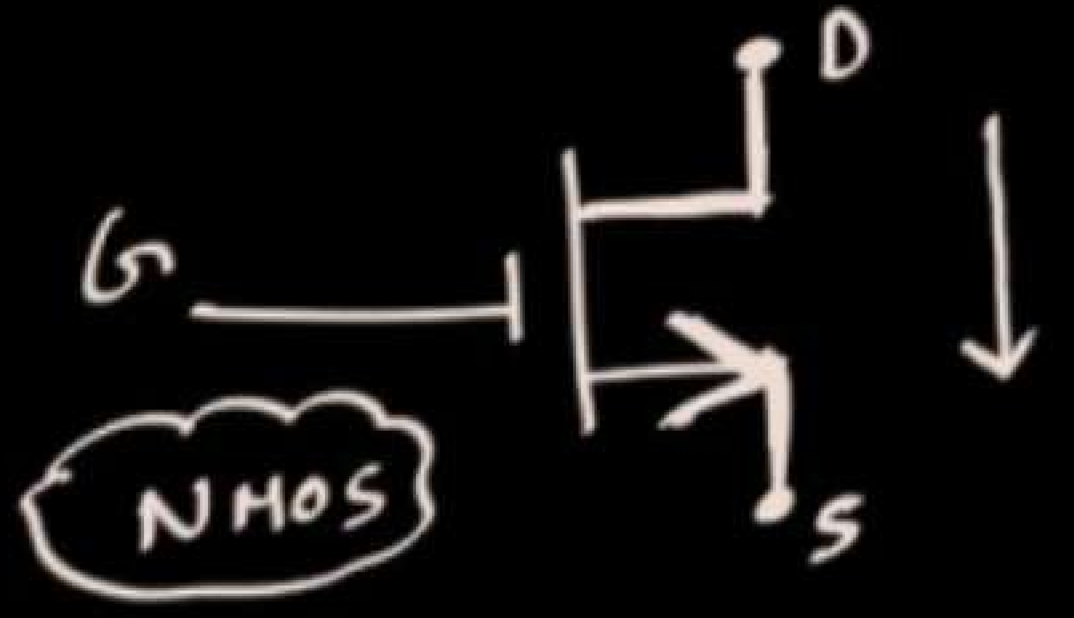



$-V_{DC}$ (Low) (or) (GND)

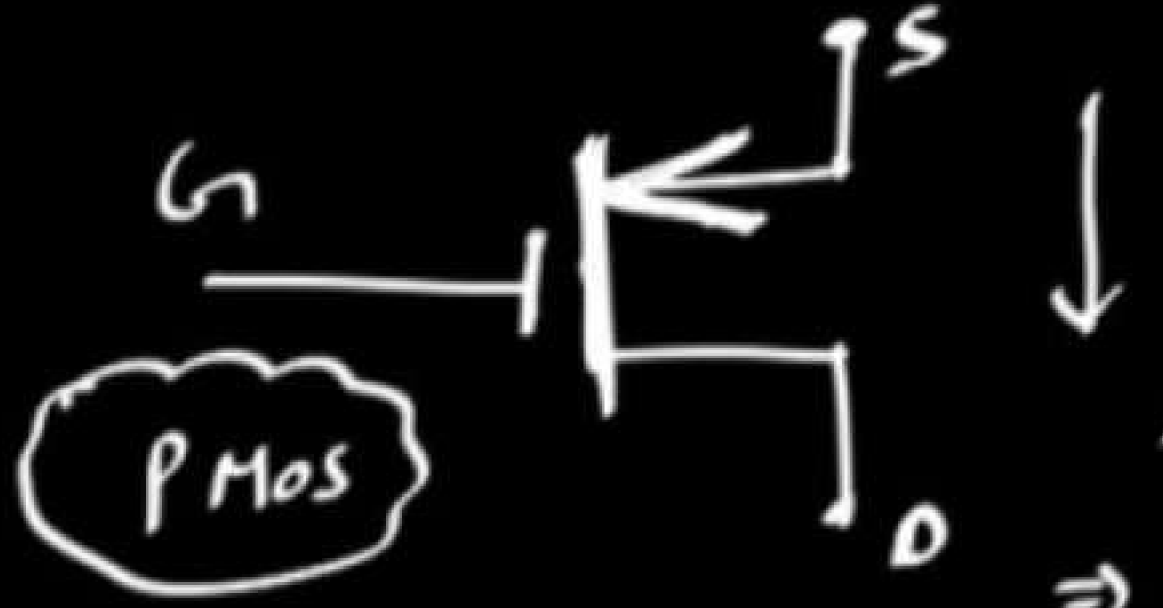
∴ $V_{GS}$ → in NMOS is
$V_{SG}$ → in PMOS.

∴ In NMOS → $V_{Th}$ = (+)ve.
In PMOS → $V_{Th}$ = (−)ve.

∴ In ANALOG

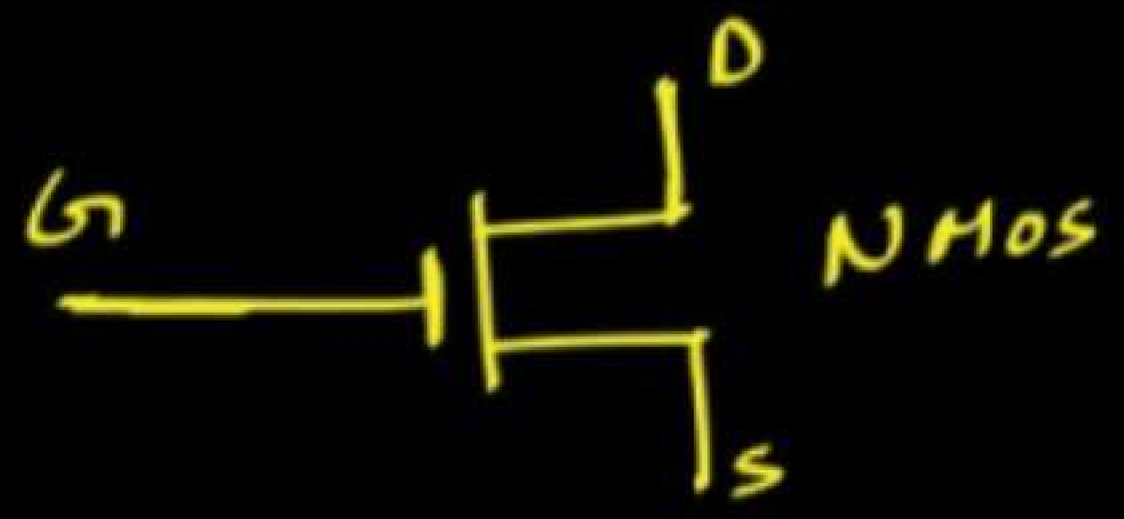


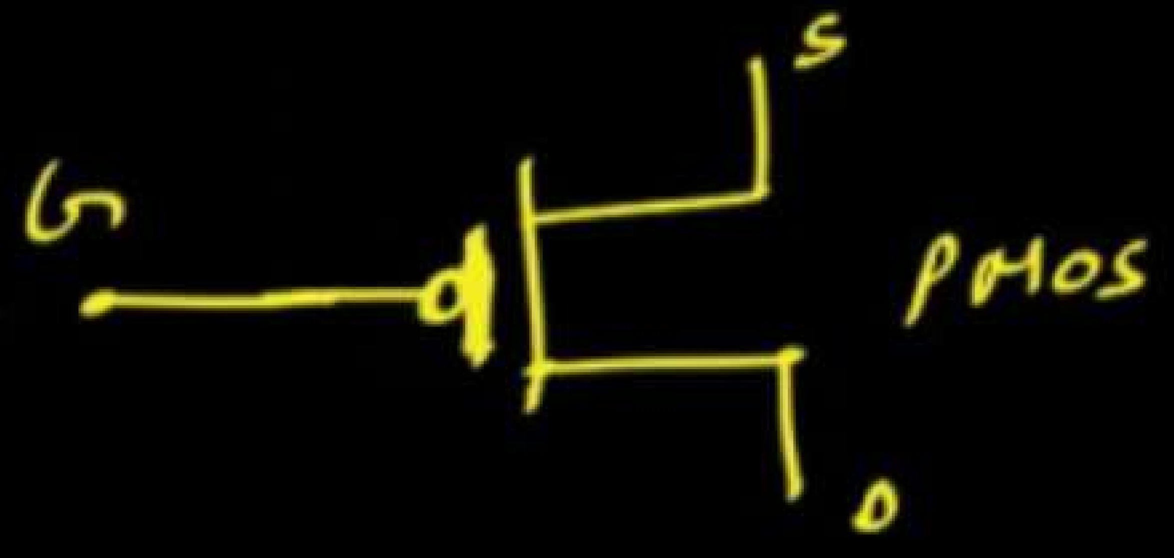

Arrow @ source
→ Conventional
Current direction.




Arrow @
Source
⇒ Current direction.

In Digital



Important NOTE →

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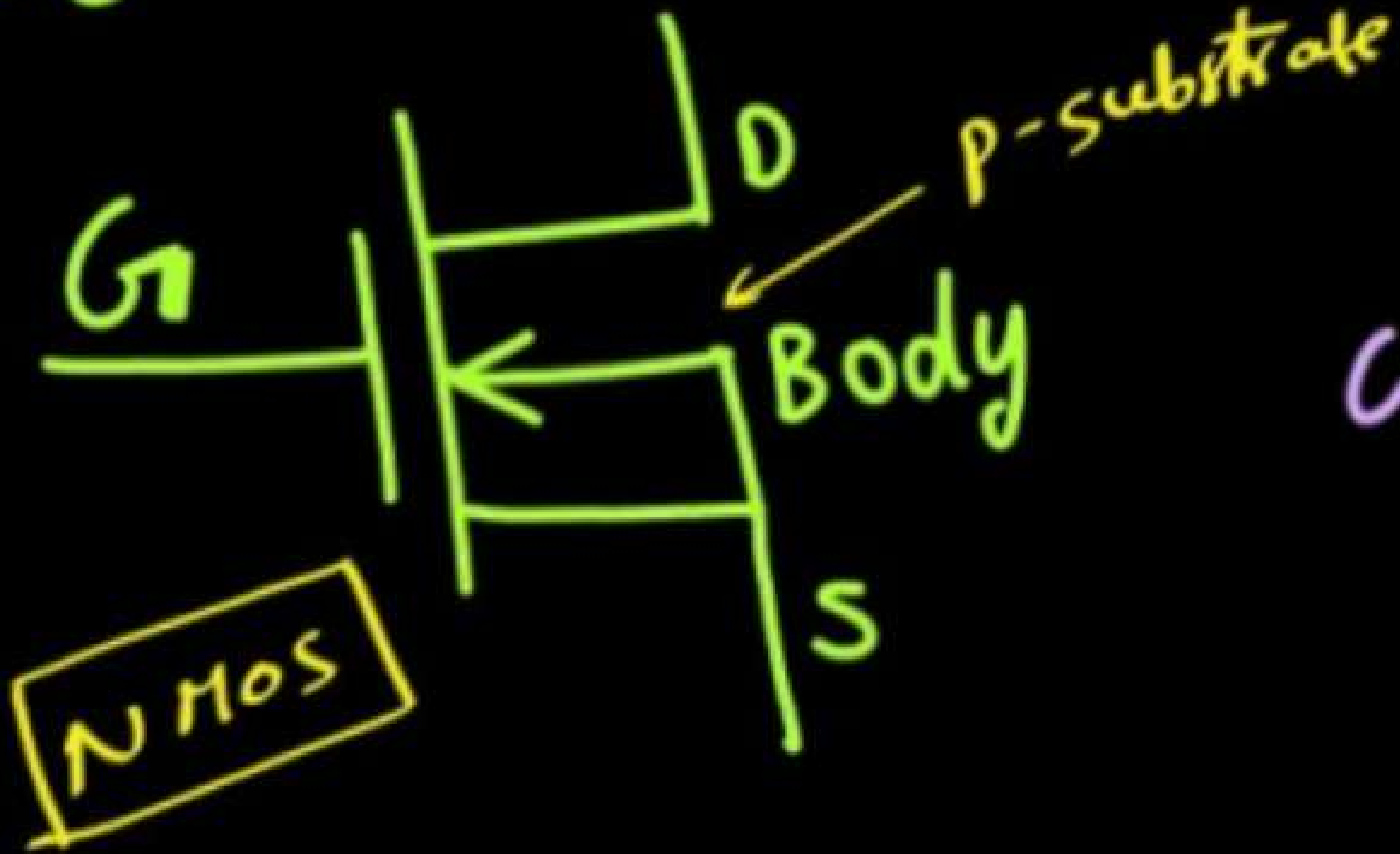
To Avoid Body Effect, we Must Select $V_{SB} = 0$ → can be done by Shorting Source & Body.




where $\gamma$ → Body Effect Parameter.

$$\gamma = \frac{\sqrt{2 q N_A^- \epsilon_{si}}}{C_{ox}'}.$$

Hence,

$$\boxed{V_{Th} = V_{Th_0} + \gamma\left[\sqrt{|V_{BS}|+|2\phi_F|} - \sqrt{|2\phi_F|}\right]}$$

$V_{Th_0} \rightarrow$ without Body Effect

Also, $\dfrac{\partial V_{Th}}{\partial V_{BS}} \rightarrow$ due to change in $V_{BS}$, how much $V_{Th}$ changes.

Sensitivity of Substrate.

## Practical MOS Diode CV characteristics →

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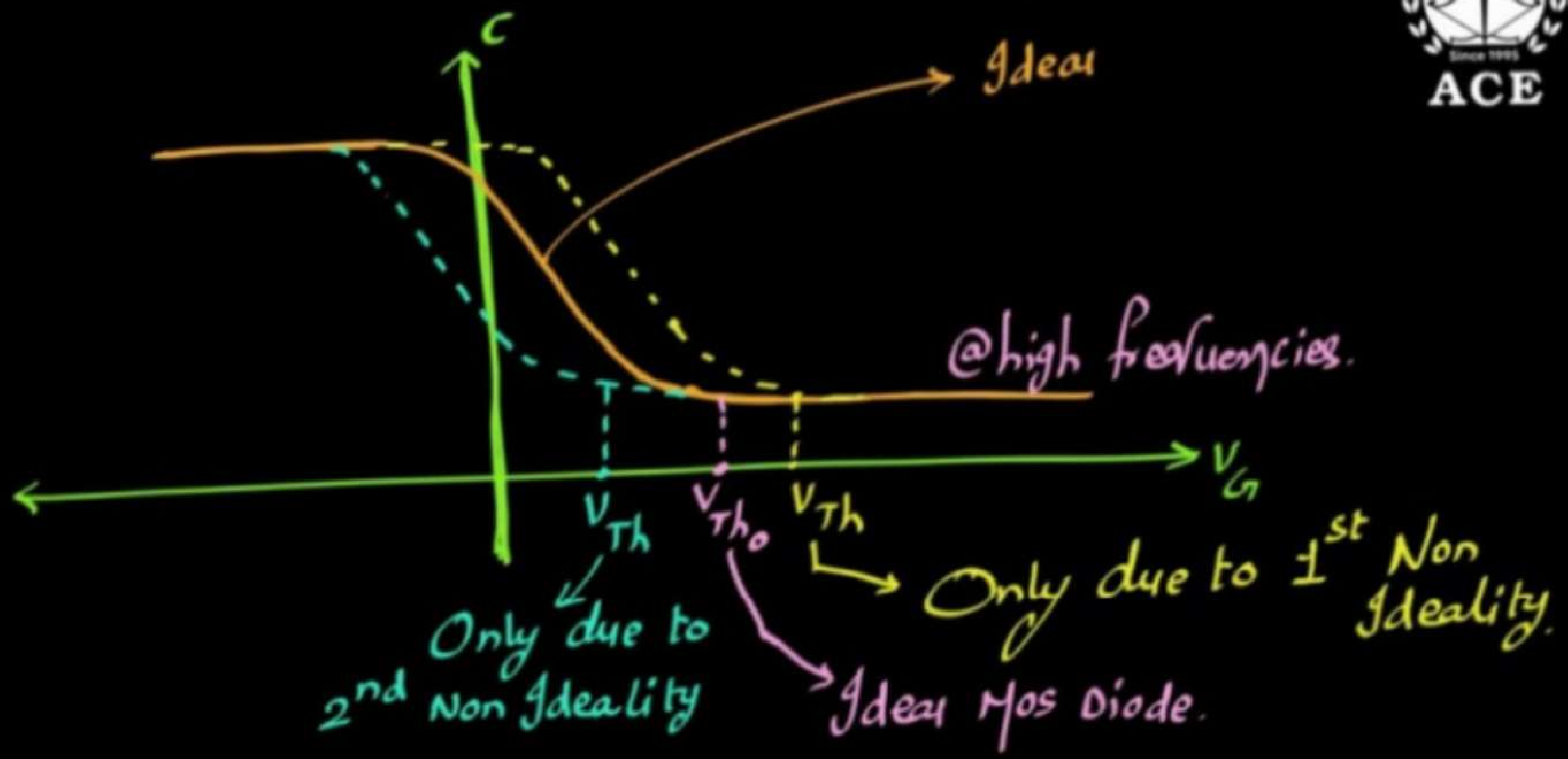
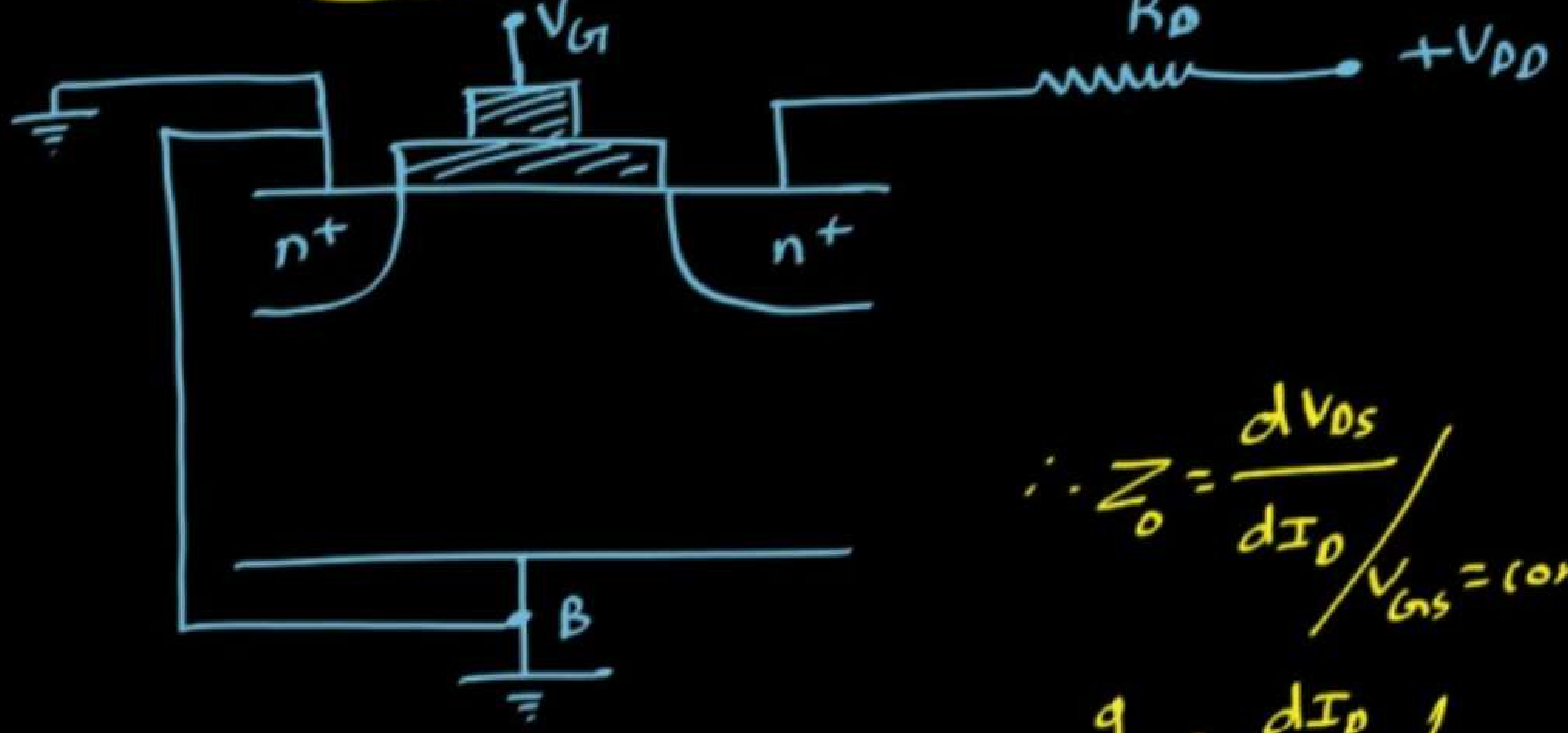
ACE



# MOSFET - VI Characteristics →




$$\therefore Z_o = \left.\frac{dV_{DS}}{dI_D}\right|_{V_{GS} = \text{const.}}$$

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS} = \text{const.}}$$

Since we know,
we need
O/P char., & Transfer char.,

↓ To find $Z_o$.

↓ To find $g_m$.

$$A_V = g_m Z_o.$$

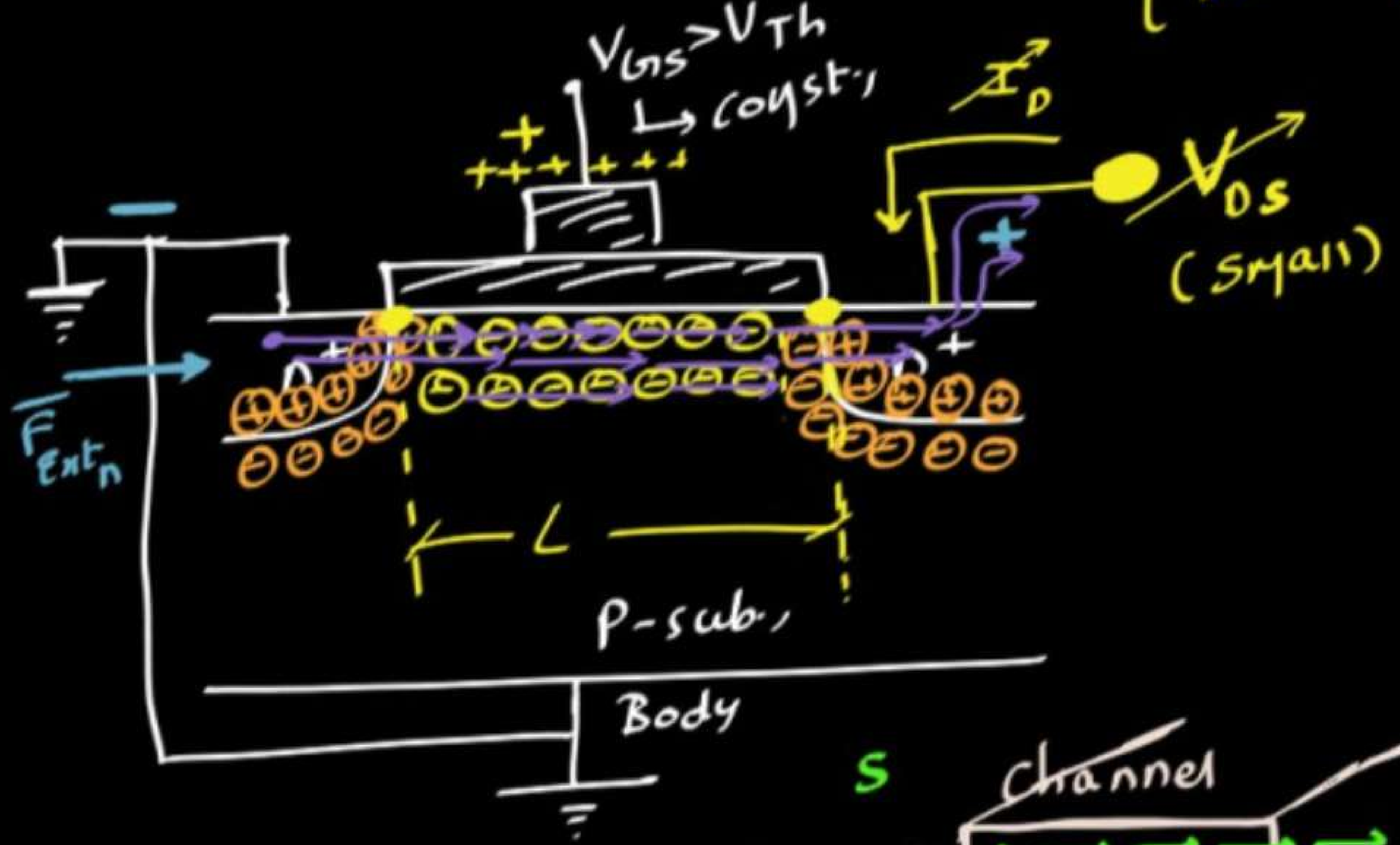
$$A_V = \frac{V_o}{V_i} = \frac{dV_o}{dV_I} = \frac{dV_{DS}}{dV_{GS}}$$

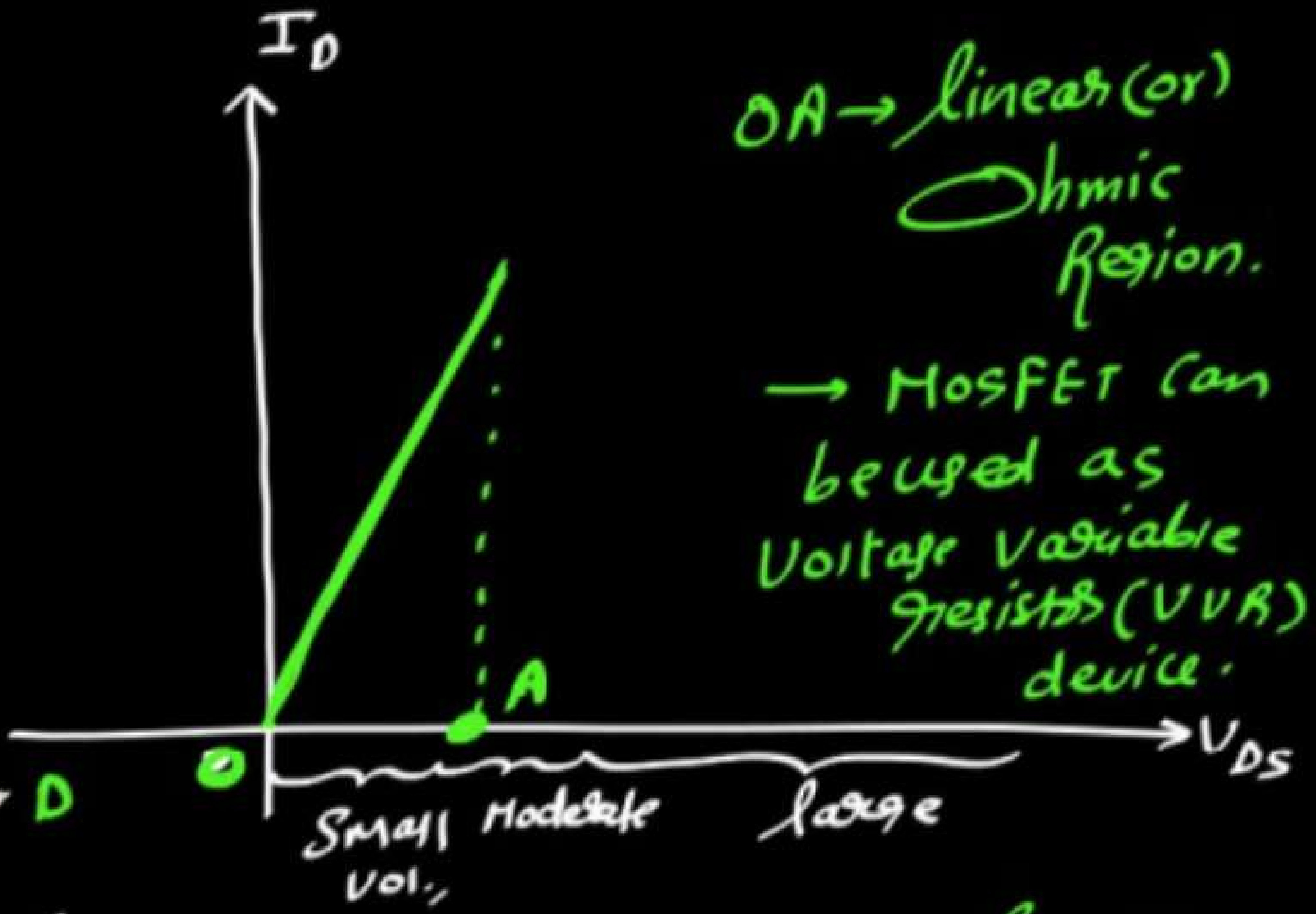
$$= \frac{dV_{DS}}{dI_D} \cdot \frac{dI_D}{dV_{GS}} = Z_o \cdot g_m.$$

O/p char., ⟶ $V_{DS}$ Vs $I_D$ by keeping $V_{GS}$ = const.,

[But $V_{GS} \geq V_{Th}$] ⟶ MOSFET → ON

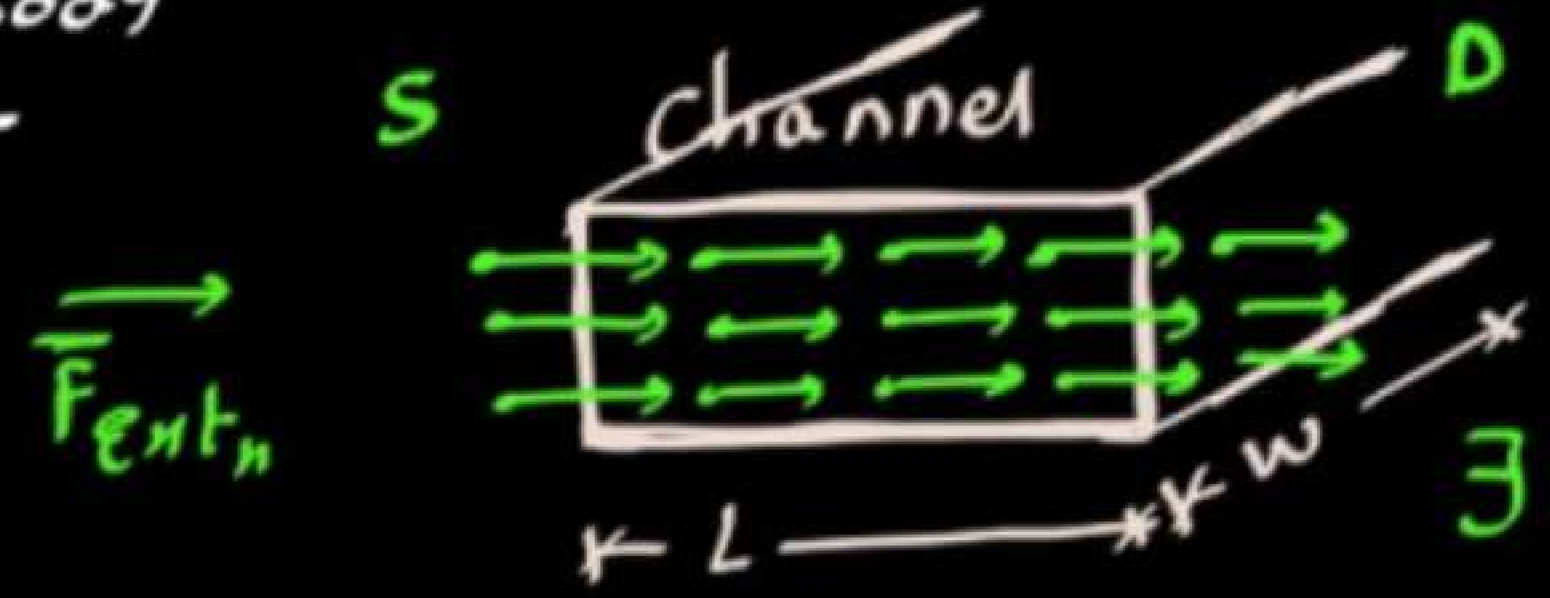
∃ channel.



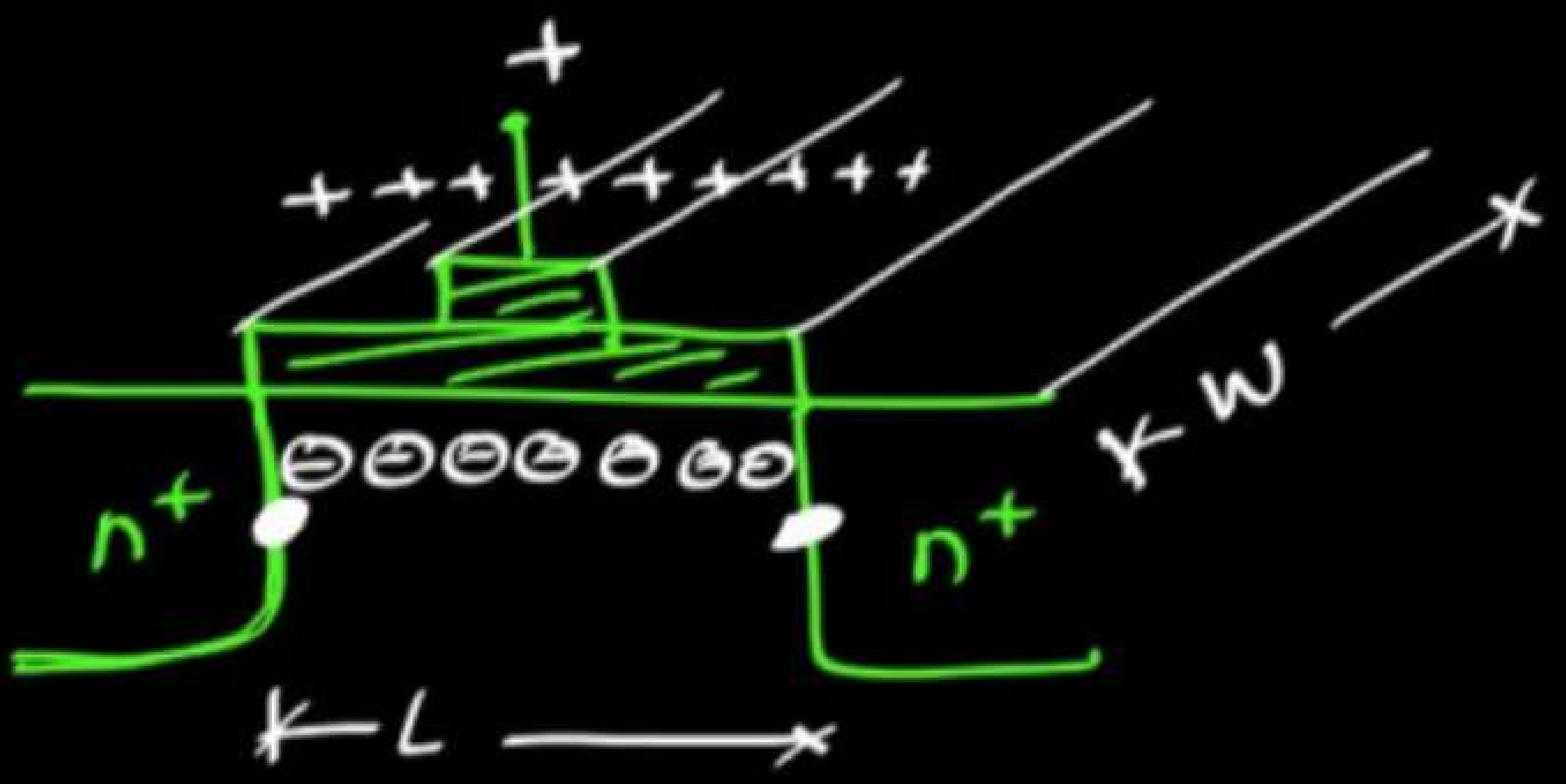




OA → linear (or) Ohmic Region.

→ MOSFET can be used as Voltage variable resistors (VVR) device.




∃ $I_D$. → Electrons are moving from S → D like moving in a conductor.




$V_1 = V_{GS} > V_{Th}$

one Fixed plate (Metal)

-ive charges in channel.

$\rightarrow V_x \leftarrow$

∃ lot of Small capacitances.

@ $V_x \rightarrow$ Let ∃ $dx$ in length 'L'.

As we know,

$$I = \frac{dq}{dt} = \frac{dq}{dx} \cdot \frac{dx}{dt}$$

∃ channel because of $C_{ox}'$ ($F/m^2$)

Also we know $\longrightarrow$

$$q = CV = C_{ox}'[WL][V_1 - V_2]$$
$$= C_{ox}'[WL](V_{GS} - V_{Th} - V_x].$$

$$\therefore \boxed{q = C_{ox}'\,(WL)\,[V_{GS} - V_{Th} - V_x]}.$$

$$\therefore \boxed{\frac{dq}{dx} = \frac{dq}{dL} = C_{ox}' W\,[V_{GS} - V_{Th} - V_x]} \rightarrow (1).$$

Similarly $\rightarrow \frac{dx}{dt} \rightarrow$ Velocity $\rightarrow v_d = \mu_n \bar{E} = \mu_n \cdot \frac{dV_x}{dx}$.

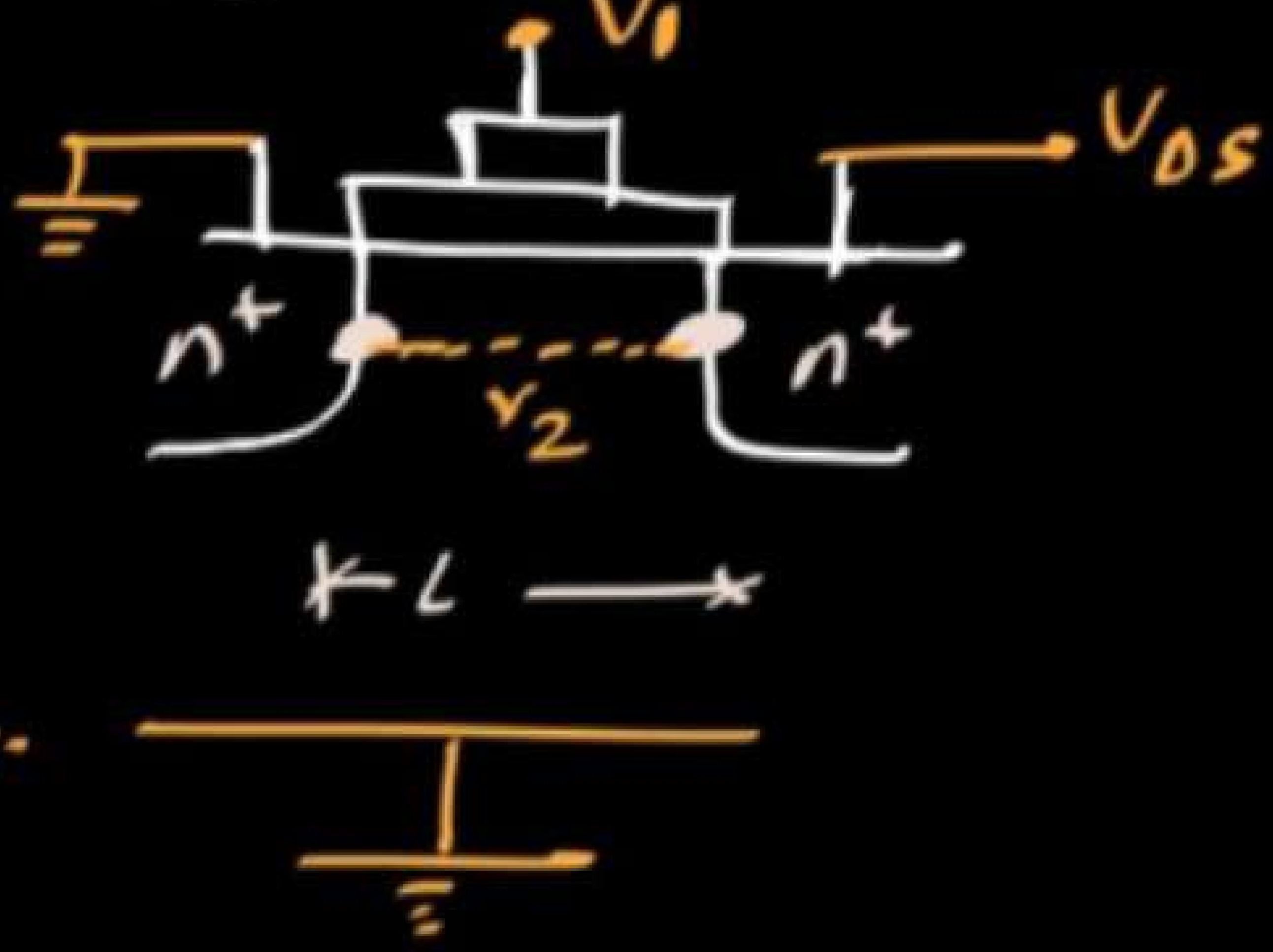
Since As Seen, The Transport is Drift. [No Diff., & No Recombination].

$$\therefore I = \frac{dq}{dx} \cdot \frac{dx}{dt} = C_{ox}' W\,[V_{GS} - V_{Th} - V_x] \cdot \mu_n \frac{dV_x}{dx}.$$

$$As \rightarrow \quad I = C_{ox}' W [V_{GS} - V_{Th} - V_x] \cdot \mu_n \cdot \frac{dV_x}{dx}$$

$$\Rightarrow \quad I \, dx = \mu_n C_{ox}' W [V_{GS} - V_{Th} - V_x] \, dV_x.$$

Integrate over Length $L \longrightarrow$




$$\Rightarrow \quad \int_0^L I \, dx = \int_0^{V_{DS}} \mu_n C_{ox}' W [V_{GS} - V_{Th} - V_x] \, dV_x.$$

$$\therefore \quad I \cdot L = \mu_n C_{ox}' W \left[ (V_{GS} - V_{Th}) V_x - \frac{V_x^2}{2} \right]$$

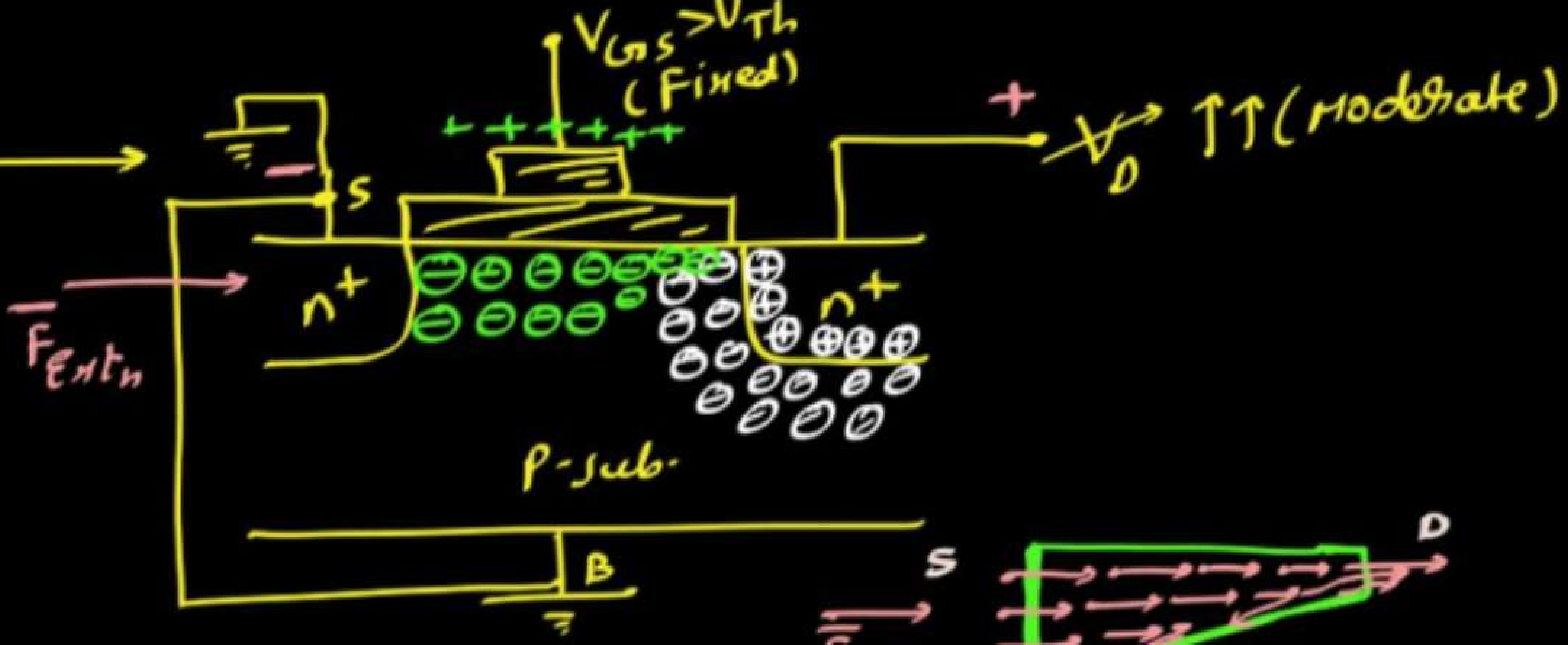
where $V_x = V_{DS}$.

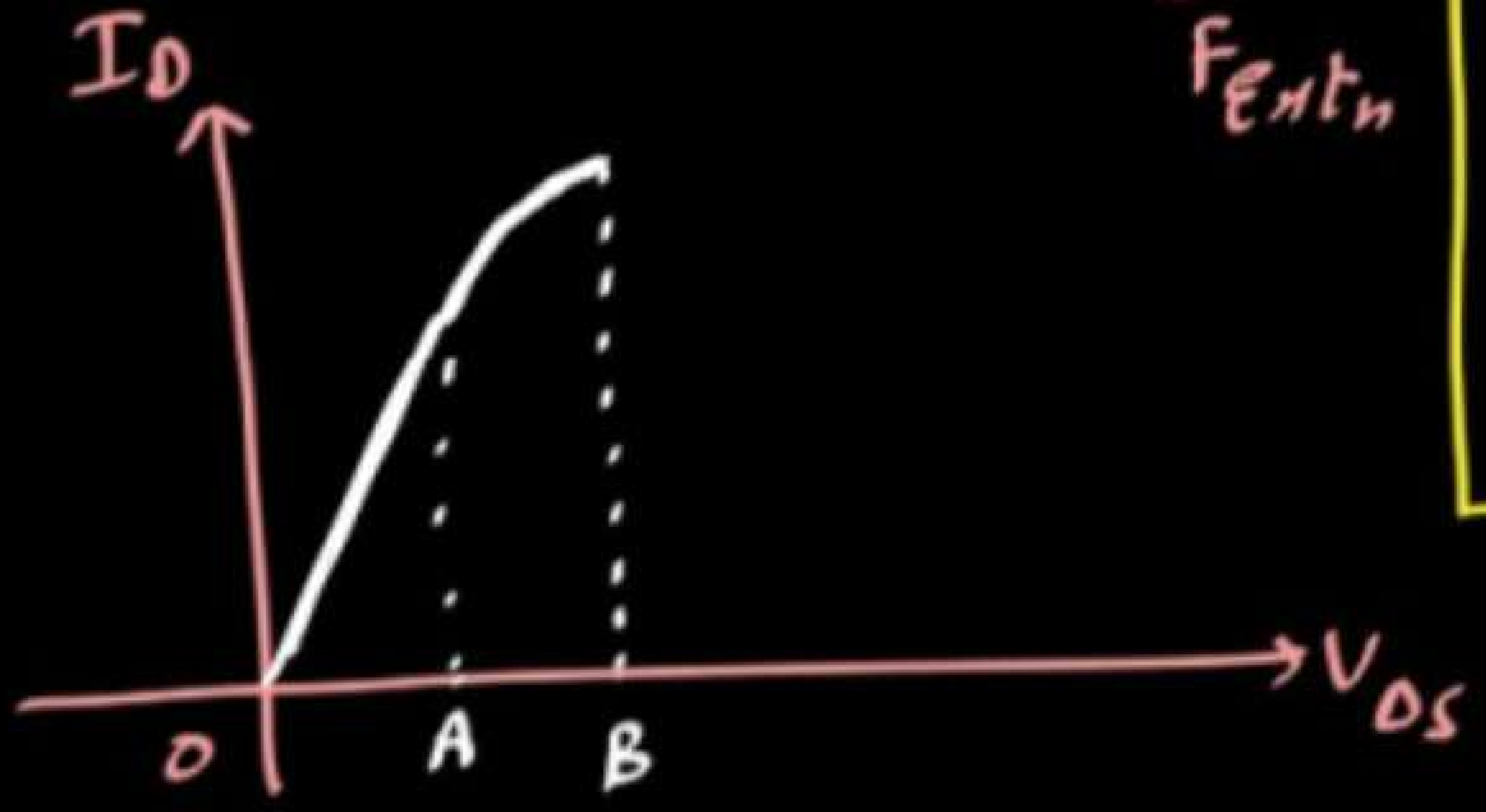
$$\therefore \quad \boxed{I = \mu_n C_{ox}' \frac{W}{L} \left[ (V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right]} \longrightarrow I_{Drain} \text{ in linear region.}$$

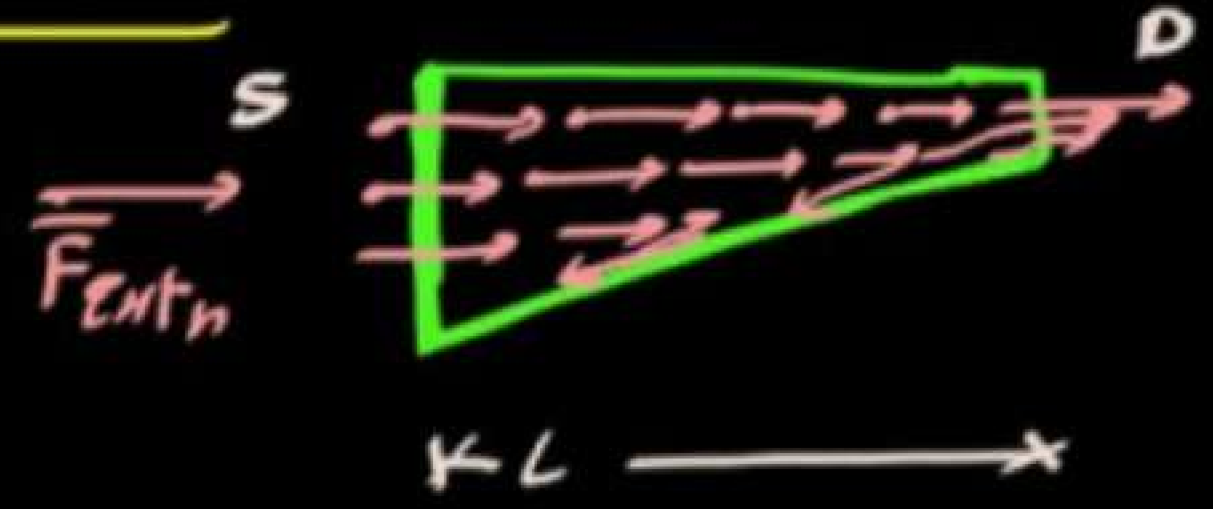
$$I_D = I_S = I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\right].$$

$\longrightarrow$ In Triode Region.

Now Let $V_{DS}$ ↑↑ $\longrightarrow$



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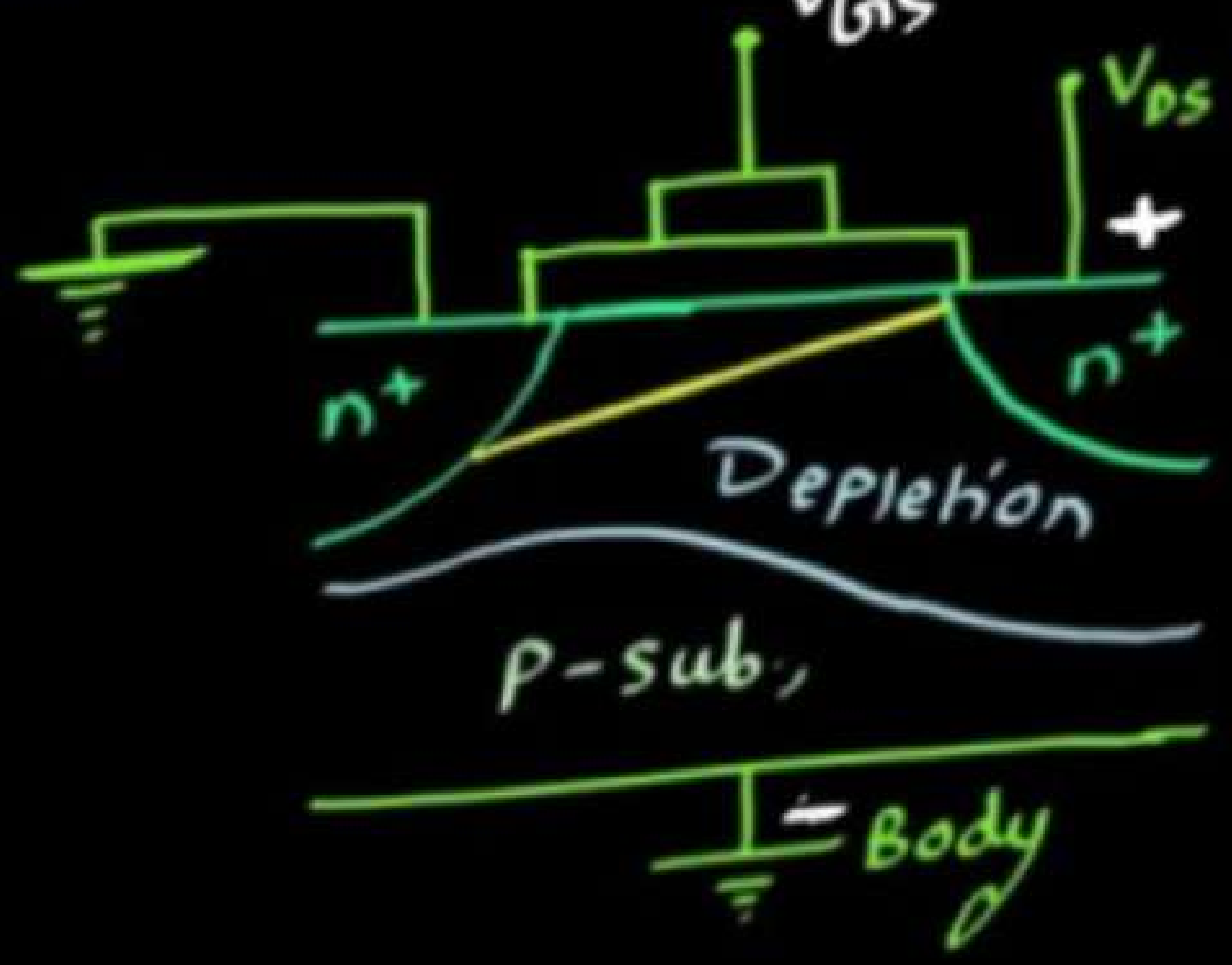
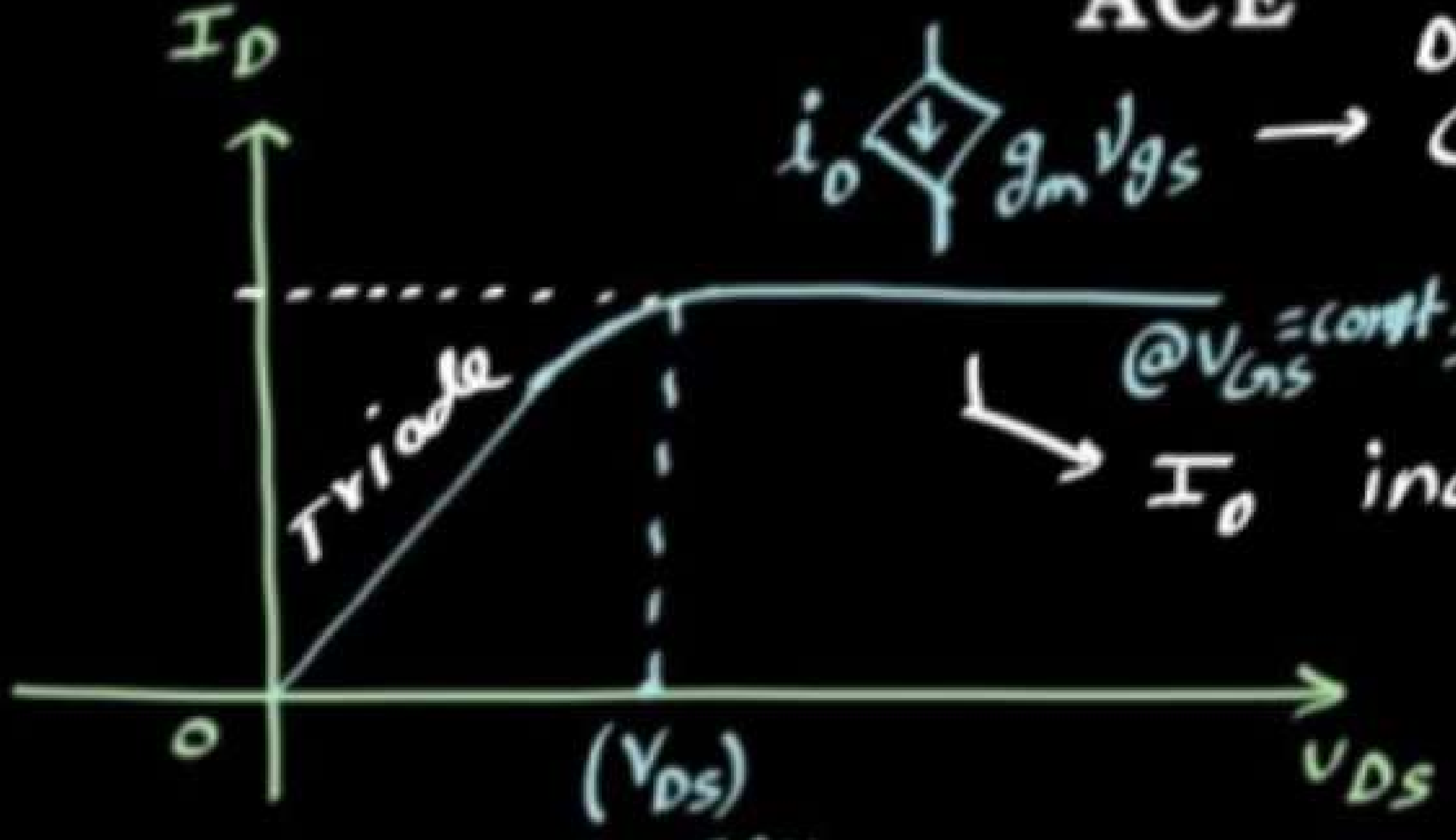
ACE

If $V_{DS}$ further increased, $V_{GS} > V_{Th}$ = const.,




$= (V_{DS})_{pinchoff}$

$i_D$ $g_m v_{gs}$ → Dependent Current source

@ $V_{GS}$ = const., → $I_D$ independent on $V_{DS}$ & depends Only on $V_{GS}$

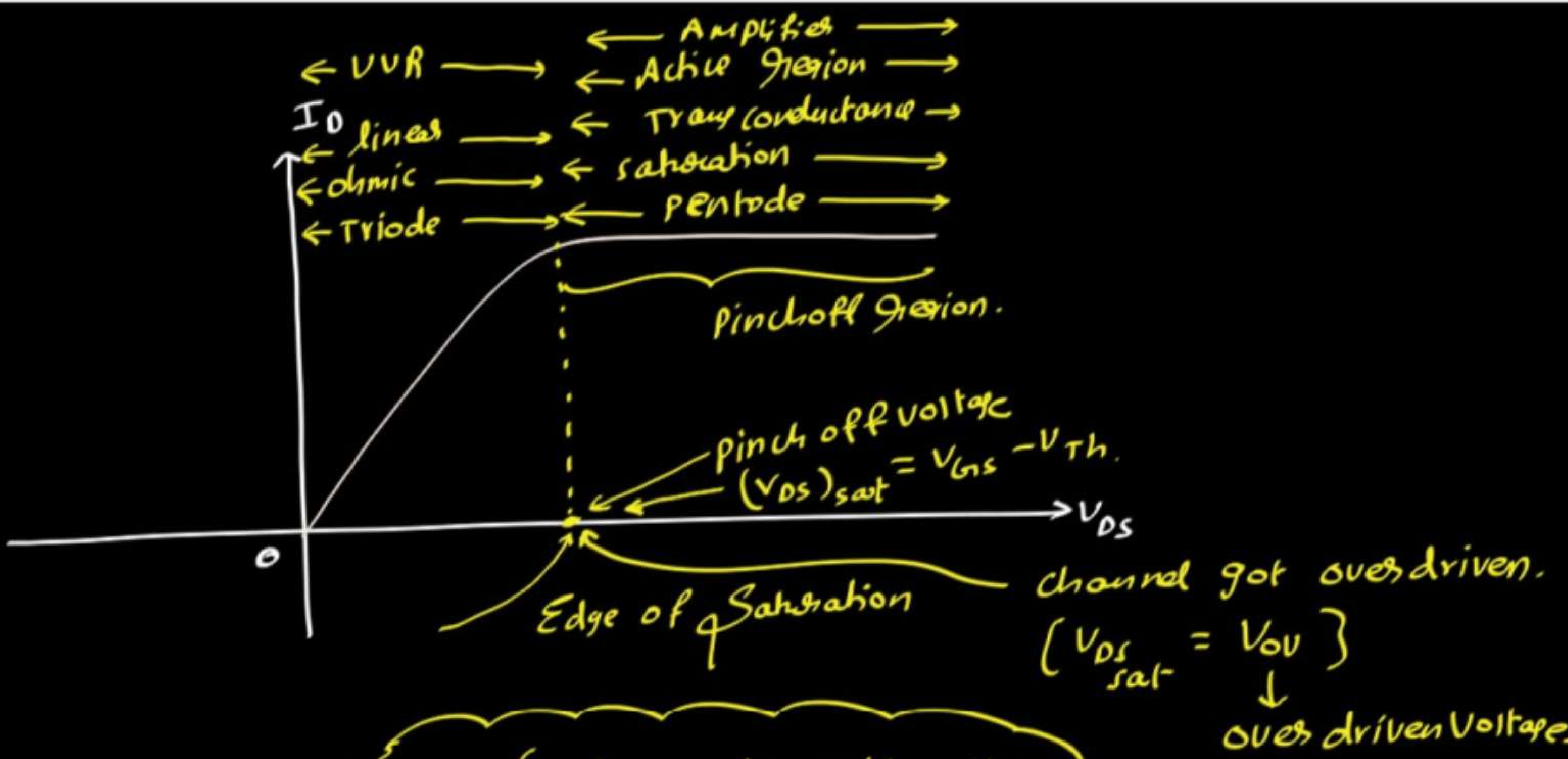
⇒ Trans conductance region.

(Saturation region).

Pentode Region.

Active Region

We can use MOSFET as an Amplifier.




$$\boxed{\therefore \ (V_{DS})_{sat} = V_{OV} = V_{GS} - V_{Th}}$$

$\therefore \quad V_{GS} < V_{Th} \longrightarrow$ MOSFET $\rightarrow$ OFF $\Big\}$ Cutoff.
$I_D = 0$

$V_{GS} > V_{Th} \longrightarrow$ MOSFET $\longrightarrow$ ON
$\longrightarrow \exists I_D$

$V_{DS} < (V_{DS})_{sat}$
$\downarrow$
linear region

$$I_D = \mu_n C_{ox}' \frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$\mu_n C_{ox}' \rightarrow$ Process Trans Conductance Parameter $\rightarrow k$ (or) $k' = A/V^2$.

$V_{DS} > (V_{DS})_{sat}$
$\downarrow$
Saturation region

$$I_D = \frac{1}{2}\mu_n C_{ox}' \frac{W}{L}\left[(V_{GS} - V_{Th})^2\right].$$
$\downarrow$
Square law.

$\therefore$ In Saturation Region,

$$I_D = \frac{1}{2} K_n \frac{W}{L} \{V_{GS} - V_{Th}\}^2.$$

$$\therefore I_D \propto (V_{GS} - V_{Th})^2$$

$\longrightarrow$ Parabolic device.

(Square law device).

Also as $V_{GS} < V_{Th} \rightarrow$ MOSFET is OFF

$\longrightarrow$ Normally OFF device.

$\therefore$ From Above Analysis $\longrightarrow$

$$I_D = \frac{1}{2}\mu_n C_{ox}' \frac{W}{L}\left(V_{GS} - V_{Th}\right)^2$$

$$V_{GS} - V_{Th} = \sqrt{\frac{2 I_D}{\mu_n C_{ox}' \left(\frac{W}{L}\right)}}$$

$$\boxed{g_m = \mu_n C_{ox}' \frac{W}{L}\left(V_{GS} - V_{Th}\right)}$$

$$\therefore \; g_m = \sqrt{2 I_D \mu_n C_{ox}' \left(\frac{W}{L}\right)}.$$

$$\therefore \; \boxed{g_m \propto \sqrt{\frac{W}{L}}}.$$

||ly

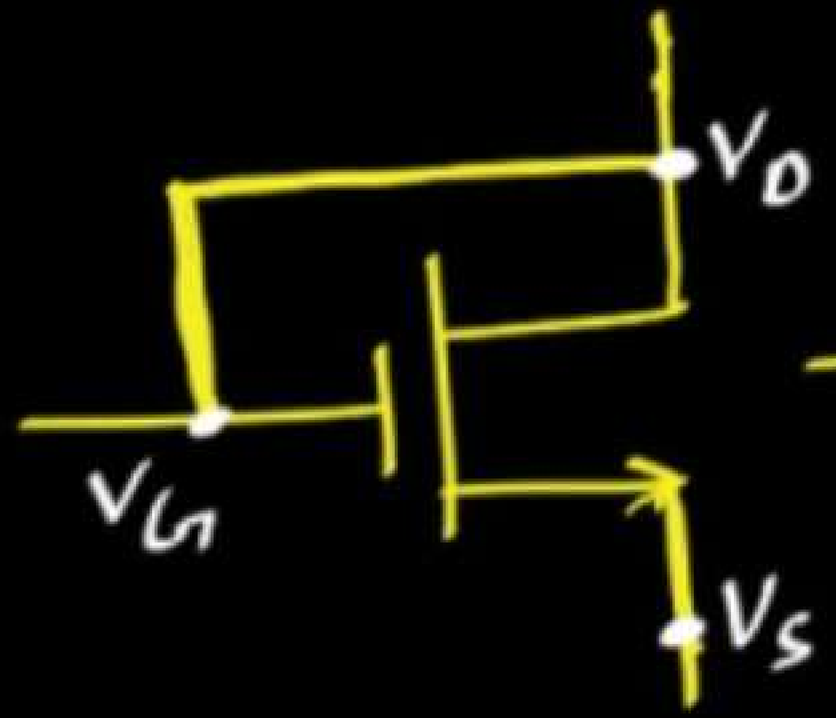
$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{Th}}$$

$$\therefore \; \boxed{g_m = \frac{2 I_D}{V_{GS} - V_{Th}}}.$$

NOTE $\longrightarrow$ (Trick) $\longrightarrow$

1). If $V_{DS} = (V_{DS})_{sat} \longrightarrow$ EOS

2).




$\longrightarrow$ Drain & GATE are Shorted.

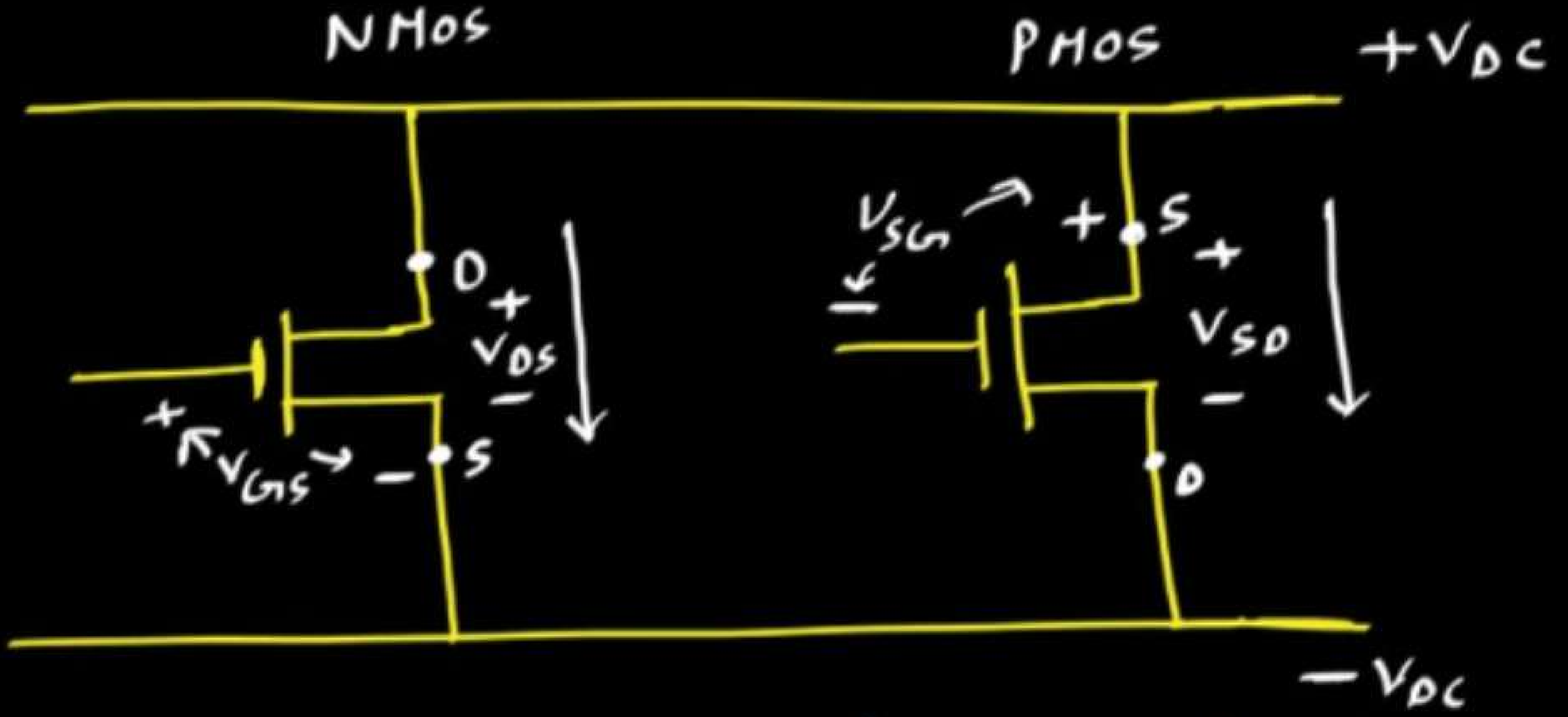
$\Rightarrow V_D = V_G$

$\Rightarrow V_{DS} = V_{GS}$

As for NMOS $V_{Th} \longrightarrow$ Must to be (+)ve for currents.

$\therefore\ V_{DS} \overset{\text{Always}}{>} (V_{GS} - V_{Th}) \Rightarrow$ Q-point Always be in Saturation.

3).




If $V_{GS} > V_{Th} \longrightarrow$ MOSFET ON

If $V_{DS} < (V_{GS} - V_{Th}) \rightarrow$ linear

$$I_D = \mu_n C_{ox}' \frac{W}{L}\left((V_{GS} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right)$$

If $V_{SG} > |V_{Th}| \longrightarrow$ MOSFET $\rightarrow$ ON

If $V_{SG} < (V_{SG} - |V_{Th}|) \longrightarrow$ linear

$$I_D = \mu_p C_{ox}' \frac{W}{L}\left((V_{SG} - |V_{Th}|)V_{SD} - \frac{1}{2}V_{SD}^2\right).$$

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In SAT., (or) Pentode (or) Active region, $I_D$ depends Only on $V_{GS}$ & independent on $V_{DS}$.

$$(V_{DS})_{sat} = V_{OV} = V_{GS} - V_{Th}$$

If $(V_{DS})_Q = (V_{DS})_{sat} \longrightarrow$ EOS [Edge of Saturation].

If $V_{GS} \geq V_{Th}$
MOSFET $\rightarrow$ ON

$\rightarrow (V_{DS})_Q > (V_{DS})_{SAT.} \Rightarrow (V_{DS})_Q > (V_{GS} - V_{Th})$
$\Rightarrow$ Saturation region (or) Pentode.

$\rightarrow (V_{DS})_Q < (V_{DS})_{SAT.} \Rightarrow (V_{DS})_Q < (V_{GS} - V_{Th})$
$\Rightarrow$ linear (Triode) region.

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In linear,

$$I_D = \mu_n C_{ox}' \frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right].$$

$\mu_n C_{ox}' \longrightarrow A/V^2 \longrightarrow$ Process Trans Conductance Parameter.

$\hookrightarrow K'$ (or) $K_n'$.

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ACE

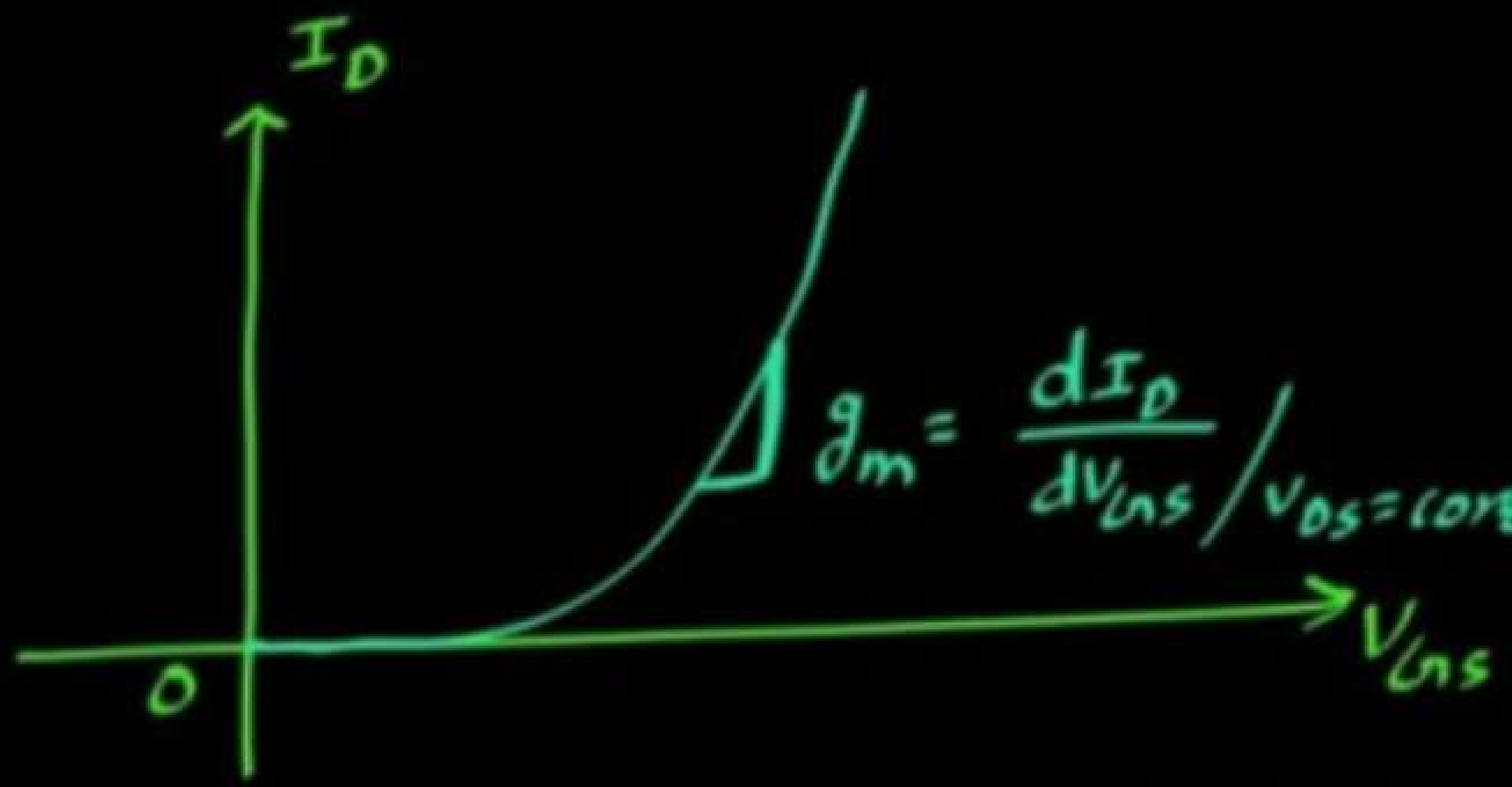
In Saturation Region $\longrightarrow$

$$I_D = \frac{1}{2}\mu_n C_{ox}' \frac{W}{L}\left[V_{GS} - V_{Th}\right]^2.$$

$$= \frac{1}{2} K_n' \frac{W}{L}\left[V_{GS} - V_T\right]^2$$

$$= K_n \left[V_{GS} - V_T\right]^2$$

$$\frac{1}{2} K_n' \frac{W}{L} \longrightarrow K_n \text{ (or) } K \text{ (or) } \beta_n.$$




$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS}=\text{const.}}$$

Transfer char.

Parabolic (or) Square law Device.

For N-MOS →

$V_{Th} = (+)ve$

$V_{GS} \geq V_{Th} \rightarrow$ To ON

$$\left.\begin{array}{l} V_{GS} \geq V_{Th} \\ \& \; V_{DS} \geq (V_{GS} - V_{Th}) \end{array}\right\} \rightarrow \text{Saturation.}$$

$$\left.\begin{array}{l} V_{GS} \geq V_{Th} \\ V_{DS} \leq (V_{GS} - V_{Th}) \end{array}\right\} \rightarrow \text{Linear.}$$

For PMOS → $V_{Th} = (-)ve.$

$V_{SG} \geq |V_{Th}| \rightarrow$ To ON.

$$\left.\begin{array}{l} V_{SG} \geq |V_{Th}| \\ V_{SD} \geq (V_{SG} - |V_{Th}|) \end{array}\right\} \rightarrow \text{Saturation}$$

$$\left.\begin{array}{l} V_{SG} \geq |V_{Th}| \\ V_{SD} \leq (V_{SG} - |V_{Th}|) \end{array}\right\} \rightarrow \text{Linear.}$$

In Linear,

$$I_D = \mu_p C_{ox} \frac{W}{L} \left[ (V_{SG} - |V_{Th}|) V_{SD} - \frac{1}{2} V_{SD}^2 \right].$$

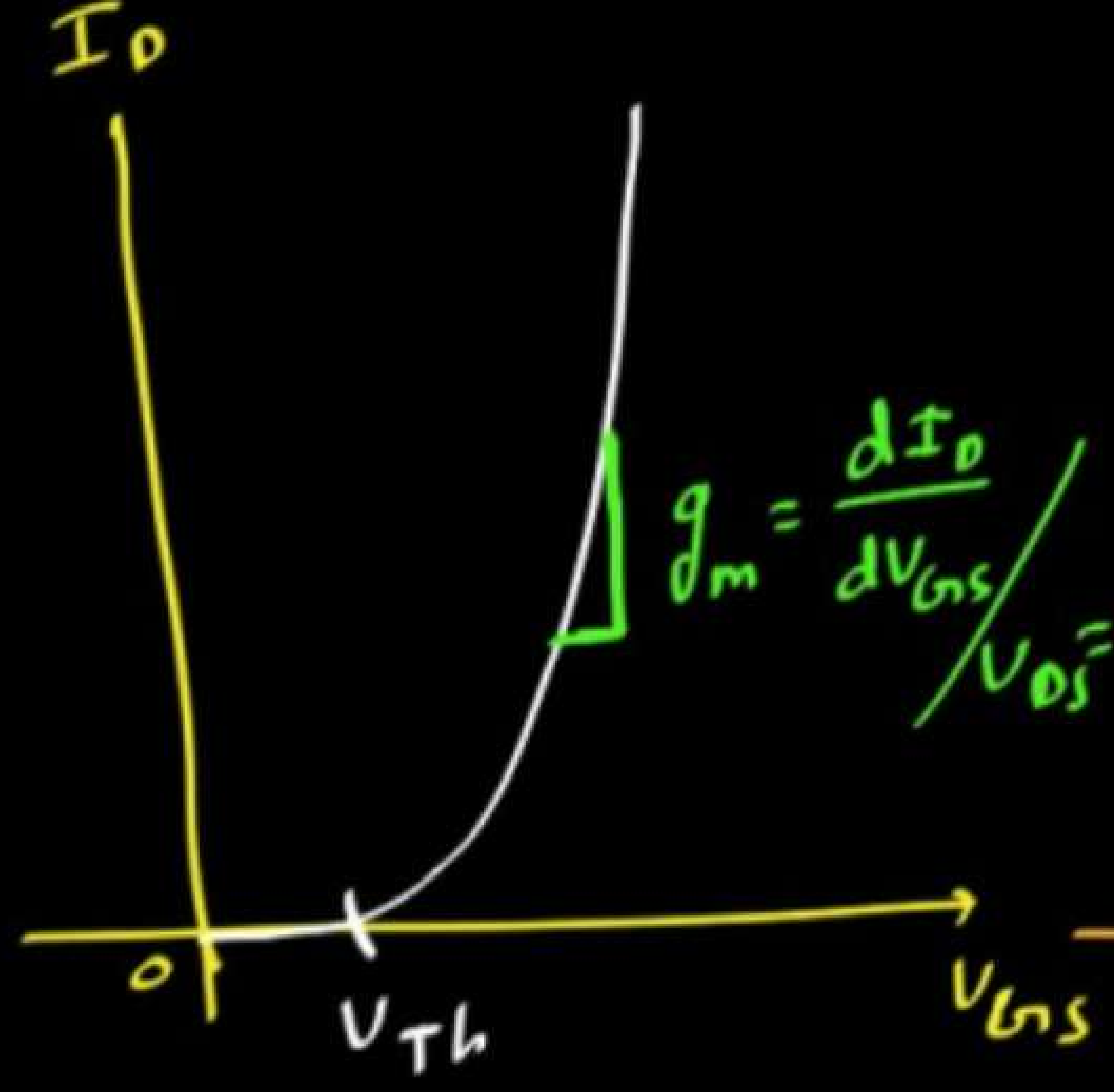
In Saturation,

$$I_D = \frac{\mu_p C_{ox} \frac{W}{L}}{2} \left( V_{SG} - |V_{Th}| \right)^2.$$

If $V_{DS} <<< (V_{GS} - V_{Th}) \longrightarrow$ Deep Triode.

$$I_D = \mu_n C_{ox} \frac{W}{L} \left( (V_{GS} - V_{Th}) V_{DS} \right).$$

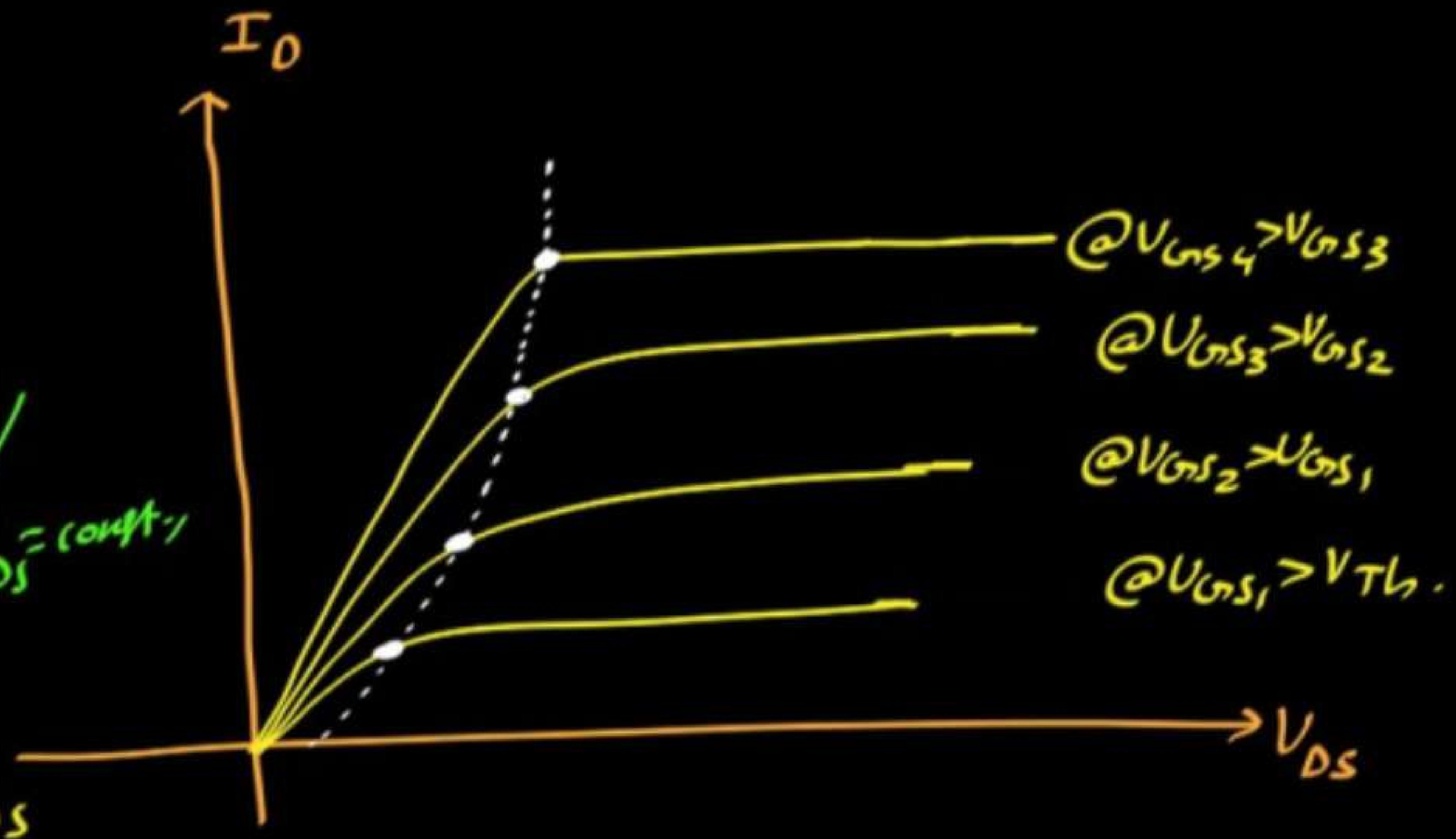
Let NMOS →




$$g_m = \frac{dI_D}{dV_{GS}}\Bigg/_{V_{DS} = \text{const.}}$$

↓

Transfer char.



# Observations →

1). 

| BJT | | MOSFET |
|---|---|---|
| B | ⟷ | G |
| E | ⟷ | S |
| C | ⟷ | D |

2). 

| BJT | | MOSFET |
|---|---|---|
| CB | ⟷ | CG |
| CE | ⟷ | CS |
| CC | ⟷ | CD |

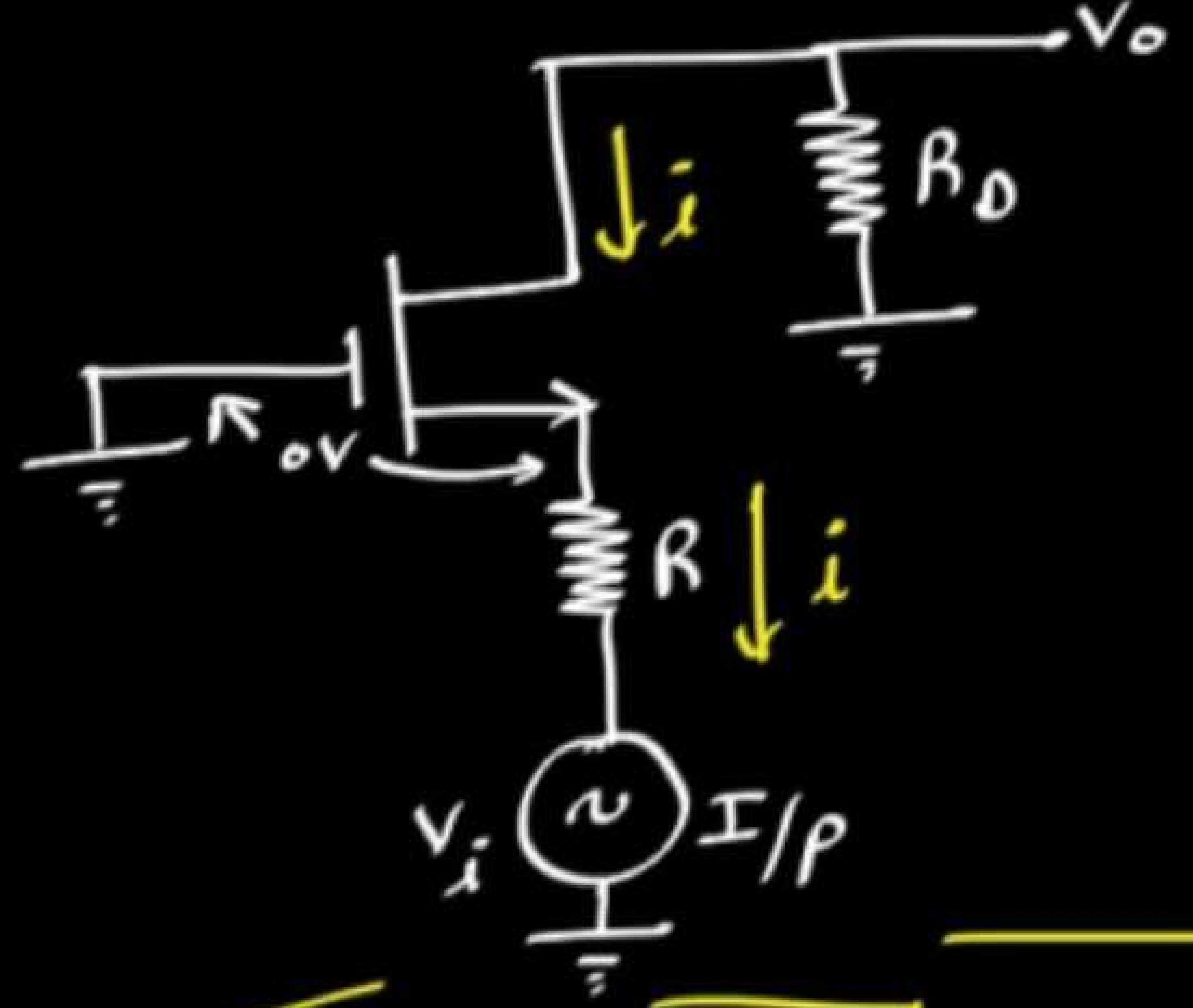
3). BJT →

| | I/P | Common | O/P |
|---|---|---|---|
| CB | E | B | C |
| CE | B | E | C |
| CC | B | C | E |

MOSFET →

| | I/P | Common | O/P |
|---|---|---|---|
| CG | S | G | D |
| CS | G | S | D |
| CD | G | D | S |

(4). I/p → S } C. GATE ⇒ I/p I = $I_S$ } I/pI = O/pI
o/p → D } o/p I → $I_D$ } Current buffer.




$V_o = -iR_D$

$V_i = -i(R) + 0 = -iR$.

$\therefore A_V = \dfrac{V_o}{V_i} = \dfrac{R_D}{R}$.

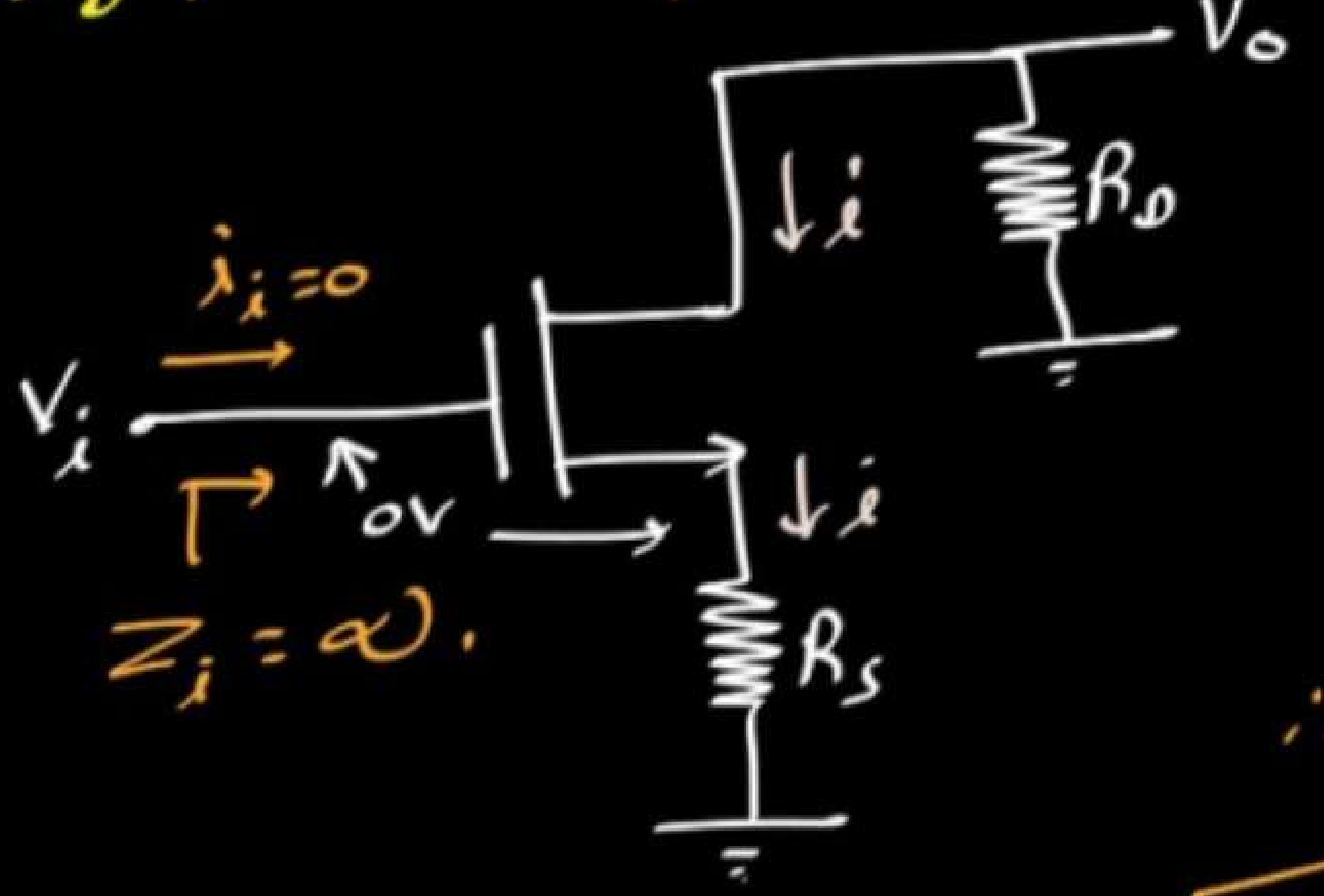
By selecting $R_D$ & R,
we can use it as a
Vol. Amp.

Current buffer.

Voltage Amplifier.

Phase buffer.
$\angle V_o, V_i = 0°$.

I/P → G
O/P → D } Common Source.




$$V_i = 0 + iR_S.$$

$$V_o = -iR_D.$$

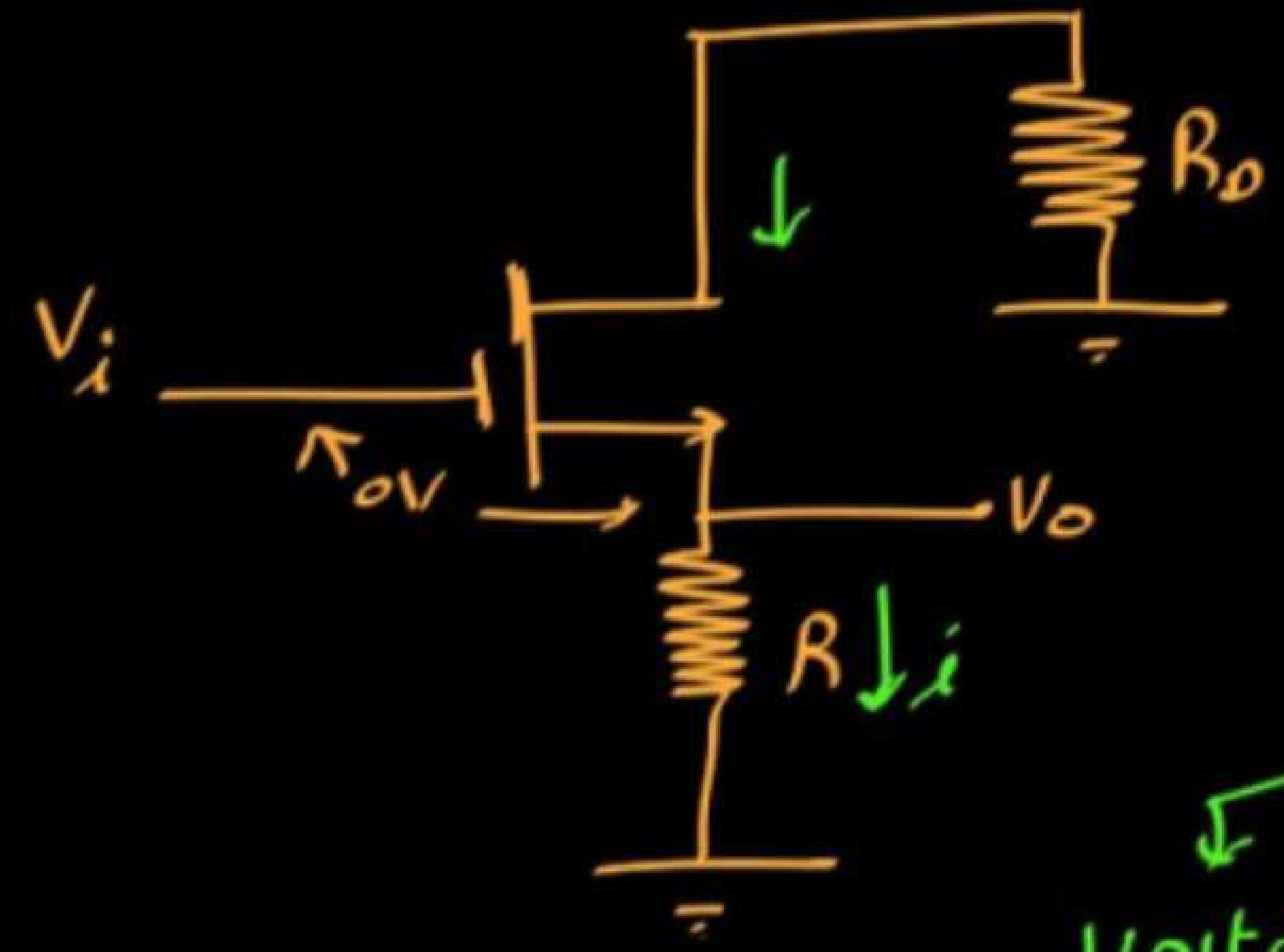
$$\therefore A_V = \frac{V_o}{V_i} \longrightarrow \frac{-R_D}{R_S}$$

Voltage Amplifier.

Phase Shifter.

I/P $\longrightarrow$ G
O/P $\longrightarrow$ S } Common Drain.

$(I_D = I_s)$.




$V_i = 0 + iR.$

$V_o = iR.$

$$\boxed{A_v = 1}$$

Voltage buffer.

Phase buffer.

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ACE

Similarly for MOSFET

Practically, If $V_{DS}\uparrow\uparrow$, channel length is getting Modulated due to huge depletion force at Drain Junction R.Bias & hence,


@ Some $V_{DS_x} = V_{ov} + \Delta V$.

$\Delta L \longrightarrow$ Pinched off & $\Delta V$ is dropped here.

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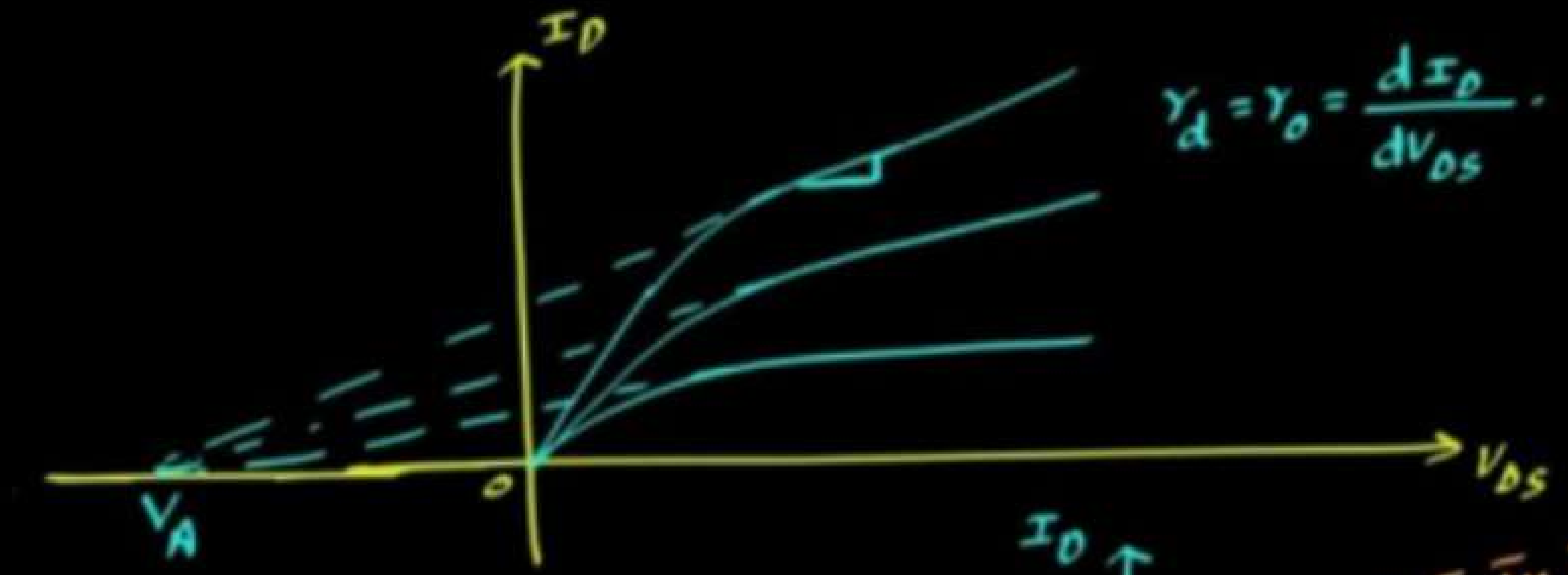
Now $L \longrightarrow$ Modified to $L'$.

$\Rightarrow$ Electrons Crossing $L'$ & when Enters in $\Delta L$ Region, they Accelerate with high Velocity due to large $V_{DS}$.

$\Rightarrow$ As $L \longrightarrow$ Changed due to $V_{DS}$ $\Rightarrow$ Channel length Modulation.

$\therefore$ $\lambda = \frac{1}{V_A}$ $\rightarrow$ Channel length Modulation Parameter.

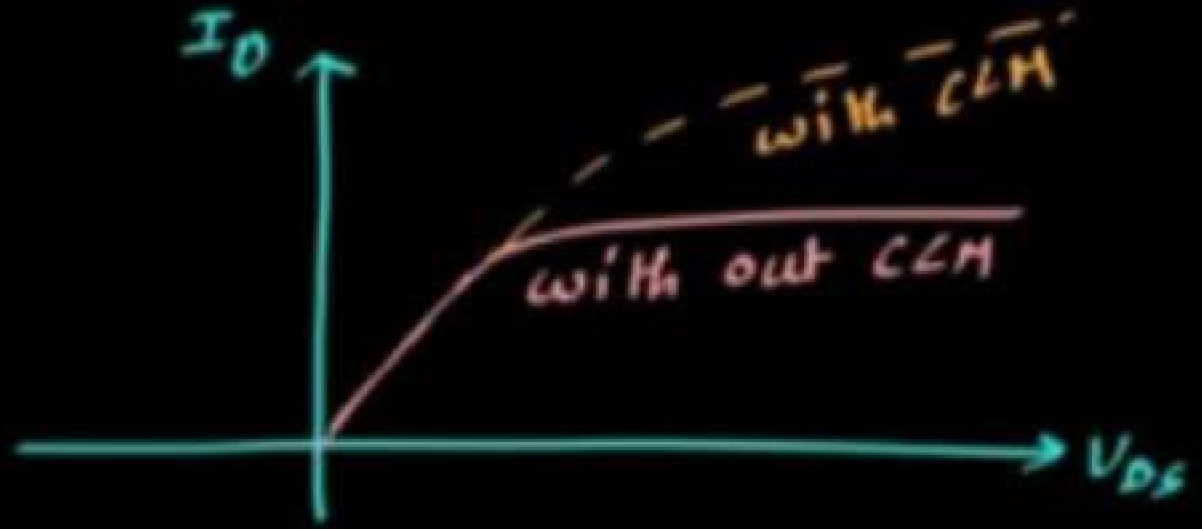



$$r_d = r_o = \frac{dI_D}{dV_{DS}}.$$

Ideally $V_A = \infty$

$\Rightarrow r_o = \infty.$

$\Rightarrow r_d = \infty.$



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with out CLM $\rightarrow$

$$I_D = \frac{1}{2}\mu_n C'_{ox}\frac{W}{L}(V_{GS}-V_{Th}).$$

with CLM $\longrightarrow$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{Th})^2(1+\lambda V_{DS}).$$

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ACE

$$L' = L - \Delta L = L\left[1 - \frac{\Delta L}{L}\right]$$

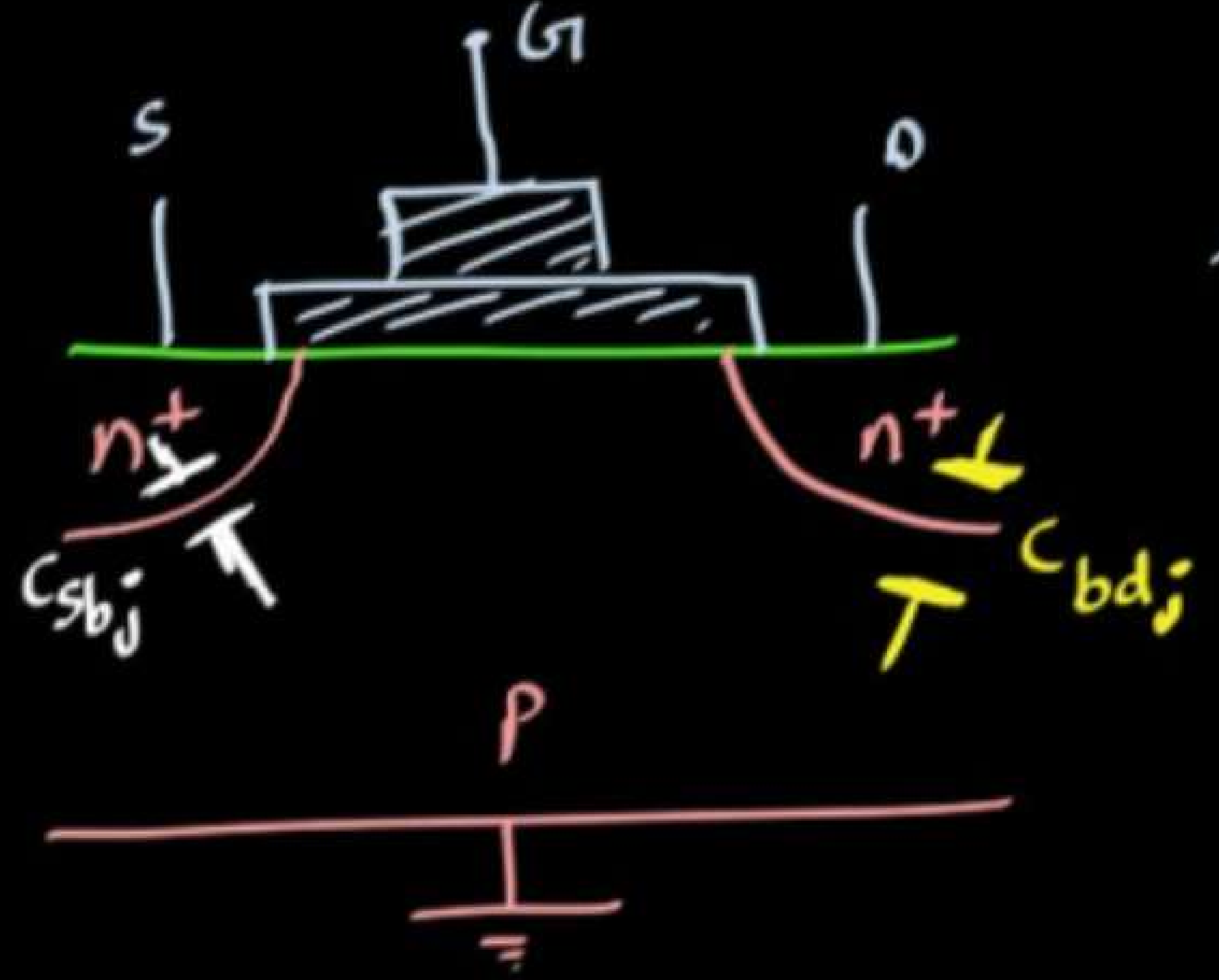
As $\frac{\Delta L}{L} \propto V_{DS} \Rightarrow \frac{\Delta L}{L} = \lambda V_{DS}$

$$\Rightarrow \lambda = \frac{\Delta L}{L} \cdot \frac{1}{V_{DS}} = \frac{1}{V_A}$$

$$\Rightarrow \boxed{L' = L[1 - \lambda V_{DS}]}$$

**

**Note** →




① → $\exists$ Source to Body Junction Capacitance.

$\exists$ Drain to Body Junction Capacitance.

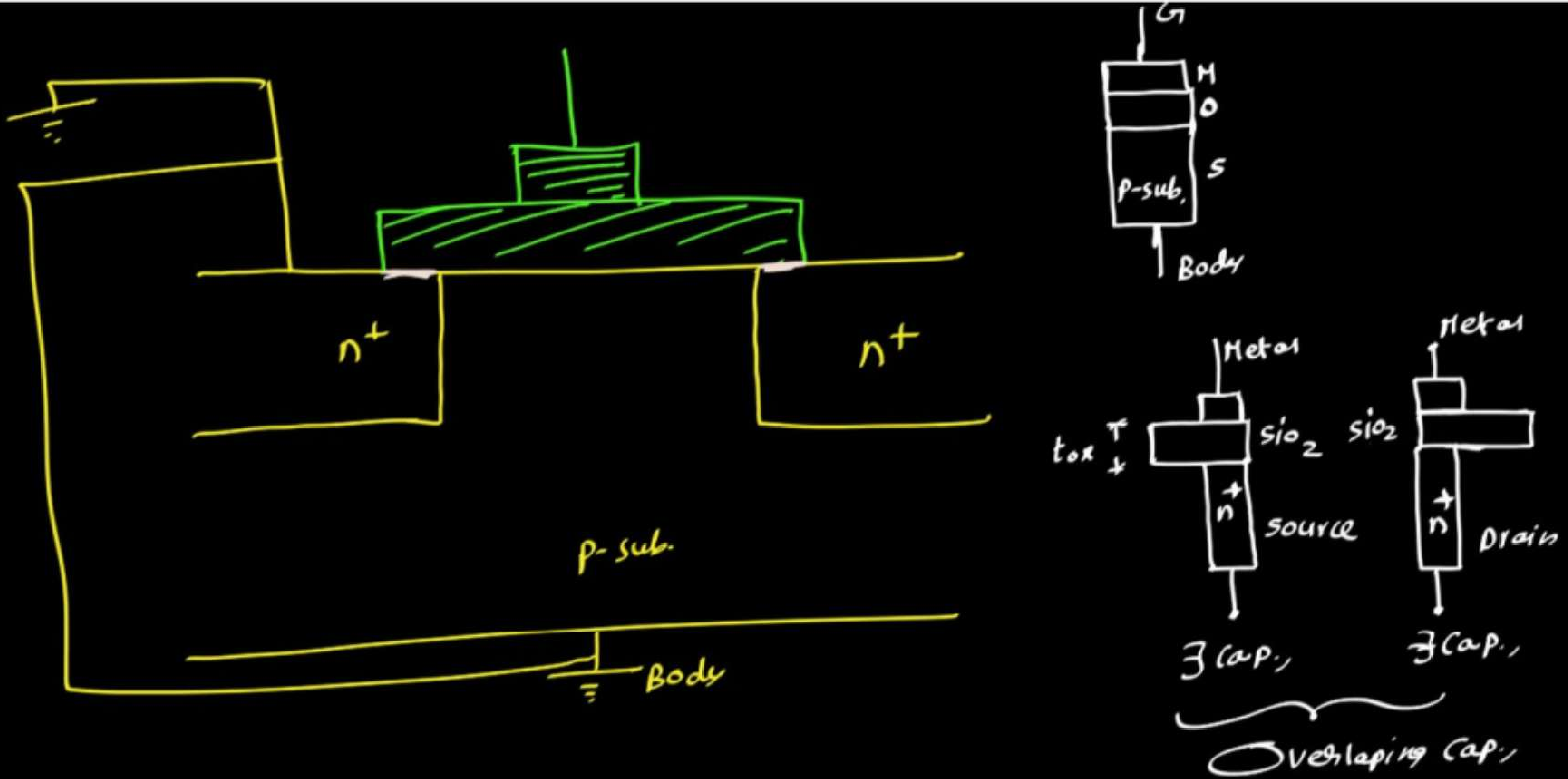
$\exists$ MOS Cap. (Metal to Body)

But As some portion of $SiO_2$ is overlaped in to Source & Drain

→ $\exists$ capacitance

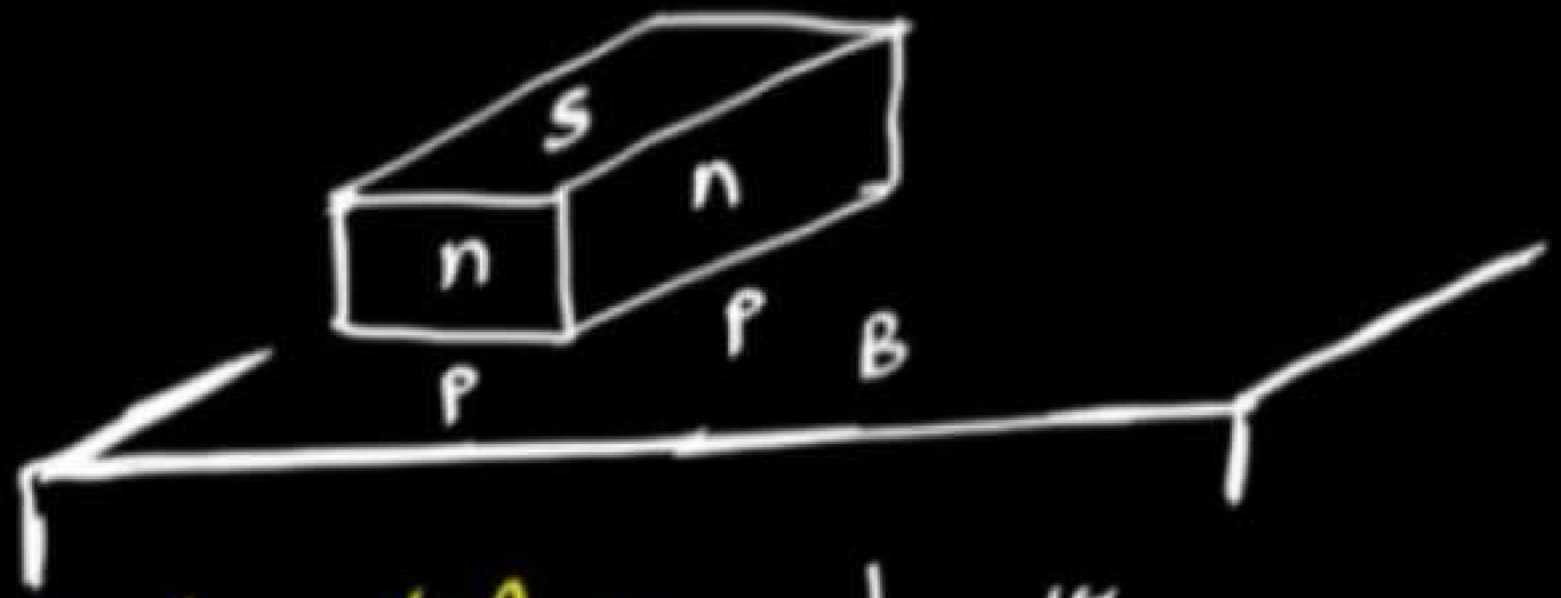
$\Rightarrow$ one plate is Metal, other plate Source
One plate is Metal, other plate Drain } Dielectric is $SiO_2$.

→ Overlapping Capacitance.



n+
n+
p-sub.
Body
G
M
O
S
p-sub.
Body
Metal
Metal
tox
SiO2
SiO2
n+
n+
Source
Drain
∃ Cap.
∃ Cap.
Overlaping Cap.

$\longrightarrow \quad C_{SB_j} = \dfrac{\epsilon_0 (\epsilon_r)_{si}}{\omega_{dep}} \times \text{Area}$




where $A = A_{front} + A_{Back} + A_{Left} + A_{Right} + A_{bottom}$.

||$^{ly}$ $C_{DB_j}$

$\longrightarrow \quad C_{overlap} = \dfrac{\epsilon_0 (\epsilon_r)_{SiO_2}}{t_{ox}} \times \text{Area}$

where $A = \delta W \longrightarrow$ overlap Area.