ACE

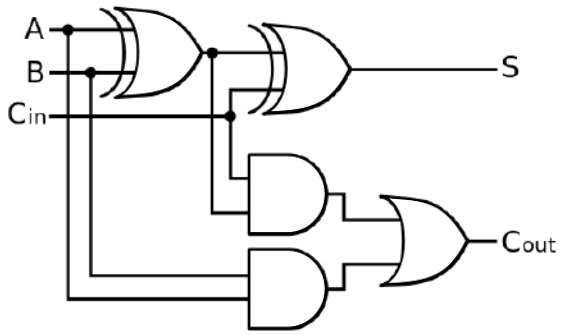
SINCE 2011

GATE | PSUs

ELECTRONICS & COMMUNICATION ENGINEERING

Digital Circuits

(**Text Book :** Theory with worked out Examples and Practice Questions)



Chapter 1 Number Systems

(Solutions for Text Book Practice Questions)

01. Ans: (d)

Sol: $135_x + 144_x = 323_x$

$(1\times x^2 + 3 \times x^1 + 5 \times x^0)+(1\times x^2+4\times x^1+ 4\times x^0)$
$= 3x^2 + 2x^1 + 3x^0$

$\Rightarrow x^2+3x+5+x^2+4x+4 = 3x^2+ 2x + 3$

$x^2 – 5x – 6 = 0$

$(x–6)\ (x+ 1) = 0$ (Base cannot be negative)

Hence $x = 6$.

(OR)

As per the given number x must be greater than 5. Let consider $x = 6$

$(135)_6 = (59)_{10}$

$(144)_6 = (64)_{10}$

$(323)_6 = (123)_{10}$

$(59)_{10} + (64)_{10} = (123)_{10}$

So that $x = 6$

02. Ans: (a)

Sol: 8-bit representation of

$+127_{10} = 01111111_{(2)}$

1's complement representation of

$– 127 = 10000000.$

2's complement representation of

$– 127 = 10000001.$

No. of 1's in 2's complement of

$– 127 = m = 2$

No. of 1's in 1's complement of

$– 127 = n = 1$

$\therefore$ m: n = 2:1

03. Ans: (c)

Sol: In 2's complement representation the sign bit can be extended towards left any number of times without changing the value. In given number the sign bit is 'X_3', hence it can be extended left any number of times.

04. Ans: (c)

Sol: Binary representation of $+(539)_{10}$:

2	539
2	269 –1
2	134 –1
2	67 –0
2	33 –1
2	16 –1
2	8 –0
2	4 –0
2	2 –0
	1 –0

$(+539)_{10} = (10000\ 11\ 0\ 11)_2 = (00100\ 0011011)_2$

2's complement $\rightarrow$ 110111100101

Hexadecimal equivalent $\rightarrow (DE5)_H$

05. Ans: 5

Sol: Symbols used in this equation are 0,1,2,3 Hence base or radix can be 4 or higher

$(312)_x = (20)_x\ (13.1)_x$

$3x^2 + 1x + 2x^0 = (2x+0)\ (x+3x^0+x^{-1})$

$3x^2+x+2 = (2x)\left(x + 3 + \frac{1}{x}\right)$

$3x^2 + x + 2 = 2x^2 + 6x + 2$

$x^2 – 5x = 0$

$x(x –5) = 0$

$x = 0$(or) $x = 5$

x must be $x > 3$, So $x = 5$

06. Ans: 3

Sol: $123_5 = x8_y$

$1 \times 5^2 + 2 \times 5^1 + 3 \times 5^0 = x.y^1 + 8 \times y^0$

$25 + 10 + 3 = xy + 8$

$\therefore xy = 30$

Possible solutions:

i. $x = 1, y = 30$

ii. $x = 2, y = 15$

iii. $x = 3, y = 10$

$\therefore$ 3 possible solutions exists.

07. Ans: 1

Sol: The range (or) distinct values

For 2's complement $\Rightarrow -(2^{n-1})$ to $+(2^{n-1}-1)$

For sign magnitude

$\Rightarrow -(2^{n-1}-1)$ to $+(2^{n-1}-1)$

Let $n = 2 \Rightarrow$ in 2's complement

$-(2^{2-1})$ to $+(2^{2-1}-1)$

-2 to $+1 \Rightarrow -2, -1, 0, +1 \Rightarrow X = 4$

$n = 2$ in sign magnitude $\Rightarrow -1$ to $+1 \Rightarrow Y = 3$

$X - Y = 1$

08. Ans: (a, b & c)

Sol: (a) When we have 10 base then we have (0 - 9) number.

when we have 16 base then we have (0 - 15) number.

when we have 8 base then we have (0 - 7) number.

So, this is correct statement as the longest digit decimal value is (k – 1) in base k system

(b) This is also true because as an example

$10 \rightarrow$ We borrow k as an significant digit

$(86)_{10}$

$-(79)_{10}$

$(06)_{10}$

(c) This statement is also true and have easy conversion as well as it has highest number of bits.

(d) Direct conversion is possible between binary & octal number system

ex: $\underbrace{100111}_{(47)_8}$

Chapter 2 Logic Gates & Boolean Algebra

01. Ans: (c)

Sol: Given 2's complement numbers of sign bits are x & y. z is the sign bit obtained by adding above two numbers. ∴ Overflow is indicated by = $\bar{x}\bar{y}z + xy\bar{z}$

Examples

1. A = +7 0111
   B = +7 0111
   14 1110 $\Rightarrow \bar{x}\bar{y}z$
2. A = +7 0111
   B = +5 0101
   12 1100 $\Rightarrow \bar{x}\bar{y}z$
3. A = –7 1001
   B = –7 1001
   –14 10010 $\Rightarrow xy\bar{z}$
4. A = –7 1001
   B = –5 1011
   –12 10100 $\Rightarrow xy\bar{z}$

02. Ans: (b)

Sol: Truth table of XOR

A	B	o/p
0	0	0
0	1	1
1	0	1
1	1	0

Stage 1:

Given one i/p = 1 Always.

1	X	o/p	
1	0	1	= $\overline{X}$
1	1	0	= $\overline{X}$

For First XOR gate o/p = $\overline{X}$

Stage 2:

$\overline{X}$	X	o/p
0	1	1
1	0	1

For second XOR gate o/p = 1.

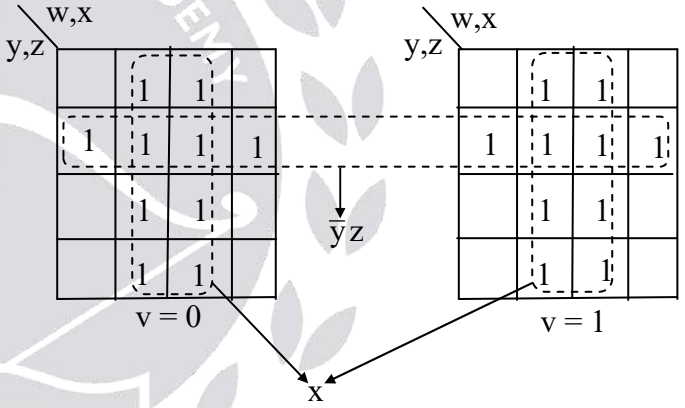
Similarly for third XOR gate o/p = $\overline{X}$ & for fourth o/p = 1

For Even number of XOR gates o/p = 1

For 20 XOR gates cascaded o/p = 1.

03. Ans: (b)

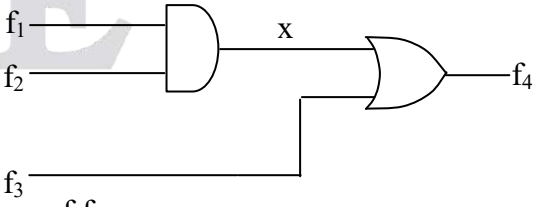
Sol:



Number of min terms = 20

04. Ans: (c)

Sol:



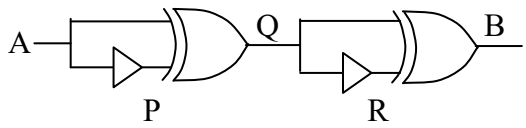
$x = f_1 f_2$

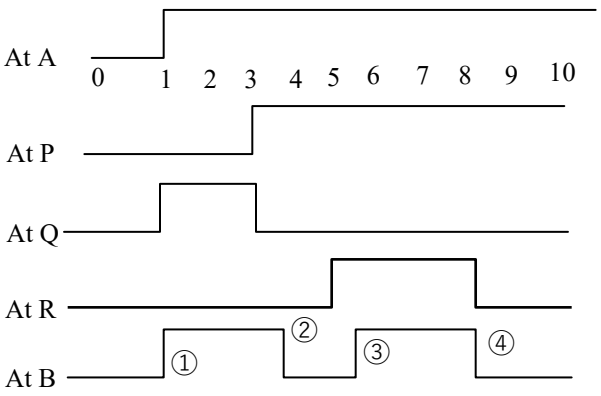
$f_4 = f_1.f_2 + f_3$

$f_2 = \sum m(6, 8)$

05. Ans: (d)

Sol:





06. Ans: (c)

Sol: $\overline{x_1} \oplus \overline{x_3} = \overline{x_1}\, x_3 + x_1 \overline{x_3} = y$

$\overline{x_2} \oplus \overline{x_4} = \overline{x_2}\, x_4 + x_2 \overline{x_4} = z$

$\left(\overline{x_1} \oplus \overline{x_3}\right) \oplus \left(\overline{x_2} \oplus \overline{x_4}\right)$

$= y \oplus z = 0$, when $y = z$

$\therefore$ option (c) is true

For all cases option A, B, D not satisfy.

07. Ans: (b)

Sol: $M(a,b,c) = ab + bc + ca$

$\overline{M(a,b,c)} = \overline{b}\overline{c} + \overline{a}\,\overline{b} + \overline{a}\,\overline{c}$

$M(a, b, \overline{c}) = ab + b\overline{c} + \overline{c}\,a$

$M(\overline{M(a,b,c)}, M(a,b,\overline{c}), c)$

$= \left(\overline{b}\overline{c} + \overline{a}\overline{b} + \overline{a}\,\overline{c}\right)(ab + b\overline{c} + a\overline{c})$

$+ (ab + \overline{b}\overline{c} + \overline{c}a)c + \left(\overline{b}\overline{c} + \overline{a}\overline{b} + \overline{a}\,\overline{c}\right)c$

$= \left(\overline{b}\overline{c} + \overline{a}\overline{b} + \overline{a}\,\overline{c}\right)(ab + b\overline{c} + a\overline{c})$

$+ \left(\overline{b}\overline{c} + \overline{a}\overline{b} + \overline{a}\,\overline{c}\right)(c) + abc$

$= ab\overline{c} + \overline{a}bc + abc + \overline{a}\overline{b}c$

$= \overline{c}[a\overline{b} + \overline{a}b] + c[ab + \overline{a}\overline{b}]$

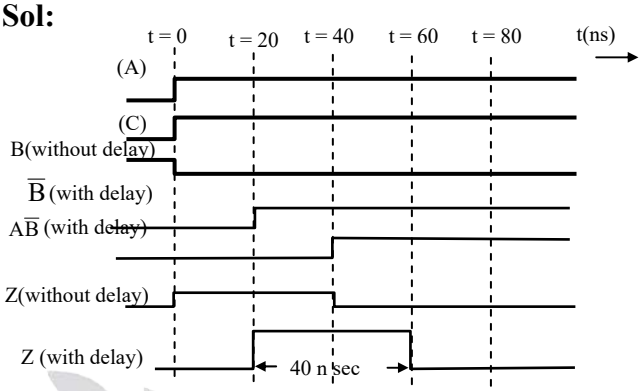
$= \sum m(1,2,4,7)$

$\therefore M(x, y, z) = a \oplus b \oplus c$

Where $x = \overline{M(a,b,c)}$, $y = M(a,b,\overline{c})$, $z = c$

08. Ans: 40

Sol:



$\therefore$ Z is 1 for 40 nsec

09. Ans: (c)

Sol: Logic gates $\overline{X} + Y = \overline{X\overline{Y}} = \overline{XY_1}$

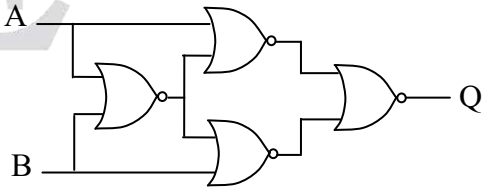
Where $Y_1 = \overline{Y}$

It is a NAND gate and thus the gate is 'Universal gate'.

10. Ans: (a & d)

Sol: **(a)** is correct because stair case operation is performed with ex-OR gate.

(d) 4 number of 2 input NOR gates are sufficient to implement 2-input Ex-NOR gate.

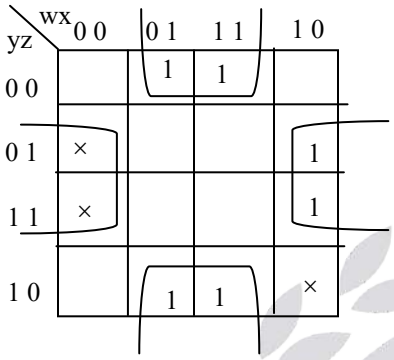


A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Chapter 3 K - Maps

01. Ans: (b)

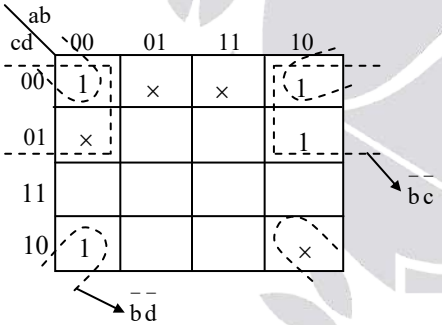
Sol:



$f = \bar{x}z + x\bar{z}$

02. Ans: (b)

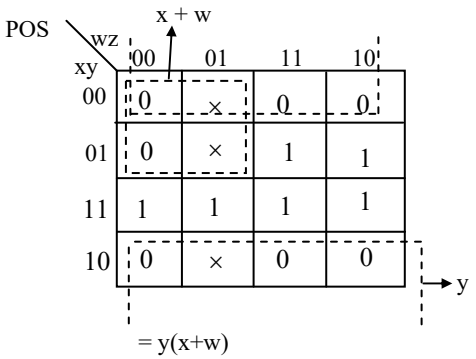
Sol:

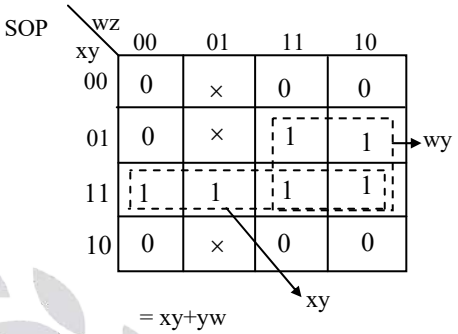


$f = \bar{b}\,\bar{d} + \bar{b}\,\bar{c}$

03.

Sol:





SOP: x y + y w

POS: y(x + w)

04. Ans: (a)

Sol: For n-variable Boolean expression,

Maximum number of minterms = 2^n

Maximum number of implicants = 2^n

Maximum number of prime implicants = $\frac{2^n}{2}$

$= 2^{n-1}$

05. Ans: (c)

Sol:

C \ AB	00	01	11	10
0	1	1	0	0
1	0	1	1	0

$F(A, B, C) = \bar{A}\bar{C} + BC$

06. Ans: 1

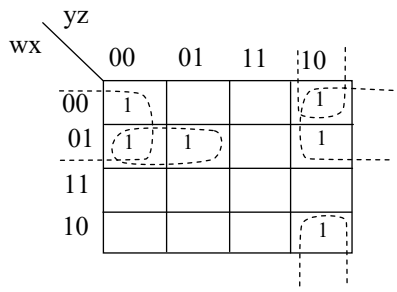
Sol: After minimization = $\left(\overline{\bar{A} + \bar{B} + \bar{C} + \bar{D}}\right)$

= ABCD

$\therefore$ only one minterm.

07. Ans: 3

Sol: $\overline{w}\,\overline{z} + \overline{w}\,x\overline{y} + \overline{x}\,y\overline{z}$

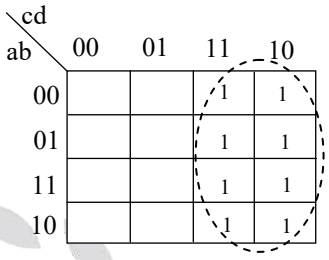


$\therefore$ Total number of prime implicants of the function 'f' is 3.

08. Ans: (a, b & c)

Sol: **(d)** is incorrect because resultant term will have 1 literal after grouping 8 number of cells.

Ex:



f = c Only 1 literals

Chapter 4 Combinational Circuits

01. Ans: (d)

Sol: Let the output of first MUX is "F_1"

$F_1 = AI_0 + AI_1$

Where A is selection line, I_0, I_1 = MUX Inputs

$F_1 = \overline{S}_1.W + S_1.\overline{W} = S_1 \oplus W$

Output of second MUX is

$F = \overline{A}.I_0 + A.I_1$

$F = \overline{S}_2.F_1 + S_2.\overline{F}_1$

$F = S_2 \oplus F_1$

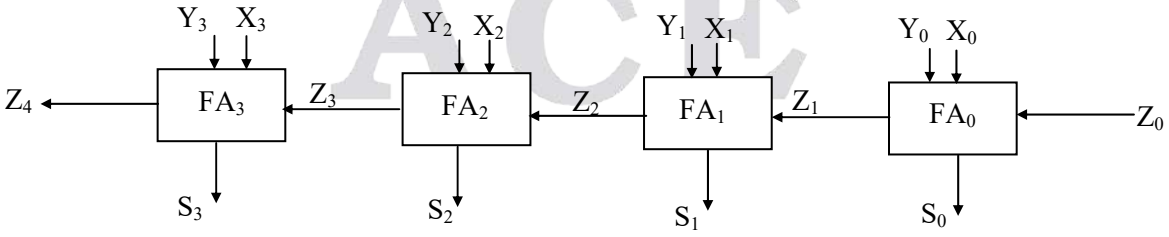
But $F_1 = S_1 \oplus W$

$F = S_2 \oplus S_1 \oplus W$

i.e., $F = W \oplus S_1 \oplus S_2$

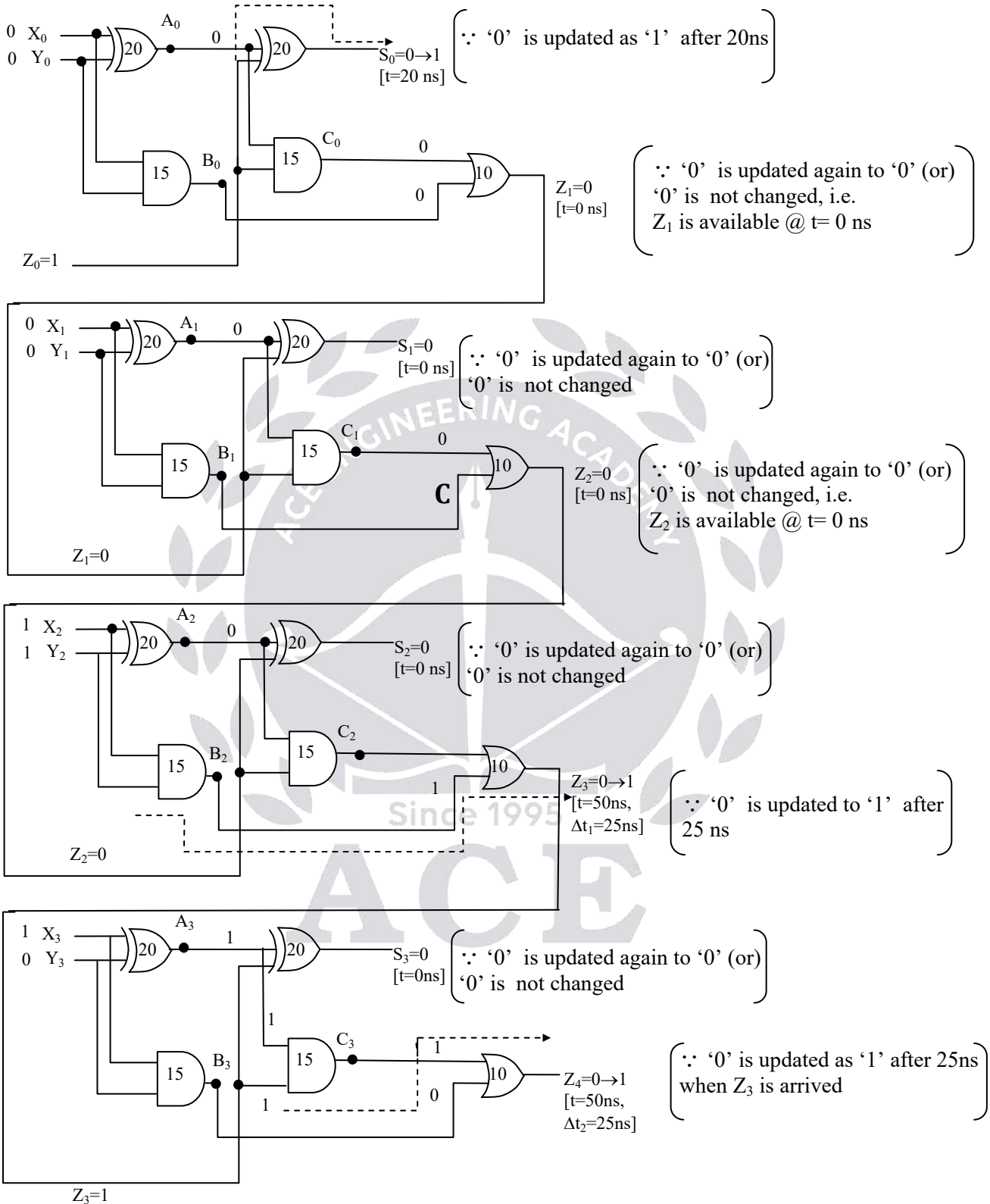
02. Ans: 50

Sol:



Initially all the output values are '0', at t = 0, the inputs to the 4-bit adder are changed to $X_3X_2X_1X_0 = 1100$, $Y_3Y_2Y_1Y_0 = 0100$

- - - - - - indicates critical path delay to get the output



Total time taken = $\Delta t_1 + \Delta t_2 = 50$ ns

i.e. critical time (or) maximum time is taken for Z_4 to get final output as '1'

03. Ans: (a)

Sol: The given circuit is binary parallel adder/subtractor circuit. It performs A+B, A–B but not A + 1 operations.

K	C_0	Operation
0	0	A+B (addition)
0	1	A+B+1(addition with carry)
1	0	A+$\overline{B}$ (1's complement addition)
1	1	A+$\overline{B}$ +1(2's complement subtraction)

04. Ans: (d)

Sol: It is expansion of 2:4 decoders to 1:8 demultiplexer A_1, A_0 must be connected to S_1, S_0 i.e.., $R = S_0$, $S = S_1$

Q must be connected to S_2 i.e., $Q = S_2$

P is serial input must be connected to D_{in}

05. Ans: 6

Sol: T = 0 → NOR → MUX 1 → MUX 2

2ns 1.5ns 1.5ns

Delay = 2ns + 1.5ns + 1.5ns = 5ns

T = 1 → NOT → MUX 1→NOR→ MUX 2

1ns 1.5ns 2ns 1.5ns

Delay = 1ns + 1.5ns + 2ns + 1.5ns = 6ns

Hence, the maximum delay of the circuit is 6ns .

06. Ans: –1

Sol: When all bits in 'B' register is '1', then only it gives highest delay.

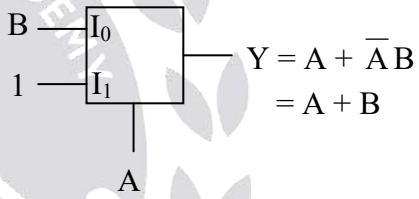
∴ '–1' in 8 bit notation of 2's complement is 1111 1111 .

07. Ans: (b & c)

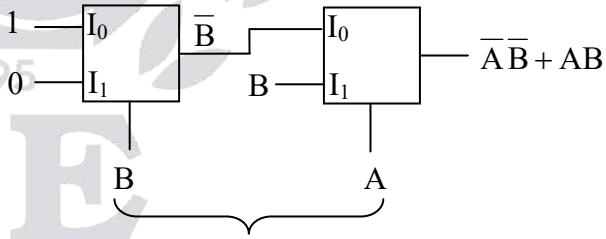
Sol: **(a)** It is incorrect because for getting $\overline{B}$ is $\overline{(A+B)} = \overline{A}\,\overline{B}$

we need one more 2×1 MUX

(b) It is correct



(c) It is correct we need minimum 2 number of 2×1 muxes for implementing 2 input exnor gate



2×1 MUX required = 2

(d) It is incorrect because one 16×1 MUX is sufficient for all 4 variable function.

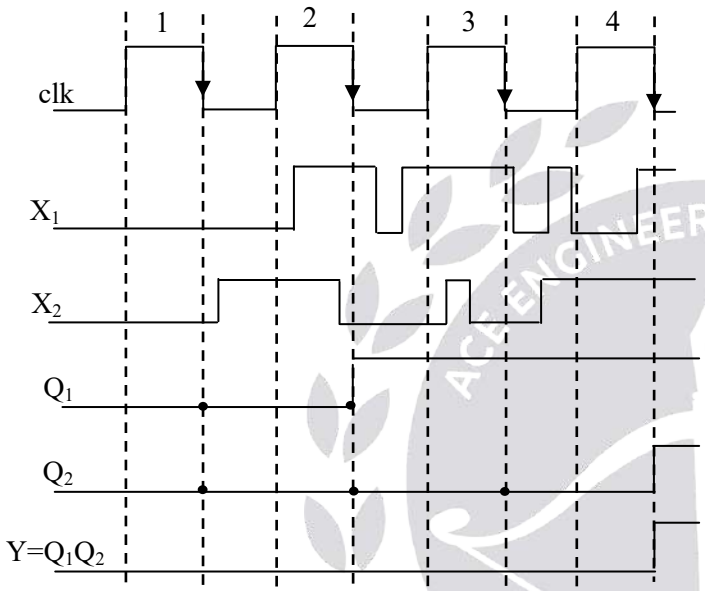
Chapter 5 Sequential Circuits

01. Ans: (c)

Sol: Given Clk, X_1, X_2

Output of First D-FF is Q_1

Output of Second D-FF is Q_2



02. Ans: 4

Sol: In the given first loop of states, zero has repeated 3 times. So, minimum 4 number of Flip-flops are needed.

03. Ans: 7

Sol: The counter is cleared when

$Q_DQ_CQ_BQ_A = 0110$

Clk	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	0	0	0

As the clear input is given to be synchronous so it waits upto the next clock pulse to clear the counter & hence the counter get's cleared during the 7^{th} clock pulse.

$\therefore$ mod of counter = 7

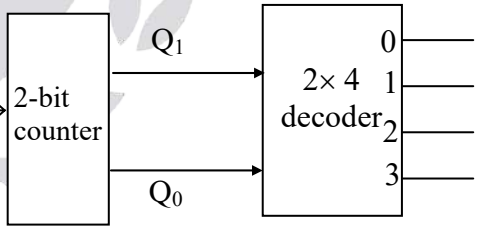
04. Ans: (b)

Sol: The given circuit is a mod 4 ripple down counter. Q_1 is coming to 1 after the delay of $2\Delta t$.

CLK	Q_1	Q_0
	0	0
1	1	1
2	1	0
3	0	1
4	0	0

05. Ans: (c)

Sol: Assume n = 2



Outputs of counter is connected to inputs of decoder

Counter outputs		Decoder inputs		Decoder outputs			
Q_1	Q_0	a	b	d_3	d_2	d_1	d_0
0	0	0	0	0	0	0	1
0	1	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0

The overall circuit acts as 4-bit ring counter

n = 2

$\therefore$ $k = 2^2 = 4$, k-bit ring counter

06. Ans: (b)

Sol:

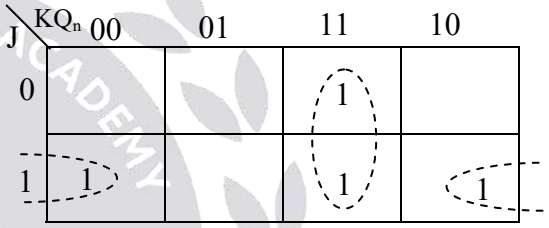
CLK	Serial in= $B \oplus C \oplus D$	A B C D
0		1 0 1 0
1	1 →	1 1 0 1
2	0 →	0 1 1 0
3	0 →	0 0 1 1
4	0 →	0 0 0 1
5	1 →	1 0 0 0
6	0 →	0 1 0 0
7	1 →	1 0 1 0

$\therefore$ After 7 clock pulses content of shift register become 1010 again

07. Ans: (b)

Sol:

J	K	Q	$\overline{Q}_n$	$T = (J + Q_n)(K + \overline{Q}_n)$	Q_{n+1}
0	0	0	1	0.1 = 0	0
0	0	1	0	1.0 = 0	1 } Q_n
0	1	0	1	0.1 = 0	0
0	1	1	0	1.1 = 1	0 } 0
1	0	0	1	1.1 = 1	1
1	0	1	0	1.0 = 0	1 } 1
1	1	0	1	1.1 = 1	1
1	1	1	0	1.1 = 1	0 } $\overline{Q}_n$



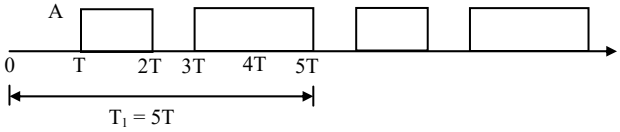
$T = J\,\overline{Q_n} + KQ_n = (J+Q_n)(K+\overline{Q_n})$

08. Ans: 1.5

Sol:

Clk	Q_1	Q_2	Q_3	Q_4	Q_5	$Y = Q_3 + Q_5$
0	0	1	0	1	0	0
1	0	0	1	0	1	1
2	1	0	0	1	0	0
3	0	1	0	0	1	1
4	1	0	1	0	0	1
5	0	1	0	1	0	0

The waveform at OR gate output, Y is [A = +5V]



Average power

$$P = \frac{V_{Ao}^2}{R} = \frac{1}{R}\left[\lim_{T_1\to\infty}\frac{1}{T_1}\int_o^{T_1} y^2(t)\,dt\right] = \frac{1}{RT_1}\left[\int_T^{2T} A^2 dt + \int_{3T}^{5T} A^2 dt\right]$$

$$= \frac{A^2}{RT_1}\left[(2T-T)+(5T-3T)\right] = \frac{A^2.3T}{R(5T)} = \frac{5^2.3}{10\times 5} = 1.5\,\text{mW}$$

09. Ans: (b)

Sol:

Present State	Next State		Output (Y)	
	X = 0	X = 1	X = 0	X = 1
A	A	E	0	0
B	C	A	1	0
C	B	A	1	0
D	A	B	0	1
E	A	C	0	1

Step (1):

By replacing state B as state C then state B, C are equal.

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	E
B	B	A
B	B	A
D	A	B
E	A	B

Step (2):

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	E
B	B	A
D	A	B
E	A	B

State D, E are equal, remove state E and replace E with D in next state.

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	D
B	B	A
D	A	B
D	A	B

Finally reduced state table is

Reduced state table		
Present state	Next state	
	X = 0	X = 1
A	A	D
B	B	A
D	A	B

$\therefore$ 3 states are present in the reduced state table

10. Ans: (c)

Sol: State table for the given state diagram

State	Input	Output
S_0	0	1
S_0	1	0
S_1	0	1
S_1	1	0

Output is 1's complement of input.

11. Ans: (c)

Sol: In state (C), when XYZ = 111, then Ambiguity occurs

Because, from state (C)

$\Rightarrow$ When X = 1, Z = 1

$\Rightarrow$ N.S is (A)

When Y = 1, Z = 1 $\Rightarrow$ N.S is (B)

12. Ans: (b & d)

Sol: (a) It is incorrect statement ripple counter is slower than synchronous counter is apply with 1 clock.

(b) It is correct statement because mod counters means it counts the number of clock pulses arriving at its clock input, which is basically we do in electronic time clocks.

(c) It is incorrect, because with the help of positive edge triggered JK-flip-flop we design binary down counter.

(d) It is correct statement because D-flipflop is easy to design and easy to get the next possible state output.

Chapter 6 Logic Gate Families

01. Ans: (b)

Sol: **V_{OH}(min):-**
(High level output voltage)
The minimum voltage level at a Logic circuit output in the logic '1' state under defined load conditions.

V_{OL}(max):-
(Low level output voltage)
The maximum voltage level at a logic circuit output in the Logical '0' state under defined load conditions.

V_{IL}(max):- (Low level input voltage)
The maximum voltage level required for a logic '0' at an input. Any voltage above this level will not be accepted as a Low by the logic circuit.

V_{IH}(min) :- (High level Input voltage)
The minimum voltage level required for logic '1' at an input. Any voltage below this level will not be accepted as a HIGH by the Logic circuit.

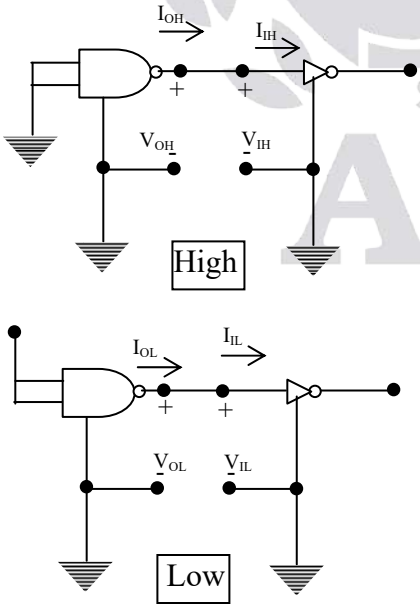


Fig: currents and voltages in the two logic states.

02. Ans: (b)

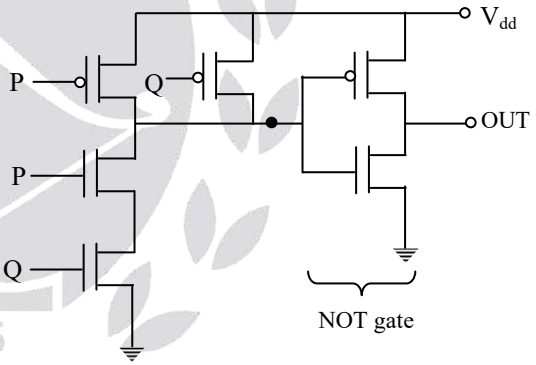
Sol: Fan out is minimum in DTL
(High Fan-out = CMOS)
Power consumption is minimum in CMOS.
Propagation delay is minimum in ECL (fastest = ECL)

03. Ans: (b)

Sol: When $V_i = 2.5V$,
Q_1 is in reverse active region
Q_2 is in saturation region
Q_3 is in saturation region
Q_4 is in cut-off region

04. Ans: (d)

Sol: The given circuit can be redrawn as below:



$OUT = \overline{(\overline{PQ})} = PQ$

$= P$ AND Q

05. Ans: (b)

Sol: As per the description of the question, when the transistor Q_1 and diode both are OFF then only output z = 1.

X	Y	Z	Remarks
0	0	0	Q_1 is OFF, Diode is ON
0	1	1	Q_1 is OFF, Diode is OFF
1	0	0	Q_1 is ON, Diode is OFF
1	1	0	Q_1 is ON, Diode is OFF

Hence $Z = \overline{X}Y$

06. Ans: (a, b & c)

Sol: **(a)** Correct statement, power consumes in CMOS is order of μW which is less than that of MOS logic gate.

(b) Correct statement ⇒ figure of merit = speed × power.

(c) It is also correct statement CMOS is made up of both P-channel & N-channel FET both have equal number.

(d) CMOS logic gate provide highest noise margin so this statement is incorrect.

Chapter 7 Semiconductor Memories

01. Ans: (b)

Sol: Square of a 4 - bit number can be at most 8 - bit number.

{ i.e $(1111)_2 = (15)_{10}$

$[(15)_{10}]^2 = (225)_{10}$}.

Therefore ROM requires 8 data lines.

Data is with size of 4 bits

ROM must require 4 address lines and 8 data lines

ROM = $2^n \times m$

n = inputs (address lines),

m = output lines

n = 4, m = 8.

02. Ans: (a)

Sol: ROM is used to design a combinational circuit. The number of address lines of the ROM is equal to the number of input variables in the truth table.

ROM is represented as $2^n \times m$ where 2^n inputs and m output lines.

[Where n = address bits]

03. Ans: (b)

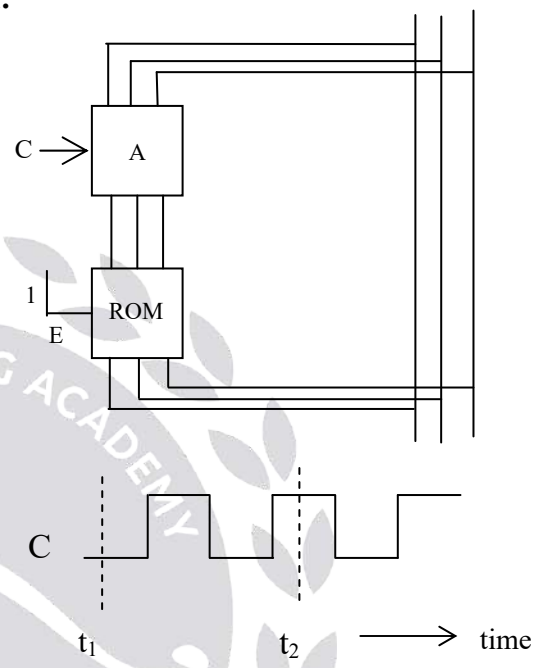
Sol:

8	4	2	1	2	4	2	1	2421 Outputs
i/p s				o/p s				
X_3	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0	
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	2
0	0	1	1	0	0	1	1	3
0	1	0	0	0	1	0	0	4
0	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	6
0	1	1	1	1	1	0	1	7
1	0	0	0	1	1	1	0	8
1	0	0	1	1	1	1	1	9
1	0	1	0	×	×	×	×	
1	0	1	1	×	×	×	×	
1	1	0	0	×	×	×	×	
1	1	0	1	×	×	×	×	
1	1	1	0	×	×	×	×	
1	1	1	1	×	×	×	×	

The outputs are in 2 4 2 1 BCD number

04. Ans: (c)

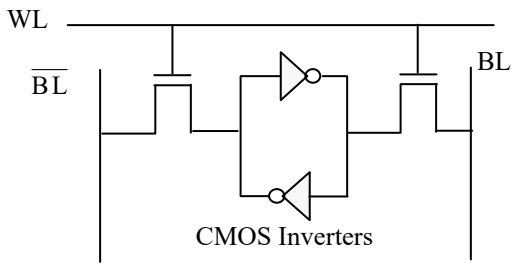
Sol:



At the rising edge of the First clock pulse the content of location $(0110)_2 = 6 \Rightarrow 1010$ appears on the data bus, at the rising of the second clock pulse the content of location $(1010)_2 = 10_2 \Rightarrow 1000$ appears on the data bus.

05. Ans: (b)

Sol: 1-bit SRAM memory cell is



In 2 Inverters, output of the 1st Inverter is connected to Gate Input of 2nd Inverter and vice versa.

06. Ans: (b & c)

Sol: **(a)** It is incorrect because ultraviolet rays are using to erase the data.

(b) It is correct, pendrive memory is example of flash memory.

(c) It is also correct, in flash it is possible to erase information either in Byte level or Block level.

(d) It is incorrect generally word size of a memory chip is 32-bit.

Chapter 8 A/D & D/A Converters

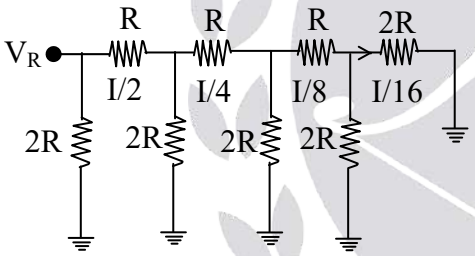
01. Ans: (b)

Sol:

CLK	Counter	Decoder	V_0
	Q_2 Q_1 Q_0	D_3 D_2 D_1 D_0	
1	0 0 0	0 0 0 0	0
2	0 0 1	0 0 0 1	1
3	0 1 0	0 0 1 0	2
4	0 1 1	0 0 1 1	3
5	1 0 0	1 0 0 0	8
6	1 0 1	1 0 0 1	9
7	1 1 0	1 0 1 0	10
8	1 1 1	1 0 1 1	11

02. Ans: (b)

Sol:



R_{equ} = (((((2R||2R)+R)||2R)+R)||2R)+R)||2R)

$R_{equ} = R = 10k\Omega$.

$$I = \frac{V_R}{R} = \frac{10V}{10k} = 1mA.$$

Current division at $\frac{I}{16}$

$$= \frac{1\times10^{-3}}{16} = 62.5\,\mu A$$

03. Ans: (c)

Sol: Net current at inverting terminal,

$$I_i = \frac{I}{4} + \frac{I}{16} = \frac{5I}{16}$$

$$V_0 = -I_i R = -\frac{5I}{16}\times 10k\Omega$$

$$= \frac{-5\times1\times10^{-3}\times10\times10^{3}}{16} = -3.125V$$

04. Ans: (d)

Sol: Given that $V_{DAC} = \sum_{n=0}^{3} 2^{n-1} b_n$ Volts

$$V_{DAC} = 2^{-1}b_0 + 2^0 b_1 + 2^1 b_2 + 2^2 b_3$$

$\Rightarrow V_{DAC} = 0.5b_0 + b_1 + 2b_2 + 4b_3$

Initially counter is in 0000 state

Up counter o/p	V_{DAC}(V)	o/p of comparator
b_3 b_2 b_1 b_0		
0 0 0 0	0	1
0 0 0 1	0.5	1
0 0 1 0	1	1
0 0 1 1	1.5	1
0 1 0 0	2	1
0 1 0 1	2.5	1
0 1 1 0	3	1
0 1 1 1	3.5	1
1 0 0 0	4	1
1 0 0 1	4.5	1
1 0 1 0	5	1
1 0 1 1	5.5	1
1 1 0 0	6	1
1 1 0 1	6.5	0

When V_{DAC} = 6.5 V, the o/p of comparator is '0'. At this instant, the clock pulses to the counter are stopped and the counter remains in 1101 state.

∴ The stable reading of the LED display is 13.

05. Ans: (b)

Sol: The magnitude of error between V_{DAC} & V_{in} at steady state is $|V_{DAC} - V_{in}| = |6.5 - 6.2|$

$= 0.3$ V

06. Ans: (a)

Sol: In Dual slope

$$\text{ADC} \Rightarrow V_{in}T_1 = V_R.T_2$$

$$\Rightarrow V_{in} = \frac{V_R T_2}{T_1}$$

$$= \frac{100\,\text{mV} \times 370.2\,\text{ms}}{300\ \text{ms}}$$

$$\text{DVM indicates} = 123.4$$

07. Ans: (d)

Sol: **Ex:** $f_{in} = 1$ kHz $\rightarrow f_s = 2$ kHz

$f_{in} = 25$ kHz $\leftarrow f_s = 50$ kHz

1. Max conversion time $= 2^{N+1}T = 2^{11}.1\ \mu s$
$= 2048\ \mu s$
2. Sampling period $= T_s \geq$ maximum conversion time
$T_s \geq 2048\ \mu s$
3. Sampling rate $f_s = \frac{1}{T_s} \leq \frac{1}{2048 \times 10^{-6}}$
$f_s \leq 488 \quad f_s \leq 500$ Hz
4. $f_{in} = \frac{f_s}{2} = 250\,\text{Hz}$

08. Ans: (b & d)

Sol: **(a)** It is incorrect, minimum number of comparator required in 'n' bit flash ADC is $2^n - 1$.

(b) It is correct (no register/counter required in flash ADC, only comparator required).

(c) It is incorrect,

Conversion time of SAR = n T_{clk}

Conversion time of Dual Slope ADC
$= (2^{n+1})\ T_{clk}$

SAR faster than Dual slope ADC.

(d) It is correct, because it compares DAC output with analog voltage & does the same till both are equal in magnitude. At this moment counter will stop. Maximum conversion time is equal to $(2^{n-1})\ T_{clk}$ of n-bit ADC. The conversion time depends on analog input voltage as well as on size of ADC.

Chapter 9 Computer Arithmetic

01. Ans: (a)

Sol: E = e + Bias

02. Ans: (c)

03. Ans: (a)

Sol: X = –14.25, S = 1, e = original exponent

E = biased Exponent,

b = biasing amount

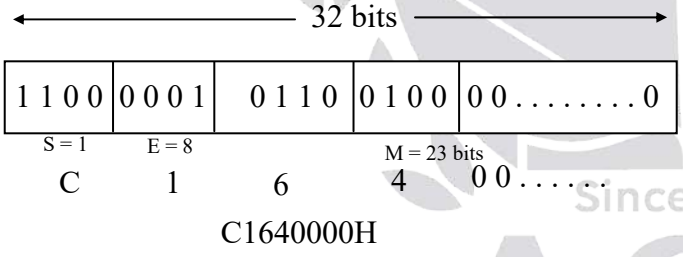
$14.25 = 1110.01 \times 2^0$

$= 1.11001 \times 2^3$

e = 3, E = 3 + 127

= 130

130 = 10000010 M = 1100100…0 (23 bits)



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Chapter 10 CPU Design

01. Ans: (d)

02. Ans: (a, b, c, d)

03. Ans: (d)

Sol: To execute interrupt cycle, the present content of PC will be pushed to stack with the help of MBR and MAR before placing ISR address in PC. (Always only MAR and MBR are used to address in Basic computer).

04. Ans: (a)

Sol: Total Size of micro-instructions = 26 bits

Size of micro-operation = 13 bits

Total inputs for the multiplexer (Status bits) inputs = 8

So the multiplexer selection lines field(Y)

= 3 bits ($2^3 = 8$)

The number of bits in the next address field size(X) = 13 – 3 = 10 bits

Size of control memory = $2^{10} = 1024$

05. Ans: (d)

Sol: $S_8 = I_1T_4 + I_2T_4 + I_3T_4 + I_4T_4$

$= I \times T_4 = T_4$

$\because\ I = (I_1 + I_2 + I_3 + I_4)$

$S_7 = (I_1T_3 + I_2T_3 + I_3T_3 + I_4T_3)$

$+ (I_3T_1 + I_3T_2 + I_3T_3 + I_3T_4) + (T_4I_3 + T_4I_4)$

$\because\ S_7 = T_3 + I_3 + T_4 \times I_4$

06. Ans: (b)

Sol: Fastest Control unit is hard-wired control unit and vertical micro-programming control unit is slowest.

07. Ans: (d)

08. Ans: (d)

Sol: All the given characteristics are belonging to RISC processor.

Chapter 11 Instruction Set & Addressing Modes

01. Ans: (a)

Sol: 1. Direct y = z[I]

2. Immediate x = 5

3. Index x = z + m

4. Auto k = c+ +

02. Ans: (c)

Sol: Register indirect addressing lets you generate lots of different addresses when a program is executed. Address register indirect addressing is so called because it uses an address register to point at the location of the operand in memory; that is, the address of an operand is obtained indirectly via an address register. Instead of telling the computer where the operand is, you tell it where the address of the operand can be found.

03. Ans: (c)

Sol: **Relative Addressing mode**: Relative Addressing mode is used in intra segment branching.

Effective Address = Program Counter + Displacement

Relative Base Addressing Mode: Effective Address = PC + BR + displacement . Where PC stands for program counter and BR stands for base register.

"The code is dependent means the option is direct addressing mode".

04. Ans: (b)

Sol: Base register addressing mode is used to relocate the program from one segment to other segment.

Chapter 12 Pipeline Organization

01. Ans: (a)

02. Ans: (b)

Sol: First task will be completed after n clocks (because there are n segments) and the remaining m-1 tasks are shipped out at the rate of one task per pipeline clock.

Therefore, n + (n–1) clock periods are required to complete m tasks using an n-segment pipeline. If all m tasks are executed without any overlap, mn clock periods are needed because each task has to pass through all n segments. Thus speed gained by an n segment pipeline can be shown as follows:

Speed up P(n) =

$$\frac{\text{number of clocks required when there is no overlap}}{\text{number of clocks required when tasks are overlapped in time}}$$

$$= \frac{mn}{n+m-1}$$

03. Ans: (c)

Sol: Max. stage delay = 160 μs

Buffer delay = 5 μs

Pipeline clock = 165 μs

$T_{1000} = (K + n - 1)\, T_p$ clock

$$= (4+999) * 165 = \left(\frac{165495}{1000}\right) \mu s$$

$= 165.5$ μs

04. Ans: (b)

Sol: For D_1 processor, maximum $T_{seg} = 4$ ns,

n = 100, k = 5

Time = 104 × 4 ns = 416 ns

For D_2 processor,

n = 100, k = 8, $T_{seg} = 2$ ns

Time = 107 × 2 ns = 214 ns

Hence, 202 ns time will be saved