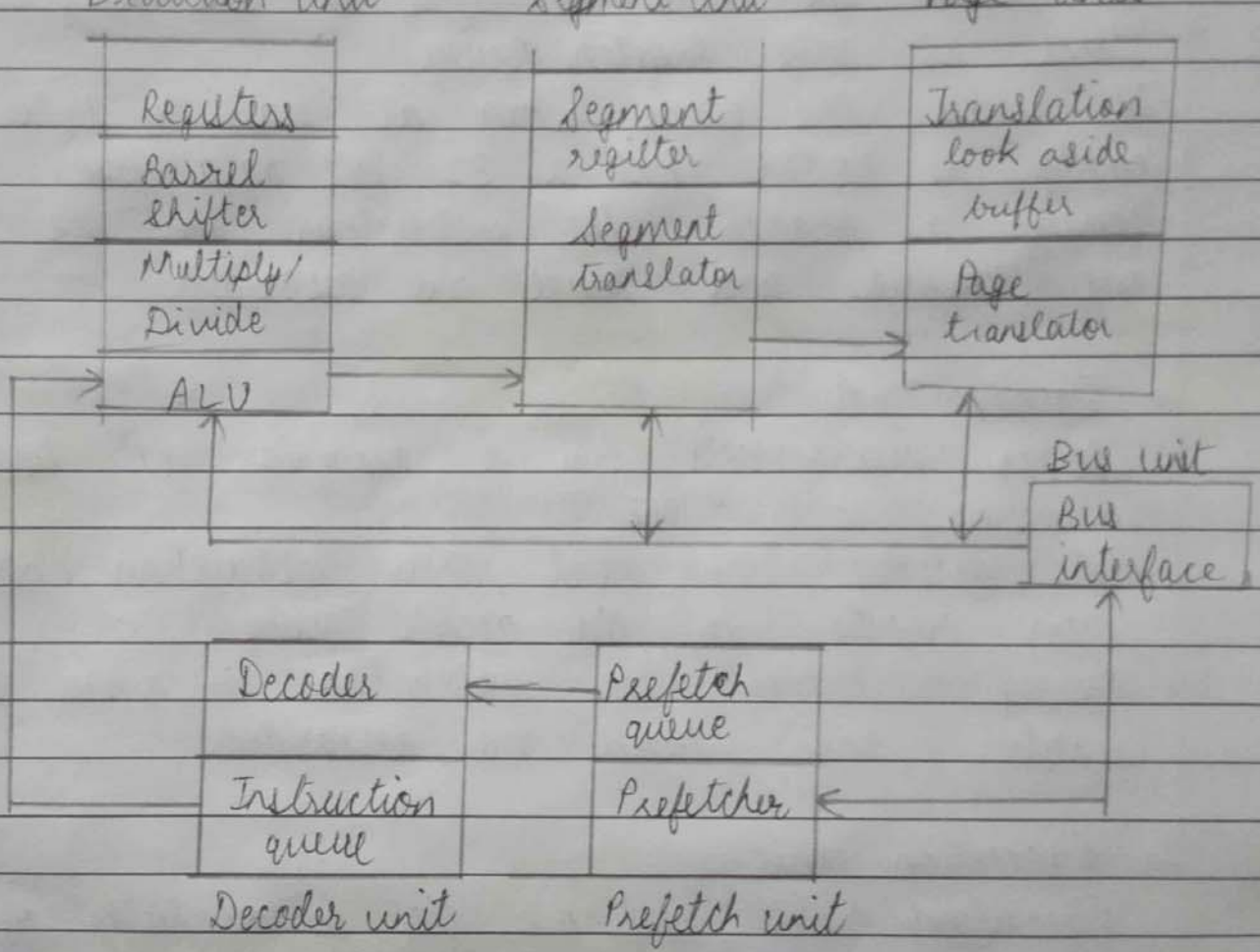
D Y PATIL
RAMRAO ADIK
INSTITUTE OF
TECHNOLOGY
NAVI MUMBAI

Q1 Illustrate the architecture of 80386DX with neat diagram.



→ Bus Unit (Bus interface unit)
This unit is responsible for transferring data in and out of the µP.
It is connected to external memory and I/O devices, using system bus.
It ~~gives~~ gets request from prefetch unit for fetching instruction and from execution unit for transferring data.

→ Prefetch unit
The Prefetch unit fetches further instructions in advance to implement pipelining.
It fetches the next 16 bytes of the program and stores it into Prefetch Queue.
It refills the queue when at least 4 bytes are empty as 80386 has a 32 bit data bus.
During a branch, the instruction in the queue are invalid and hence are discarded.

→ Decode Unit
80386 microprocess has a separate unit for decoding instructions.
It decodes the next three instruction and keep them ready in the decode Queue.
During a branch, the instruction in queue are invalid and hence are discarded.

→ Execution unit
Execution unit performs the main task of executing instructions
Normally, execution requires Arithmetic or Logic operations performed by a 32 bit ALU.
It also has dedicated circuits for 32 bit division and multiplication
A 64-bit barrel shifter is also provided for faster shifts during multiplication and division.
Operands for the ALU can either be provided in the instruction or can be taken from memory

D Y PATIL
RAMRAO ADIK INSTITUTE OF TECHNOLOGY
NAVI MUMBAI

or could be taken from the 32 bit registers like EAX, EBX etc.
Additionally there is 32 bit flag register (EFLAGS) giving the status of current result.

→ Memory Unit
The memory unit converts Virtual Address to Physical Address.
80386 microprocessor implements 64 Tera bytes of Virtual memory using segmentation and Paging
Hence the memory unit is sub-divided into Segmentation Unit and Paging unit.
Segmentation is compulsory, while Paging is optional
The segmentation unit converts logical address into linear address.
Paging unit converts linear address into physical address.

Q2 Explain the significance of branch predication mechanism in Pentium processor

- Branch Prediction logic reduces flushing problem of pipelining and avoid pipeline and EU stall if branching prediction is done correct
- ~~Else~~ Else if predicted wrong there is a performance penalty.
- In this scheme, a prediction is made concerning the branch instruction currently in pipeline.
- Prediction will be either taken or not taken

19CE1107

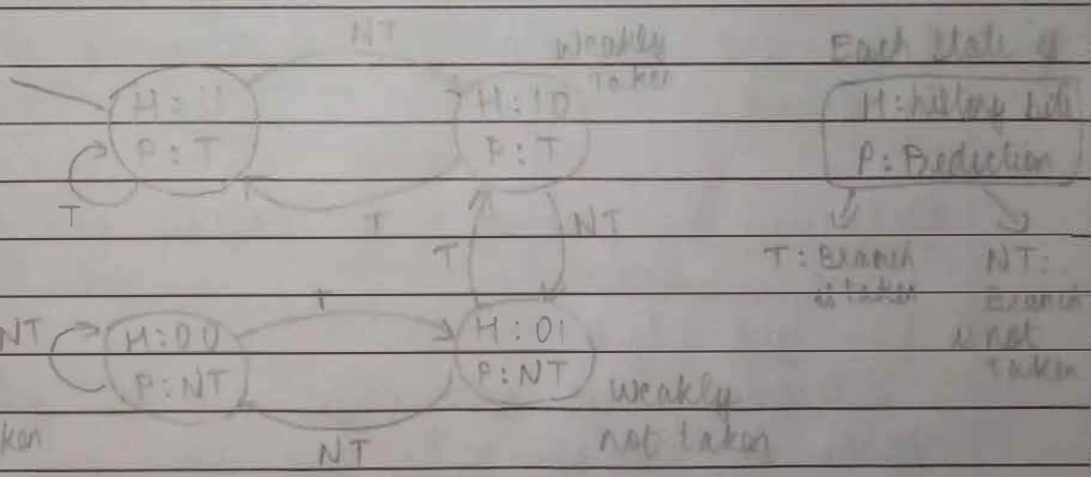
- If the prediction turns out to be true, the ~~prediction~~ pipeline will not be flushed and no clock cycle will be lost
- If the prediction is flase, the pipeline is flushed and started over with correct instruction.
- It result in a 3 cycle penalty if the branch is executed in the u pipeline and 4 cycle penalty in v-pipeline.
- It is implemented using 4-way set associative cache with 256 entries. This is referred as the Branch Target Buffer (BTB).
- The directory entry (tag) for each line contains the following information.
  - Valid Bit : indicates whether or not the entry is in use.
  - History Bit : track how often the branch has been taken
  - Source memory address that the branch instruction was fetched from.
  - If its directory entry is valid, the target address of the branch is stored in corresponding data entry in BTB.

- BTB is a look aside cache that sits off to the side of D1 stages of two pipelines and monitors for branch instructions.

- When the instruction reaches the exection stage, the branch will be either taken or not taken.

D Y PATIL
RAMRAO ADIK INSTITUTE OF TECHNOLOGY
NAVI MUMBAI

- If taken, next instruction to be executed should be the one fetched from branch target address.
- If not taken, the next instruction is the next sequential memory address.
- When the branch is taken for the first time, the execution unit provides feedback to the branch prediction logic.
- The branch target address is sent back and recorded in BTB.
- A directory entry is made containing the source memory and history bits set as strongly taken



History bits	Resulting description	Prediction Mode	If branch is taken	If branch is not taken
11	Strongly taken	Branch Taken	Remains strongly taken	Downgrades to weakly taken
10	weakly taken	Branch Taken	upgrades to strongly taken	Downgrades to weakly not taken

History Bits	Resulting Description	Prediction mode	If branch is taken	If branch is not taken
01	Weakly not taken	Branch not taken	upgrades to weakly taken	Downgrades to strongly not taken.
00	Strongly not taken	branch not taken	upgrades to weakly not taken	Remain strongly not taken.

Q3. Draw and explain the Pentium 4 NetBurst architecture in detail.

Pentium 4 processor is based on Netburst archetecture

- BTB and iTLB
  determines next instruction to be fetched from L2 cache in case of a TC miss

- The instruction decoder
  Takes bytes delivered from the L2 cache and decodes them into uops.

- The Trace Cache
  Caches uops from the instruction decoder.
  Used as L1 instruction cache
  Delivers 3 uops / clock
  The micro code ROM has the complex micro code sequences

D Y PATIL
RAMRAO ADIK INSTITUTE OF TECHNOLOGY
NAVI MUMBAI

- Uops Queue
  Holds uops from TC, ucode ROM or decode logic
  Decouples the FE from the OOO Execution Engine
- The Renamer
  Maps arch registers onto 128 deep physical register file.
- The Allocator - assigns all necessary hardware buffers in the machine from this uop to execute.
- The Scheduler - determine when a uop is ready to execute
- Execution unit
  up to 4 integer arithmetic operations per clock cycle
  1 floating point operation (including 128 bit SSE) per clock cycle.
  A memory load and store operation (upto 128 bit) each clock cycle
- 3.2 GB/sec system bus.

The net burst micro architecture delivers number of new and innovative features including
Hyper Threading technology
Hyper pipelined Technology
533 MHz or 400 MHz system bus
Execution Trace Cache
Rapid Execution Engine
as well as number of enhanced features
Advanced Transfer Cache
Advanced Dynamic Execution
Enhanced floating point and multimedia
Steaming SIMD Extensions 2 (SSE2)

Pentium 4 Block Diagram