Code: 20A04303T

R20

B.Tech II Year I Semester (R20) Supplementary Examinations April/May 2024

DIGITAL LOGIC DESIGN

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1		Answer the following: (10 X 02 = 20 Marks)	
	(a)	Convert the $(535)_{10}$ into octal number.	2M
	(b)	Define the standard form.	2M
	(c)	What do you mean by Combinational circuit?	2M
	(d)	Draw the full adder circuit.	2M
	(e)	Draw the T Flip-Flop circuit using NAND gates.	2M
	(f)	What is the purpose of counter?	2M
	(g)	How do you define Mealy machine?	2M
	(h)	What is state assignment?	2M
	(i)	What is meant by PROM?	2M
	(j)	List the advantages of FPGAs.	2M

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

2	(a)	Perform the following operations in binary: (i) $(65.265)_8$ x $(36.135)_8$, (ii) $(67.65)_8 \div (26.55)_8$.	5M
	(b)	Implement the EX-NOR gate by using NAND gates.	5M
		OR	
3	(a)	Implement the following expression using NOR gates: F(A, B, C, D) = ABC + ACD + A'BC'D'.	5M
	(b)	Implement the OR gate using NAND gates.	5M
4	(a)	Design a Full subtractor by using Multiplexer.	5M
	(b)	Design a 4 to 16 Decoder by using 2 to 4 Decoders.	5M
		OR	
5	(a)	Draw the Carry-Look-Ahead adder and explain its working principle.	5M
	(b)	Design a 8 to 3 Priority Encoder.	5M
6	(a)	Draw the RS Flip-Flop with NAND gates and explain its working.	5M
	(b)	Design a Mod-6 Synchronous counter.	5M
		OR	
7	(a)	Implement the D Flip-Flop by using JK Flip-Flop.	5M
	(b)	Draw the 4-bit Ring counter and explain its operation.	5M
8	(a)	Explain the step by step state assignment procedure.	5M
	(b)	Illustrate the conversion procedure of Moore machine to Mealy machine.	5M
		OR	
9	(a)	Summarize the reduction of state tables by using partition technique.	5M
	(b)	Explain the basic structure of the FSM with neat sketches.	5M
10	(a)	Implement the full adder by using PLA.	5M
	(b)	Develop a Verilog code for 8 to 1 Multiplexer.	5M
		OR	
11	(a)	Implement the 4 to 16 Decoder by using PAL.	5M
	(b)	Develop a Verilog code for BCD adder.	5M

*****

Code: 20A04303T **R20**

B.Tech II Year I Semester (R20) Supplementary Examinations August/September 2023

DIGITAL LOGIC DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1		Answer the following: (10 X 02 = 20 Marks)	
	(a)	Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers.	2M
	(b)	Distinguish between canonical and standard forms by giving an example.	2M
	(c)	Write the POS representation of the following SOP function: $f(x, y, z) = \sum m(0, 1, 3, 5, 7)$.	2M
	(d)	Summarize, how don't care condition in K-map help for circuit simplification.	2M
	(e)	Construct the truth table and state diagram of SR Flip Flop.	2M
	(f)	Draw the circuit diagram of Ring counter.	2M
	(g)	What is meant by the term state-reduction?	2M
	(h)	What is state equation?	2M
	(i)	Define PLA. How it differs from PROM?	2M
	(j)	Differentiate between RAM and ROM.	2M

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

2	(a)	Simplify the Boolean expression to minimum number of literals: (A+B)' (A'+B').	4M
	(b)	Convert F(x) = x + y′z into canonical form.	6M
		OR	
3	(a)	Convert the following: (i) $(53.625)_{10}$ to $(X)_2$ (ii) $(3FD)_{16}$ to $(X)_2$ (iii) $(A69.8)_{16}$ to $(X)_{10}$	6M
	(b)	Implement Exclusive OR function involving three variables using only NAND function.	4M
4	(a)	Reduce the following function using K-Map. F(A, B, C, D, E) = Σm(1, 4, 8, 10, 11, 20, 22, 24, 25, 26) + d(0,12, 16, 17).	6M
	(b)	Design Full subtractor by using Universal Gates.	4M
		OR	
5	(a)	Explain the design procedure for multiplexers and draw the logic diagram of a 4-to-1 line multiplexer with logic gates.	5M
	(b)	Explain the working and functions of decoders.	5M
6	(a)	Design and implement 4-bit binary counter using D flip flop.	6M
	(b)	Explain a right shift register.	4M
		OR	
7	(a)	Design T Flip Flop using Logic Gates.	5M
	(b)	Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, use JK flip-flops.	5M
8	(a)	Explain in detail about moore and melay circuits.	5M
	(b)	Explain the relationship between the state table and ASM Chart.	5M
		OR	

Contd. In page 2

9	(a)	Construct Moore and Mealy state diagram that will detect input sequence 10110, when input pattern is detected, z is asserted high. Give state diagram for each state.	6M
	(b)	Explain the different methods of Race free state assignment.	4M
10	(a)	Explain different types ROMs.	5M
	(b)	Write a HDL model of the 4-bit binary to gray code converter.	5M
		OR	
11	(a)	Implement the following Boolean functions using PLA with 3 AND gates. F1 (ABC) = ∑ (3, 5, 7), F2 = ∑(4, 5, 7).	5M
	(b)	Discuss in detail about the FPGA with suitable diagrams.	5M

*****