

B.Tech II Year I Semester (R20) Supplementary Examinations April/May 2024

COMPUTER ORGANIZATION

(Common to CSIT, IT, AI&DS, CSE(AI), CSE(DS), CSE(AI&ML), CSE(IOT), CSE(CS) and CSE)

Time: 3 hours

Max. Marks: 70

PART – A
(Compulsory Question)

1 Answer the following: (10 X 02 = 20 Marks)

- | | |
|----------------------------------|----|
| (a) Define multiprocessor. | 2M |
| (b) What is full adder? | 2M |
| (c) Define fetch cycle. | 2M |
| (d) What is direct addressing? | 2M |
| (e) Define main memory. | 2M |
| (f) What is virtual memory? | 2M |
| (g) What is hardware interrupt? | 2M |
| (h) What is DMA? | 2M |
| (i) What is parallel processing? | 2M |
| (j) What is pipelining? | 2M |

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

- | | | |
|-----------|---|-----|
| 2 | Explain the role of stack in evaluating arithmetic expression. | 10M |
| OR | | |
| 3 | Explain various types of instruction formats with example. | 10M |
| 4 | Explain the design of multi-bus organization of CPU. | 10M |
| OR | | |
| 5 | How to represent floating point numbers in computer. | 10M |
| 6 | Describe virtual memory using demand paging. | 10M |
| OR | | |
| 7 | Explain mapping procedures to implement cache memory. | 10M |
| 8 | How DMA is used for bulk amount of data transfer between computer and peripheral devices? | 10M |
| OR | | |
| 9 | Explain asynchronous data transfer mechanisms. | 10M |
| 10 | Explain the role of array processors in parallel processing. | 10M |
| OR | | |
| 11 | Discuss about pipelining. | 10M |

B.Tech II Year I Semester (R20) Supplementary Examinations August/September 2023

COMPUTER ORGANIZATION

(Common to CSE (CS), IT, CSE, CSE (AI), CSE (AI&ML), AI&DS, CSE (IOT) and CSE (DS))

Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

- 1 Answer the following: (10 X 02 = 20 Marks)
- | | |
|---|----|
| (a) Draw the basic functional units of a computer. | 2M |
| (b) Compare Multi-Processor and uniprocessor. | 2M |
| (c) Define Instruction Format. | 2M |
| (d) Compute BCD Adder. | 2M |
| (e) Relate about virtual memory. | 2M |
| (f) Justify mapping procedures adopted in the organization of a Cache Memory. | 2M |
| (g) What is function of about DMA controller? | 2M |
| (h) Invent about Priority Interrupt. | 2M |
| (i) What are the major characteristics of a pipeline? | 2M |
| (j) What is parallel processing? | 2M |

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

- | | | |
|-----------|---|-----|
| 2 | (a) Explain about instruction cycle. | 5M |
| | (b) Organize any three best addressing modes with example. | 5M |
| OR | | |
| 3 | Prioritize different functional units of a computer. | 10M |
| 4 | (a) Perform arithmetic operation on binary using 2's complement representation:
(i). (+42) + (-13) (ii) (-42) – (-13). | 5M |
| | (b) Convert the following numbers with the indicated bases to decimal;
(i) (12121) ₃ (ii) (4310) ₅ (iii) (50) ₇ . | 5M |
| OR | | |
| 5 | (a) Describe the importance of encoders. | 5M |
| | (b) Evaluate floating point representation. | 5M |
| 6 | Examine the following:
(i) Memory mapped I/O.
(ii) I/O Registers.
(iii) Hardware Interrupts. | 10M |
| OR | | |
| 7 | (a) Compose associate memory with block diagram. | 5M |
| | (b) Determine mapping procedures of cache memory. | 5M |
| 8 | (a) Elaborate interrupt with suitable example. | 5M |
| | (b) Distinguish isolated versus memory. | 5M |
| OR | | |
| 9 | (a) Justify virtual memory and its importance. | 5M |
| | (b) Examine TLB with necessary diagram. | 5M |
| 10 | (a) Classify array processors. | 5M |
| | (b) Discover Interconnection structures. | 5M |
| OR | | |
| 11 | (i) Describe the data and control path techniques in pipelining
(ii) Prove inter processor communication | 10M |
