UNIT-V

TIMERS, PHASE LOCKED LOOPS & ~~D-A and A-D converters~~

Introduction:-

The 555 timer is basically a monolithic timer circuit and it is one of the most versatile linear integrated circuit devices in practical use.

Main features of IC 555 timer:-

1. The 555 timer, in IC form is available in 3 types of packages.
   * 8-pin metal can
   * 8-pin mini DIP and 14-pin DIP.
   * 14 pin DIP actually consists of 2 numbers of 555 timer fabricated on the same chip and is named as IC 556.

2. It is basically a monolithic timer device. It can be employed with advantage when accurate and highly stable time delays or oscillations are to be generated. Time delays ranging from a few microseconds to several hours are obtainable.

3. It has 2 operating modes: as monostable multivibrator and as astable multivibrator.

4. The supply voltage for the timer can vary over a wide range: 4.5V to 18V for the SE/NE 556 version and 2V to 18V for the TLC 555 version.

5. It has a high current output, and is capable of handling 200mA load current (both source and sink curve).

6. Operating temperature ranges from -55°C to +125°C for the SE 555 version, and from 0°C to 70°C for the NE 555 version.

7. The output of the IC 555 timer is compatable with both TTL and CMOS circuit.

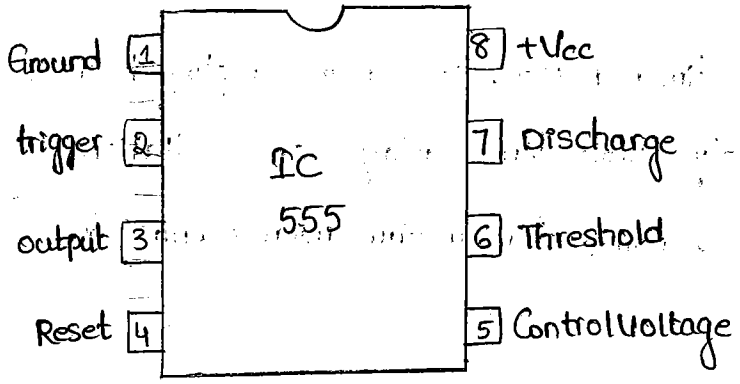
8. It has very good temperature stability.

9. like all general-purpose op-Amps, it is highly reliable in operation and is Easy to use.

10. Cost wise, it is cheap.

PIN Diagram of IC 555 timmer:-

The pin diagram of 8-pin mini DIP and 8-pin metal can packages.



1. Ground:-

All the voltages are measured with respect to this terminal.

2. Trigger:-

The external trigger pulse is applied to this terminal. The output voltage of the timer depends on the amplitude of the trigger pulse. If the voltage at this pin is greater than 2/3 Vcc (Vcc is the Supply Voltage), the output is low.

3. Output:-

When the trigger input is slight less than Vcc/3 Comparator-2 o/p is high. This output is given to reset input of R-S flip-flop.

For this pin the Load is Connected, It can be Connected in 2 ways.

1. Between pin 3 and ground
2. Between pin3 and pin8.

The load connected between pin 3 and 8 is termed as normally ON load, and the load connected between pin 3 and 1 is called normally off load.

* The current which is flows through normally ON load is called Sink Current.
* The current which is flows through normally off load is called Source Current.

for IC 555 timer, the peak value of source or sink current is 200mA.

4. Reset:-

This is an interrupt to the timing device.

When pin 4 is grounded, it stops the working of device and makes it off. Thus, pin 4 provides on/off feature to the IC 555 timer.

5. Control Voltage:-

This pin is nothing but inverting terminal of Comparator. An external voltage applied to this terminal controls the pulses width of the output waveform.

When an external voltage is applied to pin 5, both trigger and threshold voltages vary, and the result of that output voltage pulse width changes.

The pulse duration may also be controlled by means of a potentiometer connected between pin 5 and ground.

* If external input applied to pin 5 is alternating, then the reference level of Comparator 1 keeps on changing above & below $2/3\ V_{cc}$. Due to this, the variable pulse width output is possible. This is called pulse width Modulation.

6. Threshold:-

This forms the non inverting (+) input terminal of Comparator 1. When the voltage at this terminal exceeds the threshold voltage $2/3\ V_{cc}$, the output of Comparator 1 goes high, as a result of which the timer output goes to,

for threshold $> \frac{2}{3} V_{cc}$, flip-flop → set, Q → high, o/p - low.

for threshold $< \frac{1}{3} V_{cc}$, flip-flop → reset, Q → low, o/p →

7. Discharge:-

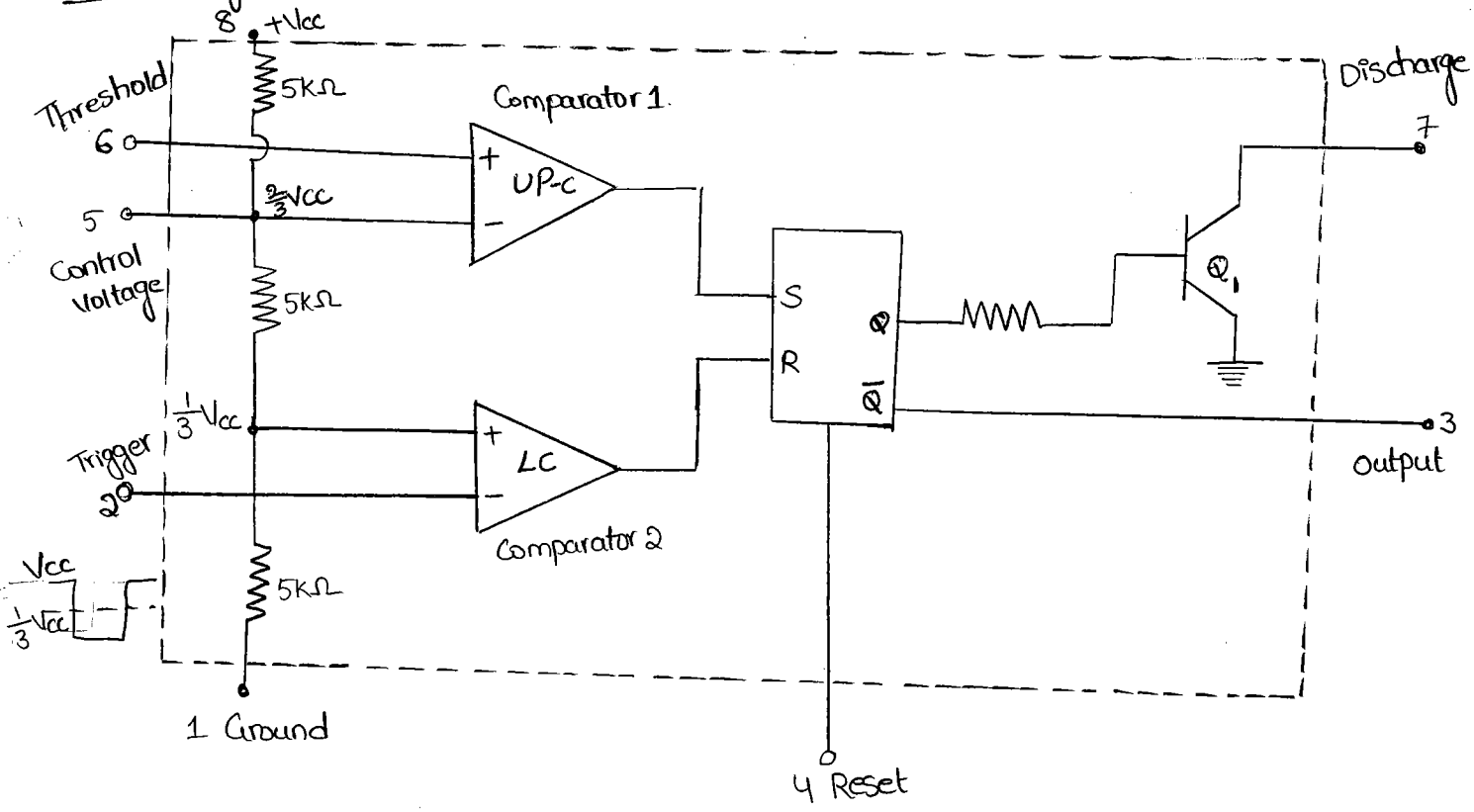
This pin is internally connected to the collector terminal of the discharge transistor Q_1.

During normal operation, when the timer output is high, Q_1 is cutoff, and when the output is low, Q_1 is saturated and it short circuits the external capacitor 'C' to be connected across it.

8. $+V_{cc}$ Supply:-

The supply voltage (ranging from 5V to 18V) is applied to this terminal. The voltage is with respect to ground.

Block diagram of IC 555 timer:-

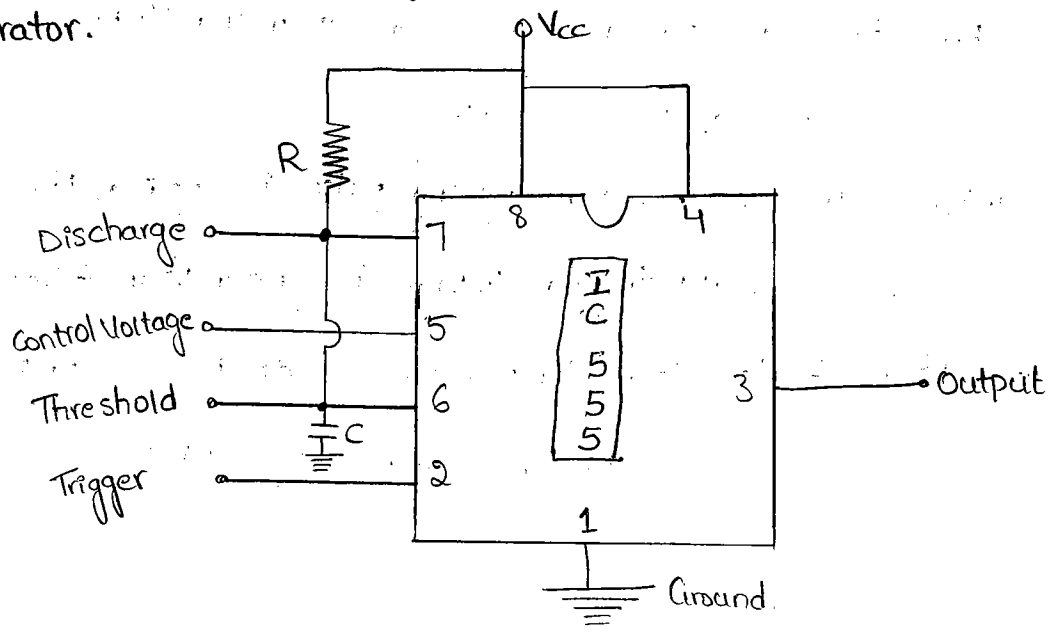


Monostable multivibrator Using IC 555:-

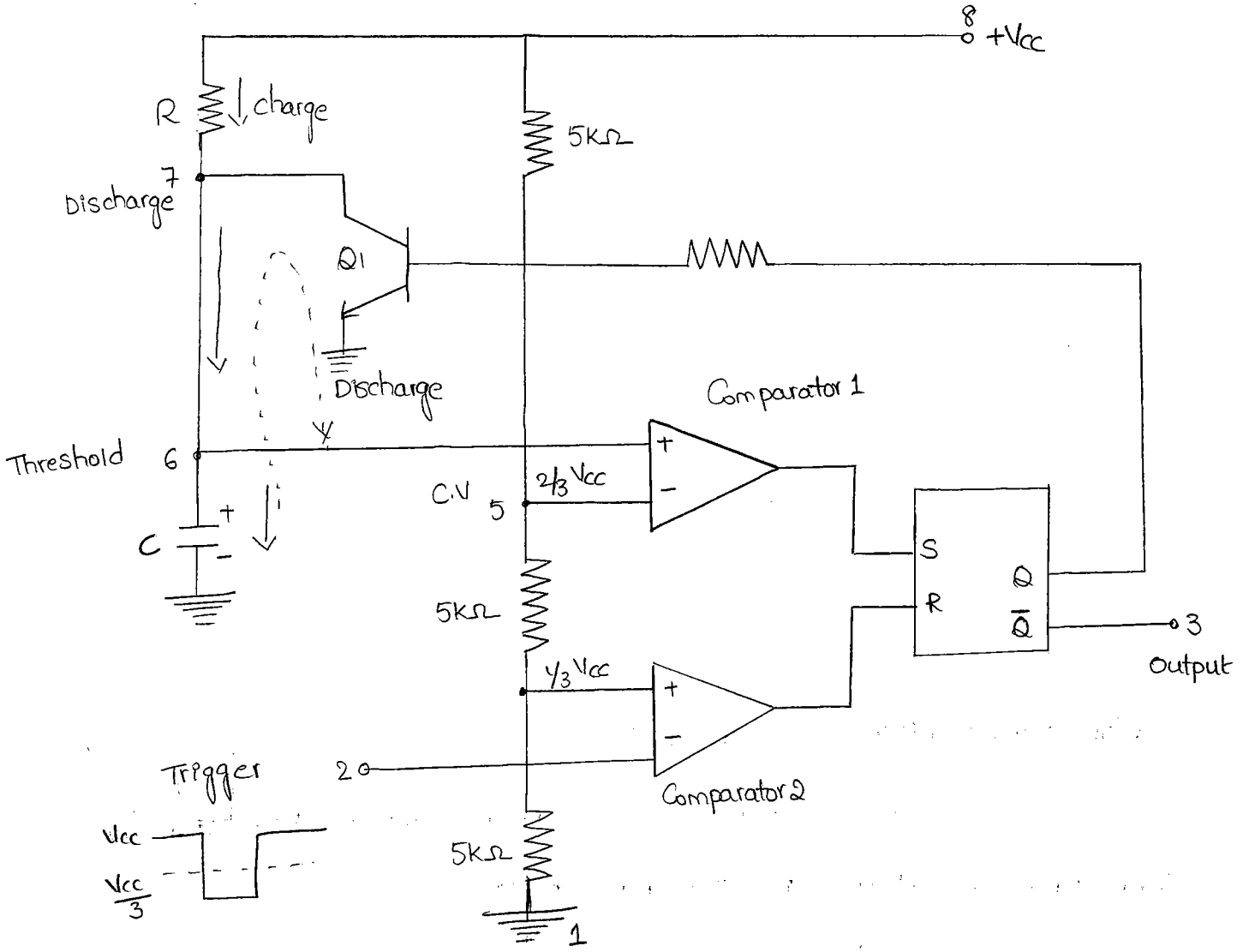
IC 555 Can be operated as a monostable multivibrator by Connecting an external resistor and capacitor.

The circuit has only one stable state. When trigger is applied, it produces a pulse at the output and return back to its stable state. The duration of the pulse depends on the values of R and C.

As it has only one stable state it is called one short multi-vibrator.



Monostable multivibrator Using 555 timer:-



Circuit operation:-

The flip-flop is initially set ie; S=1, Q=1 is high.

$\bar{Q}$=0

This drives the transistor Q_1 in Saturation.

Then the capacitor discharges Completely and Voltage across it is nearly zero. The output at pin 3 is low.

When a trigger i/p, a low going pulse is applied, then circuit state remains unchanged till trigger voltage is grater than 1/3 Vcc. when it becomes less than 1/3 Vcc, then Comparator 2 output goes high. This resets the flip-flop. So Q goes low and $\bar{Q}$ goes high. [Q=0 & $\bar{Q}$=1]

low Q makes the transistor Q_1 off. Hence capacitor starts charging through resistance R.

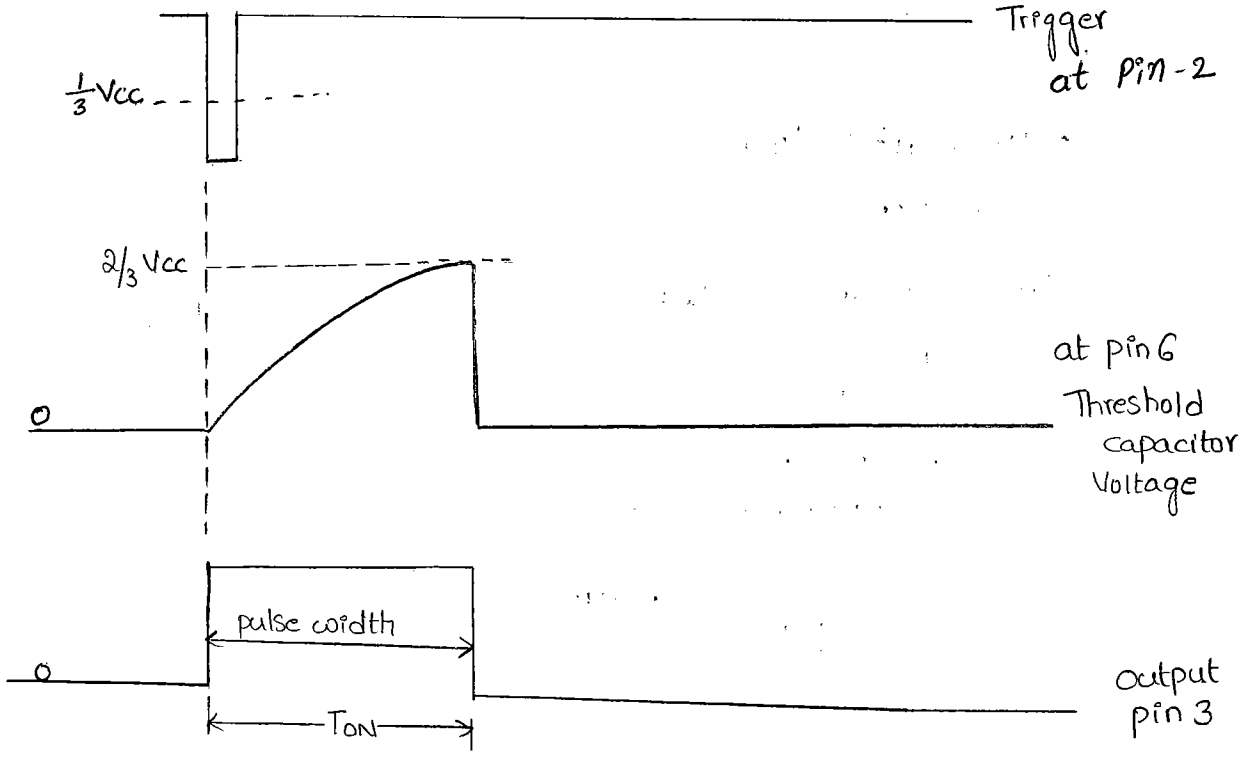
The voltage across capacitor increases exponentially. The voltage is nothing but the threshold voltage at pin 6. When this voltage becomes more than $\frac{2}{3}V_{cc}$, then Comparator 1 output goes high. This sets the flip-flop.

ie; Q becomes high and $\bar{Q}$ is low. This high Q drives the transistor Q_1 in Saturation. Thus capacitor 'C' quickly discharges through Q_1.

* So it can be noted that Vout at pin 3 is low at start, when trigger is less than $\frac{1}{3}V_{cc}$ it becomes high and when threshold is grater than $\frac{2}{3}V_{cc}$ again becomes low, till next trigger pulse occurs.

* So a rectangular coave is produced at the output. The pulse width of the rectangular pulse is Controlled by the charging time of capacitor. This depends on the time constant RC. Thus RC Controls the pulse.

Wave forms of monostable operation:-



Derivation of pulse width:

The voltage across capacitor increases exponentially.

$$V_c = V(1 - e^{-t/RC})$$

$$V_c = \frac{2}{3} V_{cc}$$

$$\frac{2}{3} V_{cc} = V_{cc}(1 - e^{-t/RC})$$

$$\frac{2}{3} V_{cc} - V_{cc} = -V_{cc} e^{-t/RC}$$

$$\left(\frac{2}{3} - 1\right) V_{cc} = -e^{-t/RC} \times V_{cc}$$

$$-\frac{1}{3} V_{cc} = -(e^{-t/RC}) V_{cc}$$

$$-(e^{-t/RC}) = -1/3$$

$$e^{-t/RC} = 1/3$$

$$e^{-t/RC} = 1/3$$

$$\ln(e^{-t/RC}) = \ln\left(\frac{1}{3}\right)$$

$$\frac{-t}{RC} = \ln\left(\frac{1}{3}\right)$$

$$t = RC \ln\left(\frac{1}{3}\right)$$

$$t = 1.1RC$$

* Design monostable multivibrator using 555 timer to produce a pulse width of 100msec.

pulse width $T = 100msec$

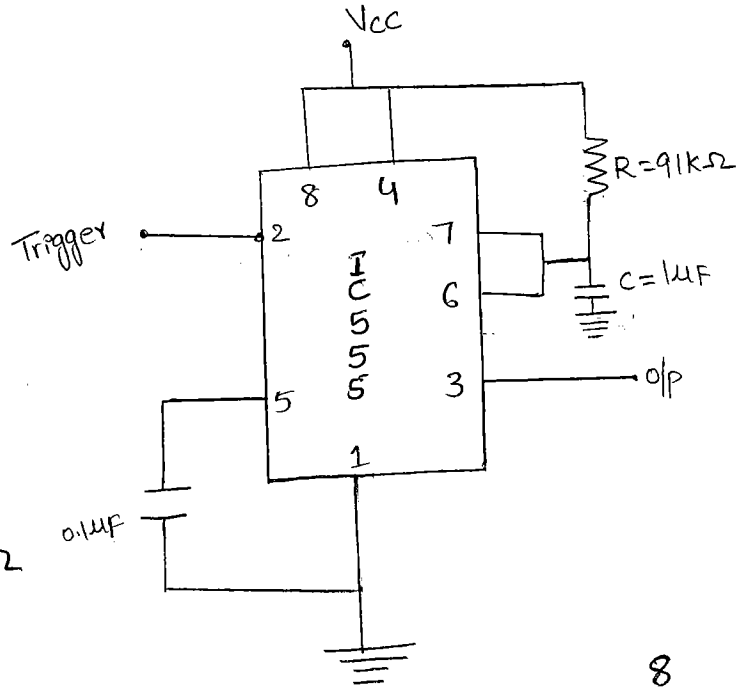
$T = 1.1RC$

Let us assume $C = 1\mu F$

$$R = \frac{T}{1.1 \times C}$$

$$R = \frac{100 \times 10^{-3}}{1.1 \times 1 \times 10^{-6}} = \frac{10^{-1}}{11 \times 10^{-7}}$$

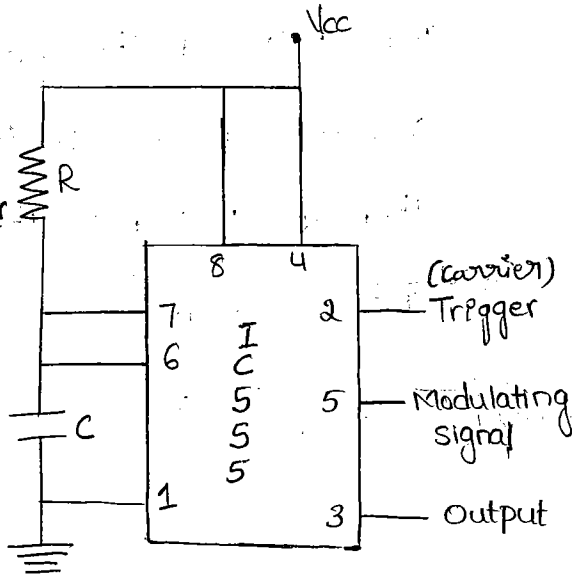
$$R = \frac{1}{11 \times 10^{-6}} = 90.91K\Omega$$



Applications of monostable multivibrator:-

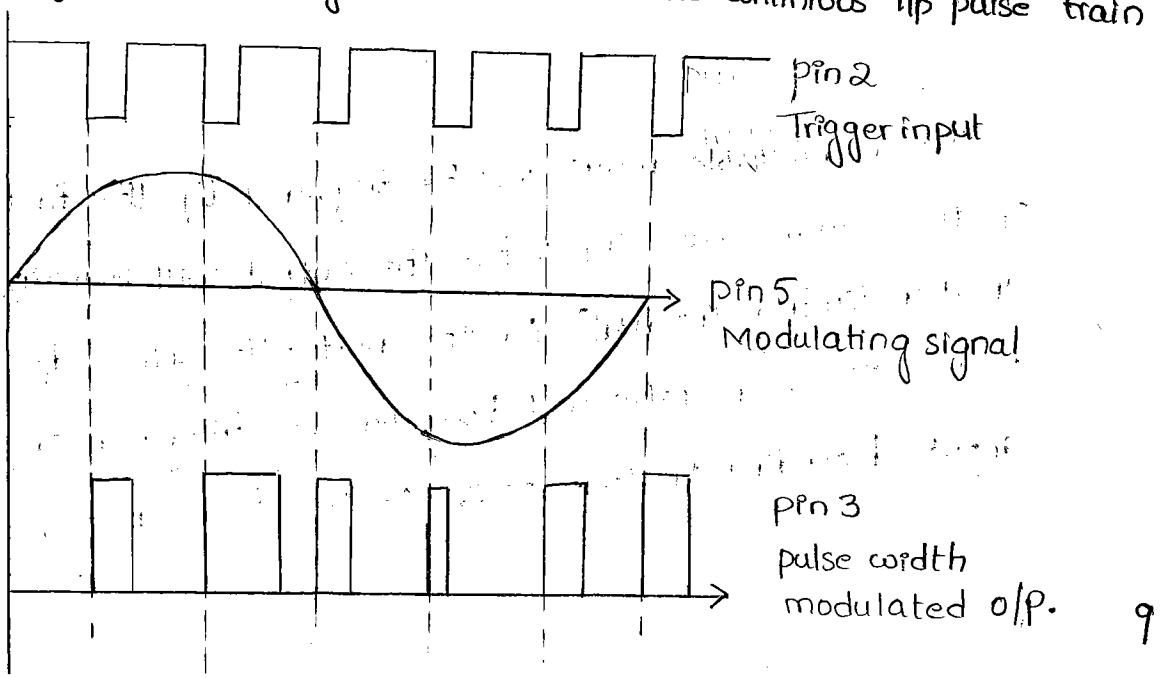
1. pulse width modulation
2. frequency divider
3. pulse stretching
4. linear Ramp generator
5. Missing pulse detector.

pulse width modulation:-



It is basically a monostable multivibrator with a modulating input signal applied at the Control input (pin5). By the application of Continious trigger at pin2 a series of output pulses are obtained, the duration of ~~output~~ pulse width depends on the modulating input at pin 5.

The modulating signal at pin 5 gets Super imposed upon the already existing voltage 2/3 Vcc at the inverting input terminal of Comparator 1. This intern changes the threshold level of the Comparator 1 and the Output pulse width modulation taken place. There the duty cycle Only Varies keeping the frequency same as that of the Continious i/p pulse train trigger.

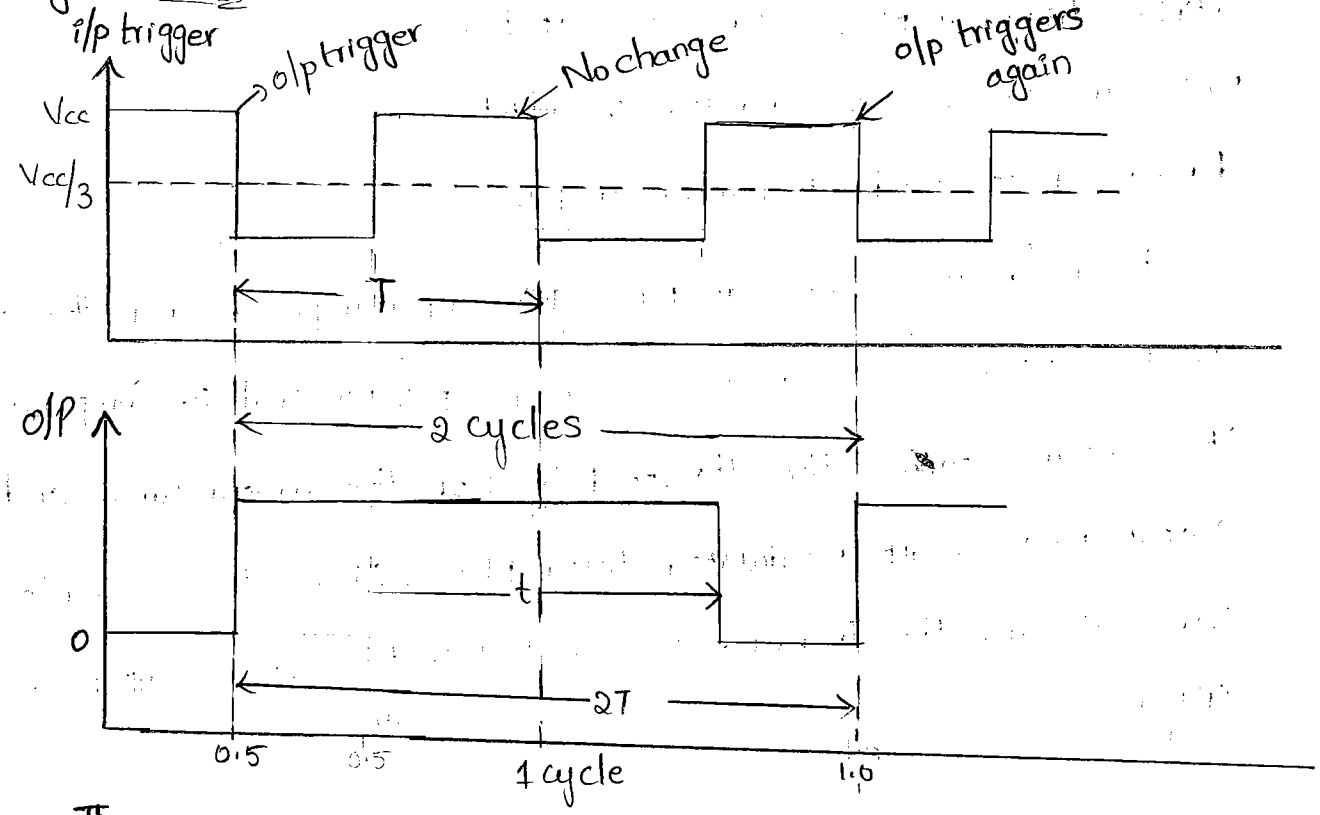


from the output waveform that the pulse duration varies according to the modulating signal level, but the frequency of the output pulses is same as that of the trigger input signal.

frequency divider:-

Monostable multivibrator, application of trigger pulse gives a positive going pulse on the output. The same monostable circuit can be used as a frequency divider. If the timing circuit interval is adjusted to be longer than the period of the input signal.

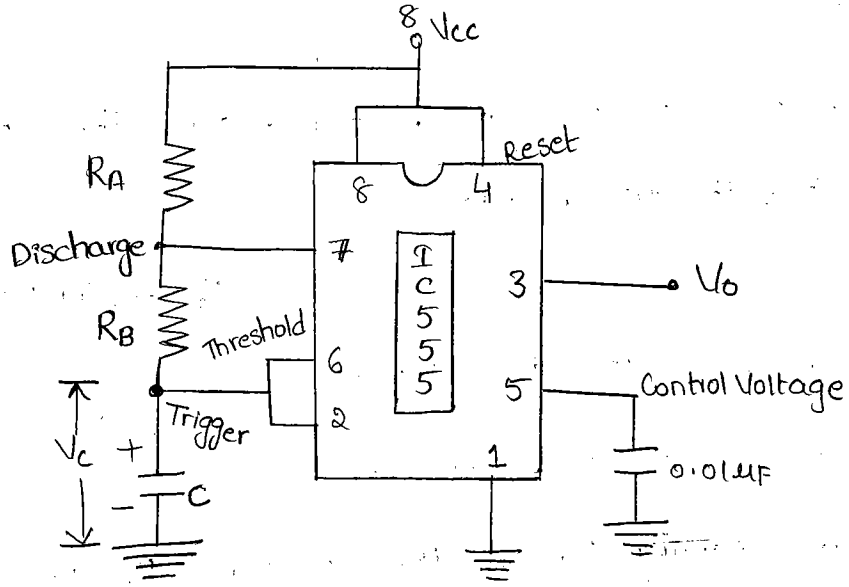
Input & output waveforms of the monostable multivibrator as a divided by 2-circuit:-



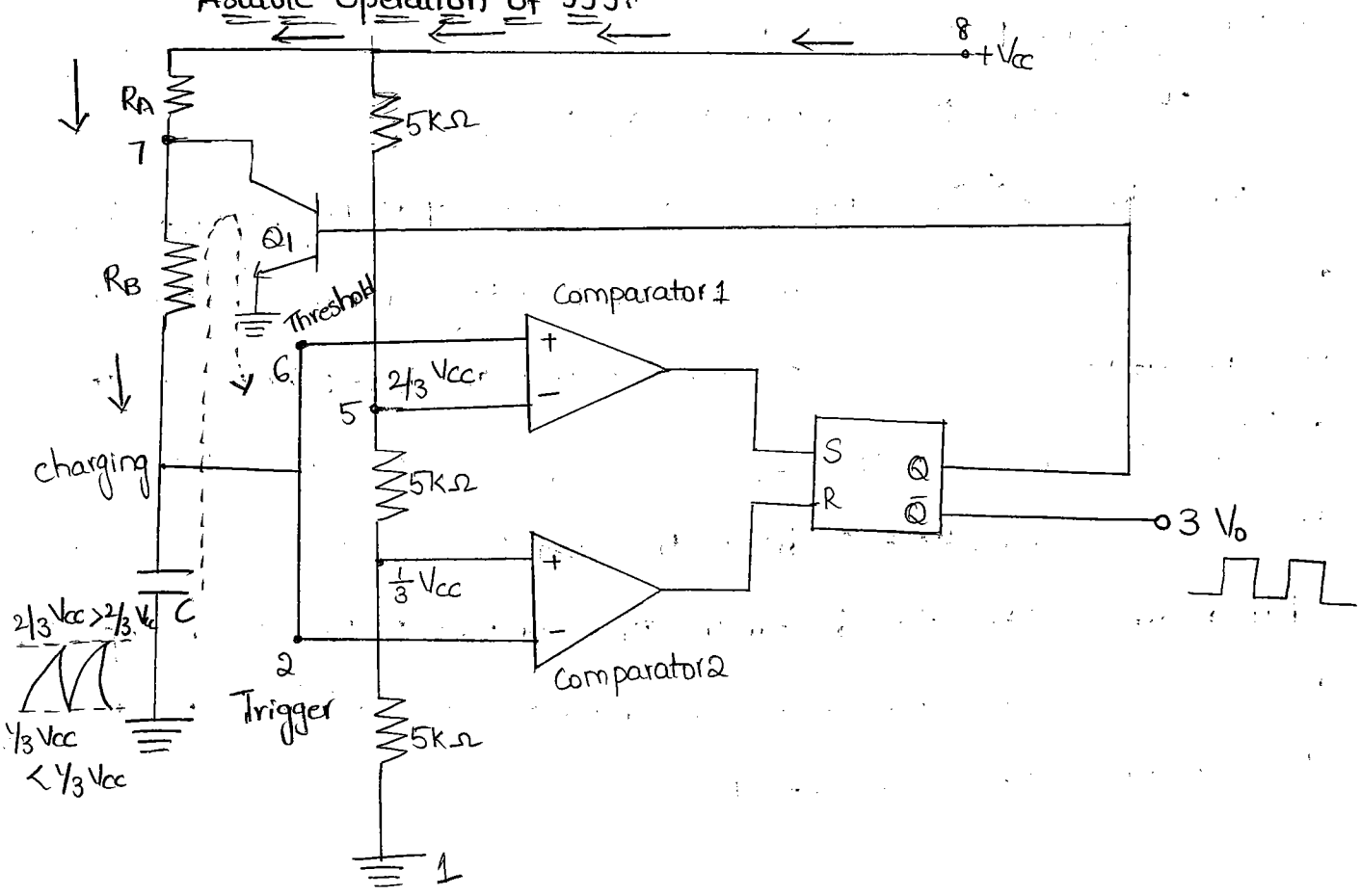
The monostable multi will be triggered by the first -ve going edge of the square wave input but the output will remain high (because of greater timing interval) for the next -ve going edge of the i/p square wave. The monostable will however be triggered on the 3rd -ve going input depending on the choice of the time delay.

Astable multivibrator using 555 timer:-

IC 555 timer can be Connected as a Astable multivibrator. The threshold is connected to the trigger input. Two external resistances R_A, R_B and a capacitor 'C' is used in the circuit.



Astable Operation of 555:-



Circuit Operation:-

The circuit has no stable state. The circuits changes its state alternately. Hence the operation is called free running (non-sinusoidal) oscillator.

$S=1, Q=1$ o/p = low.

* when the flip-flop is set, Q is high which drives the transistor Q_1 in saturation and the capacitor gets discharged. Now, the capacitor voltage is nothing but the trigger voltage.

While discharging when it becomes less than $1/3\ V_{cc}$, Comparator 2 output goes high. This resets the flip-flop. Hence Q goes low & $\bar{Q}$ goes high.

The low Q makes the transistor off.

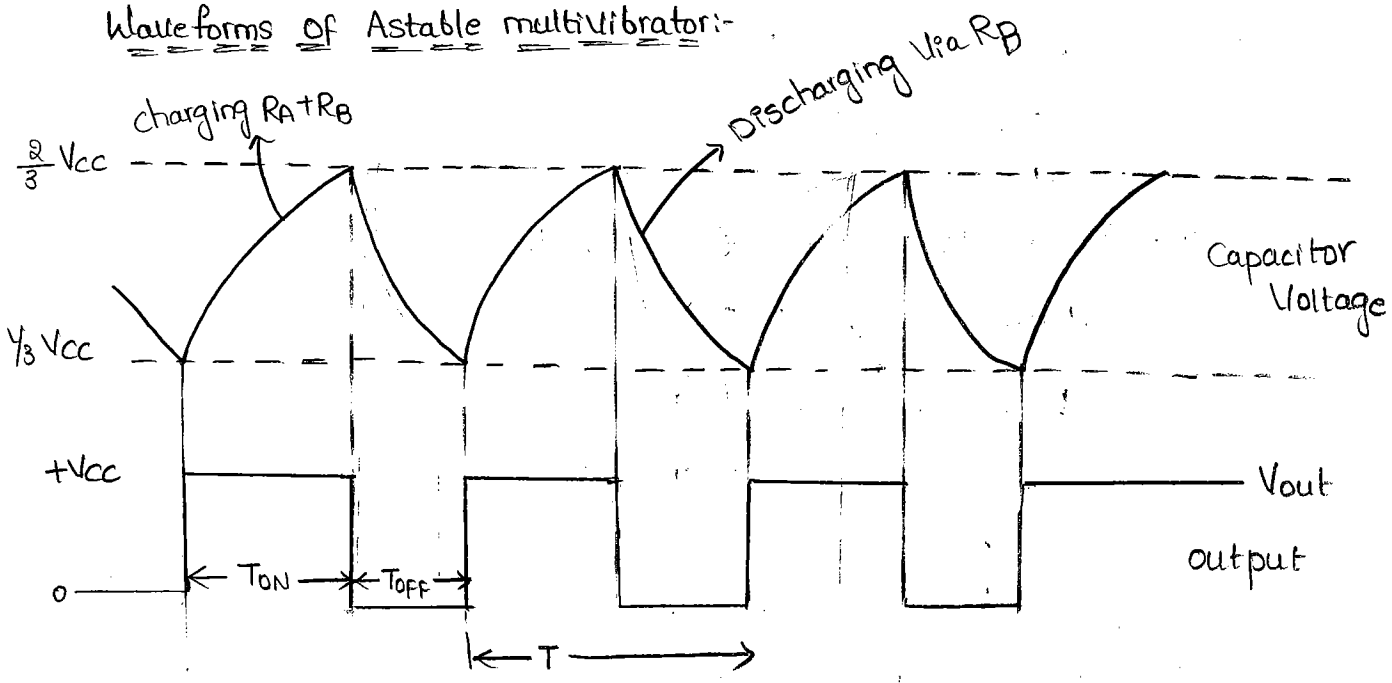
Thus capacitor starts charging through the resistance R_A, R_B and V_{cc}. The charging path is shown by the thick arrows. As total, resistance in the charging path is (R_A+R_B),

The charging time constant is $(R_A+R_B)C$.

Now the capacitor voltage is also a threshold voltage. while charging, capacitor voltage increases ie; the threshold voltage increases. when it exceeds $2/3\ V_{cc}$, then the Comparator 1 output goes high which sets the flip flop. The flip-flop output Q becomes high. and output at pin 3. ie; $\bar{Q}$ becomes low. High Q drives transistor Q_1. This path is shown by dotted arrows. Thus the discharging time constant is R_BC. when capacitor voltage becomes less than $1/3\ V_{cc}$, Comparator 2 output goes high, resetting the flip-flop. This cycle repeats.

Thus when capacitor is charging output is high, while when it is discharging the output is low. The output is a rectangular wave. The capacitor voltage is exponentially rising and falling.

Waveforms of Astable multivibrator:-



Duty cycle:-

Generally the charging time constant is grater than the discharging time constant. Hence at the output, the wave form is not symmetric. The high output remains for longer period than low output.

Duty cycle:- It is defined as the ratio of ON time ie; high output to the total time of one cycle.

ω = time for output is high = T_{ON}

T = time of one cycle.

D = Duty cycle = ω/T

$$\% D = \frac{\omega}{T} \times 100\%$$

Capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by.

$$V_c = V_{cc}(1-e^{-t/RC})$$

The time t_1 taken by the ckt to charge from 0 to $\frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}(1-e^{-t_1/RC})$$

$$\frac{2}{3}V_{cc} - V_{cc} = -V_{cc}e^{-t_1/RC}$$

$$-\frac{V_{cc}}{3} = -V_{cc}e^{-t_1/RC}$$

$$\boxed{t_1 = 1.09\,RC}$$

and the time t_2 to discharge from 0 to $\frac{1}{3}V_{cc}$ is

$$\frac{1}{3}V_{cc} = V_{cc}(1-e^{-t_2/RC})$$

$$\frac{1}{3}V_{cc} - V_{cc} = -V_{cc}e^{-t_2/RC}$$

$$-\frac{2}{3}V_{cc} = -V_{cc}e^{-t_2/RC}$$

$$\boxed{t_2 = 0.405\,RC}$$

So, the time to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ is

$$t_{ON} = t_{High} = t_1 - t_2$$

$$t_{ON} = t_{High} = 1.09RC - 0.405RC$$

$$\boxed{t_{ON} = 0.69\,RC}$$

for the given ckt $\boxed{t_{ON} = 0.69(R_A + R_B)C}$

* The output is low while the capacitor discharges from $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$ and the voltage across the capacitor is given by

$$\frac{2}{3}V_{cc}e^{-t/RC} = \frac{1}{3}V_{cc}$$

$$t = 0.69RC$$

for given ckt $\boxed{t_{low} = 0.69R_BC}$

R_A & R_B are in the charge path, but only R_B is in the discharge path.

$$T = t_{high} + t_{low}$$

$$T = 0.69(R_A + R_B)C + 0.69R_BC$$

$$T = 0.69(R_A + 2R_B)C.$$

$$f = \frac{1}{T} = \frac{1}{0.69(R_A + 2R_B)C}$$

$$\text{Duty cycle } \%D = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

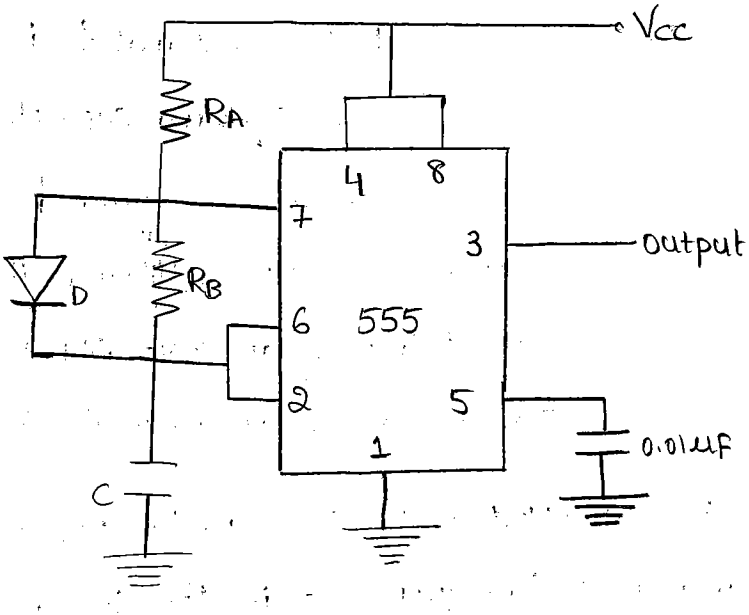
$$\%D = \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C} \times 100$$

$$\%D = \frac{R_A + R_B}{R_A + 2R_B} \times 100.$$

* If R_A is much Smaller than R_B, Duty cycle approches to 50% and o/p waveform approches to square wave.

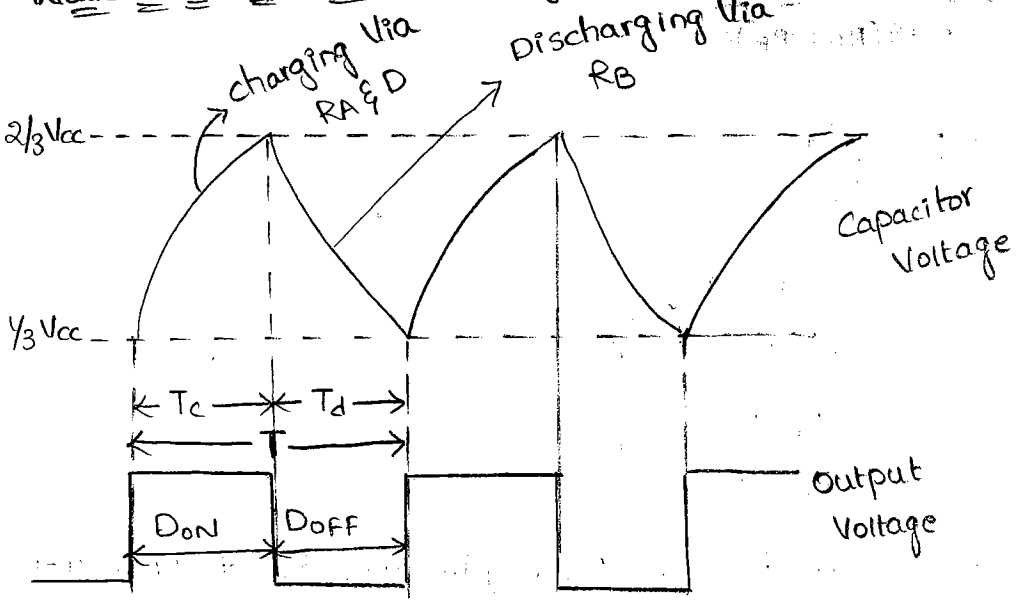
Applications of Astable multivibrator:-

1. Square wave generator:-



* To get exactly 50% Duty cycle ie; square wave o/p it is necessary to modify the astable timer ckt. In the modified circuit, the capacitor 'C' charges through R_A and diode 'D' and discharges through R_B. To obtain square wave (50% duty cycle) resistance R_B is adjusted such that it is equal to the Summation of resistance R_A and the forward resistance of diode 'D'. Usually, potentiometer is used for exact adjustments of resistors.

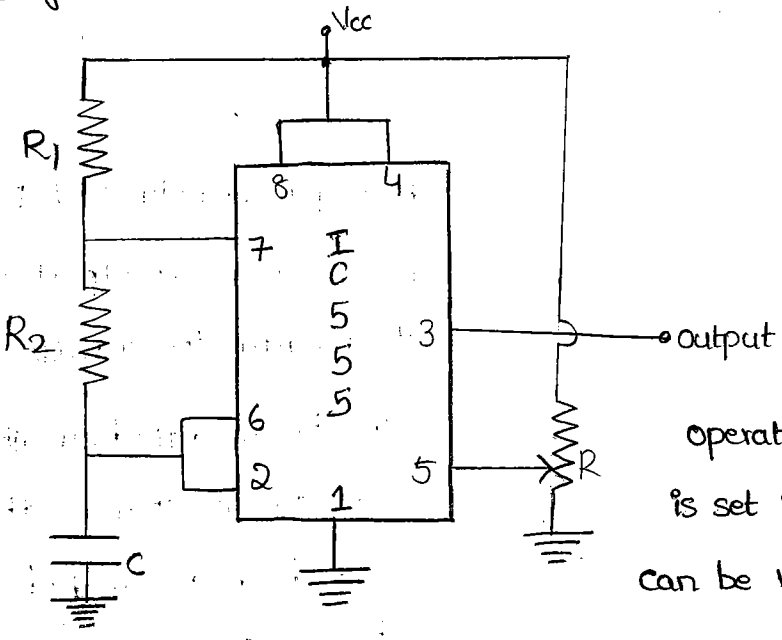
Waveforms of Square wave generator:-



$T_c = T_d$

$\% D = 50\%$

Voltage Controlled oscillator (VCO):-



R = External Variable resistor

R_1, R_2 → External field resistors

C → External capacitor

In an IC 555 timer device operating as astable multivibrator the voltage is set initially at 2/3 Vcc. This voltage can be varied externally also by a suitable mechanism. When the control voltage is changed, the upper threshold voltage changes and as a consequence of it, the time needed for the capacitor to charge to the set value of the upper threshold voltage also changes. Also for the same reason, the discharge time changes. A change of charging and discharging times implies that the time period changes. This changes the frequency of the output voltage.

Thus we see that the frequency of the output voltage of an astable multivibrator using IC555 can be controlled by varying the control voltage externally.

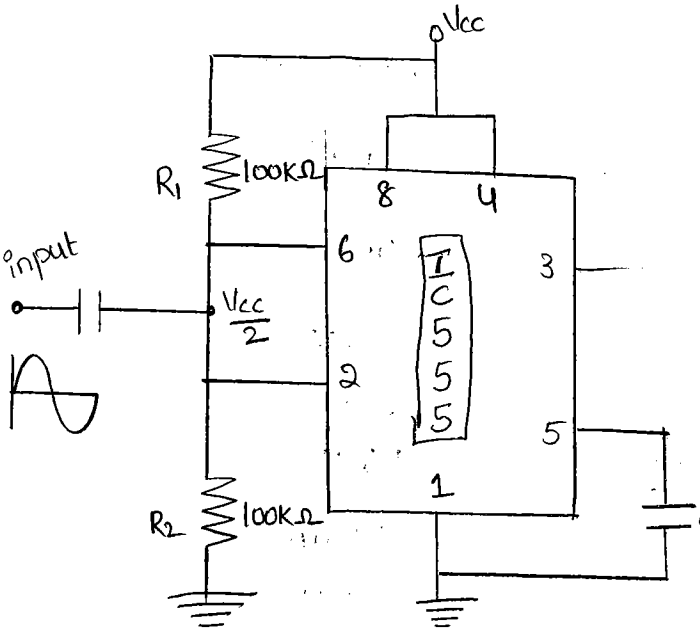
In practice the Control Voltage is changed externally by means of a potentiometer arrangement.

A Variable resistor 'R' Connected between Vcc and ground supplies the necessary external Control Voltage, and this is applied to the Control Voltage terminal of the timer device, thus charging the upper threshold Voltage.

Let the Control Voltage be increased. This increases the upper threshold Voltage ($> \frac{2}{3} V_{cc}$). Hence the capacitor charging time and discharging time increases. The time period 'T' of the output Voltage increases, and as a result the frequency of oscillations 'f' would decreases ($f = \frac{1}{T}$).

* Thus the output frequency can be Controlled by means of Control Voltage Variations by external mechanism.

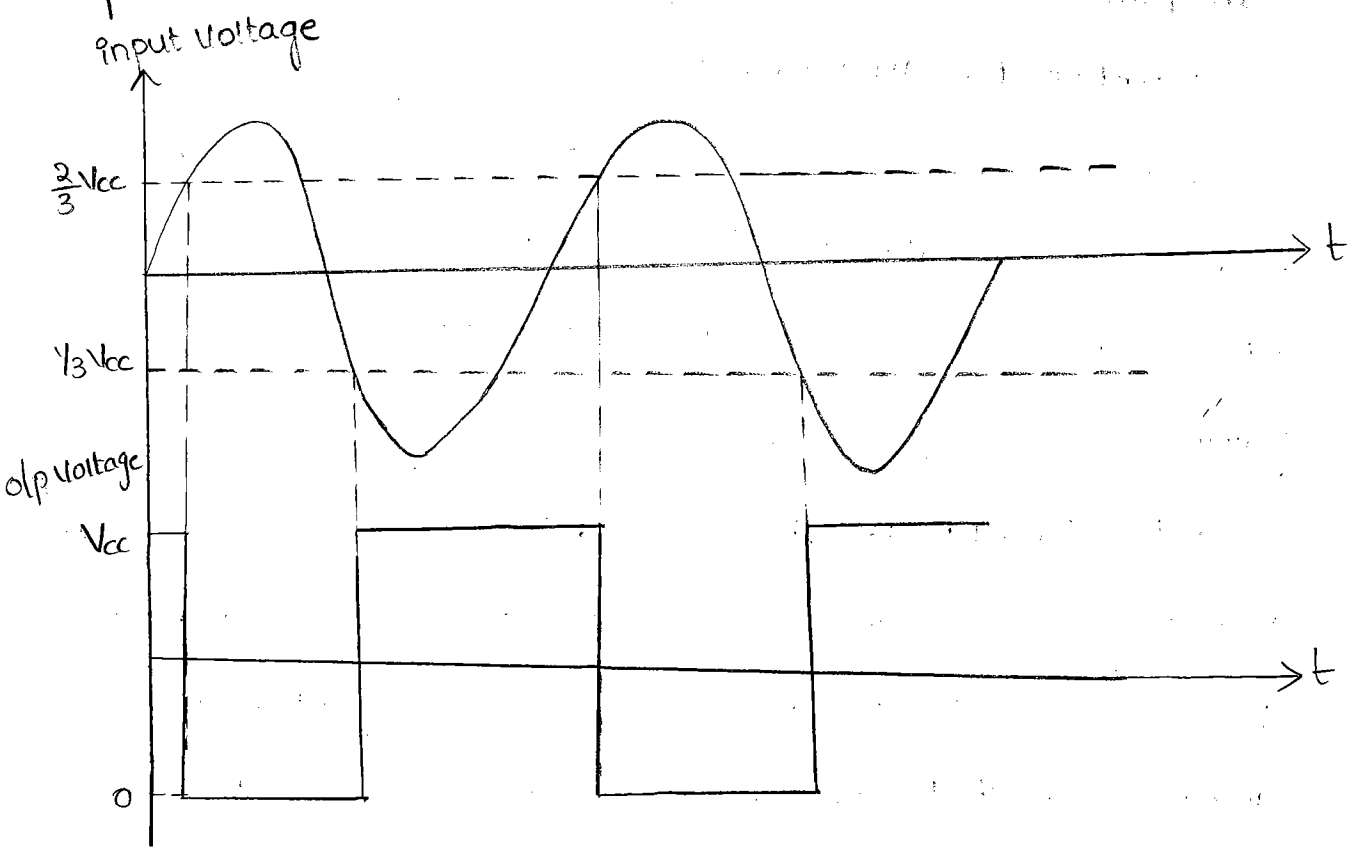
555 timer as a schmitt trigger:-



An astable multivibrator can be converted in to regenerative Comparator ie; schimitt trigger, by joining the 2 internal Comparators together (pin 6 & 2) and biasing them at $\frac{V_{cc}}{2}$ by a potential division network Consisting of equal resistors. The input signal is applied at the Common point.

When the input signal makes the input level reach $\frac{2}{3} V_{cc}$, the threshold Comparator trips making the output Low. Similarly, the trigger Comparator switches the output to high when the input signal level goes down to $\frac{1}{3} V_{cc}$. Thus a sine wave input of Sufficient

amplitude results in a square wave output.



Specifications of 555 timer:-

Supply Voltage	18V
power dissipation	600mw
Typical Values at T=25°c	SE555
Supply Voltage	4.5 to 18 V
Supply current (for V_{cc}=15V, $R_L=\infty$)	3mA
Supply current (V_{cc}=15V, $R_L=\infty$)	10mA
Threshold Voltage	$\frac{2}{3}V_{cc}$
Trigger Voltage (for V_{cc}=15V)	5V
(for V_{cc}=5V)	1.67V
Trigger current	0.5μA
Reset Voltage	0.7V
Reset Current	0.1mA
Current Voltage level : For V_{cc}=15V	10V
V_{cc}=5V	3.33V
Output Voltage (low)	0.1V
Output Voltage (high)	12.5V

phase locked loop (PLL):-

phase locked loop is abbreviated as PLL,

* Basically PLL is a closed loop system which is designed to lock the output frequency and phase to the frequency and phase of the i/p signal.
* PLL's are available in monolithic IC form and hence they are in expensive, and are extensively used in modern Communication systems.

They are used in applications such as.

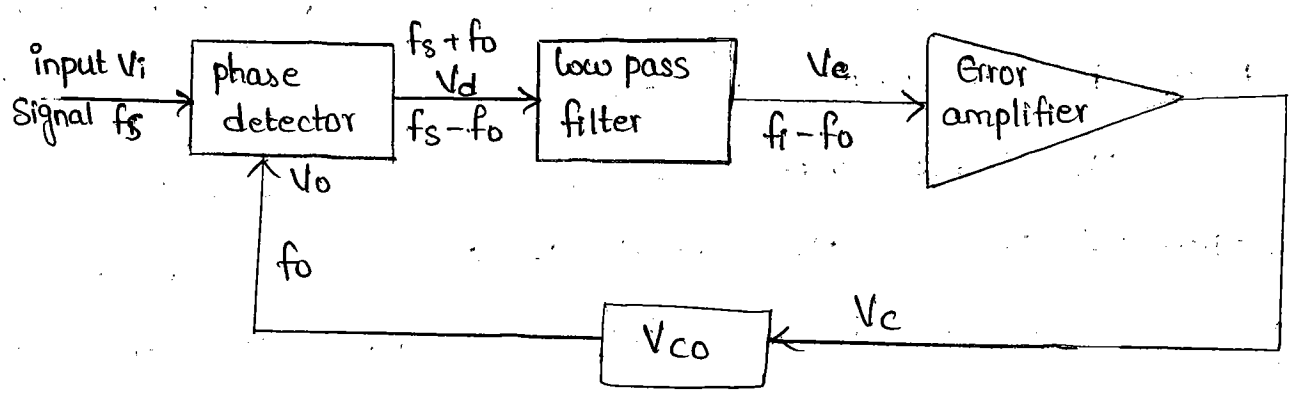
* frequency synthesis
* frequency modulation / demodulation
* AM detection
* Tracking filters
* FSK demodulator
* Tone detector

* In the PLL the output frequency (Vco) is compared with the input frequency and adjusted until its is equal to it. The input voltage is thus tracked and locked, hence the name phase locked loop.

Block diagram of PLL:-

Block diagram of PLL Consists of

1. phase detector
2. Low pass filter
3. Error amplifier
4. Voltage controlled oscillator (Vco).



* phase detector:-

The circuit has 2 input terminals. The signal to be processed (V_i) is given to one of the inputs, the second input is fed by the reference signal V_o. It compares the phase and frequency of the 2 inputs.

If the 2 signals differ in frequency or/and phase, an error voltage V_d is generated. It is basically a multiplier circuit and produces the sum $f_i + f_o$ and difference $f_i - f_o$ frequencies and dc component.

Low pass filter:-

It is an active low-pass. It removes the high frequency component ($f_s + f_o$) from its input and passes the difference frequency signal ($f_s - f_o$). When $f_i = f_o$, it eliminates $2f_o$ and passes only the dc signal.

Error amplifier:-

Differency frequency component ($f_i - f_o$) & dc signal is amplified.

Voltage Controlled Oscillator:-

It is a free running oscillator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can be shifted to either side by applying a dc control voltage V_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence

The input for voltage Controlled oscillator is output of error amplifier (V_c). The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts the signal is said to be in capture range.

The Vco continious to change frequency till its output frequency fo is exactly the same as the input signal frequency fi. The circuit is then said to be locked. once locked the output frequency fo at Vco is identical to fs except for a finite phase difference ϕ. This ϕ generates a corrective control voltage Vc to shift the Vco frequency fo ato fs and there by maintain the lock once locked PLL tracks the frequency changes of the input signal.

If the frequency of the input signal suddenly changes (say increases by Δf_i) at a particular instant (say t=0), the phase of the input signal starts leading the phase of the reference signal.

The phase error increases with time. The phase detector ϕ_d develops a signal V_d which also increases with time. As a result the output of the filter V_c will also increases. This causes the Vco to increase its frequency

The phase error becomes small now and after some settling time, the Vco will oscillate at a frequency that is exactly the frequency of the input signal.

The Vco now operates at a frequency which is grater than its free running frequency by Δf. If this tracks the frequency of the incomming signal and lock in.

Thus we see that, a PLL passes through 3 states during its normal operation: free running state, capture state and phase-locked state.

Lock in range:-

Once the PLL is locked, it can track frequency of the incoming signal. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock in range or tracking range.

Capture range:-

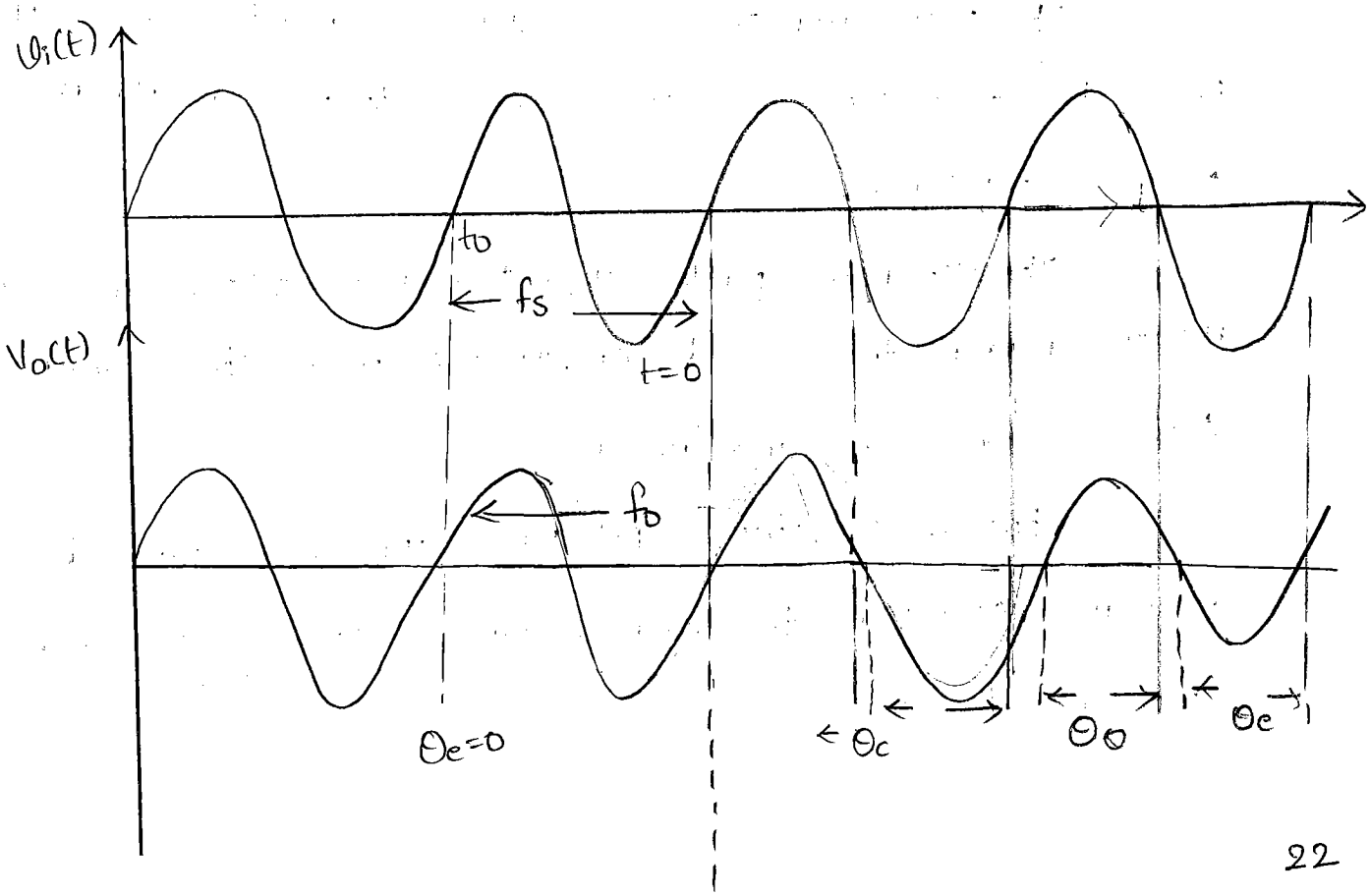
The range of frequencies over which PLL can acquire lock with an input signal is called the capture range.

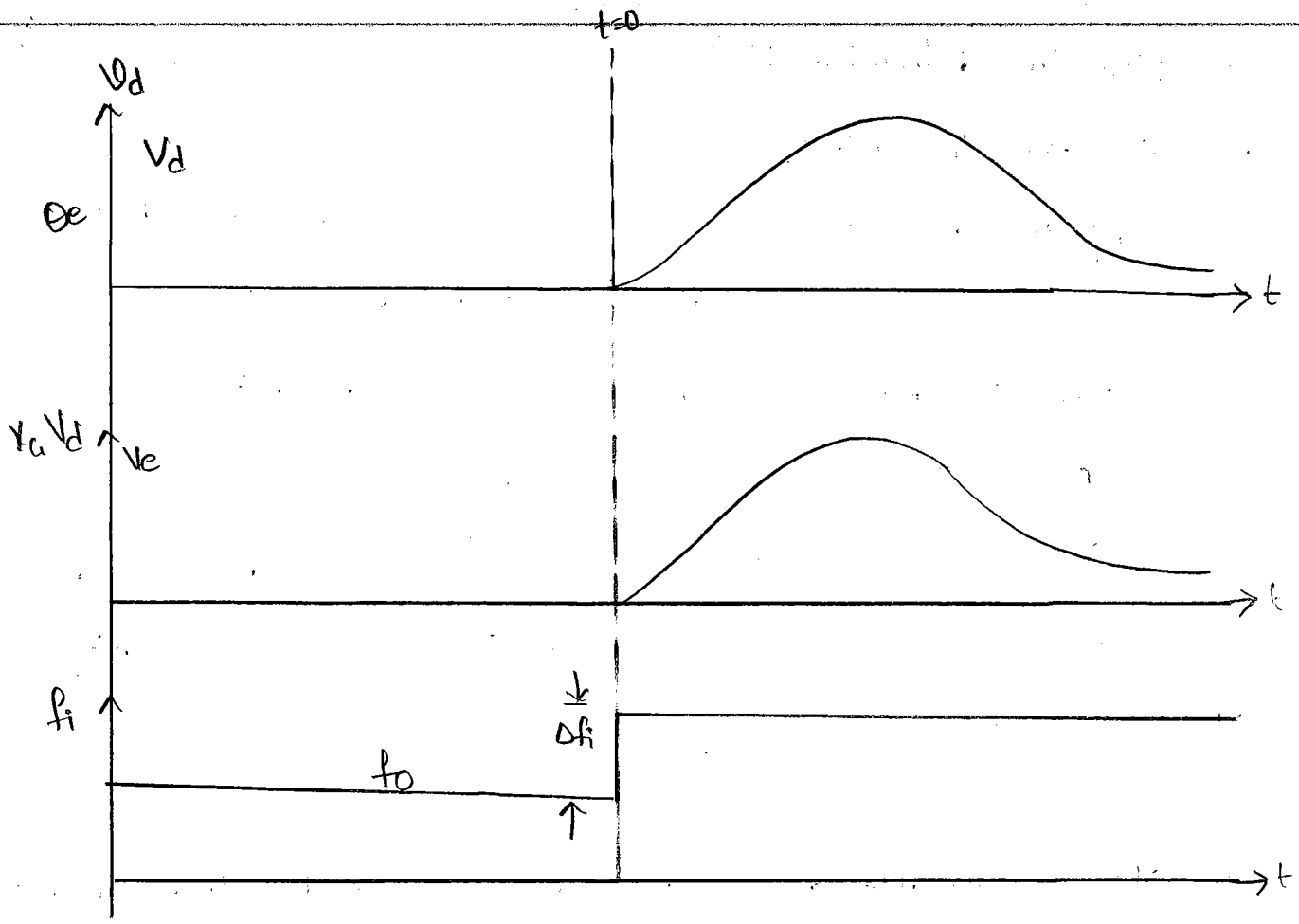
This is also expressed as % of f_0.

Pull in time:-

The total time taken by the PLL to establish lock is called pull in time. This depends on the initial phase and frequency difference between the 2 signals as well as on the overall loop gain & loop filter.

PLL Action:-





Simple explenation for Voltage Controlled oscillator:-

Intially the PLL is in the free running state, when the output of amplifier is applied to Vco as its Control Voltage, based on the Control Voltage the Vco shifts its frequency in order to make it equal to input frequency. During this action, the PLL is said to be in capture mode, Once the output frequency of Vco becomes equal to frequency of i/p signal, $f_{in} - f_{out} = 0$. In this Condition the PLL is said to be in locked mode. In the locked state the PLL tracks the frequency of input signal.

This cycle repeats and the PLL tracks the changes in input frequency (ie; for various inputs).

565 phase locked loop (565 PLL)

Monolithic phase locked loop:-

All the different blocks of PLL are available as independent IC packages and can be externally inter connected to make a PLL.

Monolithic PLL's are SE/NE 560 series introduced by signetices and LM 560 series by national semiconductor.

The SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges.

565 PLL:-

This is available as a 14 pin DIP package and as to pin metal can package the output frequency at the Vco.

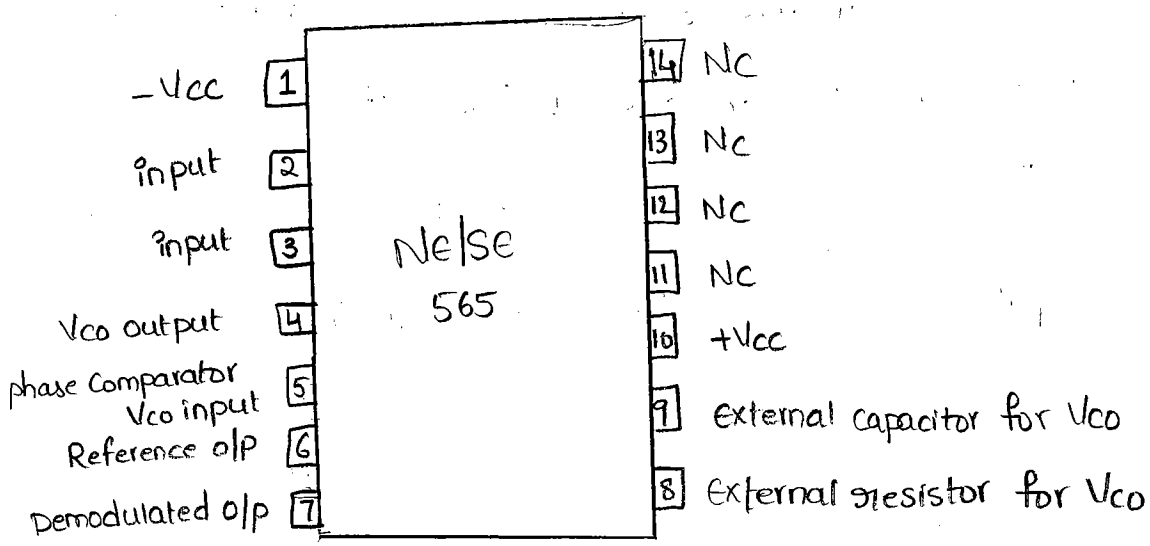
$$f_0 = \frac{1.2}{4R_TC_T} \text{ Hz.}$$

R_T, C_T = External resistor & Capacitor

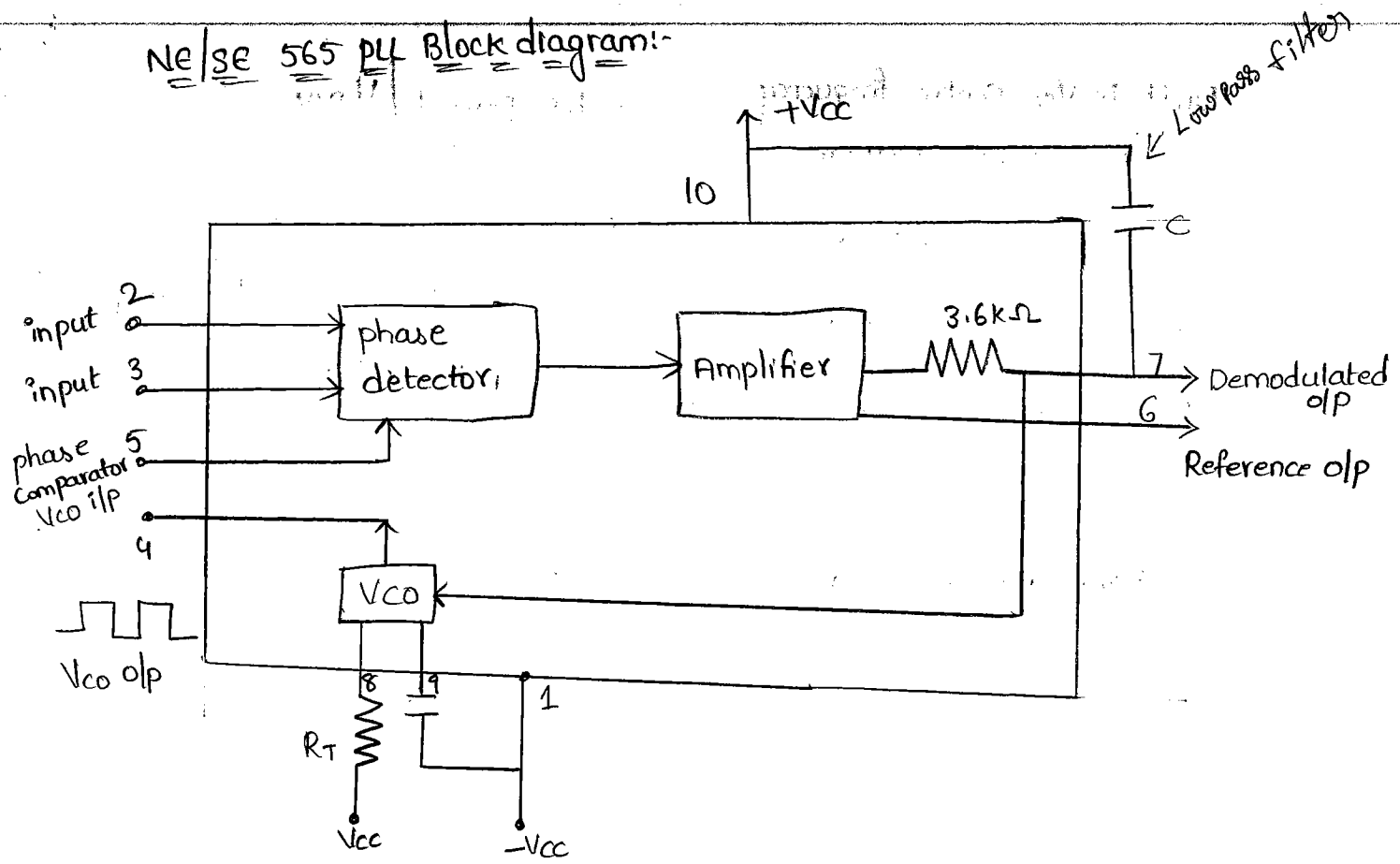
R_T = between 2kΩ & 20kΩ.

The Vco free running frequency is adjusted with R_T & C_T to be at the centre of the input frequency range.

pin diagram



NE/SE 565 PLL Block diagram:-



The phase locked loop is internally broken between the Vco o/p and the phase Comparator input. A short ckt between pins 4 and 5 Connects the Vco output to the phase Comparator so as to Compare fo with i/p signal fs.

A Capacitor 'c' is Connected between pin 7 and pin 10 to make a LPF with the internal resistance of 3.6kΩ

Conversion ratio of the phase detector of 565 PLL as $k\phi = \frac{0.7-(-0.7)}{\Pi} = \frac{1.4}{\Pi}$

Electrical parameters of 565 PLL are:-

Operating frequency range	: 0.001 Hz to 500kHz
Operating voltage range	: ±6V to ±12V
input level	: 10mV rms min to 3V p-p max
input impedance	: 10kΩ typical
Output Sink Current	: 1mA. typical
Drift in Vco Centre frequency with temperature	: 300 ppm/°c. (parts per million per degree Centigrade)

Drift in Vco Centre frequency with Supply Voltage : 1.5 percent / V max

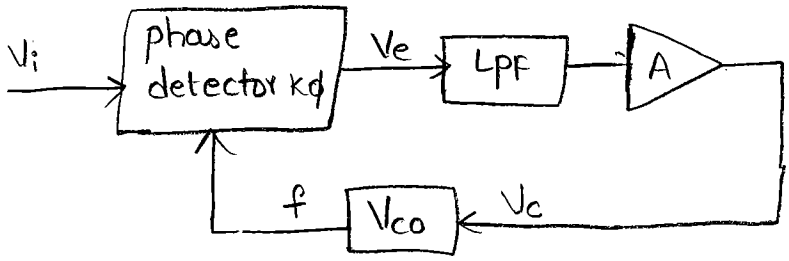
Triangle coave amplitude : 2.4 Vpp at ±6 Supply Voltage

Square coave amplitude : 5.4 Vpp at ±6 v supply Voltage

Band coidth adJustment Range : < ±1 to ±60%.

Derivation for lock-in-range:-

Block diagram to determine lock-range.



Output Voltage of a phase detector is

$$V_e = K_\phi(\phi - \pi/2) \quad -(1)$$

ϕ = phase error

Voltage

The output of phase detector is filtered by the loco-pass filter to remove the high-frequency components. The output of the filter is amplified by a gain A and then applied as the Control Voltage V_c to the V_{co} as given by.

$$V_c = AV_e = AK_\phi(\phi - \pi/2) \quad -(2)$$

This Control Voltage V_c coill result in a shift in the V_{co} frequency from its center frequency f_o to a frequency f,

$$f = f_o + K_v V_c \quad -(3)$$

K_v = Voltage to frequency transfer Coefficient of the V_{co}.

When the pll is locked in to the input signal frequency f_i, we have

$$f = f_i = f_o + K_v V_c \quad -(4)$$

Substitute ② in ④

$$f_i = f_0 + K_V K_\phi A(\theta - \pi/2)$$

$$f_i - f_0 = K_V K_\phi A(\theta - \pi/2)$$

$$\theta - \pi/2 = \frac{f_i - f_0}{K_V K_\phi A}$$

$$\theta = \frac{\pi}{2} + \frac{f_i - f_0}{K_V K_\phi A} \quad -⑤$$

The maximum output voltage magnitude available from the phase detector across for $\phi = \pi$ and 0 radian.

$$V_c(max) = \pm K_\phi \pi/2 \qquad V_c = K_\phi(\phi - \pi/2).$$

The corresponding value of the maximum control voltage available to drive the VCO will be.

$$V_c(max) = \pm K_\phi(\pi/2)A \quad -⑥$$

Substitute ⑥ in ④

$$f = f_i = f_0 \pm K_V K_\phi(\pi/2)A.$$

$$f = f_0 \pm \Delta f_L$$

where $2\Delta f_L$ will be lock-in frequency range given by.

$$\text{Lock range} = 2\Delta f_L = K_V K_\phi A\pi.$$

$$\Delta f_L = K_V K_\phi A\pi/2 \quad -⑦$$

The lock in range is symmetrically locked with respect to VCO free running frequency f_0 for PLL565.

We have $K_V = \frac{8f_0}{V}$ —⑧

$$V = +V_{cc} - (-V_{cc}) \quad -⑨$$

for PLL565 $K_\phi = \frac{1.4}{\pi}$ and $A = 1.4$ —⑩

Substitute 8, 9, 10 in ⑦ $\Delta f_L = K_V K_\phi A\pi/2$

$$\Delta f_L = \frac{8f_0}{V}\frac{1.4}{\pi}(1.4)\pi/2$$

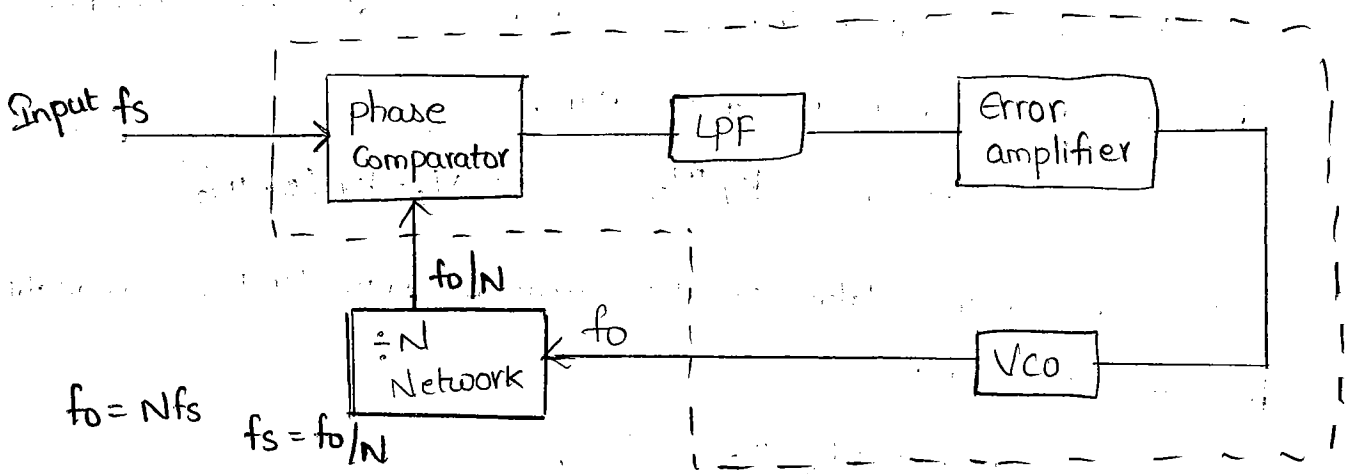
$$\Delta f_L = \pm \frac{7.84 f_o}{V} \text{ Hz}$$

$$\Delta f_{cap} = \pm \left[\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C} \right]^{1/2} \text{Hz}.$$

↑ Capture Range.

Applications of PLL:-

frequency multiplication:-



* Above fig is the block diagram for a frequency multiplier using PLL 565.

Here a dived by N network is inserted b/w the Vco output (pin4) and the phase Comparator input (pin5).

Since the output of the divider is locked to the input frequency fi, the Vco is actually running at a multiple of the input frequency.

In the blocked state, the Vco output frequency $f_o = Nf_i$

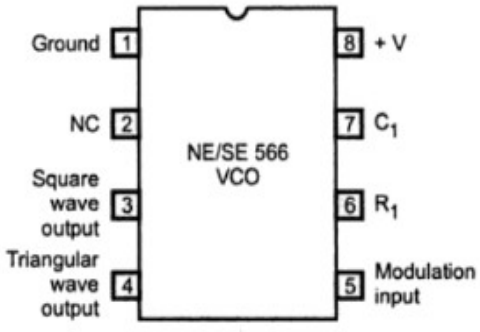
By selecting proper divided by 'N' network, coe can obtain desired multiplication. for Er, to obtain output frequency $f_o = 6f_i$, divided by N should be equal to 6.

IC Applications
UNIT-V

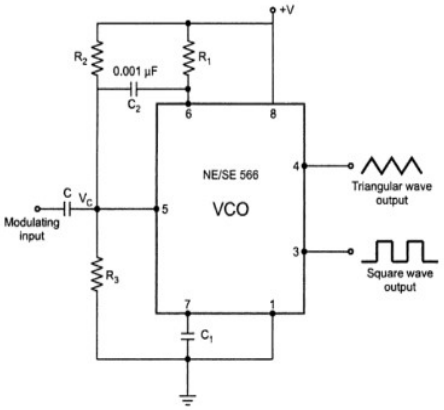
TOPICS:

- Voltage Controlled Oscillator (IC 566)
- VOLTAGE TO FREQUENCY CONVERTER
- Applications of VCO

Voltage Controlled Oscillator (IC 566)

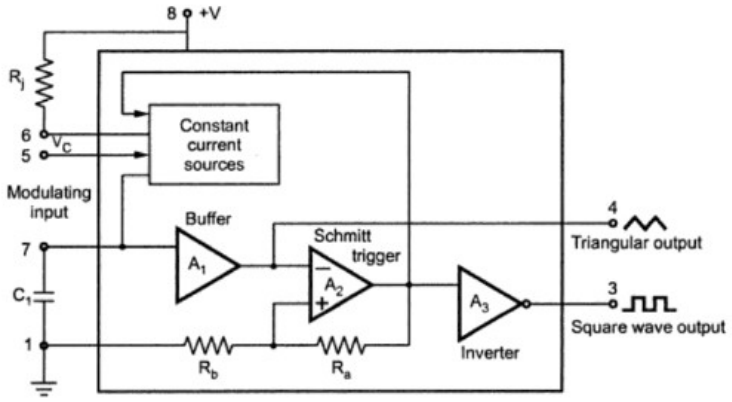


Pin diagram of IC 566 VCO



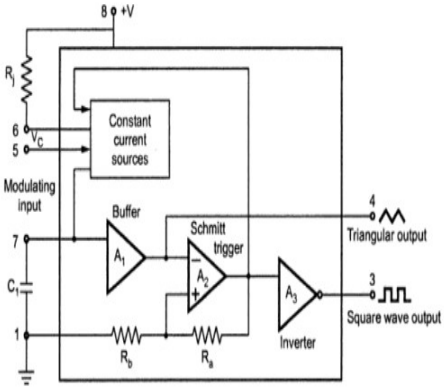
Typical connection diagram of 566 VCO

Voltage Controlled Oscillator (IC 566)

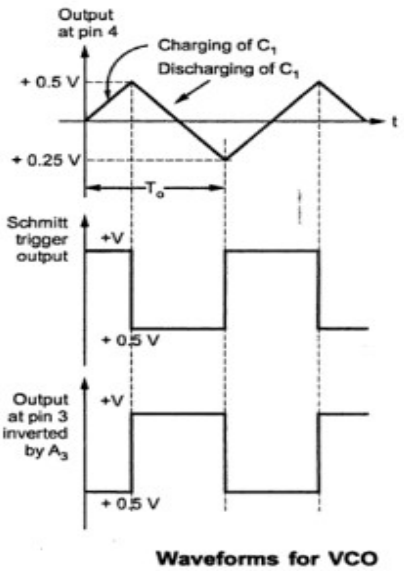


- Block diagram of IC 566 VCO

Voltage Controlled Oscillator (IC 566)



$$f_o = \frac{1}{\frac{2(+V - V_C)}{C_1 R_1 (+V)}}$$



Waveforms for VCO

VCO:

- Applications of VCO:
  - FM modulation
  - Signal generation (Triangular & square)
  - Function generation
  - FSK demodulator
  - Frequency multipliers

VOLTAGE TO FREQUENCY CONVERTER:

- V-F conversion factor is a very important parameter for VCO

$$K_v = \frac{\Delta f_o}{\Delta V_c}$$

ΔV_c = change in the control voltage producing change of Δf_o in the frequency.

Let f'_o = New frequency

f_o = original frequency

$\Delta f_o = f'_o - f_o$ w

VOLTAGE TO FREQUENCY CONVERTER:

- While V_c is changed by ΔV_c to achieve this,
- From expression of f'_o ,

$$f'_o = \frac{2[+V-(V_c-\Delta V_c)]}{C_1R_1(+V)}$$

$$f_o = \frac{2[+V-(V_c)]}{C_1R_1(+V)}$$

$$\Delta f_o = f_2 - f_1 = \frac{2\Delta V_c}{C_1R_1(+V)}$$

$$\Delta V_c = \frac{R_1C_1\Delta f_o(+V)}{2} \quad \rightarrow (1)$$

VOLTAGE TO FREQUENCY CONVERTER:

- With no modulating input voltage,
- Control voltage V_c = (7/8)(+V)
- If fo is the original frequency then,

$$f_o = \frac{2\left[+V-\frac{7}{8}(V)\right]}{C_1R_1(+V)} = \frac{0.25}{C_1R_1}$$

using the value of R1 C1 from the (1)

$$f_o = \frac{0.25}{\frac{2\Delta V_c}{f_o(+V)}}$$

VOLTAGE TO FREQUENCY CONVERTER:

$$K_v = \frac{\Delta f_o}{\Delta V_c} = \frac{f_o}{0.125(+V)}$$

$$\boxed{K_v = \frac{8 f_o}{(+V)}}$$

- Where fo is the original frequency
- This is the required voltage to frequency conversion factor.

Voltage Regulator:

The function of a **voltage regulator** is to maintain a constant DC voltage at the output irrespective of voltage fluctuations at the input and (or) variations in the load current. In other words, voltage regulator produces a regulated DC output voltage.

Voltage regulators are also available in Integrated Circuits (IC) forms. These are called as **voltage regulator ICs**.

Types of Voltage Regulators:

There are **two types** of voltage regulators −

- Fixed voltage regulator
- Adjustable voltage regulator

Fixed voltage regulator

A **fixed voltage regulator** produces a fixed DC output voltage, which is either positive or negative. In other words, some fixed voltage regulators produce positive fixed DC voltage values, while others produce negative fixed DC voltage values.

78xx voltage regulator ICs produce positive fixed DC voltage values, whereas, 79xx voltage regulator ICs produce negative fixed DC voltage values.

There are 7 output voltage options available such as 5, 6, 8,12, 15, 18, 24 V.

These regulators are available in two types of packages

- Metal Package (TO-3 Type)
- Plastic package (TO-220 Type)

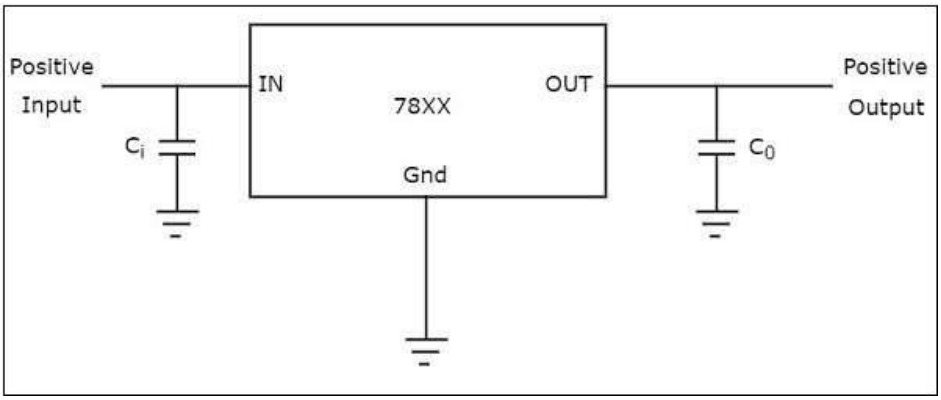
The following points are to be noted while working with **78xx** and **79xx** voltage regulator ICs −

- "xx" corresponds to a two-digit number and represents the amount (magnitude) of voltage that voltage regulator IC produces.
- Both 78xx and 79xx voltage regulator ICs have **3 pins** each and the third pin is used for collecting the output from them.
- The purpose of the first and second pins of these two types of ICs is different −
    - The first and second pins of **78xx** voltage regulator ICs are used for connecting the input and ground respectively.
    - The first and second pins of **79xx** voltage regulator ICs are used for connecting the ground and input respectively.

Examples

- 7805 voltage regulator IC produces a DC voltage of +5 volts.
- 7905 voltage regulator IC produces a DC voltage of -5 volts.

The following figure shows how to produce a **fixed positive voltage** at the output by using a fixed positive voltage regulator with necessary connections.



In the above figure that shows a fixed positive voltage regulator, the input capacitor C_i is used to prevent unwanted oscillations and the output capacitor, C_0 acts as a line filter to improve transient response.

C_i value is around 0.33 uF

C_0 value is around 1 uF

IC 723 Voltage Regulator:

The popular general purpose precision regulator is IC 723. It is a monolithic linear integrated circuit in different physical packages. The pin diagram of IC 723 Voltage Regulator along with the various packages is shown in the Fig. (a), (b) and (c).

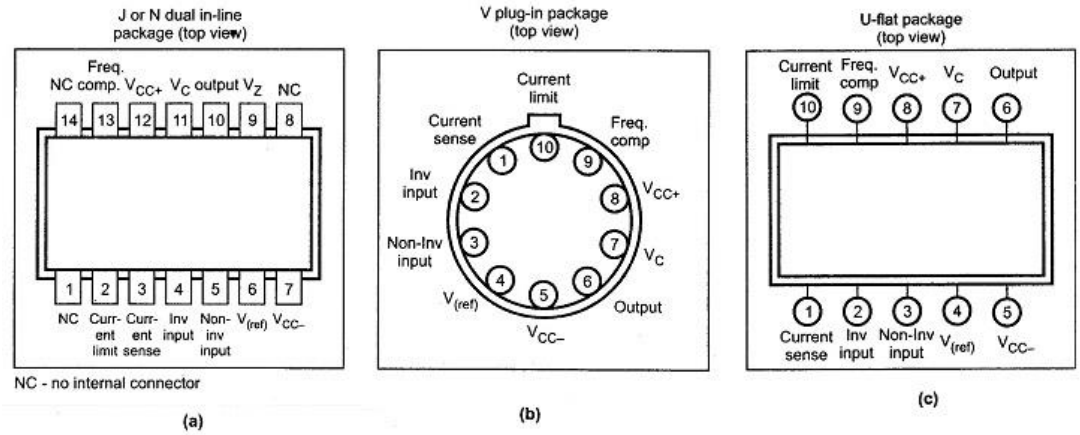


Fig. 2.109 Available packaging for the μA723 precision voltage regulator

Features of IC 723:

1. It works as voltage regulator at output voltage ranging from 2 to 37 volts at currents upto 150 mA.
2. It can be used at load currents greater than 150 mA with use of suitable NPN or PNP external pass transistors.
3. Input and output short-circuit protection is provided.
4. It has good line and load regulation (0.03%).
5. Wide variety of applications of series, shunt, switching and floating regulator.
6. Low temperature drift and high ripple rejection.
7. Low standby current drain.
8. Small size, lower cost.
9. Relative ease with which power supply can be designed.
10. It provides a choice of supply voltage.

Functional Block Diagram of IC 723:

The functional block diagram of IC 723 Voltage Regulator can be divided into four major blocks:

1. Temperature compensated voltage reference source, which is zener diode.
2. An op-amp circuit used as an error amplifier.
3. A series pass transistor capable of a 150 mA output current.
4. Transistor used to limit output current.

The functioning of the above blocks can be explained with the help of a simplified functional block diagram of IC 723 Voltage Regulator as shown in the Fig. 2.110.

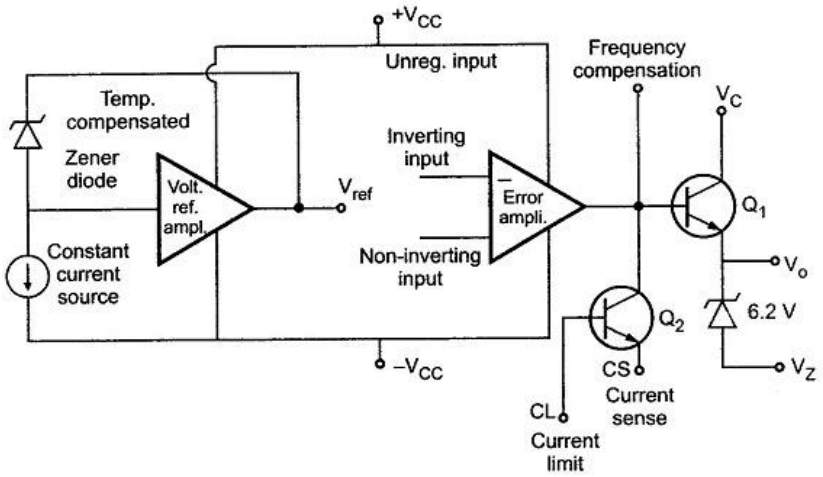


Fig. 2.110 Functional block diagram

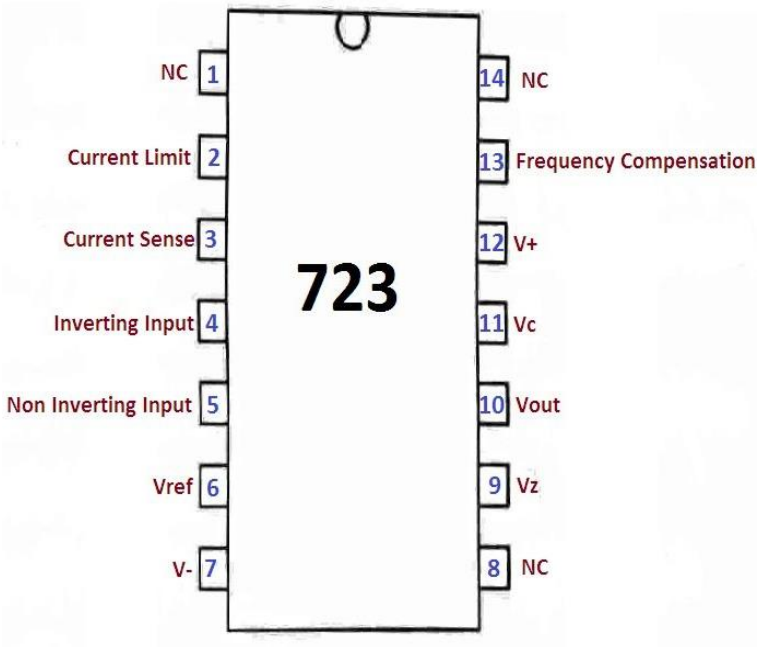


Fig: Pin diagram of IC 723

Temperature compensated zener diode, constant current source and reference amplifier constitutes the reference element. In order to get a fixed voltage from zener diode, the constant current source forces the zener to operate at a fixed point.

Output voltage is compared with this temperature compensated reference potential of the order of 7 volts. For this V_{ref} is connected to the non-inverting input of the error amplifier.

This error amplifier is high gain differential amplifier. It's inverting input is connected to the either whole regulated output voltage or part of that from outside. For later case a potential divider of two scaling resistors is used. Scaling resistors help in getting multiplied reference voltage or scaled up reference voltage.

Error amplifier controls the series pass transistor Q_1, which acts as variable resistor. The series pass transistor is a small power transistor having about 800 mW dissipation. The unregulated power supply source (< 36V d.c.) is connected to collector of series pass transistor.

Transistor Q_2 acts as current limiter in case of short circuit condition. It senses drop across R_{sc} placed in series with regulated output voltage externally.

The frequency compensation terminal controls the frequency response of the error amplifier. The required roll-off is obtained by connecting a small capacitor of 100 pF between frequency compensation and inverting input terminals.

The internal structure can be represented in more simplified form as shown in the Fig. 2.111.

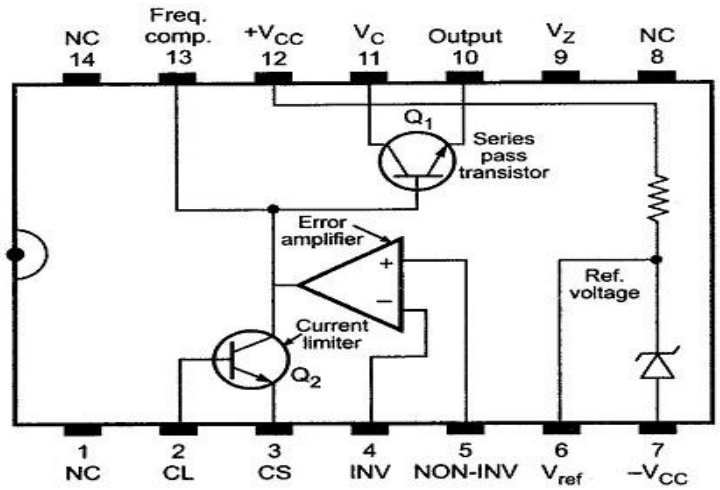


Fig. 2.111 Simplified internal structure of IC 723

Both noninverting and inverting terminals of the error amplifier are available on outside pins of IC 723. Due to this, device becomes versatile and flexible to use. Only restriction is that internal reference voltage is 7 volts and therefore we have to use two different circuits for getting regulated outputs of below 7 volts and above 7 volts.

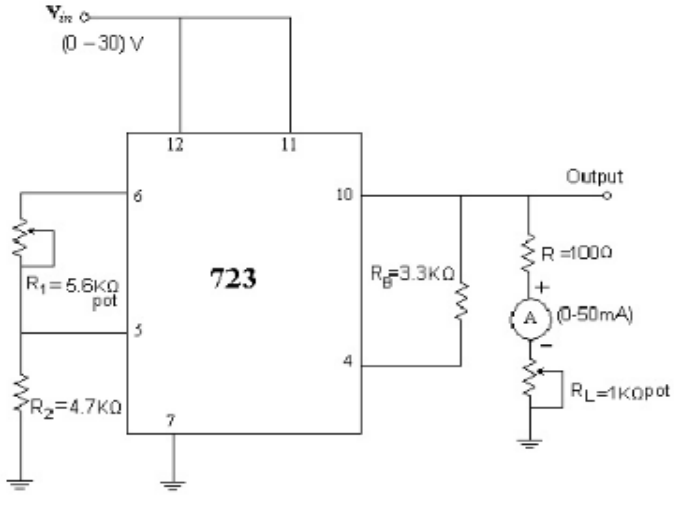


Fig: Low voltage regulator using IC 723

The output of low voltage regulator is given by

$$V_0 = 7.15 * \left(\frac{R_2}{R_1 + R_2}\right)$$

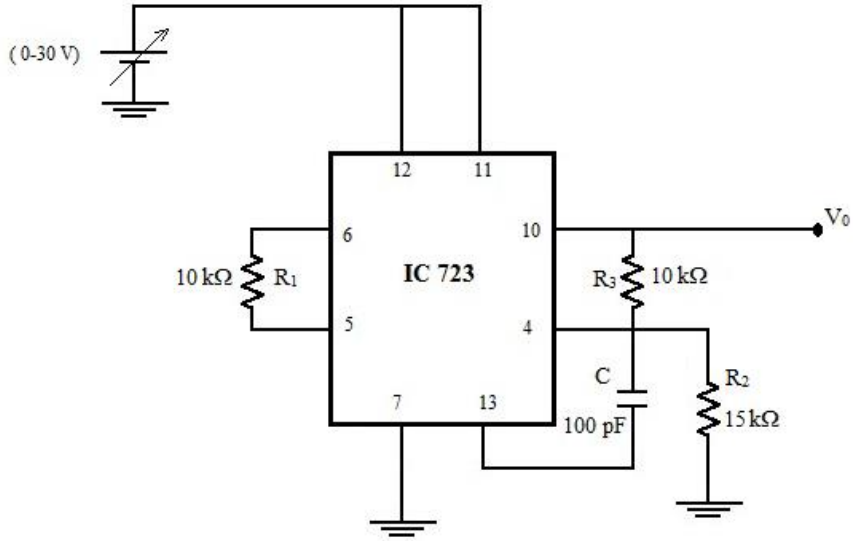


Fig: High voltage regulator using IC 723

The output of a high voltage regulator using IC732 is given by

$$V_0 = \quad 7.15 * (1 + \frac{R_1}{R_2})$$

Applications of IC 723 Voltage Regulator:

The various Applications of IC 723 Voltage Regulator are namely:

- Basic Low-voltage Regulator (V_o = 2 to 7 volts)
- Low Voltage High Current Regulator
- Basic Positive High Voltage Regulator
- Positive High Voltage High Current Regulator
- Negative Voltage Regulator

Adjustable voltage regulator

An adjustable voltage regulator produces a DC output voltage, which can be adjusted to any other value of certain voltage range. Hence, adjustable voltage regulator is also called as a **variable voltage regulator**.

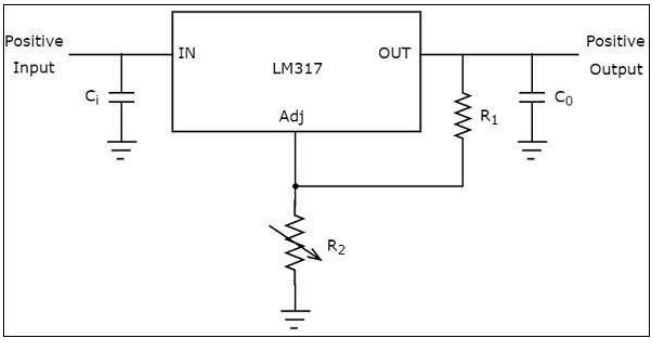
The DC output voltage value of an adjustable voltage regulator can be either positive or negative.

LM317 voltage regulator IC:

LM317 voltage regulator IC can be used for producing a desired positive fixed DC voltage value of the available voltage range.

LM317 voltage regulator IC has 3 pins. The first pin is used for adjusting the output voltage, second pin is used for collecting the output and third pin is used for connecting the input.

The adjustable pin (terminal) is provided with a variable resistor which lets the output to vary between a wide range.



The above figure shows an unregulated power supply driving a LM 317 voltage regulator IC, which is commonly used. This IC can supply a load current of 1.5A over an adjustable output range of 1.25 V to 37 V.

The voltage across the feedback resistor R1 is a constant 1.25V reference voltage, V_{ref} produced between the "output" and "adjustment" terminal. The adjustment terminal current is a constant current of 100uA. Since the reference voltage across resistor R1 is constant, a constant current i will flow through the other resistor R2, resulting in an output voltage of:

$$V_{OUT} = 1.25\left(1+\frac{R_2}{R_1}\right)$$

Then whatever current flows through resistor R1 also flows through resistor R2 (ignoring the very small adjustment terminal current), with the sum of the voltage drops
across R1 and R2 being equal to the output voltage, Vout. The input voltage, Vin must be at least 2.5 volts greater than the required output voltage to power the regulator.

If we know the value of the required output voltage, Vout and the feedback resistor R1 is say 240 ohms, then we can calculate the value of resistor R2 from the above equation. For example, our original output voltage of 9V would give a resistive value for R2 of:

R1.((Vout/1.25)-1) = 240.((9/1.25)-1) = 1,488 Ohms

or 1,500 Ohms (1.5 k Ω) to the nearest preferred value. In practice, resistors R1 and R2 would normally be replaced by a potentiometer so as to produce a variable voltage power supply, or by several switched preset resistances if several fixed output voltages are required.

Problem :-

1. Design monostable Multivibrator using 555 timer to produce a pulse width of 10msec.

Sol:- $T = 10\,msec.$

$$T = 1.1\,RC$$

Let us assume $C = 1\,\mu F$

$$R = \frac{T}{1.1 \times C}$$

$$R = \frac{10 \times 10^{-3}}{1.1 \times 10^{-6}}$$

$$= 9k\Omega.$$

problem :-

* Design a Astable multivibrator to operate 10KHz with duty cycle of 40%.

Sol:- $f_o = 10KHz$

$D = 40\%$

$T_c = 0.693 (R_A) C$

$T_d = 0.693 (R_B) C$.

$T = T_c + T_d$

$= 0.693 (R_A + R_B) C$

$$D = \frac{T_c}{T} = \frac{0.693 (R_A) C}{0.693 (R_A + R_B) C}$$

$$D = \frac{T_c}{T} = \frac{R_A}{R_A + R_B}.$$

$$D = \frac{R_A}{R_A + R_B}.$$

Given $D = 0.4$.

$0.4 (R_A + R_B) = R_A$.

$0.4 R_B = R_A - 0.4 R_A$

$R_B = \frac{0.6}{0.4} R_A$

$\boxed{R_B = 1.5 R_A}$ — (1)

$$f = \frac{1}{T}$$

$$f = \frac{1}{0.693(R_A + R_B)C}$$

$$(R_A + R_B) = \frac{1}{0.693(f)C} \quad - (2).$$

Assume, $C = 0.01\,\mu F$ — (3).

Sub — (1) & (3) in — (2).

$$R_A + 1.5R_A = \frac{1}{0.693\,(10\times10^{3})\,0.01\times10^{-6}}$$

$$2.5\,R_A =$$

$$R_A = 5.7k\Omega.$$

$$R_B = 8.6k\Omega.$$