D/A AND A/D CONVERTERS

Most of the real-world physical quantity such as voltage, current, temperature, pressure and time etc., are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store (or) transmit the analog signal without introducing considerable error because of the superimposition of noise as in the amplitude modulation. Therefore, for processing, transmission and storage purpose, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to Analog (D/A) conversion.

Thus, Data converters are of two types:-

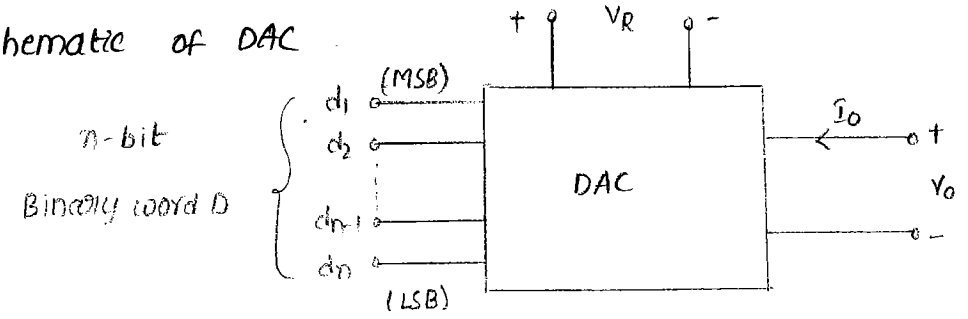
(1) Analog - to - Digital converters (ADC)

(2) Digital - to - Analog converters (DAC)

The function of ADC is just the opposite of function of DAC

Digital - to - Analog converters (DAC):-

Basic schematic of DAC



The input to the DAC is a n-bit binary word D. whose digits are $d_1, d_2, d_3, d_4 \ldots\ldots d_n$ (1's and 0's)

i.e, $D = d_1\ d_2\ d_3\ d_4 \ldots\ldots d_n$ Ex:- D = 1010110

The n-bit binary word D is combined with a reference voltage V_R to give an analog output signal.

The output of a DAC can be either a voltage (or) current

For voltage output DAC, the D/A converter is mathematically described as

$$V_0 = K\ V_{FS}\ (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \ldots\ldots + d_n 2^{-n}) \longrightarrow (1)$$

where V_0 = output voltage ; V_{FS} = Full scale output voltage

K = scaling factor usually adjusted to unity

$d_1, d_2 \ldots\ldots d_n$ = n-bit binary fractional word with the decimal point located at the left.

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$,

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$.

There are various ways to implement eqn (1). some of resistive techniques are

(1) Weighted resistor DAC

(2) R-2R ladder

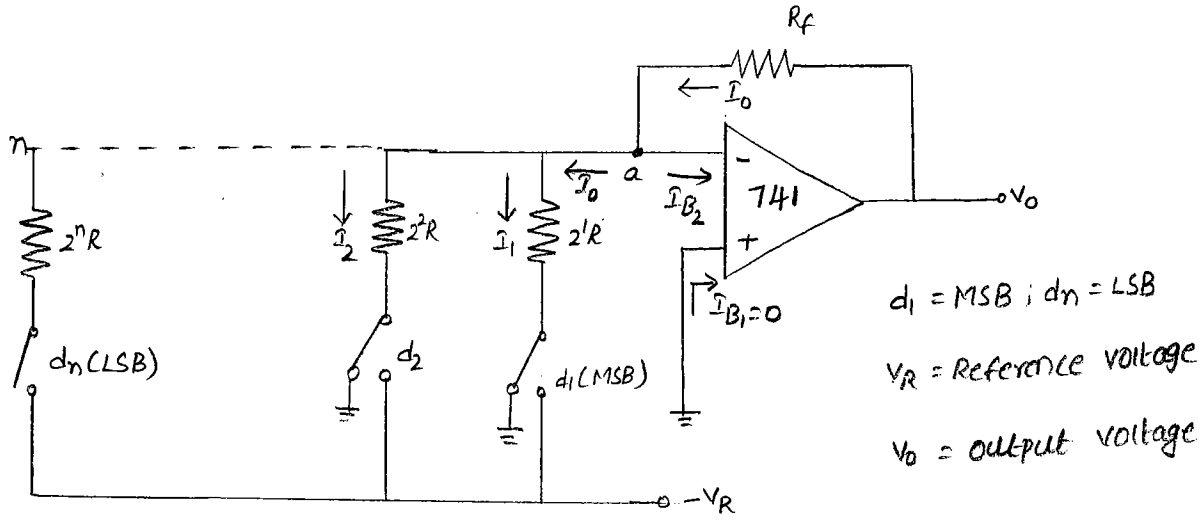
(3) Inverted R-2R ladder

(1) Weighted resistor DAC:-

Binary weighted resistor DAC

This is the one of the simplest circuit uses a summing amplifier with a binary weighted resistor network.

Circuit diagram for binary weighted resistor DAC:-



$2R, 2^2R, 2^3R \ldots\ldots 2^nR$ are weighted resistors.

It has n- Electronic switches $d, d_2 \ldots\ldots d_n$ controlled by binary input word.

These switches are single pole double throw (SPDT).

If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$)

If the input bit is '0', the switch connects the resistor to ground.

Let $I_1, I_2, I_3 \ldots\ldots, I_n$ denotes the currents through the resistors and I_0 be the current in the feedback path.

Apply KCL at node A,

$$I_0 = I_1 + I_2 + I_3 + \ldots\ldots + I_n + I_{B_2}$$

$I_{B_1} = 0 \quad \Rightarrow \quad I_0 = I_1 + I_2 + I_3 + \cdots + I_n$

$$I_1 = \frac{V_R}{2R} d_1 \;, \quad I_2 = \frac{V_R}{2^2 R} d_2 \;, \quad I_n = \frac{V_R}{2^n R} d_n$$

$$I_0 = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \cdots + \frac{V_R}{2^n R} d_n$$

$$I_0 = \frac{V_R}{R} \left(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right) \longrightarrow ②$$

The output voltage $V_0 = R_f I_0 \longrightarrow ③$

Substitute ② in ③ $\Rightarrow V_0 = \frac{V_R}{R} \left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right] R_f$

$$V_0 = \left(\frac{R_f}{R}\right) V_R \left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right]$$

When $R_f = R$, $V_0 = V_R \left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right] \longrightarrow ④$

compare Eq ④ & eq ①,

$K = 1$; $V_R = V_{FS}$ = Full scale output voltage

$$V_0 = K V_{FS} \left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right]$$

The circuit uses a -ve reference voltage. So the analog output voltage is +ve staire case.

Let the input be a 3-bit binary word $D = d_1 d_2 d_3$. Since there are 3 bits i.e, $n = 3$, the no. of digital inputs possible is $2^3 = 8$.

	d_1	d_2	d_3
D_1	0	0	0
D_2	0	0	1
D_3	0	1	0
D_4	0	1	1
D_5	1	0	0
D_6	1	0	1
D_7	1	1	0
D_8	1	1	1

$D_1 = d_1 d_2 d_3 = 0\,0\,0 \Rightarrow V_0 = V_R[0+0+0] = 0V$

$D_2 = d_1 d_2 d_3 = 0\,0\,1 \Rightarrow V_0 = V_R[0+0+1\times 2^{-3}] = V_R/8 \ V$

$D_3 = d_1 d_2 d_3 = 0\,1\,0 \Rightarrow V_0 = V_R[0+1\times 2^{-2}+0] = \frac{V_R}{4} V = \frac{2V_R}{8} V$

$D_4 = d_1 d_2 d_3 = 0\,1\,1 \Rightarrow V_0 = V_R[0+1\times 2^{-2}+1\times 2^{-3}] = 3V_R/8 \ V$

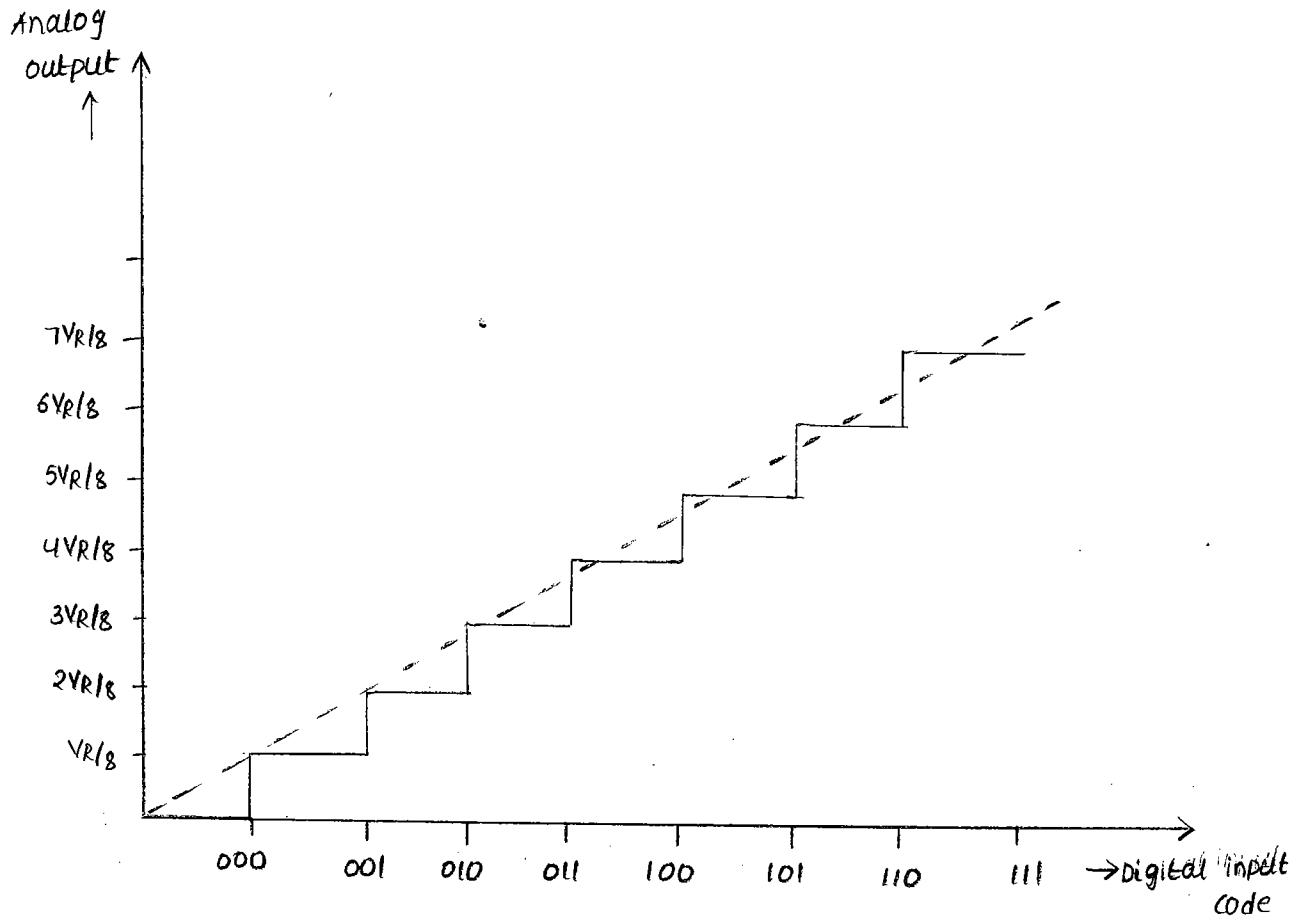
$D_5 = d_1 d_2 d_3 = 1\,0\,0 \Rightarrow V_0 = V_R[1\times 2^{-1}+0+0] = 4V_R/8 \ V$

$D_6 = d_1 d_2 d_3 = 1\,0\,1 \Rightarrow V_0 = V_R[1\times 2^{-1}+0+1\times 2^{-3}] = 5V_R/8 \ V$

$D_7 = d_1 d_2 d_3 = 1\,1\,0 \Rightarrow V_0 = V_R[1\times 2^{-1}+1\times 2^{-2}+0] = 6V_R/8 \ V$

$D_8 = d_1 d_2 d_3 = 1\,1\,1 \Rightarrow V_0 = V_R[1\times 2^{-1}+1\times 2^{-2}+1\times 2^{-3}] = \frac{7V_R}{8} V$

Transfer characteristics of a 3-bit DAC:-



- The reference voltage is -ve. The analog output voltage is +ve for a 3-bit weighted resistor DAC.
- op-Amp is connected in inverting mode, it can be also connected in Non-inverting mode.
- The op-Amp is simply working as a current to voltage converter.
- The polarity of the reference voltage is selected in accordance with the type of the switch used.

  Ex:- For TTL compatible switches, the reference voltage should be +5V and output will be -Ve.
- The accuracy and stability of op-amp DAC depends upon the accuracy of the resistors.

The DAC using binary weighted resistors has the following drawbacks:-

- It is not used for more than 8-bits because

The circuit requires wide range of binary weighted resistors. As the no. of bits increases, the required range of resistors also increases.

Ex:- 8 bit DAC uses resistors of $2R, 2^2R, 2^3R, \ldots\ldots, 2^8R$.

Thus the value of largest resistor corresponding to 8^{th} bit i.e, d_8 is 128 times the smallest resistor value. It is practically not possible to design such large value of resistors. This limitation does not permits the use of binary weighted resistor DAC for more than 8-bits.

- It is not practicable to fabricate large value of resistors on one chip.

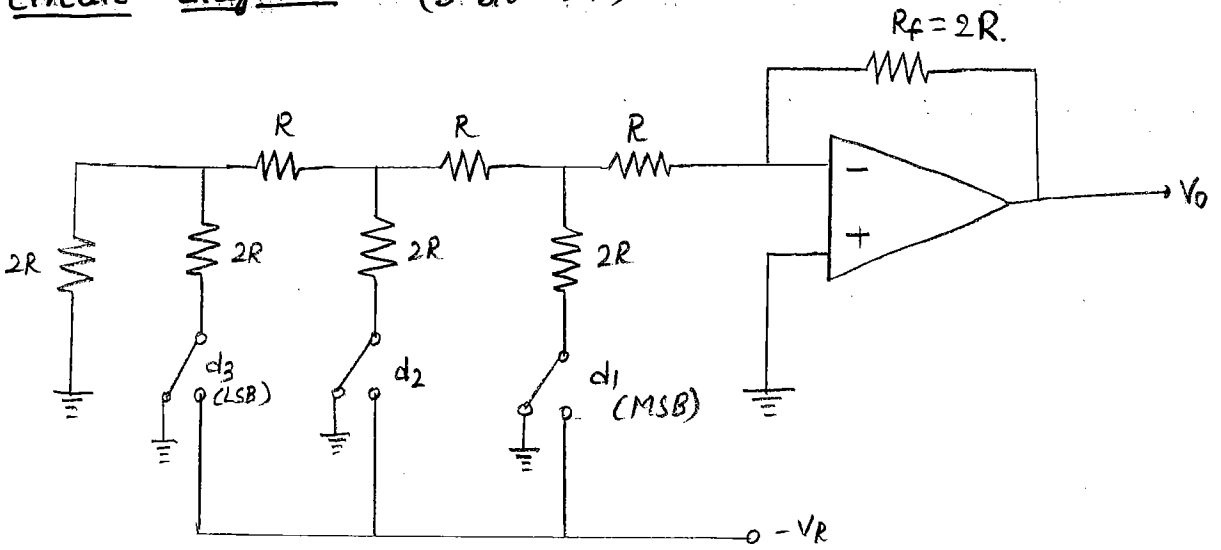
This drawbacks are overcome in the R-2R ladder type D/A converters.

R-2R ladder D to A converter:-

This type of DAC uses only 2 values of resistors, and hence it is Easy to fabricate all resistors on a chip. The usual values of the resistors range from 2.5 KΩ to 20KΩ.

- The resistors (R-2R) are so arranged as to form a ladder Network.

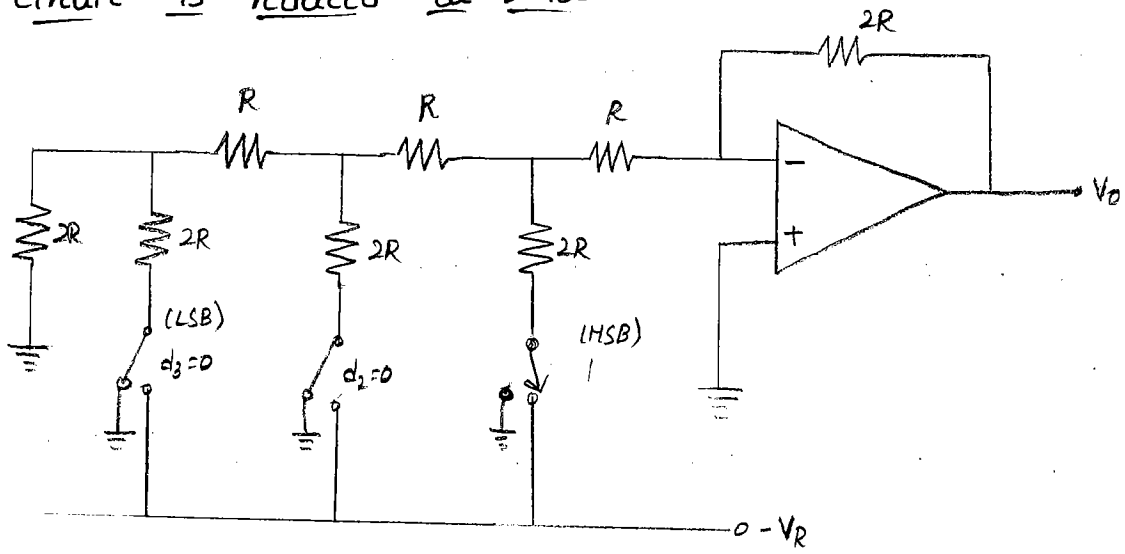
Circuit diagram:- (3-bit DAC)



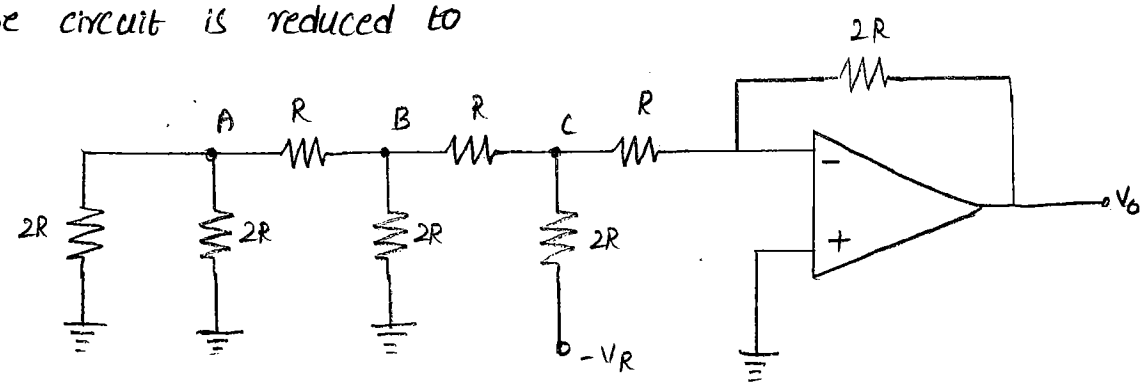
Let the digital input be a 3-bit binary word given as

$D = 100$, $d_1 = 1$, $d_2 = 0$, $d_3 = 0$

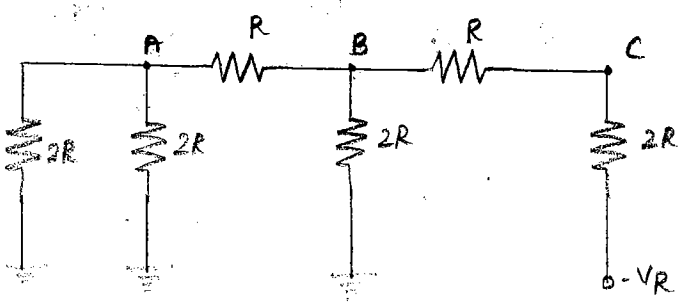
The circuit is reduced at $D = 100$



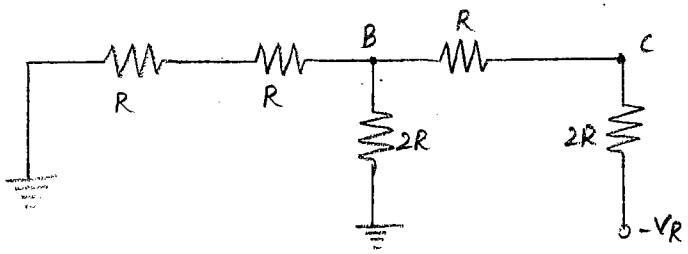
The circuit is reduced to



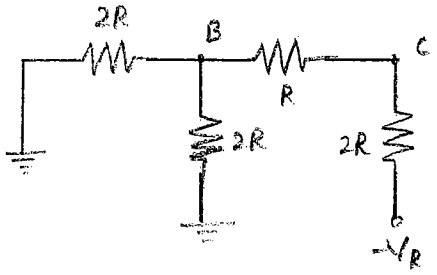
To find Equivalent resistance at node C.



$$2R \,//\, 2R = \frac{2R \times 2R}{2R+2R} = \frac{4R^2}{4R} = R$$

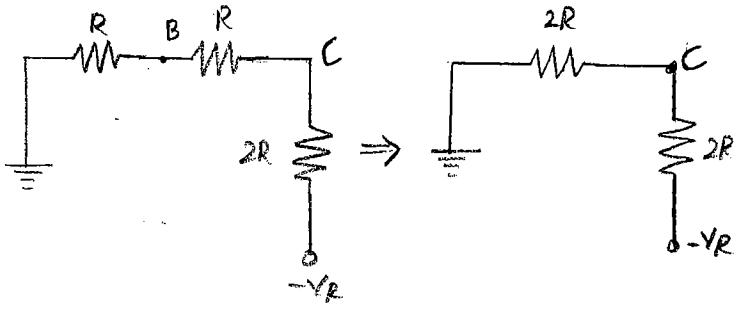


$$R+R = 2R$$

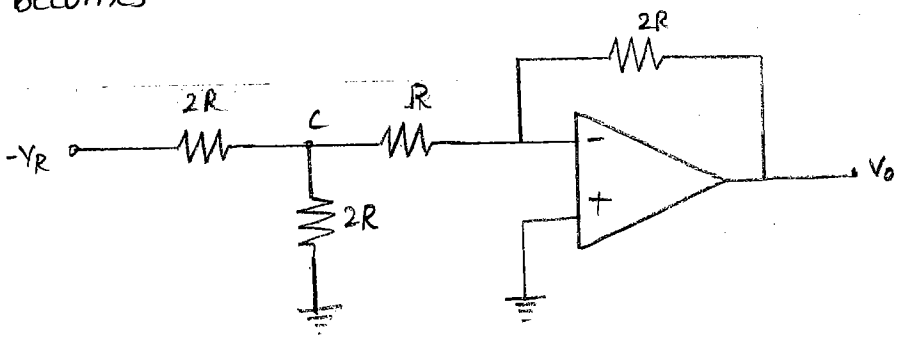


$2R \,//\, 2R = R$

$\Rightarrow$



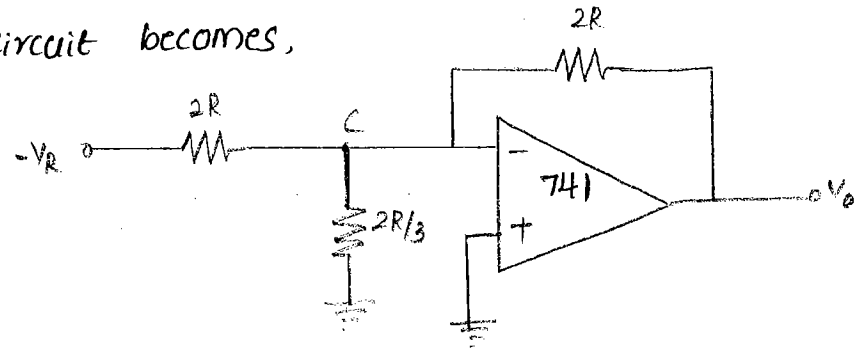
The circuit becomes



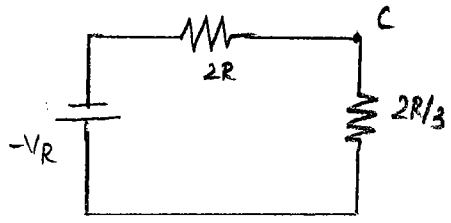
According to virtual ground concept, the potential at inverting terminal is zero.

$$R \,//\, 2R = \frac{R \times 2R}{R+2R} = \frac{2R^2}{3R} = 2R/3$$

The circuit becomes,



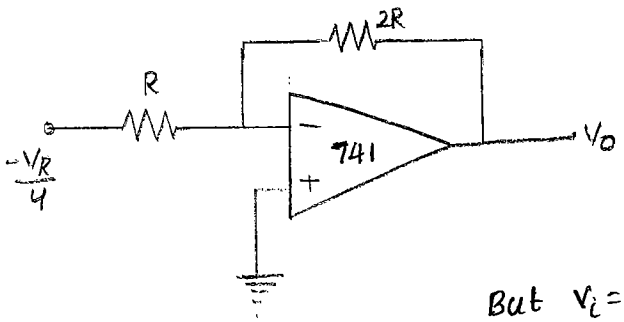
potential at C is



$$V_C = -V_R \frac{2R/3}{2R+2R/3} = \frac{-V_R\left(\frac{2R}{3}\right)}{\frac{6R+2R}{3}}$$

$$V_C = \frac{-V_R(2R)}{8R} = -V_R(1/4)$$

The circuit may be redrawn.



$$V_o = \left(\frac{-R_f}{R_1}\right) V_i = \frac{-2R}{R} V_i$$

$$\frac{V_o}{V_i} = -2$$

But $V_i = \frac{-V_R}{4} \Rightarrow V_o = -2\left(\frac{-V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$

$$\boxed{V_o = \frac{V_{FS}}{2}}$$

Similarly for the binary input 001 $V_o = V_{FS}/8$

similarly for 4-bit (or) 8-bit binary input, the analog output can be determined.

Drawbacks:-

In the DtoA converters studied above, it is seen that the current in every one of the resistors changes, as and when the input data changes. An increase of current results in more heat being generated and thus there is large dissipation of power.

As a result of it, non-linearity of operation sets as this is highly undesirable in practice.

This drawback is overcome in the inverted R-2R ladder DAC.

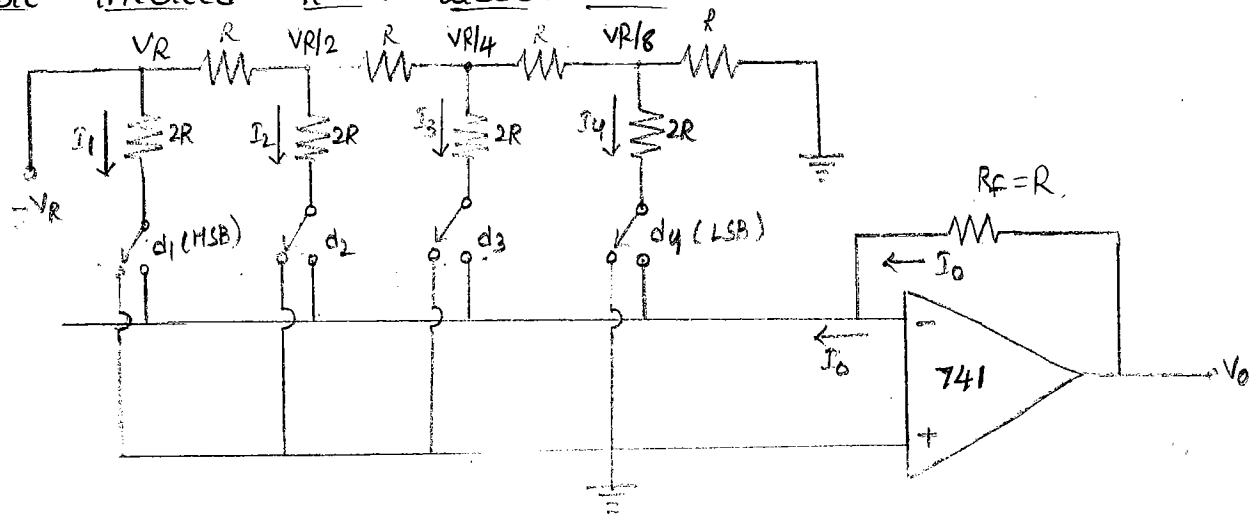
Advantages of R-2R ladder NETWORK:-

(1) Easier to build accurately as only 2 precision metal film resistors are required.

(2) No. of bits can be expanded by adding more sets as of same R/2R values.

Inverted R-2R ladder Digital to Analog converter:-

4-bit inverted R-2R ladder DAC



→ It may be observed that the positions of MSB & LSB are interchanged. (Compare with the R-2R ladder DAC)

→ The arrangement of switches is such that the input binary word connects the switches to either ground (or) the inverting input terminal.

→ The switch d_1 is at logic '0', ~~to the left~~ It connects to ground, to the left. The current through 2R resistor flows to ground.

When the switch d_1 is at logic 1 to the right, the current through 2R sinks to the virtual ground.

Here the current divides equally at each of the nodes.

The reason for this is the equivalent resistance to the right (or) to the left of any node is exactly 2R.

The currents are

$$I_1 = \frac{V_R}{2R} \; ; \; I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2} \; ; \; I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_4 = \frac{V_R/8}{2R} = \frac{V_R}{16R} = \frac{I_1}{8} \; , \; I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

output voltage $V_0 = -I_0 R_f$

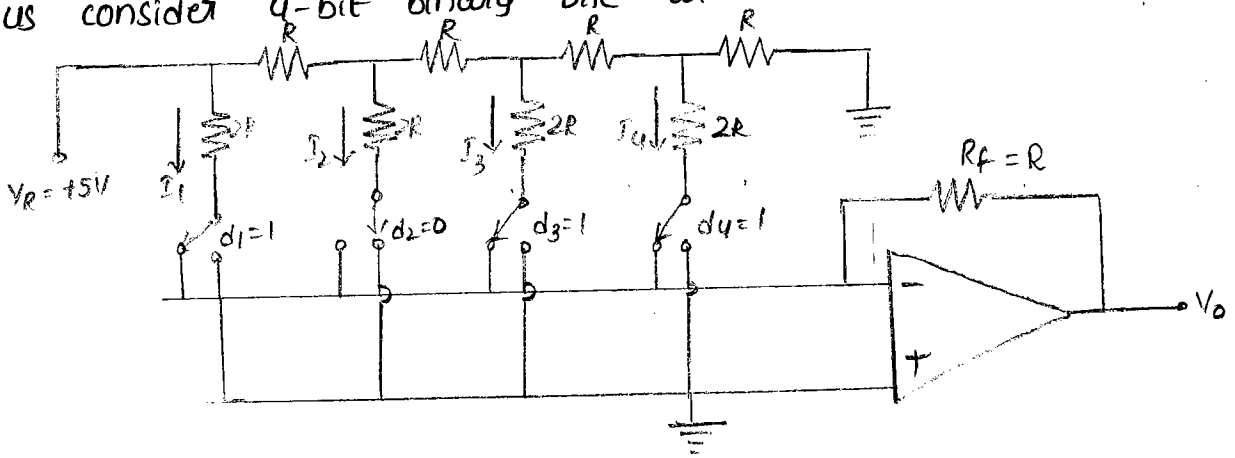
$$+ I_0 = I_1 + I_2 + I_3 + I_4$$

$$V_0 = -(I_1 + I_2 + I_3 + I_4) R_f = -R_f \left[\frac{V_R}{2R} d_1 + \frac{V_R}{4R} d_2 + \frac{V_R}{8R} d_3 + \frac{V_R}{16R} d_4\right]$$

$$V_0 = -\frac{R_f}{R} V_R \left[2^{-1} d_1 + 2^{-2} d_2 + 2^{-3} d_3 + 2^{-4} d_4\right]$$

$$R_f = R \Rightarrow V_0 = -V_R \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right]$$

Let us consider 4-bit binary DAC with binary input 1011 & $R_f = R$



$$V_0 = -V_R \left[1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4}\right]$$

$$V_0 = -V_R \left[0.6875\right] = +5 \times 0.6875 \Rightarrow V_0 = 3.4375\,V$$

Compare R-2R and weighted resistor types of DACs

R-2R Ladder DAC	Weighted resistor DAC
(1) R-2R ladder DAC requires only 2 values of resistors i.e, R & 2R usually the values of R varies from 2.5 kΩ to 10kΩ	(1) Weighted resistor DAC requires wide range of binary weighted resistors. As the no. of bits increases the required range of resistors are also increases.
(2) Since the value of resistances are small and easily available, this technique is suitable for integrated circuit fabrication.	(2) Since the value of resistances are very high & it is not possible to fabricate such large values of resistors in integrated circuits.
(3) By increasing the no. of R-2R resistors. More no. of bits can be converted into analog.	(3) In a 8-bit DAC the value of largest resistor of 8^{th} bit i.e. d_8 is 128 times the smallest resistor value. Since accurate design of such large value of resistors is not possible, it is not used for more than 8-bits
(4) The analysis of the circuit is complicated.	(4) Analysis of this circuit is Easy.
(5) It is more preferable for even wide range of bits. Hence, it is most widely used type DAC.	(5) It is not preferable practically.

Specifications of D/A converters (or) parameters of D/A converters:-

The characteristics of a D/A converters, which are generally specified by the manufacturers are:-

(1) Resolution (2) Linearity (3) Accuracy (4) Setting time

(5) Temperature sensitivity (6) Monotonicity (7) Conversion time

(8) Stability.

(1) **Resolution**:- Resolution can be stated as the no. of different analog outputs that can be provided by a DAC.

Thus the resolution of an n-bit DAC is 2^n

$$\text{Resolution} = 2^n \quad ; n = \text{No. of digital inputs.}$$

2nd definition:- Resolution of a DAC can also be stated as, the variation in the analog output due to 1 LSB variation in the digital input.

For an n-bit DAC, $\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$; V_{OFS} = Full scale output voltage.

Also we can define:-

The smallest possible change in the output voltage as a fraction of the full-scale range is called the resolution. It depends on the No. of bits in the input digital word.

If there are n-bits, the resolution is Equal to $\frac{V_{OFS}}{2^n - 1}$

For a 8-bit DAC, the number of possible output voltages is

2^8 i.e, 256.

The smallest possible change is 1/256 of full scale range

V_{OFS} = 5.1 V, n = 8 ; Resolution = $\frac{V_{OFS}}{2^n - 1}$ = $\frac{5.1}{2^8 - 1}$ = 20 mV / LSB

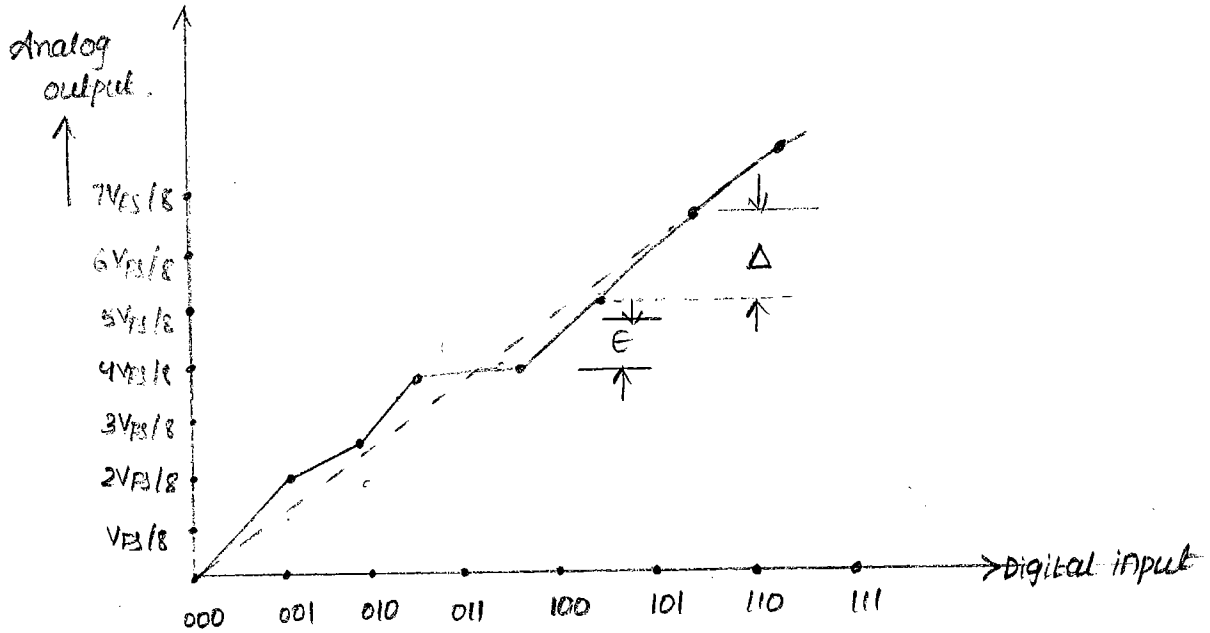
This implies that a change in the digital input by 1LSB causes a change of a 20mV in the analog output.

$\boxed{V_0 = \text{resolution} \times D}$; D = Decimal Equivalent of binary i/p.

(2) Linearity :- Linearity describes how close the measured output appears to its ideal (actual) transfer characteristics.

Thus, the linearity of a DAC is defined as a measure of its accuracy.

Linearity curve of a 3-bit DAC :-



(3) Accuracy :- Accuracy is defined as the difference between the measured output & the actual output (or ideal output)

i.e, closeness of measured output of converter to the actual o/p.

Ideally, the output voltage of a DAC should not differ from the expected output (or) at the worst, the difference should not exceed $\pm \frac{1}{2}$ of its LSB.

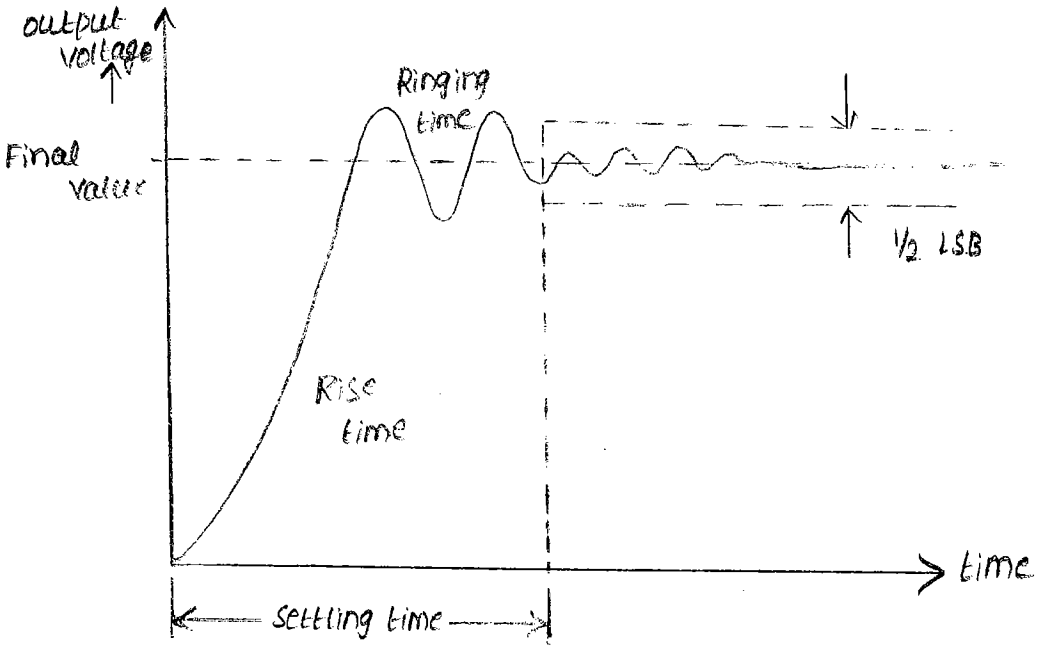
$$\text{Accuracy} = \frac{V_{OFS}}{(2^n-1)^2}$$

, V_{OFS} = Full scale output voltage.

(4) Settling time:-

It is defined as the time taken by the output of converter to reach and stay with in $\pm \frac{1}{2}$ LSB of its final value for a given change in the input.

* settling time of a converter varies from 100ns to 10μsec.



(5) Temperature Sensitivity:-

The analogue output voltage for a given digital i/p word changes with temperature. This is caused by the variation

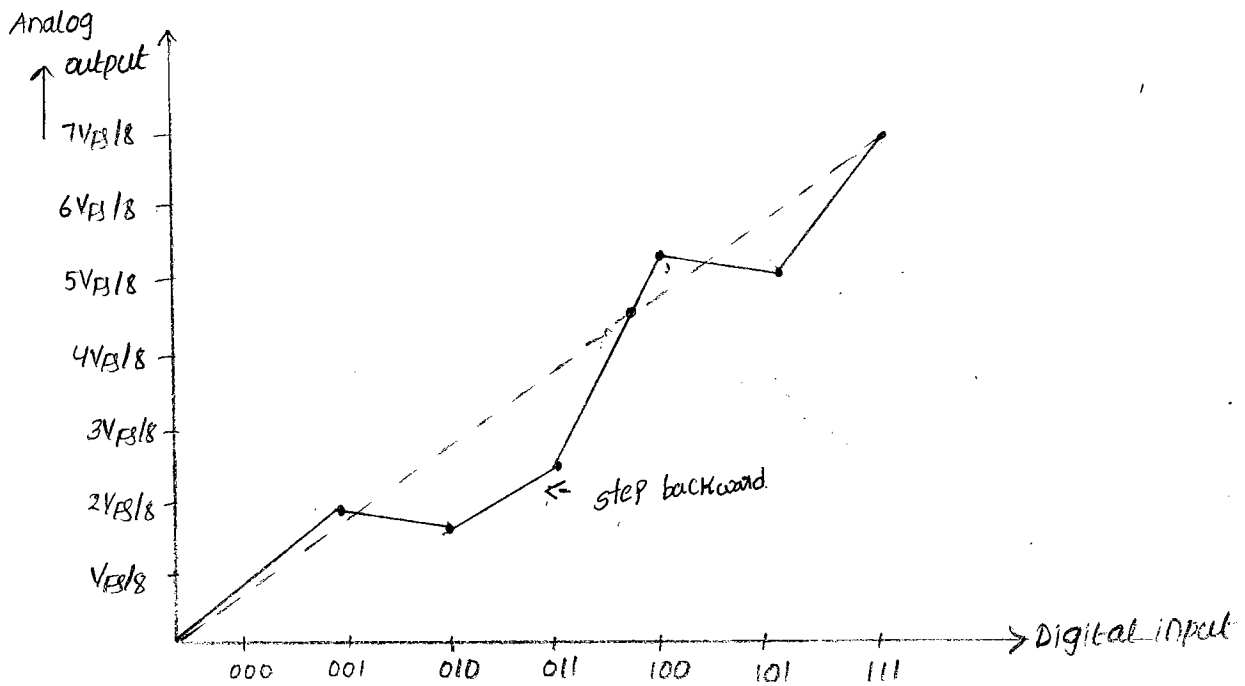
of the resistor values and the reference voltage with temperature. It is specified as ± PPm/°C

(6) Monotonicity:- Monotonicity of DAC is defined as no. of variation (or) linear increase in the analog output for an increase in the digital input.

A DAC is said to have good monotonicity if it do not miss any step backward, when stepped through its entire range by a counter.

If the output of DAC does not increases linearly (or) sometimes decreases for a linear increase in input, then the DAC is said to be Non-monotonic DAC. A DAC is monotonic, provided its linearity Error is maintained $\leq \pm \frac{1}{2}$ LSB at Each output.

Transfer characteristics of monotonic DAC:-



(7) conversion time :-

It is the time required for conversion of analog signal into its digital equivalent, it is also called setting time. It depends on the response time of the switches and output of amplifier.

It is one of the most important performance parameters of ADC. The conversion time of ADC depends on

→ The conversion technique Employed.

→ propagation delay of components used in the circuit.

(8) Stability :-

The performance of a converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity Error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.

→ Errors :-

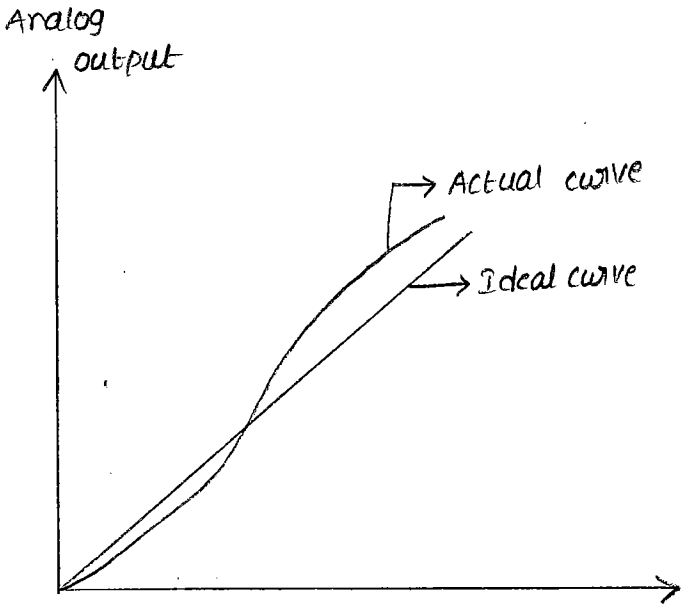
In relation to Digital to Analog converter, there are 3 types of Errors.

(1) Linearity Error (2) offset Error (3) Gain Error.

(1) Linearity Error :-

The transfer characteristics of a DAC is practically a straight line passing through the origin. However in actual practice, the transfer curve may not be exactly linear.

Definition :- Linear error may be defined as the difference between the actual output & the ideal output of DAC.

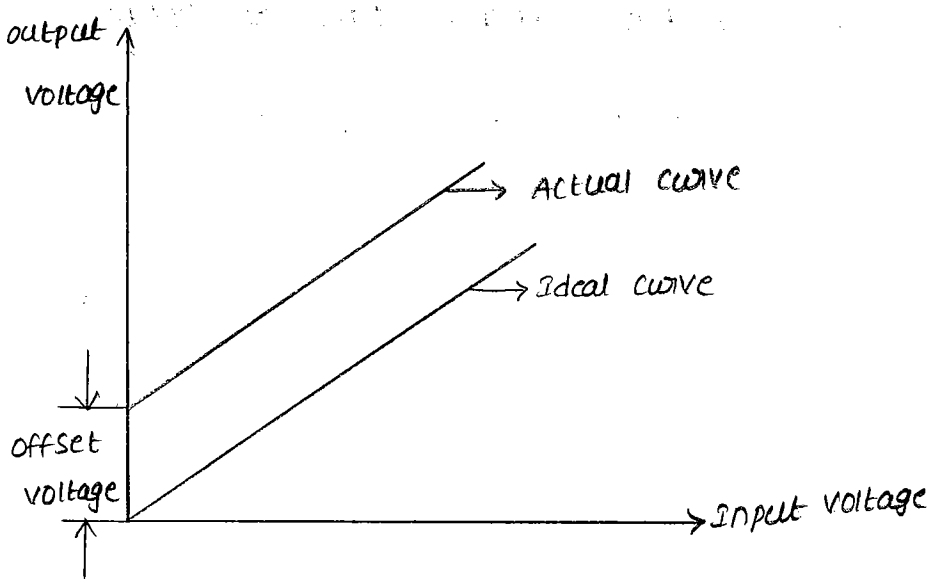


* Linear Error is caused mainly by Errors in the current source resistor values.

(2) Offset Error :-

Ideally, when the input to the DAC is zero, the output must be zero. But in practical DAC, it is observed that even for zero input, there is small output voltage. This is due to the fact that the op-Amp used in DAC ckt has offset voltage and leakage currents are present in the current switches.

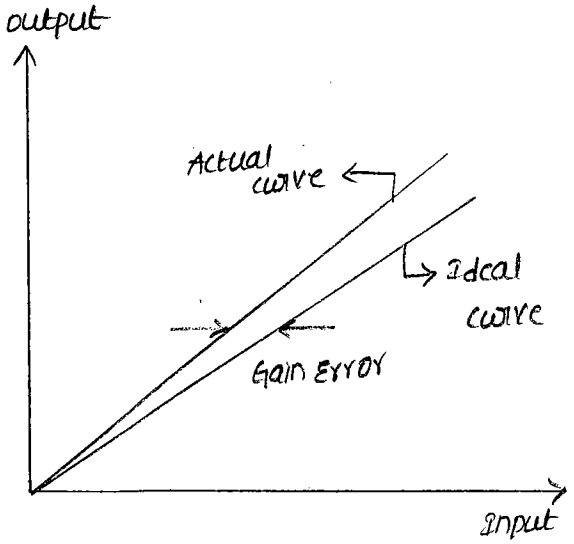
Definition :- Offset Error is defined as the non-zero level of the output voltage, when the input is zero.



(3) Gain Error:-

Gain Error is defined as the difference blw the calculated gain and the actual gain, in related to a current-to-voltage converter.

* Gain Error is caused by errors in the feedback resistors of the op-Amp.



* IC 1408 DAC

IC 1408 is a monolithic 8-bit DAC, it is mainly consists of R-2R ladder, switches and the feedback resistor, all incorporated in a single chip. Such DAC's are available for 8-bit (or) 16-bit resolution.

The 8-bit DAC 1408 is one such typical monolithic IC, with a current output. The converter is compatible with both

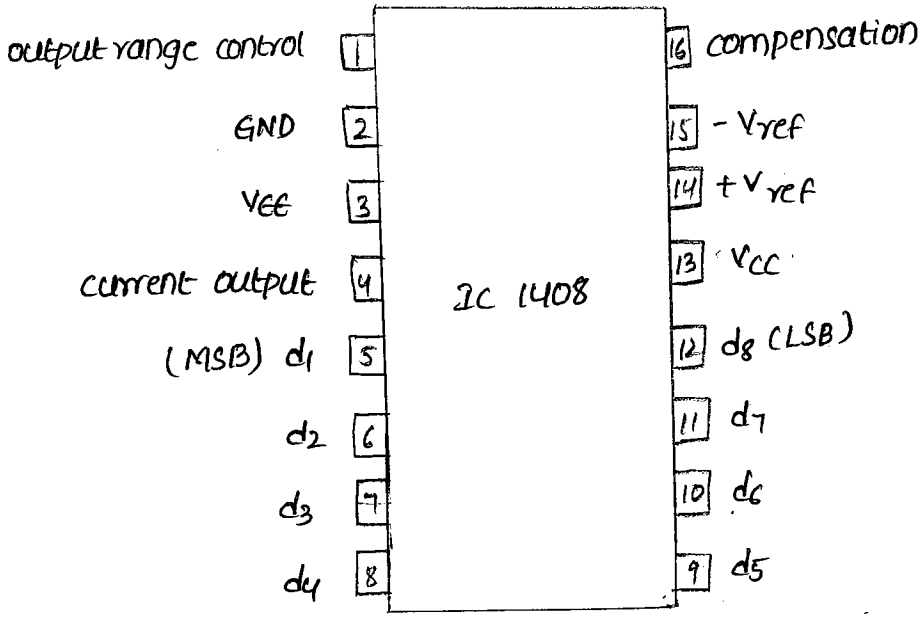
TTL & CMOS logic. It has setting time of 300ns.

There are 8 input data lines $d_1, d_2, \ldots, d_8$.

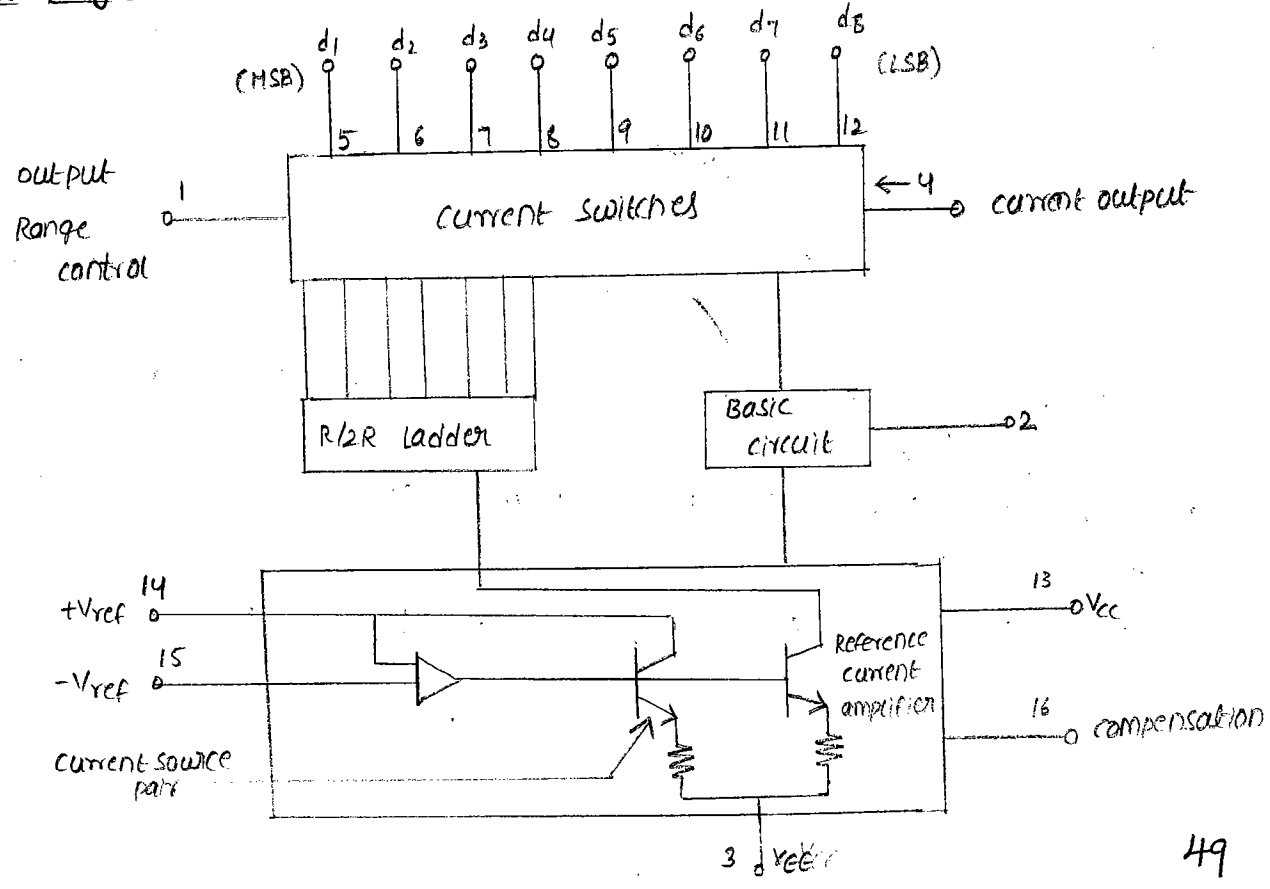
d_1 = MSB d_8 = LSB

It requires 2 power supplies $V_{cc} = +5V$ & $-V_{ee} = -5V$ and a reference current of 2mA for full scale input.

Pin diagram of 8-bit DAC 1408:-



Block diagram:-

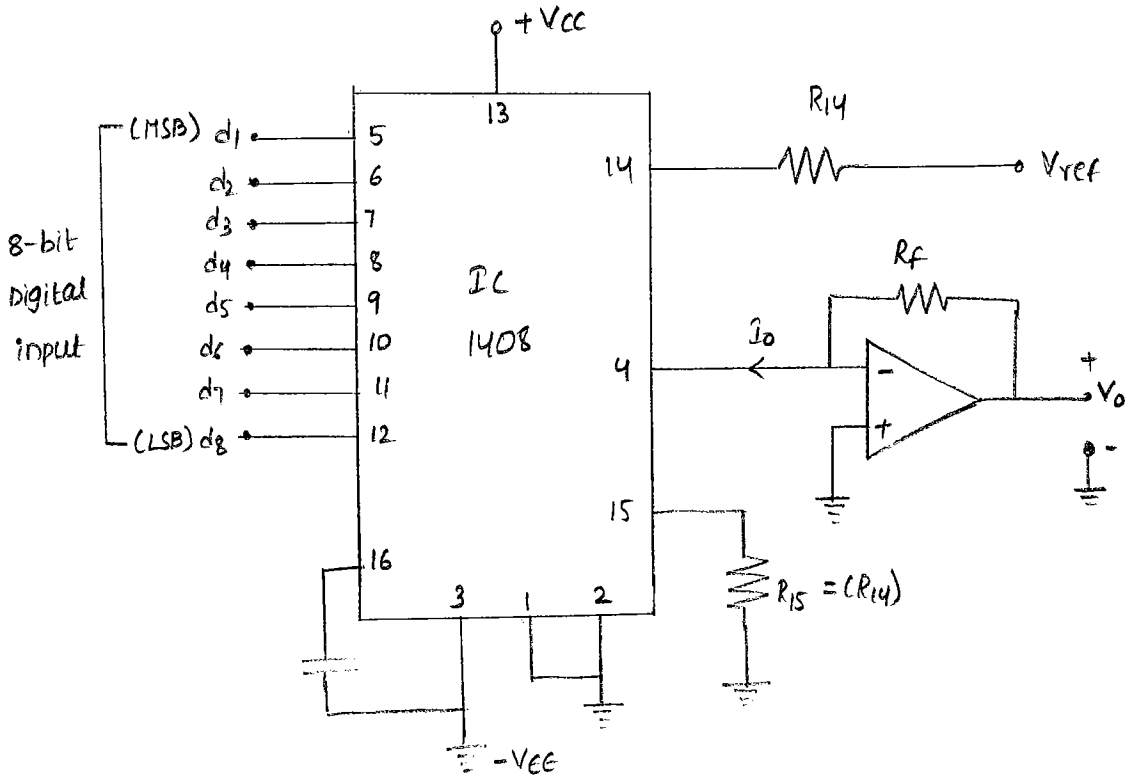


The reference voltage V_{ref} and resistor R_{14} determines the total current source. Resistor R_{15} is equal to R_{14} so as to match the input impedance of the current source Amplifier

output current $I_0 = \frac{V_{ref}}{R_{14}} \left[\frac{d_1}{2^1} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \frac{d_4}{2^4} + \frac{d_5}{2^5} + \frac{d_6}{2^6} + \frac{d_7}{2^7} + \frac{d_8}{2^8} \right]$

$$I_0 = \frac{V_{ref}}{R_{14}} \sum_{i=1}^{8} d_i \, 2^{-i} \qquad d_i = 0 \text{ (or) } 1$$

Typical circuit of IC 1408 DAC:-



Characteristics of 1408 IC:-

(1) power supply range → $V_{cc} = +5V$; $V_{ee} = -5V$ to $-15V$

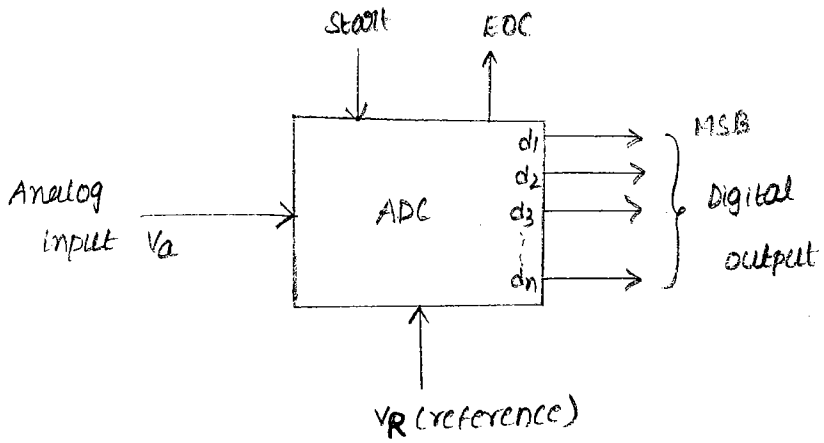
(2) Reference current for maximum input scale → 2mA

(3) Maximum output current → 1.992 mA

(4) Setting time → 300 nsec ; (5) Accuracy → 0.19%

Analog to Digital converter:-

Block diagram of ADC:-



Analog to Digital converter allow an analog i/p voltage & produces an o/p binary word $d_1, d_2, d_3, \ldots, d_n$.

$$D = d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}$$

An ADC has 2 additional control lines.

The start input to tell the ADC when to start the conversion and the EOC [End of conversion] output to announce when the conversion is completed.

Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD (or) LED displays.

ADC's are classified broadly into 2 groups according to their conversion technique.

(1) Direct type ADCs

(2) Integrating type ADCs (Indirect)

Direct type ADCS

It compares a given analog signal with the internally generated equivalent signal.

This group includes

-> Flash (comparator) type converter

-> counter type converter

-> Tracking (or) service converter

-> Successive approximation type converter.

Integrating type ADCS:-

Integrating type ADC'S perform conversion in an indirect manner by first changing the analog input signal to a linear function of time (or) frequency and then to a digital code.

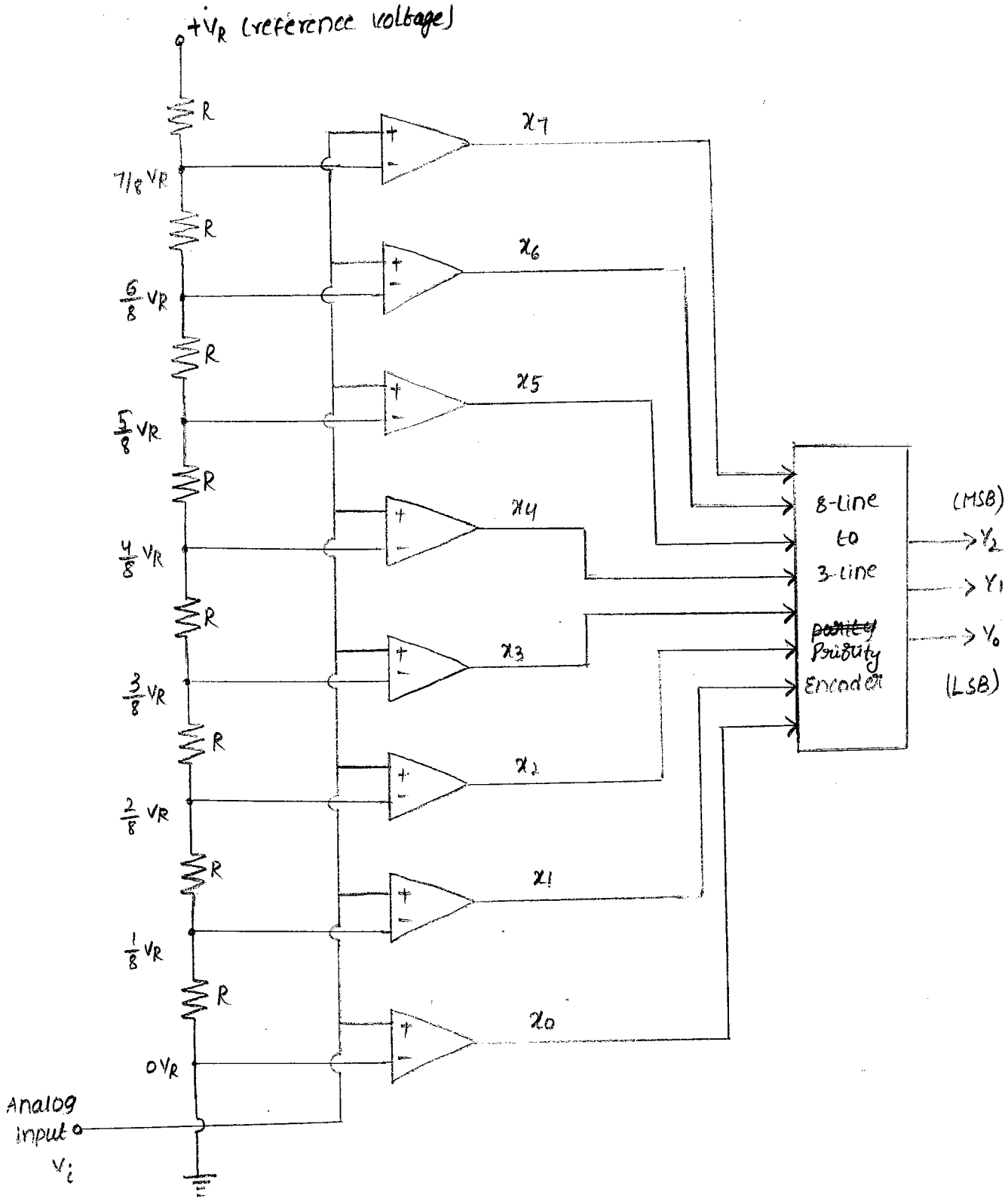
The 2 most widely used integrating type of converters are (1) charge balancing DADC (2) Dual slope DADC

Direct type ADC:.

The parallel comparator (Flash) A/D converters:-

It is the simplest A/D converters and at the same time the fastest and most expensive technique.

Flash type A/D converter (3-bit)



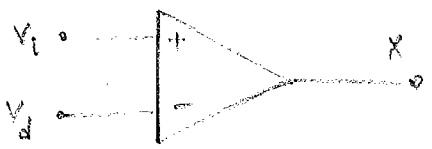
The circuit consists of a resistive divider network, 8 op-Amp comparators and a 8-line to 3-line encoder.

Since all the resistors are equal value, the voltage levels available at the nodes are equally divided between the

reference voltage V_R and the ground.

The purpose of the circuit is to compare the analog i/p voltage V_a with each of the node voltages.

Truth table for the comparator



voltage input	Logic output X
$V_i > V_d$	X = 1
$V_i < V_d$	X = 0
$V_i = V_d$	previous value.

Truth table for the ADC :-

Input voltage V_i	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to 1/8 V_R	0	0	0	0	0	0	0	1	0	0	0
1/8 V_R to 2/8 V_R	0	0	0	0	0	0	1	1	0	0	1
2/8 V_R to 3/8 V_R	0	0	0	0	0	1	1	1	0	1	0
3/8 V_R to 4/8 V_R	0	0	0	0	1	1	1	1	0	1	1
4/8 V_R to 5/8 V_R	0	0	0	1	1	1	1	1	1	0	0
5/8 V_R to 6/8 V_R	0	0	1	1	1	1	1	1	1	0	1
6/8 V_R to 7/8 V_R	0	1	1	1	1	1	1	1	1	1	0
7/8 V_R to 8/8 V_R	1	1	1	1	1	1	1	1	1	1	1

Encoder compares the code resulting from the comparators into binary code.

Advantages:-

→ It has high speed, as the conversion takes place simultaneously rather than sequentially.

→ Typical conversion time is less.

→ conversion time is limited only by the speed of the comparator and of the ~~primary~~ priority Encoder.

Dis-advantages:-

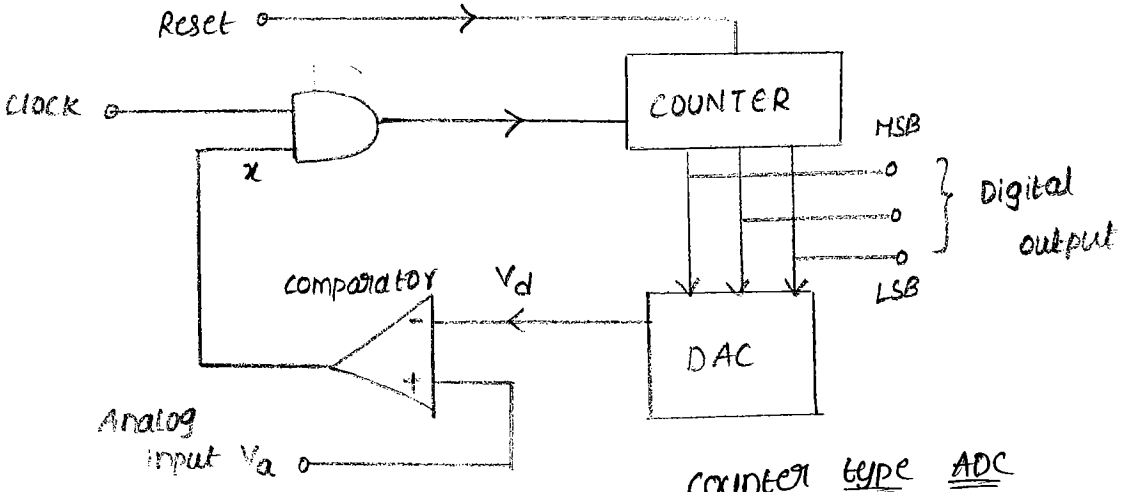
→ The number of comparators required almost doubles for each added bit

→ The larger value of n, the more complex is the priority encoder.

Counter type A/D converters (or ADC using DAC):-

The counter type ADC is also referred to ADC using DAC, since the ckt uses a DAC.

The basic principle Employed in this type of ADC is that the linear ramp can be produced by connecting the o/p of a counter to the i/p of a DAC.



Counter type ADC

Circuit operation :-

→ Initially, the counter is cleared by appling a reset signal & it displays 0000

→ The output of the DAC also will be '0'

→ When the analogue input signal is larger than the input from DAC, the AND gate is Enabled and the clock steps up the counter to 0001

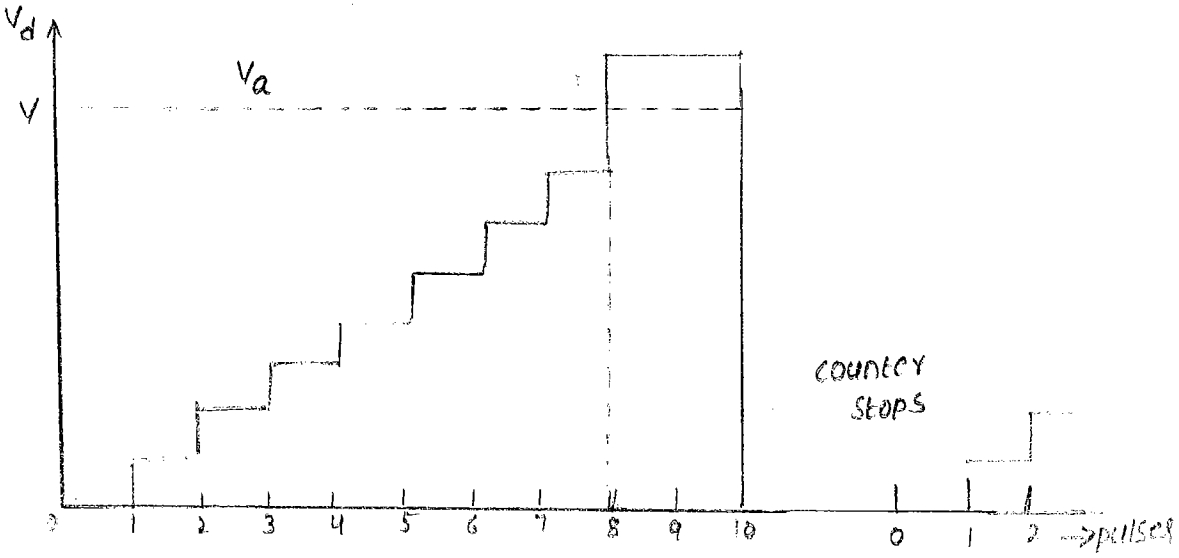
→ As long as the output of the DAC is smaller than the analog input, the clock signal continues to increase the count number.

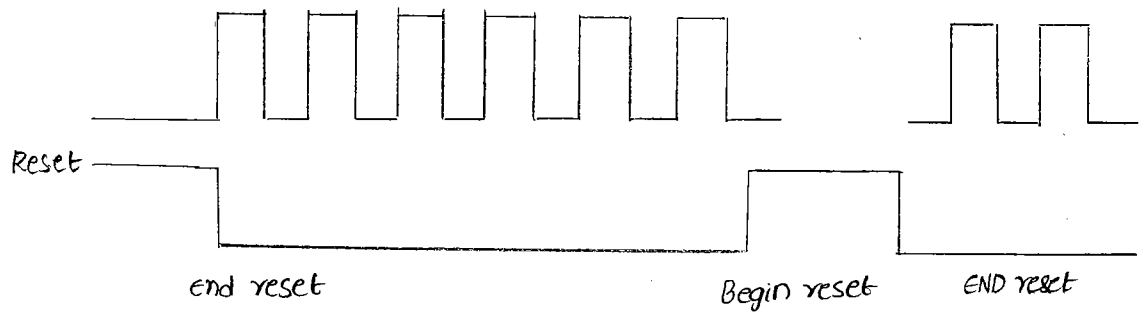
→ The moment the DAC output exceeds the analog input voltage, the AND gate is disabled & the clock no longer steps up the counter.

→ The counter output displayed by the counter represents the digital equivalent of the analog input signal.

→ The counter can be started again to get a new reading by applying the reset pulse.

Waveforms :-





Because of the appearance of the waveform V_0, the counter converter is also called ramp converter.

Advantage :-

Its operation is simple and it requires less hardware components.

Disadvantages :-

→ Its conversion time depends on the amplitude of the analog ip voltage. Therefore, for a high ip voltages, the conversion time will be high.

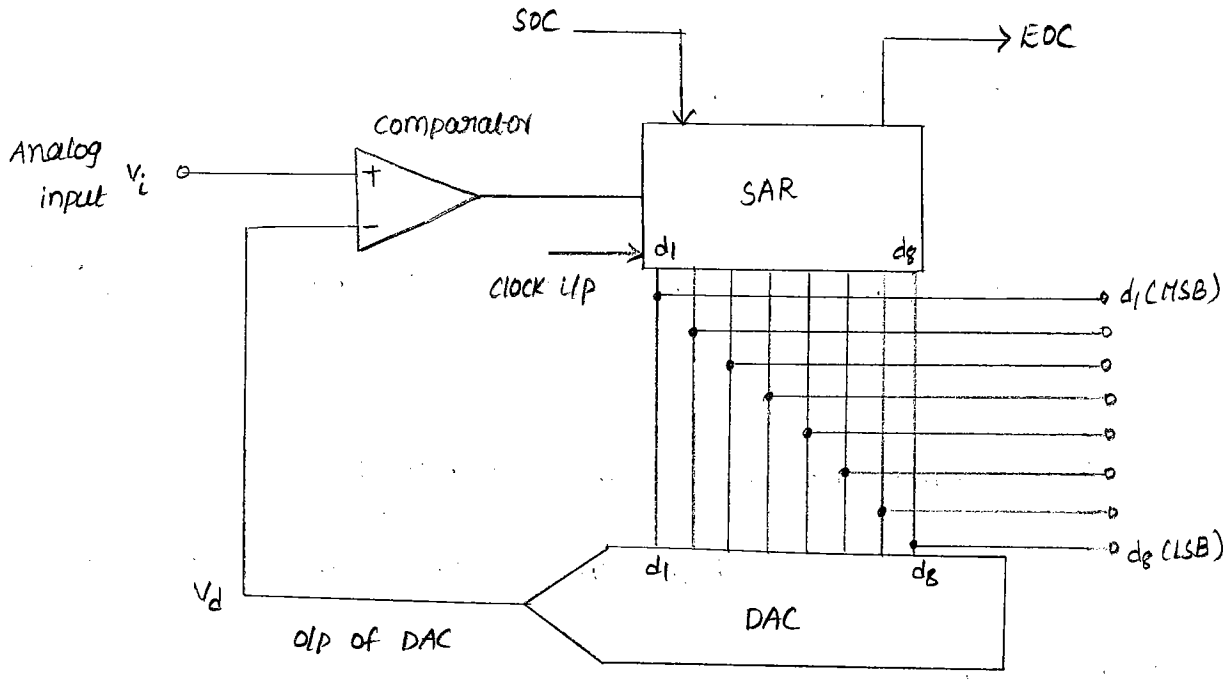
→ The counter has to be reset for every new count.

Successive approximation ADC converter:-

A successive approximation A to D converter is based on a very Efficient code searching strategy called binary search.

The searching process is very fast, an-bit conversion being completed in only n clock periods.

Block diagram of Successive approximation ADC:-



SOC : Start of conversion EOC: End of conversion.

- The ckt uses a SAR, DAC and a comparator.
- The External clock i/p sets the internal timing parameters.
- The SOC signal starts the process of conversion and the activated EOC signal announces the end of the conversion process.

Operation :-

The SOC signal initiates the process of search. The SAR sets the MSB (MOST significant bit) $d_1 = 1$, as soon as the START signal arrives, and all other bits are set to 0.

If the converter is a 8-bit converter, the initial setting would be 10000000. The output V_d of the DAC for this trial code is compared with the analog input V_i.

If the analog input V_i is greater than the DAC O/P V_d, it implies that the trial code 10000000 is less than the correct digital representation of V_i. The MSB d_1 is left at 1 and the next lower significant bit is set at 1, and the process is repeated.

If, on the other hand, the input V_i is less than the DAC output V_d, it implies that the trial code 10000000 is greater than the correct digital representation of V_i in such an Event, the MSB is set to 0, and the next lower significant bit is set to 1, and the process is repeated.

Thus, the above process of comparision is repeated for all the subsequent bits, one at a time until all bit positions have been tested.

The comparator changes state whenever the DAC o/p crosses V_i and this activates the EOC command.

conversion sequence :-

correct digital representation	SAR o/p V_d at different stages	comparator output
10110010	10000000	1
	11000000	0
	10100000	1
	10110000	1
	10111000	0
	10110100	0
	10110010	1
	10110011	0

comparator o/p after comparing all 8-bits = 10110010

Digital representation of analog i/p.

* The time required for one conversion from analog to digital depends on both the clock period T and the number of bits n.

conversion time, $T_c = T(n+1)$

Advantages :-

→ provides Excellent resolution.

→ It's conversion speed is high.

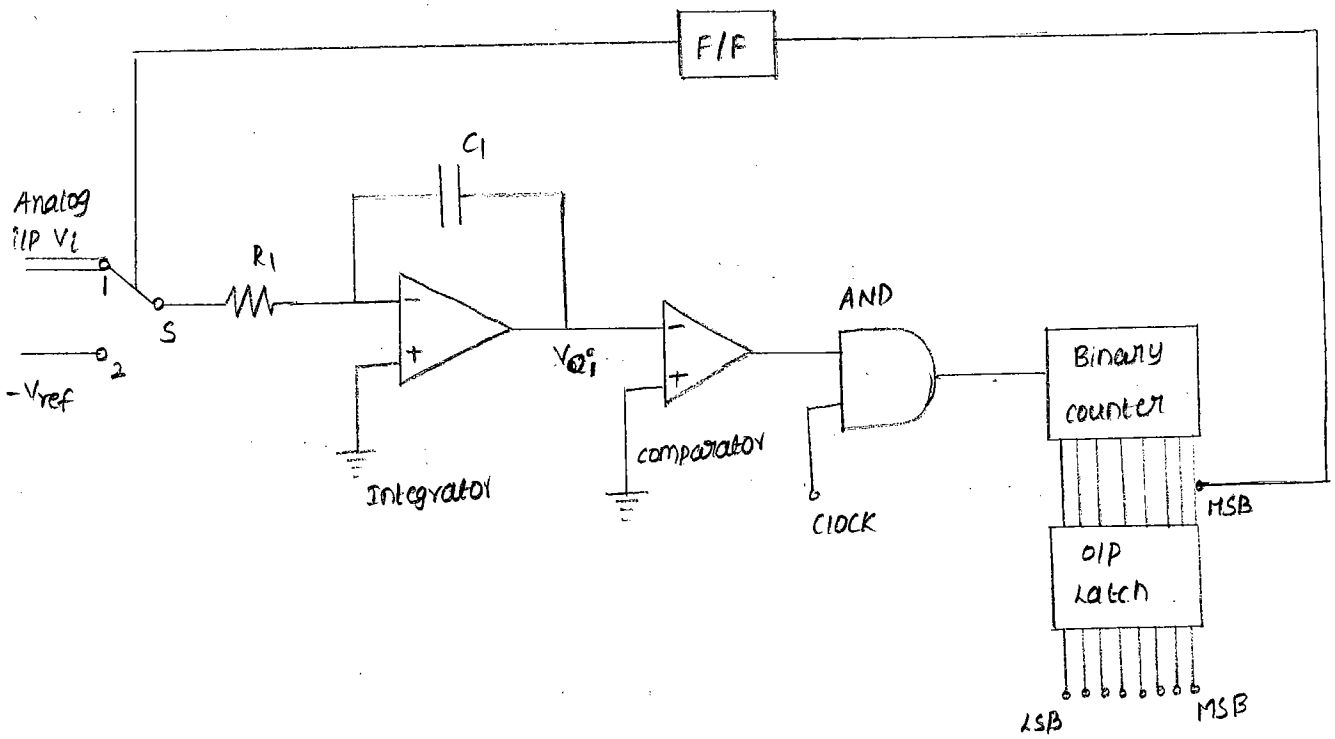
Dual slope DAC/ADC:-

The dual slope DAC is an integrator type D to A converter. Its accuracy is quite high, Even though the speed of operation is quite low.

The ckt uses an integrator & a flip-flop in addition to a comparator and binary counter.

In the dual slope DAC, the analog input voltage and a reference voltage are both converted into time periods by means of an integrator, and are then measured by means of a counter.

Block diagram:-



The integrator is a ramp generator.

There is a switch arrangement S by which the integrator input can be switched btw the analog i/p voltage V_i and a -ve reference voltage $-V_{ref}$

The switch is controlled by the MSB of the binary counter.

- When the MSB is a logic 0, the switch closes on terminal 1 at which the input voltage is applied.
- When the MSB is a logic 1, the switch closes on terminal 2 at which the reference voltage is applied.

Operation :-

Let Analog switch close on terminal 1 at t=0. The analog input voltage V_i gets applied at the inverting terminal of the integrator.

The integrator output is given as

$$V_{o1} = \frac{-1}{R_1C_1}\int_0^{t_1} V_i\,dt = \frac{-V_i t_1}{R_1 C_1} \quad ; V_{o2} = \frac{-1}{R_1C_1}\int_0^{t_2} -V_{ref}\,dt = \frac{V_{ref}}{R_1C_1}t_2$$

V_{o1} is o/p for analog i/p V_{o2} is o/p for Vref voltage

If V_i is assumed to be constant over the interval 0 to t_1, R_1C_1 is the time constant of integrator.

- The integrator output voltage is applied to the comparator. The comparator output goes high, it Enables the AND gate and the clock pulses reach the counter.

At the End of 2^n clock periods, the MSB of the counter goes high. This causes the output of the flip flop to go high with the result that the analog switch S from position 1 to position 2, and connect reference voltage to the integrator inverting terminal.

Simultaneously the binary counter gets reset the -ve reference voltage $-V_R$ which now forms the i/p to the integrator makes the output of the integrator increase as a +ve linear ramp. When it reaches zero level, the comparator output goes low, and this disables the AND gate and the result of it is that the clock pulses cease to reach the counter. The counter stops at a count corresponding a time interval t_2.

Since the integrator output voltage, originally zero drops to a definite voltage V in time t_1, and rises to the original voltage V_i zero in time t_2.

charge voltage = Discharge voltage

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1} \Rightarrow V_i t_1 = V_R t_2 \text{ (or) } t_2 = \frac{V_i t_1}{V_R}$$

In the above Expression for t_2, V_R & t_1 are fixed. Hence $\boxed{t_2 \propto V_i}$

That is t_2 is directly proportional to the analog input voltage hence is a measure of it. The output of the counter is binary number which corresponds to time t_2.

Thus the binary digital output of the counter is also proportional to the analog input.

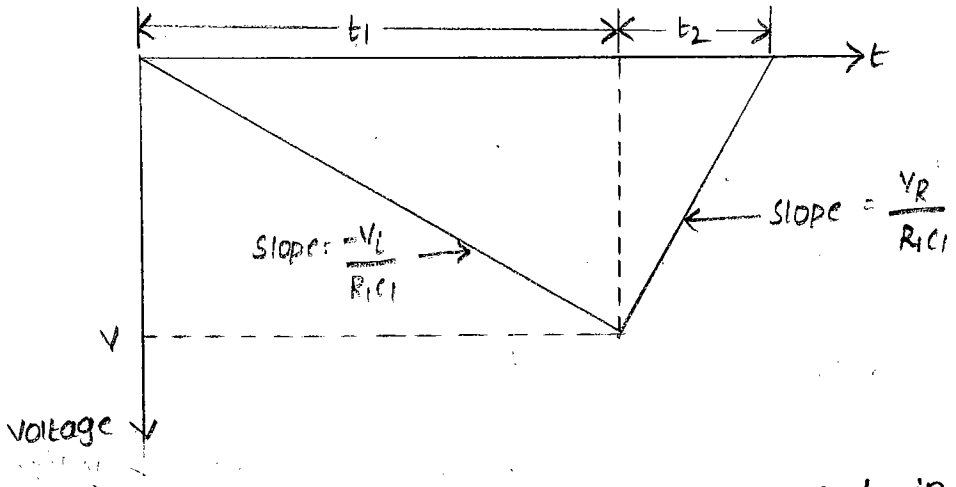
We have digital output of the counter = (counts/sec) t_2

But $t_2 = V_i t_1 / V_R$

Digital output of the counter = (count/sec) $\cdot t_1 \left(\frac{V_i}{V_R}\right)$

The counter output is displayed suitably.

The waveform of the integrator output voltage:-



The dual slope ADC is very widely used in practice in view of its many advantages.

Advantages:-

→ It posses a high degree of accuracy

→ It is cheap

→ Its performance is not adversely affected by change of temperature.

Demerits:- Speed of operation is some what low.

Compare merits and Demerits of A/D converters:-

(1) Flash (or) parallel comparator type ADC

Merits

→ It is the fastest ADC compared to all other ADCs. Its conversion time is $\leq$ 100ns

→ Its circuit design is simple.

Demerits

→ Its accuracy is low

→ It is not suitable for analog to digital conversion with more than 3 (or) 4 digital output bits.

→ Since this technique requires $2^n - 1$ comparators, the number of comparators increases with the increase of number of bits.

(2) Successive Approximation type ADC:-

Merits:-

→ Its conversion speed is high

→ It provides excellent resolution

→ It requires less hardware

Demerits :- Its conversion process is long compared to flash type ADC.

(3) counter type ADC:-

Merits:-

→ Its operation is simple

→ It requires less hardware components.

Demerits:-

→ Its conversion time depends on the amplitude of the Analog input voltage. Therefore, for a high input voltage, the conversion time will be high.

→ The counter has to be reset for every new count.

(4) Tracking type ADC:-

Merits:-

(1) Its conversion time is low i.e, the process of analog to digital conversion is very fast compared to counter type ADC.

(2) It requires a few hardware components.

Demerits:-

(1) The conversion time is not constant & varies based on the last converted value.

(2) The output of ADC will be maintained with in 1 LSB of the correct digital value as long as the V_a (Analog input voltage) varies slowly, But for a rapid change in V_a, the effective tracking with the changes in V_a cannot be achieved.

(3) It needs an additional logic circuit to control the operations of up/down counter.

(5) Dual slope ADC:-

Merits

(1) It has high accuracy

(2) It provides Extremely high resolution.

(3) It is economical

(4) Highly immune to temperature & noise.

Demerits:-

(1) Its major drawback is that the conversion time is very high. Therefore, its speed of conversion is very low.

(2) It is only suitable for slowly varying signals.

Problems

(1) Design an Astable multivibrator using an op-amp to generate a frequency of 1KHz.

Sol Time period of Astable is given by $T = 2R_f C \ln\left[\frac{2R_1+R_2}{R_2}\right]$

$$T = \frac{1}{f} = \frac{1}{1KHz} = \frac{1}{1\times10^{+3}} = 1\times10^{-3}\ sec = 1\ msec.$$

Assuming $\ln\left[\frac{2R_1+R_2}{R_2}\right] = 1$

$$2R_1 + R_2 = e^1 \cdot R_2$$

$$2R_1 = 2.718\,R_2 - R_2$$

$$= 1.718\,R_2$$

$$R_2 = \frac{2}{1.718}R_1 = 1.16\,R_1$$

$\therefore R_2 = 1.16\,R_1$

Assume $R_1 = 10\ K\Omega$

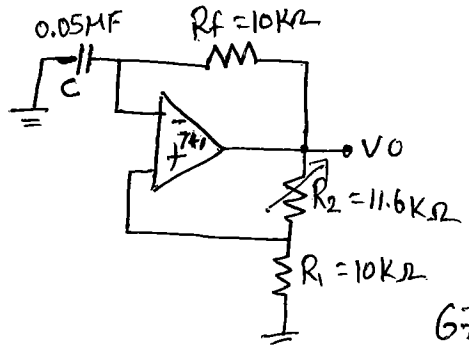
$\therefore R_2 = 10\times1.16 = 11.6\ K\Omega$ (we can use 20KΩ Potentiometer)

Now $T = 2R_f C$

assume $C = 0.05\ MF$.

$$1\times10^{-3} = 2R_f(0.05\times10^{-6})$$

$$R_f = 10\ K\Omega$$



(2) Calculate the values of the LSB, MSB & full scale output voltage for an 8-bit DAC for 0 to 10V range.

Sol Given, $n = 8$.

o/p Range = 0 to 10 V

$\therefore$ Full scale output voltage = $V_{OFS} = 10\,V$

$$LSB = \text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{10}{2^8 - 1} = \frac{10}{256-1} = \frac{10}{255}$$

$$= 0.039\,V$$

$$= 39\,mV$$

$$MSB = \frac{V_{OFS}}{2} = \frac{10}{2} = 5V$$

$$\rightarrow \left[V_0 = V_R \left[\underbrace{d_1 2^{-1}}_{MSB=1} + d_2 2^{-2} + \cdots \right] \right]$$

(3) Find the digital output of an dual slope ADC, having $t_1 = 83.33$ ms and V_R as 200 mV for an input voltage of 100mV, & the clock frequency is 12KHz.

$$t_2 = \left(\frac{V_i}{V_R}\right) t_1 = \left(\frac{100}{200}\right) 83.33 \times 10^{-3} = 416.65\ m.s$$

$$\text{clock} = 12KHz = 12000 \text{ counts/sec.}$$

$$\text{Digital output} = \left(\frac{\text{Counts}}{\text{sec}}\right) t_2 = 12000 \times 416.65 \times 10^{-3}$$

$$\simeq 5000 \text{ counts.}$$

$$(5000)_{10} = \underbrace{(100\ 111000\ 1000)_2}_{o/p}$$

④ Calculate the number of bits required to represent a full scale voltage of 10 volts with a resolution of 5 mV.

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$$

$$2^n = \frac{V_{OFS}}{\text{Resolution}} + 1 = \frac{10}{5\times10^{-3}} + 1 = 2001$$

$$n \simeq 11$$

⑤ LSB of 9-bit DAC is represented by 19.6 mVolts.

(i) Find output of DAC for an input, 10110 1101 & 01101 1011.

(ii) what is full scale output voltage.

Sol

(i) $(10110\ 1101)_2 = (365)_{10}$

o/p voltage = Resolution × D

$= 19.6 \times 365 \times 10^{-3} = 7.154$ V.

$(01101\ 1011)_2 = (219)_{10}$

o/p voltage = $19.6\times10^{-3} \times 219 = 4.29$ V

(ii) $V_{OFS} = (2^n - 1) \cdot \text{Resolution}$

$= (2^9 - 1) \times 19.6 \times 10^{-3}$

$= 10$ V

→ What output voltage would be produced by a DAC controller whose o/p range is 0 to 10V and whose input binary number is: (i) 0110 (4 bit DAC) (ii) 10111100 (8 bit DAC).

(i) Given, $V_{OFS} = 10V$

4 bit DAC $N = 4$

Binary = $(0110) = (6)_{10}$

(B) (D)

Resolution = $\frac{V_{OFS}}{2^n - 1} = \frac{10}{2^4 - 1} = \frac{10}{15} = 0.667\,V$

$V_0 = R \times D$

$= (0.667)\ (6) = 4\,V$

(ii) $N = 8$

$V_{OFS} = 10V$

$(10111100)_2 = (188)_{10}$

(B) (D)

Resolution = $\frac{V_{OFS}}{2^n - 1} = \frac{10}{2^8 - 1} = 0.039\,V$

$V_0 = R \times D$

$= (0.039)\ (188) = 7.37\,V$.

→ The LSB of a 10-bit DAC is 20m volts. calculate,

(i) percentage resolution?

(ii) Full-scale range?

(iii) Output voltage for input, 1011001101?

Given, $N = 10$

Resolution = 20mV

(i) percentage resolution = $R \times 100$

$= (20 \times 10^{-3}) \times 100$

$= 0.2\%$

(ii) $V_{OFS} = ?$

$$R = \frac{V_{OFS}}{2^n - 1}$$

$$V_{OFS} = (2^n - 1)R = (20 \times 10^{-3})(2^{10} - 1)$$

$$\boxed{V_{OFS} = 20.46\ V}$$

(iii) Binary data $= (1011001101)_2$

$D = (717)_{10}$

$V_0 = R \times D$

$= (20 \times 10^{-3})(717)$

$$\boxed{V_0 = 14.34\ V}$$

→ The basic step of a 9 bit DAC is 10.3 mv. If "000000000" represents 0V. what output is Produced if the input is "101101111"?

Given $R = 10.3$ mV

$B = (101101111)_2$

$$V_D = R \times D$$

$$= (10.3 \times 10^{-3})\ (367)$$

$$\boxed{V_D = 3.78\ V}$$