Code: 20A04602T **R20**

B.Tech III Year II Semester (R20) Regular Examinations August 2023

VLSI DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1		Answer the following: (10 X 02 = 20 Marks)	
	(a)	What are the advantages of BiCMOS process compare with the CMOS?	2M
	(b)	List the fabrication procedures for IC Technologies.	2M
	(c)	Define scaling and explain it.	2M
	(d)	Explain difference between stick diagram and layout diagram.	2M
	(e)	Write about the clocked CMOS logic and its usage.	2M
	(f)	What are the issues involved in driving large capacitive loads in VLSI circuits?	2M
	(g)	Draw 2-bit comparator.	2M
	(h)	Write the Comparison between FPGA and CPLD.	2M
	(i)	What is BIST?	2M
	(j)	What is the need for testing?	2M

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

2		Draw the fabrication steps of CMOS transistor and explain its operation in detail.	10M
		OR	
3		Draw the fabrication steps of NMOS transistor and explain its operation in detail.	10M
4	(a)	Draw the flow chart of VLSI Design flow and explain the operation of each step in detail.	6M
	(b)	Draw the stick diagram for three input AND gate.	4M
		OR	
5		What is the purpose of design rule? What is the purpose of stick diagram? What are the different approaches for describing the design rule? Give three approaches for making contacts between poly silicon and discussion in NMOS circuit.	10M
6	(a)	Describe about the methods for driving large capacitive loads.	5M
	(b)	Describe about the choice of fan – in and fan – out selection in gate level design.	5M
		OR	
7		Explain the following: (i) Switch logic. (ii) Sheet resistance R_s and its concepts to MOS.	10M
8	(a)	Design a shift register with the dynamic latch operated by a two-phase clock.	5M
	(b)	Explain the working principle of Ripple carry adder using Transmission Gates.	5M
		OR	
9	(a)	Explain the detailed logic configurable Block Architecture of FPGA.	5M
	(b)	Write a note on the different Parameters influencing low power design.	5M
10		Explain about design for testability.	10M
		OR	
11		Explain the following in detail: (i) Scan design techniques. (ii) Testability and practices.	10M

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R20

B.Tech III Year II Semester (R20) Supplementary Examinations January 2024

VLSI DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a)	Why NMOS technology is preferred more than PMOS technology?	2M
(b)	What is pass transistor?	2M
(c)	List out the sources of static and dynamic power consumption.	2M
(d)	Explain about the contact cuts and approaches.	2M
(e)	Write about the clocked CMOS logic and its usage.	2M
(f)	Define Fan-in and Fan-out.	2M
(g)	Design a 2-bit Parity generator.	2M
(h)	What is Booth's algorithm?	2M
(i)	Explain about the principle of Built in Self Test.	2M
(j)	Explain about test Principles used for testing.	2M

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

2	(a)	Derive the relationship between I_{ds} and V_{ds}.	5M
	(b)	Determine the pull-up to pull down ratio for NMOS inverter driven by another NMOS Inverter.	5M
		OR	
3	(a)	Write about BiCMOS fabrication in a n-well process with a diagram.	5M
	(b)	Distinguish between Bipolar and CMOS devices technologies in brief.	5M
4	(a)	Discuss about the stick diagrams and their corresponding mask layout examples.	5M
	(b)	Draw the stick diagram of p-well CMOS inverter and explain the process.	5M
		OR	
5	(a)	Explain λ-based Design Rules in VLSI circuit Design.	5M
	(b)	Draw the Layout Diagrams for CMOS Inverter.	5M
6	(a)	Explain different capacitances present in CMOS design	5M
	(b)	Explain the concept of MOSFET as switches with suitable example.	5M
		OR	
7		Explain in detail about sheet Resistance R_s and its concepts to MOS.	10M
8	(a)	Explain the operation of a basic 4 bit adder.	5M
	(b)	Explain about Gate – arrays.	5M
		OR	
9	(a)	Explain about the various factors influencing low power design.	5M
	(b)	Discuss about the standard cells.	5M
10	(a)	Discuss the need for testing.	5M
	(b)	Why the chip testing is needed? At what levels testing a chip can occur?	5M
		OR	
11	(a)	Explain about Scan design techniques.	5M
	(b)	Why stuck – at faults occur in CMOS circuits? Explain with suitable logical diagram.	5M

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