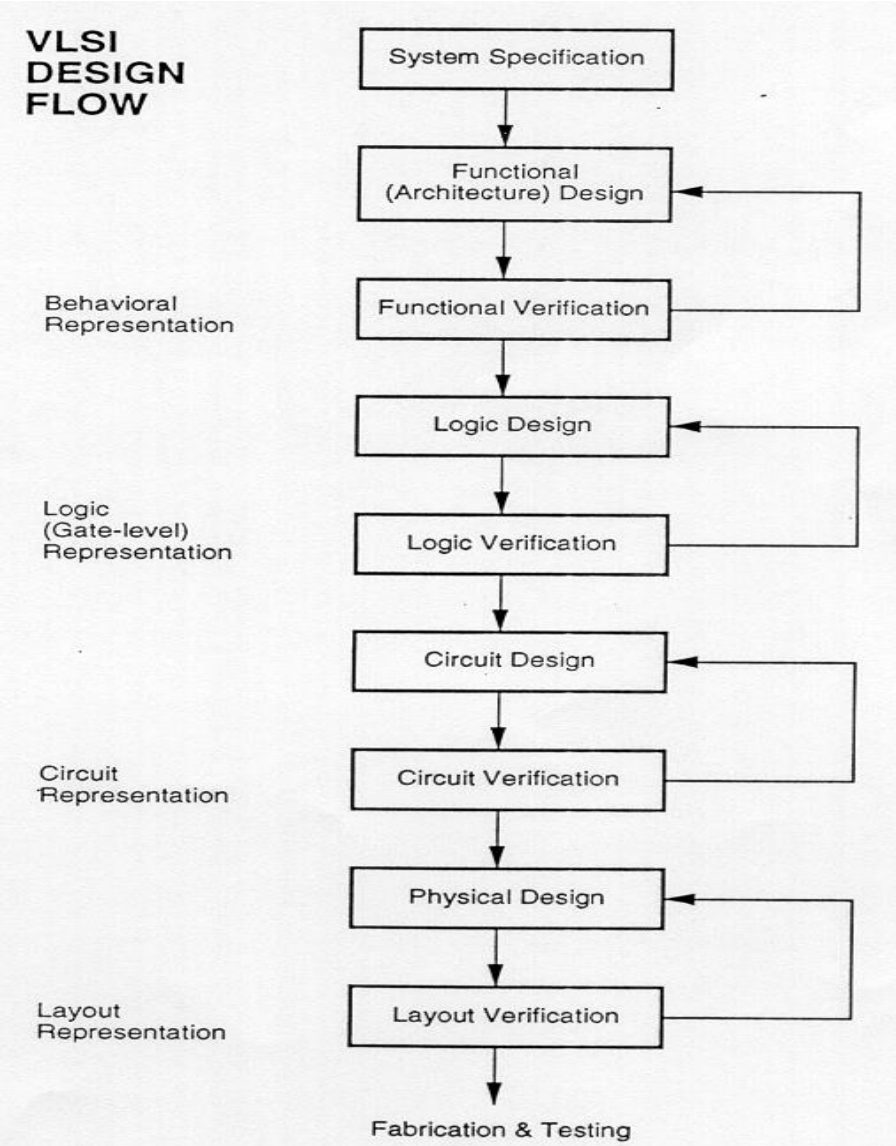
1. a) Explain VLSI design flow.



System specifications:

- The objective of the desired final product is written in this step.
- The designated cost of the system, its performance, architecture, and how the system will communicate with the external world are to be determined.
- The design specification should be provided by the users or clients.

Architectural design:

- The basic architecture of the desired design must meet the system specifications of the desired design.
- Architectural design includes the integration of analog and mixed-signal blocks, memory management, internal and external communication, power requirements, and choice of process technology and layer stacks.

Functional design or Behavioural design:

- The main objective of this is to generate design a high-performance architectural design within the cost requirements posed by the specifications.

Logic Design:

- The structure of the desired design is added to the behavioral representation of the desired design.
- The main specifications to be considered for logic design are logic minimization, performance enhancement, and testability.
- Logic design must also consider the problems associated with test vector generation, error detection, and error correction.

Circuit Design:

- The logic blocks of the desired design are replaced by resistors, capacitors, and transistors.
- Circuit simulation of the desired design is done at this stage, in order to verify the timing behavior of the desired system.

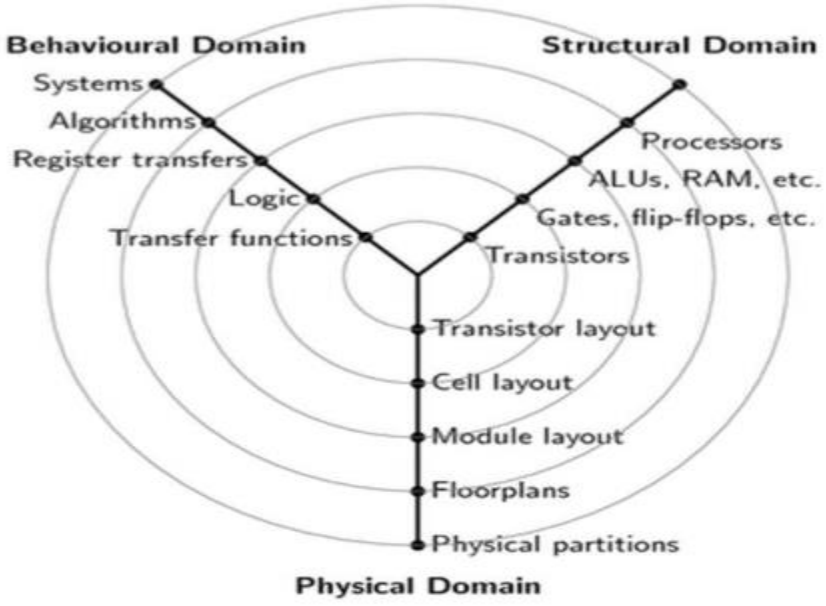
Physical Design:

- The actual layout of the desired system is done.
- Actual layout of the desired system can affect the area, correctness, and performance of the final desired product.
- Errors such as short circuits, open circuits, open channels, etc may result if the design rules are not respected.

Y-chart:

- Introduced by D. Gajski
- Design flow for most logic chips, using design activities on the three different axes (domains).

Behavioral domain Structural domain Geometrical layout domain

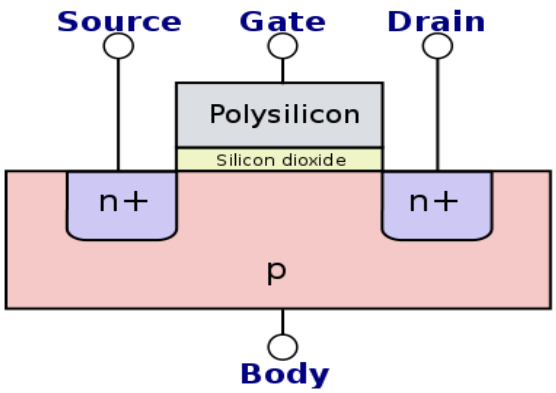


Gajski-Kuhn Y-chart

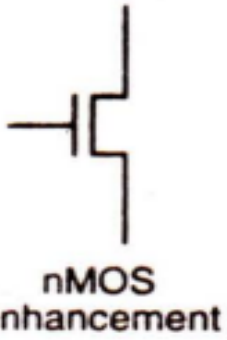
2. **b) What are the steps involved in the nMOS/pMOS fabrication? Explain with neat sketches?**

Fabrication of NMOS transistor:

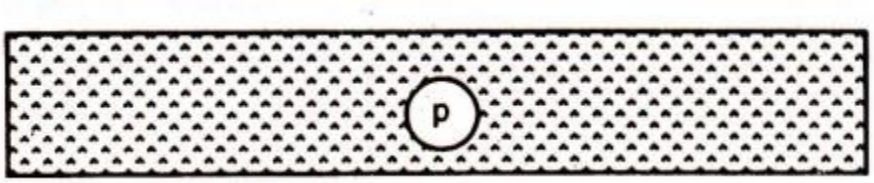
NMOS structure:



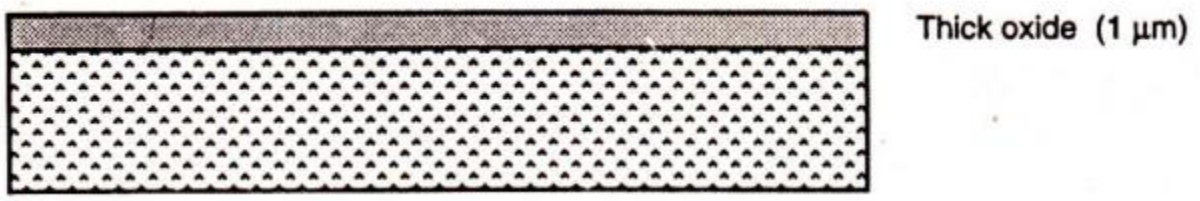
NMOS symbol:



1. Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required p-impurities are introduced as the crystal is grown.

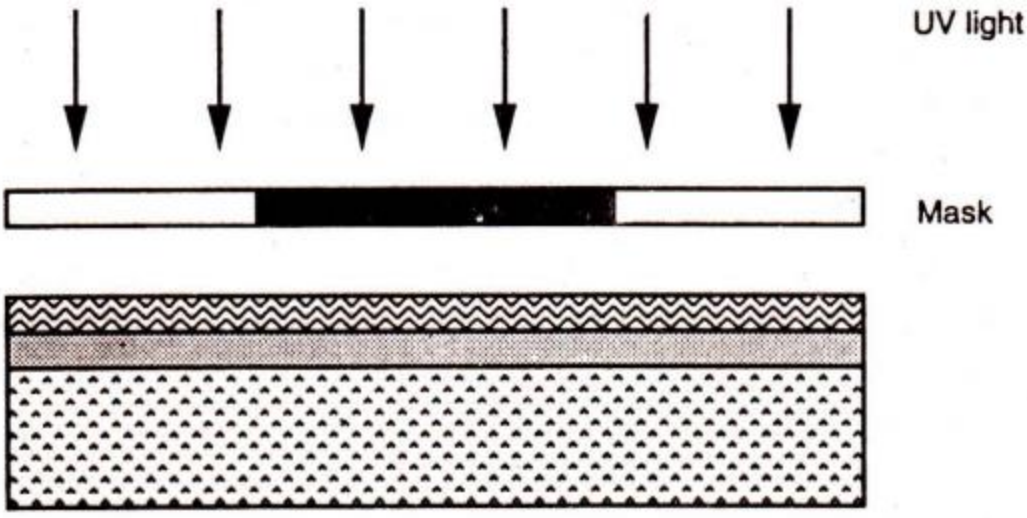


2. A layer of silicon dioxide (SiO_2), typically 1 μm thick, is grown all over the surface of the wafer to protect the surface, act as a barrier to dopants during processing, and provide a generally insulating substrate on to which other layers may be deposited and patterned.



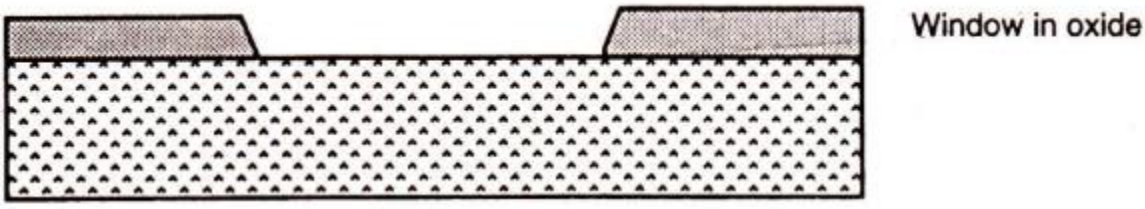
3. The surface is now covered with a photoresist which is deposited onto the wafer and spun to achieve an even distribution of the required thickness.

4. The photoresist layer is then exposed to ultraviolet light through a mask which defines those regions into which diffusion is to take place together with transistor channels.

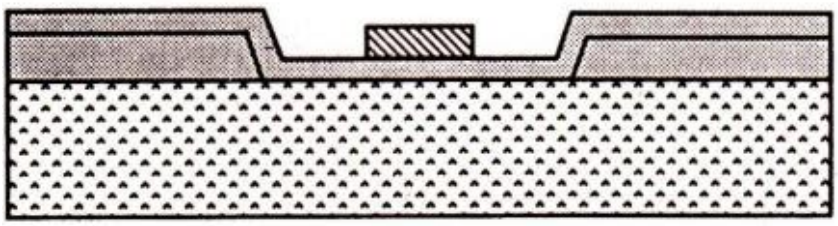


Those areas exposed to ultraviolet radiation are polymerized (hardened), but that the areas required for diffusion are shielded by the mask and remain unaffected.

5. These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask.

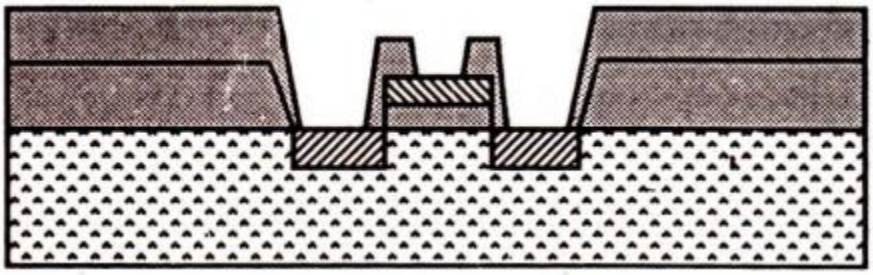


6. The remaining photoresist is removed and a thin layer of SiO_2 (0.1 μm typical) is grown over the entire chip surface and then polysilicon is deposited on top of this to form the gate structure. The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapor deposition (CVD). In the fabrication of fine pattern devices, precise control of thickness, impurity concentration, and resistivity is necessary.
7. Further photoresist coating and masking allows the polysilicon to be patterned (as shown in Step 6).

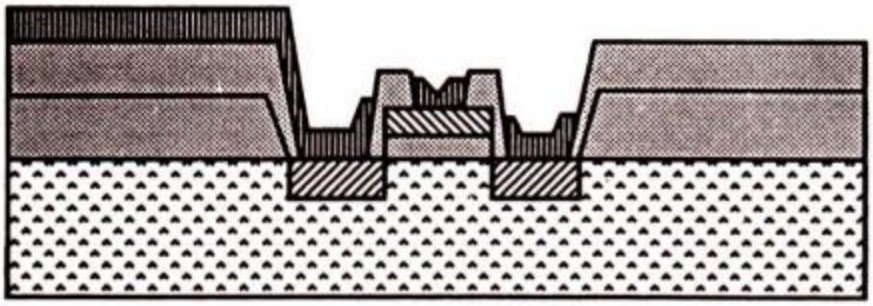


8. Then the thin oxide is removed to expose areas into which n-type impurities are to be diffused to form the source and drain as shown. Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity (for example, phosphorus) over the surface as indicated in Figure 1.8. Note that the polysilicon with underlying thin oxide act as masks during diffusion--the process is self-aligning. 8.

9. Oxide (Si02) is grown over all again and is then masked with photoresist and etched to expose selected areas of the polysilicon gate and the drain and source areas where connections (i.e. contact cuts) are to be made.



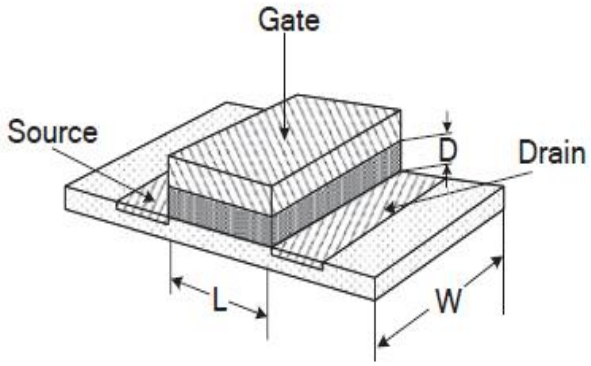
10. The whole chip then has metal (aluminum) deposited over its surface to a thickness typically of 1μm. This metal layer is then masked and etched to form the required interconnection pattern.



2. a) Derive the relationship between drain to source current I_{ds} verses drain to source voltage V_{ds} in non-saturated and saturated region.

I_{ds} : Drain to source current:

L - Channel length of the transistor
W- Width of the transistor.
D – Thickness of the oxide layer.
ε - Permittivity of the oxide layer.
I_{DS} -Dr ain to source current
V_{DS} -Drain to source voltage
Q - Charge induced in the channel
τ - Electron transit time



- The voltage on Gate induces a charge in the channel between Source and Drain.
- This charge is then moved from source to drain under the influence of electric field created by voltage applied between Drain and Source V_{DS} .

Hence the current I_{DS} is given by

$$I_{ds} = \frac{Charge\ induced\ in\ the\ channel}{Electron\ transit\ time}$$

$$I_{ds} = \frac{Q_c}{\tau}$$

Where, $\tau = \frac{Length\ of\ the\ channel}{Velocity} = \frac{L}{\vartheta}$

$$Velocity\ of\ the\ electron\ \vartheta = \mu E_{ds}$$

Where,

μ = Mobility of the electron or hole

μ_n – 1250 cm^2 /V sec, μ_p– 480 cm^2 /V sec

$$E_{ds} = Electric\ field$$

$$E_{ds} = \frac{V_{ds}}{L}$$

$$Velocity\ of\ the\ electron\ \vartheta = \mu \frac{V_{ds}}{L}$$

Substituting in τ,

$$\tau = \frac{L^2}{\mu V_{ds}}$$

Case i: Non saturated region

Let the charge induced in the channel due to gate voltage is given by

$$\boldsymbol{Q_c = E_g \varepsilon_o \varepsilon_{ins} WL}$$

Where,

E_g ε_{ins} ε_0 -- Charge / unit area

E_g - Avg. electric field gate to channel

ε_{ins} - Relative permittivity of insulation between gate and channel – 4 for SiO_2

ε_0 - Permittivity of free space - 8.854 x 10^{-4} F/cm

Since the voltage along the channel varies linearly with distance X from source due to IR drop in the channel, hence the average V_{DS} is V_{ds} / 2

The effective gate voltage $V_g = V_{gs} - V_t$

$$E_g = \frac{\left[(V_{gs} - V_t) - \frac{V_{DS}}{2}\right]}{D}$$

D = Oxide thickness

Substituting in the charge expression

$$Q_C = \frac{\epsilon_{ins}\epsilon_0\, WL}{D}\left[(V_{gs} - V_t) - \frac{V_{DS}}{2}\right]$$

Substituting Q_c & τ in I_{ds} expression,

$$I_{DS} = \frac{\mu . V_{DS}}{L^2}\frac{\epsilon_{ins}\epsilon_0\, WL}{D}\left[(V_{gs} - V_t) - \frac{V_{DS}}{2}\right]$$

$$I_{DS} = \frac{\mu\, \epsilon_{ins}\epsilon_0}{D}\frac{W}{L}\left[(V_{gs} - V_t) - \frac{V_{DS}}{2}\right]V_{DS}$$

$$I_{DS} = K\frac{W}{L}\left[(V_{gs} - V_t) - \frac{V_{DS}}{2}\right]V_{DS}$$

Where,

$$K = \frac{\mu\, \epsilon_{ins}\epsilon_0}{D}$$

Case ii : Saturation region

In saturation region $V_{ds} = V_{gs} - V_t$

Substituting in I_{ds}

$$I_{DS} = K\frac{W}{L}\left[(V_{gs} - V_t) - \frac{V_{DS}}{2}\right]V_{DS}$$

$$I_{DS} = K\frac{W}{L}\left[(V_{gs} - V_t)V_{DS} - \frac{V_{DS}.V_{DS}}{2}\right]$$

$$I_{DS} = K\frac{W}{L}\left[\left((V_{gs} - V_t)^2\right) - \frac{(V_{gs} - V_t)^2}{2}\right]$$

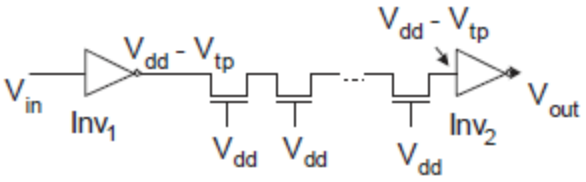
$$I_{DS} = K\frac{W}{L}\frac{(V_{gs} - V_t)^2}{2}$$

2. b) Compare CMOS, Bipolar, BiCMOS technologies.

CMOS	BiPolar
1. Low static power dissipation	High power dissipation
2. High input impedance	Low input impedance
3. Scalable Threshold voltage	
4.High noise margin	Low voltage swing logic
5. High package density	Low package density
6. Low output drive current	High output drive current
7. Bidirectional capability (Source & drain are interchangeable)	Unidirectional
8. Low g_m (g_m α V_{in})	High g_m (g_m α e^{Vin})
9. High delay sensitivity to load (Fan out limitations)	Low delay sensitivity

3. a) Derive the pull up to pull down ratio for an NMOS inverter driven by another NMOS inverter through a pass transistor.

An nMOS Inverter Driven Through Pass Transistors



An nMOS inverter is driven through one or more pass transistors as shown in Fig. As we have seen a pass transistor passes a weak high level. If *V*dd is applied to the input of a pass transistor, at the output, we get (*V*dd–*V*tp), where *V*tp is the threshold voltage of the pass transistor. Therefore, instead of *V*dd, a degraded high level (*V*dd–*V*tp) is applied to the second inverter. We have to ensure that the same voltage levels are produced at the outputs of the two Inverters in spite of different input voltage levels.

For $V_{in} = V_{dd}$,
Pull up – Saturation- Current source
Pull down – linear – resistor
For pull down transistor

$$\boldsymbol{I_{ds}} = K\,\frac{W_{pd1}}{L_{pd1}}\left[(V_{dd} - V_{tn})\,V_{ds1} - \frac{{V_{ds1}}^2}{2}\right]$$

$$R_1 = \frac{V_{sd1}}{I_{ds1}} = \frac{1}{K}\,\frac{L_{pd1}}{W_{pd1}}\,\frac{1}{\left(V_{dd} - V_{tn} - \frac{V_{ds1}}{2}\right)}$$

$$\frac{V_{ds1}}{2}\ factor,\ R_1 = \frac{Z_{pd1}}{K}\,\frac{1}{(V_{dd} - V_{tn})}$$

$$I_1 = I_{ds} = K\,\frac{W_{pu1}}{L_{pu1}}\,\frac{\left(-V_{tdp}\right)^2}{2}$$

For depletion pull up transistor, $V_{gs} = 0$

$$I_1 R_1 = V_{out1} = \frac{Z_{pd1}}{Z_{pu1}}\left(\frac{1}{V_{dd} - V_{tn}}\right)\frac{\left(-V_{tdp}\right)^2}{2}$$

Similarly, for the second inverter

$$R_2 \approx \frac{Z_{pd2}}{K}\,\frac{1}{\left[\left(V_{dd} - V_{tp}\right) - V_{tn}\right]}$$

$$I_2 = K\,\frac{1}{Z_{pu2}}\,\frac{(-V_{td})^2}{2}$$

$$V_{out2} = I_2\,R_2 = \frac{Z_{pd2}}{Z_{pu2}}\,\frac{1}{(V_{dd} - V_{tp} - V_{tn})}\,\frac{(-V_{td})^2}{2}$$

$$V_{out1} = V_{out2}\ then,\ I_1 R_1 = I_2 R_2$$

$$\frac{Z_{pu2}}{Z_{pd2}} = \frac{Z_{pu1}}{Z_{pd1}}\,\frac{(V_{dd} - V_{tn})}{(V_{dd} - V_{tp} - V_{tn})}$$

Substituting $V_{tn} = 0.2\ V_{dd}$ & $V_{tp} = 0.3\ V_{dd}$

$$\frac{Z_{pu2}}{Z_{pd2}} = \frac{4.0}{2.5}\frac{Z_{pu1}}{Z_{pd1}} \; or \; \frac{Z_{pu2}}{Z_{pd2}} \approx 2.\frac{Z_{pu1}}{Z_{pd1}} = \frac{8}{1}$$

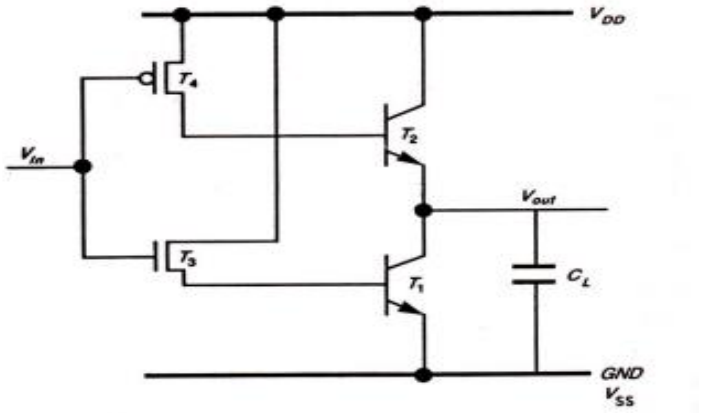
Z_{pu} / Z_{pd} = 8/1

If an inverter is driven through one or more pass transistors, it should have inverter ratio Z_{pu} / Z_{pd} = 8/1

3. b) Draw and explain about BICMOS inverter.

In BiCMOS technology, MOS switches are used to perform the logic function and bipolar transistors to drive the output loads.

BiCMOS inverter:



V_{in}	T_1	T_2	T_3	T_4	V_{out}
0V	OFF	ON	OFF	ON	V_{DD} - V_{BE}
V_{DD}	ON	OFF	ON	OFF	V_{CESAT}

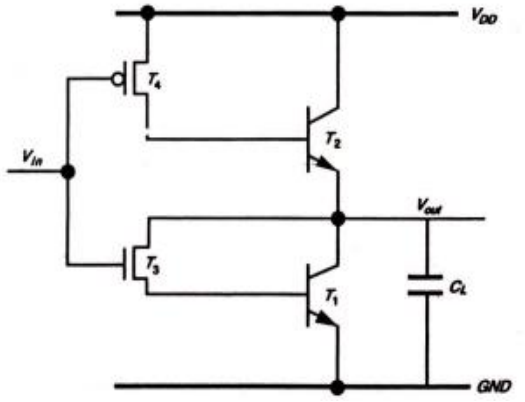
Advantages:

- The output logic levels will be good .
- The inverter has a high input impedance.
- The inverter has a low output impedance.
- Has high current drive capability
- Has relatively small area.
- The inverter has high noise margins.

Disadvantages:

- DC path through V_{DD} and V_{SS} through T_3 & T_1 Hence static power dissipation.
- No discharge path for current.

Modified circuit for no static current flow:



V_{in}	T_1	T_2	T_3	T_4	V_{out}
0V	OFF	ON	OFF	ON	V_{DD} - V_{BE}
V_{DD}	ON	OFF	ON	OFF	V_{BE}

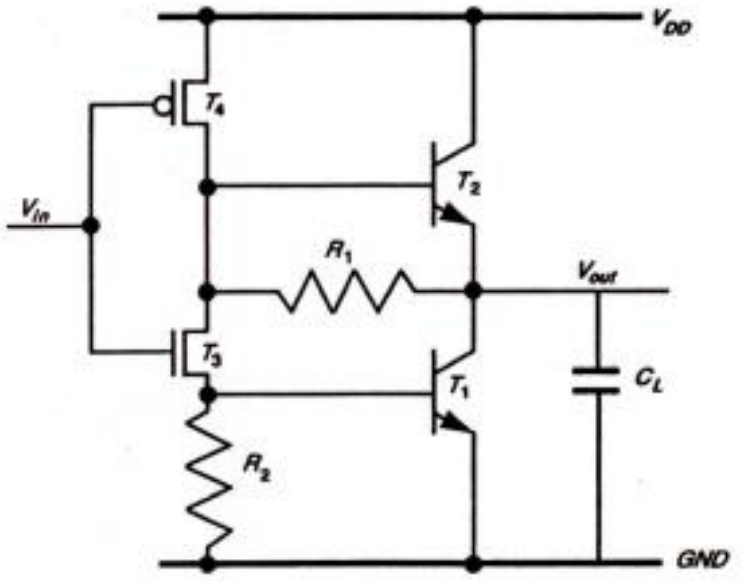
Advantage:

- **DC path is eliminated.**

Limitation:

- **Voltage swing is reduced**.

Improved version for better voltage levels:



V_{in}	T_1	T_2	T_3	T_4	V_{out}
0V	OFF	ON	OFF	ON	$V_{DD} - IR_1$
V_{DD}	ON	OFF	ON	OFF	IR_2

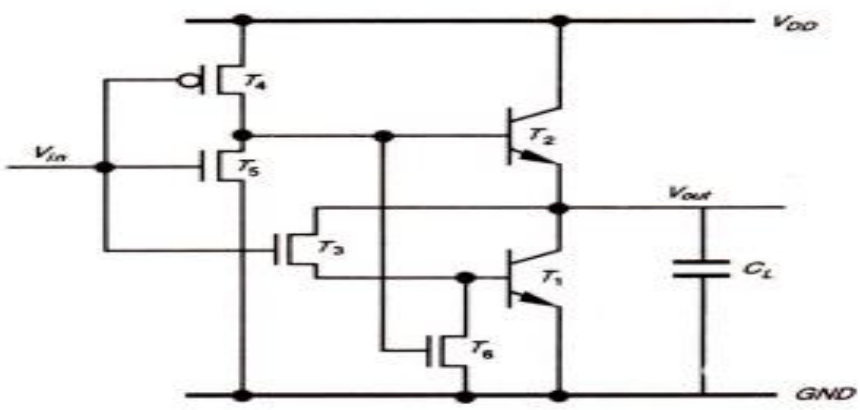
Advantages:

- Provides the improved swing of output voltage.
- Provides discharge paths for base current during turn-off.

Limitation:

- On chip resistors of suitable value is not always convenient.
- Resistors are space-consuming.

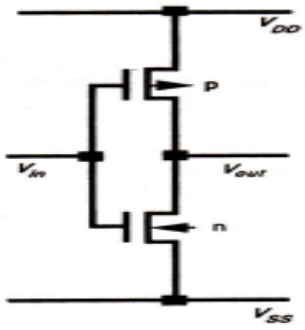
Improved version for base current discharge:



V_{in}	T_1	T_2	T_3	T_4	T_5	T_6	V_{out}
0V	OFF	ON	OFF	ON	OFF	ON	$V_{DD} - V_{BE}$
V_{DD}	ON	OFF	ON	OFF	ON	OFF	V_{BE}

4. a) Explain the operation of CMOS inverter with voltage and current characteristics.

CMOS inverter:



The operation of CMOS inverter can be explained in 5 regions.

Region 1: **($0 \le V_{in} < V_{tn}$)**

V_{in} = logic 0, p-transistor is fully turned on while the n-transistor is fully turned off. Thus no current flows through the inverter and the output is directly connected to V_{DD} through the p-transistor. A good logic 1 output voltage is thus present at the output.

Region 5: **($V_{dd} - V_{tp} \le V_{in} < V_{dd}$)**

V_{in} = logic 1, the n-transistor is fully on while the p-transistor is fully off. Again, no current flows and a good logic 0 appears at the output.

Region 2: **($V_{tn} < V_{in} < V_{inv}$)**

The input voltage has increased to a level which just exceeds the threshold voltage of the n-transistor. The n-transistor conducts and has a large voltage between source and drain; so it is in saturation. The p-transistor is also conducting but with only a small voltage across it, it operates in the unsaturated resistive region. A small current now flows through the inverter from V_{DD} to V_{SS}. As currents voltage drops at the output.

Region 4: **($V_{inv} < V_{in} < V_{dd} - V_{tp}$)**

Similar to region 2 but with the roles of the p- and n-transistors reversed. However, the current magnitudes in regions 2 and 4 are small and most of the energy consumed in switching from one state to the other is due to the larger current which flows in region 3.

Region 3: **($V_{in} = V_{inv}$)**

For the input which is equal to the threshold voltage of the inverter. The region in which the inverter exhibits gain and in which both transistors are in saturation.

The currents in each device must be the same since the transistors are in series

$$V_{gs}^{pd} = V_{inv}$$

$$V_{gs}^{pu} = V_{in} - V_{dd} = V_{inv} - V_{dd}$$

$$I_{dsn} = \frac{1}{2} K_n \frac{W_n}{L_n} (V_{inv} - V_{tn})^2$$

$$I_{dsp} = -\frac{1}{2} K_p \frac{W_p}{L_p} \left(V_{inv} - V_{dd} - V_{tp}\right)^2$$

Equating the currents,

I_{dsp} =- I_{dsn}

$$or\ \frac{\beta_n}{2}(V_{inv}-V_{tn})^2 = -\frac{\beta_p}{2}(V_{inv}-V_{dd}-V_{tp})^2$$

$$\frac{(V_{inv}-V_{dd}-V_{tp})^2}{(V_{inv}-V_{tn})^2} = -\frac{\beta_n}{\beta_p}$$

$$or\quad \frac{V_{inv}-V_{dd}-V_{tp}}{V_{inv}-V_{tn}} = -\sqrt{\frac{\beta_n}{\beta_p}}$$

$$or\qquad V_{inv}\left(1+\sqrt{\frac{\beta_n}{\beta_p}}\right) = V_{dd}+V_{tp}+V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}$$

$$V_{inv} = \frac{V_{dd}+V_{tp}+V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1+\sqrt{\frac{\beta_n}{\beta_p}}}$$

$\beta_n = \beta_p$ *and* V_{tn} = - V_{tp}

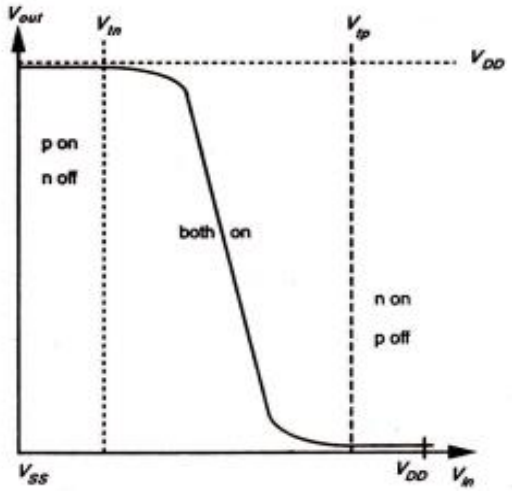
V_{inv} = V_{dd}/ 2

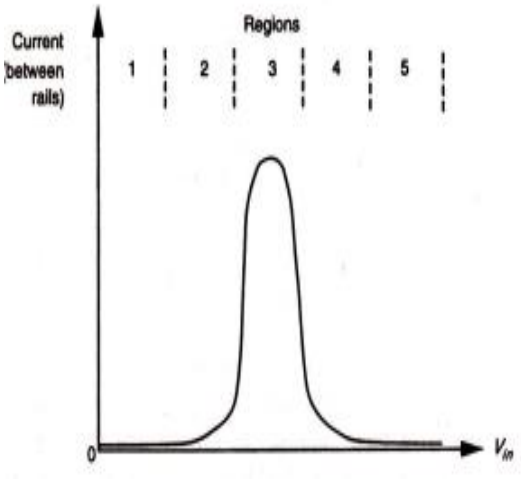
$$\frac{K_n}{K_p} = \frac{\mu_n}{\mu_p} \approx 2.5$$

To make $\beta_n = \beta_p$,

$$\left[\frac{W}{L}\right]_p = 2.5\left[\frac{W}{L}\right]_n$$

Voltage and Current characteristics:



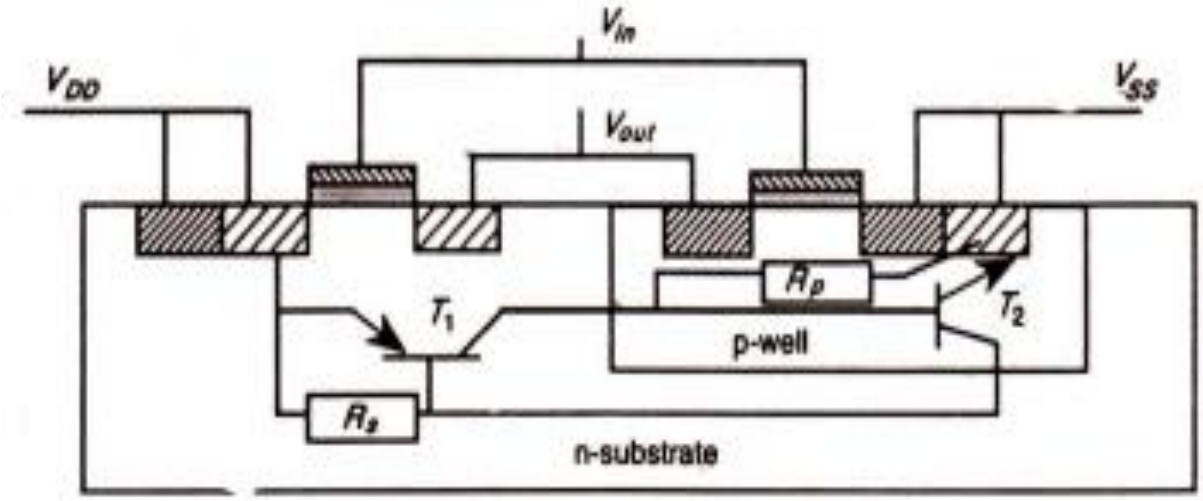


b) What is latch–up explain the condition with remedial measures?

Latch up in CMOS:

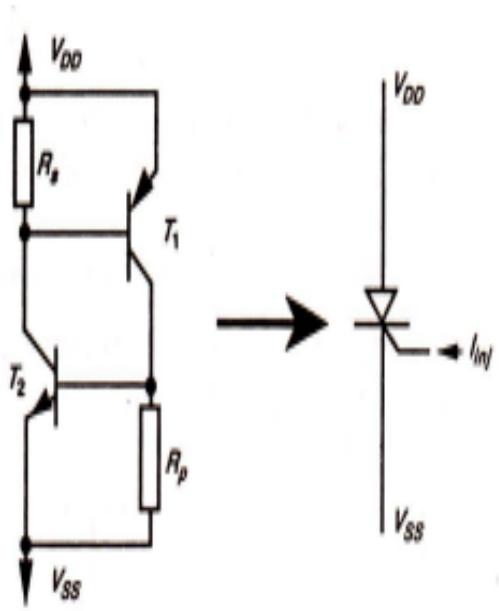
- A condition in which the parasitic components give rise to the establishment of low-resistance conducting paths between V_{DD} and V_{SS} with disastrous results.
- Occurs in the p-well and n-well CMOS processes.
- Due to the relatively large number of junctions which are formed in these structures, the consequent presence of parasitic transistors and diodes.
- Latch-up may be induced by glitches on the supply rails or by incident radiation.

Consider a P-Well process, the key parasitic components associated with a p-well structure are

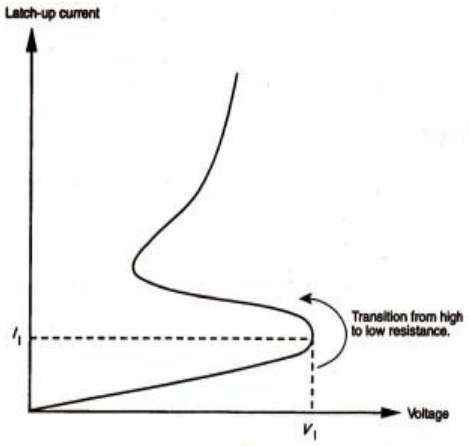


- There are two transistors and two resistances (associated with the p-well and with regions of the substrate) which form a path between V_{DD} and V_{SS}.
- If sufficient substrate current flows to generate enough voltage across R_s to turn on transistor T_1, this will then draw current through R_p and, if the voltage developed is sufficient, T_2 will also turn on, establishing a_self-sustaining low-resistance path between the supply rails.
- If the current gains of the two transistors are such that $\beta_1 \times \beta_2 > 1$, latch-up may occur.

- With no injected current, the parasitic transistors will exhibit high resistance, but sufficient substrate current flow will cause switching to the low-resistance state.



Once latched-up, this condition will be maintained until the latch-up current drops below I_l.

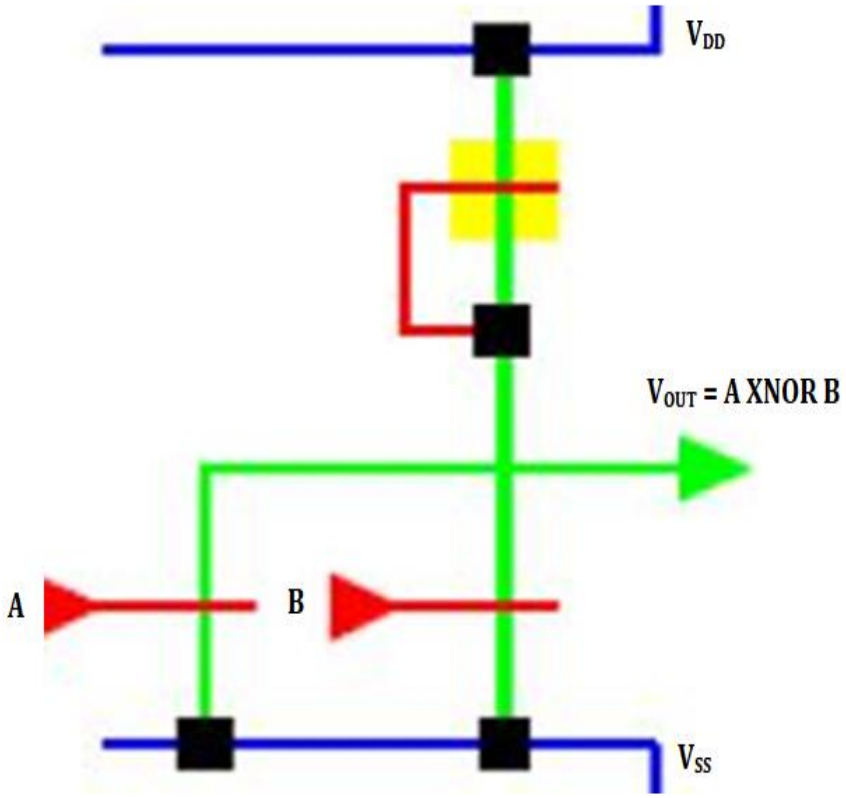


Remedies for the latch-up problem:

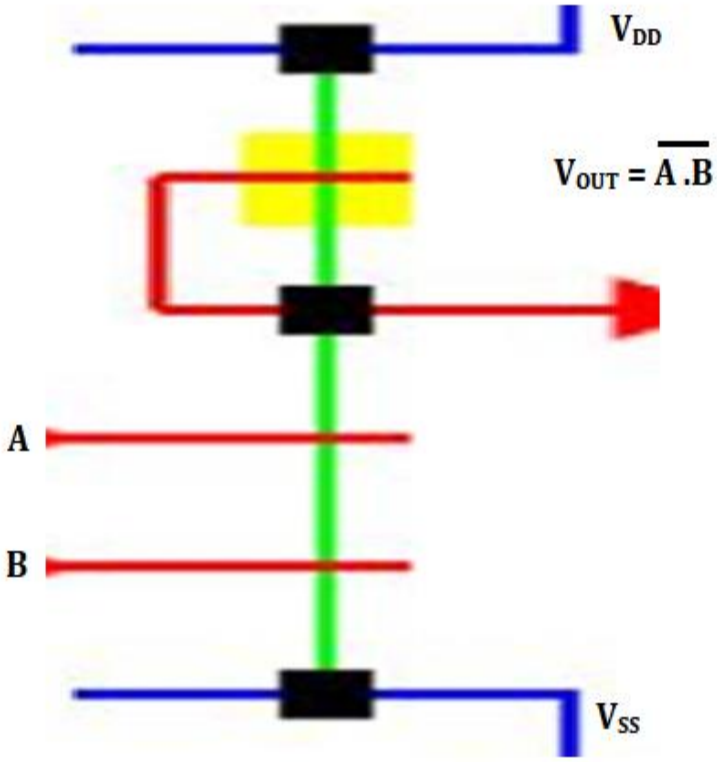
- Increase in substrate doping levels with a consequent drop in the value of R_s
- Reducing R_p by control of fabrication parameters and by ensuring a low contact resistance to V_{ss}
- Introduction of guard rings.

5. a) Design a stick diagram for two input nMOS NAND and NOR gates.

NMOS NOR gate:



NMOS NAND gate:



b) Derive the expressions for trans conductance, output conductance and figure of merit.

Transconductance (g_m):Non saturation

Trans conductance is defined as

$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} | V_{ds} = constant$

Transconductance in terms of transistor parameters:

$$I = \frac{Q}{t}$$

$\partial I_{ds} = \frac{\partial Q}{\tau_{ds}}$

Since,

$$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$$

Substituting in I_{ds}

$$\partial I_{ds} = \frac{V_{ds}.\mu \partial Q}{L^2}$$

Since

$$\partial Q_c = C_g \partial V_{gs}$$

$$\partial I_{ds} = \frac{C_g \mu V_{ds} \partial V_{gs}}{L^2}$$

$$\frac{\partial I_{ds}}{\partial V_{gs}} = \frac{C_g \mu V_{ds}}{L^2}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{C_g \mu V_{ds}}{L^2}$$

In saturation,

$$v_{DS} = V_{gs} - V_t$$

$$g_m = \frac{C_g \mu}{L^2}(V_{gs} - V_t)$$

$$\therefore g_m = \frac{\mu \in_{ins} \in_o W}{DL}(V_{gs} - V_t) \qquad \because C_g = \frac{\in_{ins} \in_o WL}{D}$$

$$\therefore g_m = \beta(V_{gs} - V_t)$$

- Since g_m is proportional to width (W), it can be increased by increasing width but it increases input capacitance and area occupied.

Output conductance(g_{ds}):

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{(C_g \mu V_{gs})}{L^2}$$

Figure of merit(w_o): Signifies about the frequency response of the device.

$$W_o = \frac{g_m}{C_g}$$

$$= \frac{\frac{\mu \epsilon_{ins} \epsilon_o W}{DL}(V_{gs} - V_t)}{\frac{\epsilon_{ins} \epsilon_o WL}{D}}$$

$$= \frac{\mu}{L^2}(V_{gs} - V_t)$$

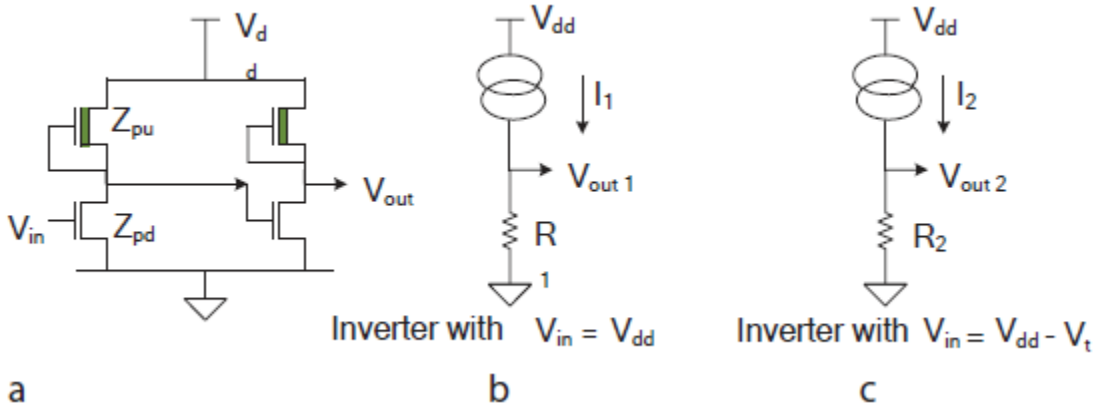
- Higher gate voltage and higher electron mobility provide better frequency response.

  μ_n – 1250 cm^2 /V sec, μ_p– 480 cm^2 /V sec

6. a) Derive the pull up to pull down ratio for an NMOS inverter driven by another NMOS inverter.

Different inverter ratios will be necessary for correct and satisfactory operation of the inverters.

An nMOS Inverter Driven by Another Inverter



An nMOS inverter driven by another inverter;
b inverter with *V*in = *V*dd; and

c inverter with *V*in = *V*dd – *V*t. nMOS n-type metal–oxide–semiconductor, *V*in voltage input to the inverter, *V*dd positive supply rail, *V*t inverter threshold voltage

Let us consider an nMOS inverter with depletion-type transistor as an active load is driving a similar type of inverter as shown in Fig. In order to cascade two or more inverters without any degradation of voltage levels, we have to meet the condition *V*in = *V*out = *V*inv; and for equal margins, let us set *V*inv = 0.5 *V*dd. This condition is satisfied when both the transistors are in saturation, and the drain current is given by

Cascading inverters without degradation

$V_{in} = V_{out} = V_{inv} = 0.5V_{dd}$

Both the transistors are in saturation

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs} - V_t)^2}{2}$$

For depletion mode transistor,

$$I_{ds}^{pu} = K\frac{W_{pu}}{L_{pu}}\frac{(-V_{tdp})^2}{2}, \; V_{gs} = 0V$$

For enhancement mode transistor

$$I_{ds} = K\frac{W_{pd}(V_{inv} - V_{tn})^2}{2L_{pd}}$$

Equating currents,

$$\frac{W_{pd}}{L_{pd}}(V_{inv} - V_{tn})^2 = \frac{W_{pu}}{L_{pu}}(-V_{tdp})^2$$

$Z_{pd} = L_{pd} / W_{pd}$ & $Z_{pu} = L_{pu} / W_{pu}$

Z = aspect ratio

$$\frac{1}{Z_{pd}}(V_{inv} - V_{tn})^2 = \frac{1}{Z_{pu}}(-V_{tdp})^2$$

$$\sqrt{\frac{Z_{pu}}{Z_{pd}}}(V_{inv} - V_{tn}) = -V_{tdp}$$

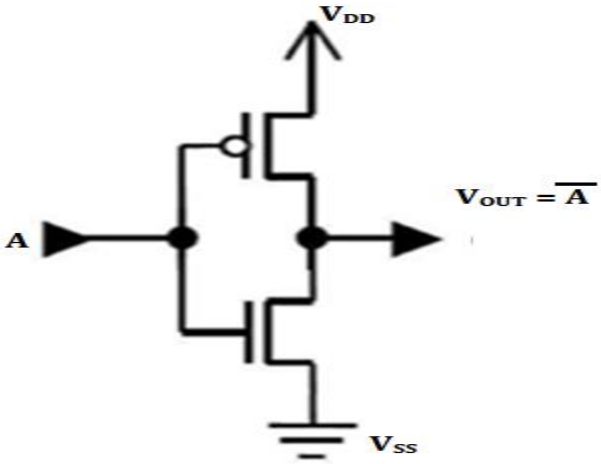
$$V_{inv} = V_{tn} - \frac{V_{tdp}}{\sqrt{\frac{Z_{pu}}{Z_{pd}}}}$$

Substituting $V_{tn} = 0.2V_{dd}$, $V_{tdp} = -0.6V_{dd}$, $V_{inv} = 0.5V_{dd}$

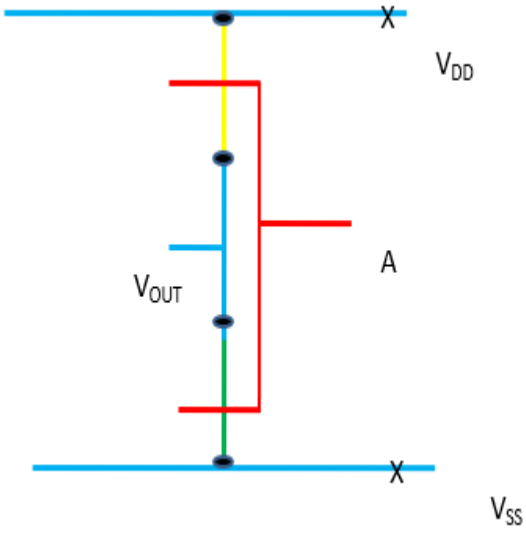
$$Z_{pu} / Z_{pd} = 4/1$$

b) Draw the stick diagram and layout for a CMOS inverter indicating the design rules.

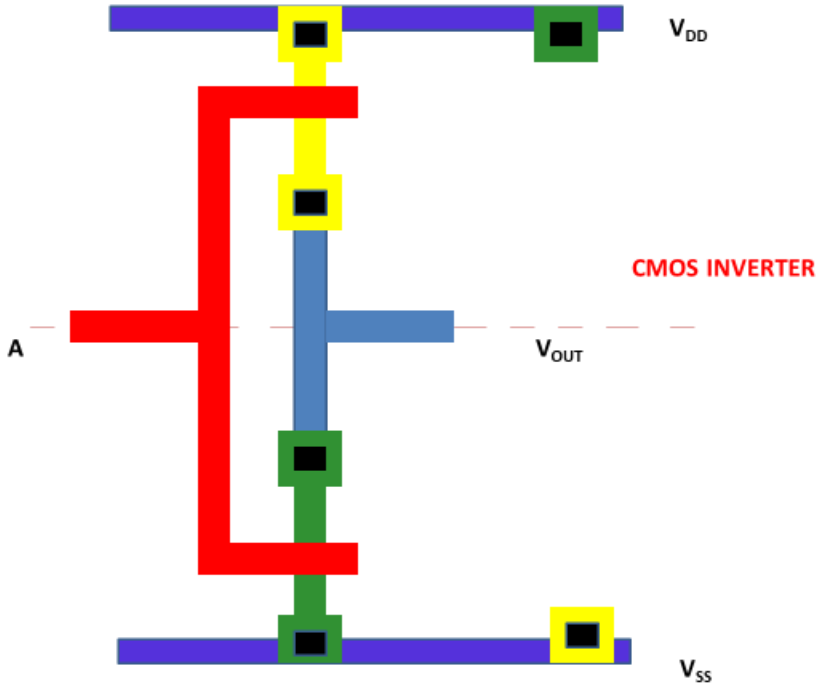
CMOS inverter:



CMOS stick diagram:



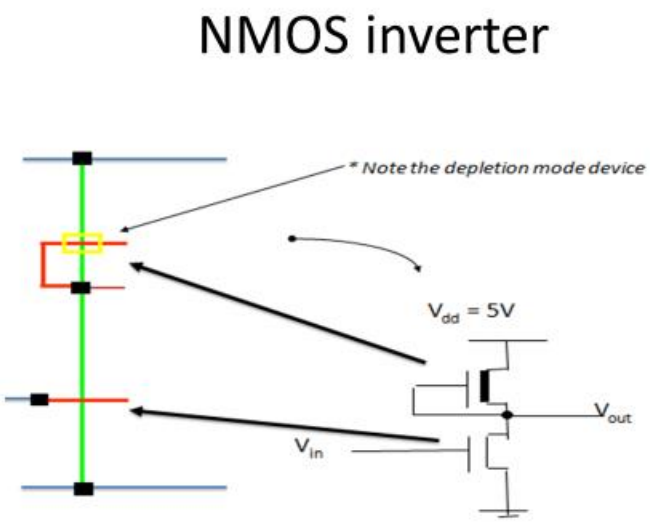
Layout:



7. Explain the operation of NMOS inverter and compare the characteristics with various pull up loads.

8. What are the steps involved in the CMOS fabrication? Explain with neat sketches.

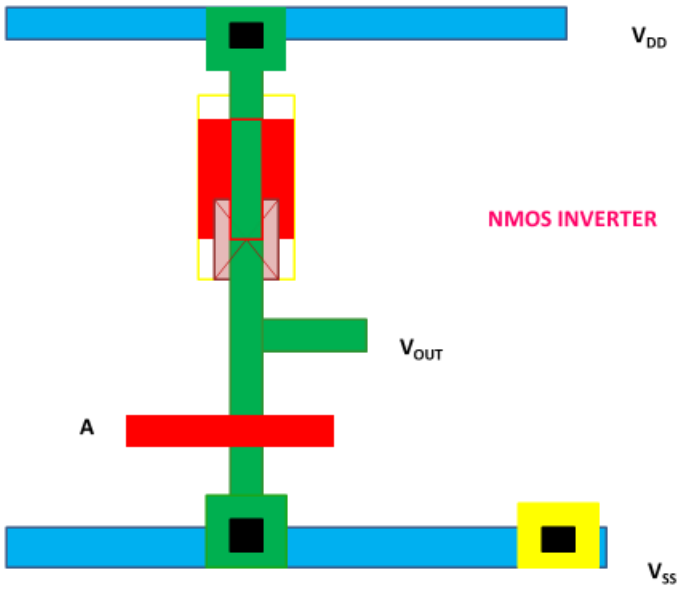
Stick diagrams:

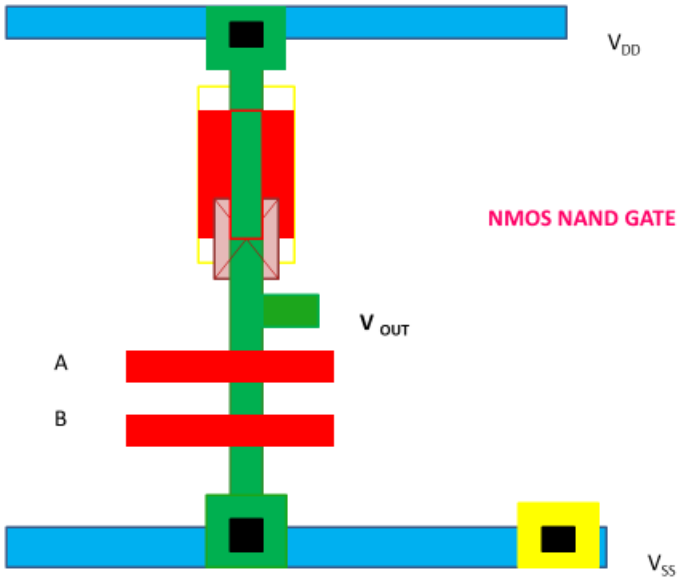


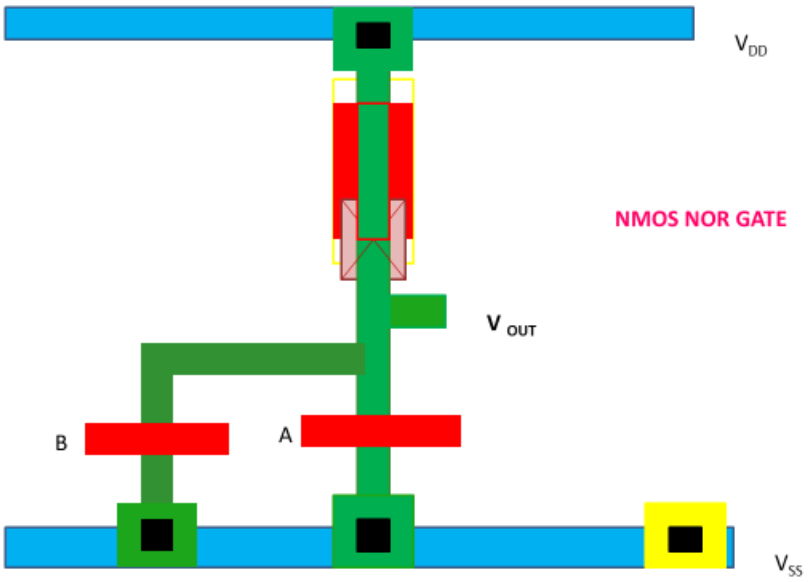
CMOS NAND GATE:

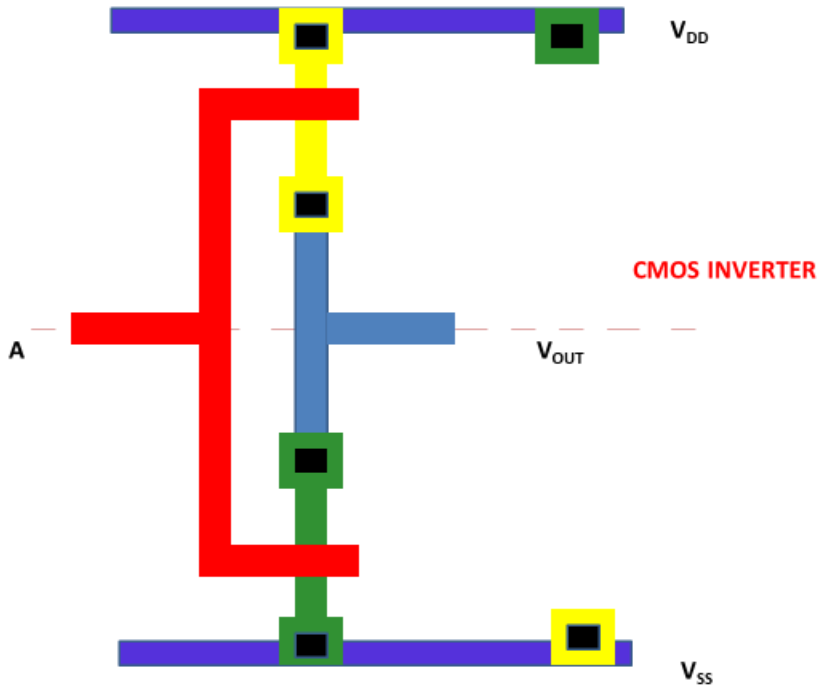
CMOS NOR GATE:

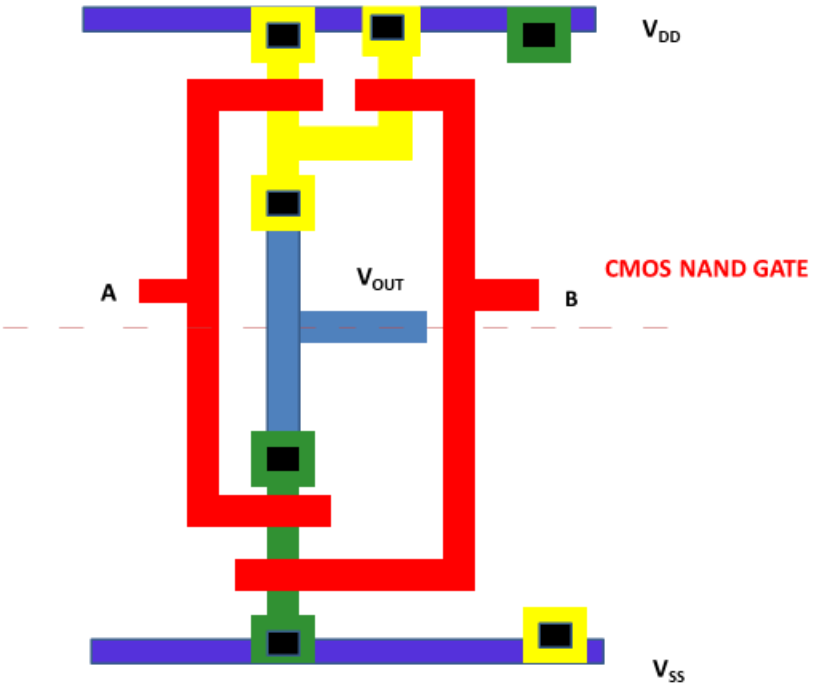
Layouts:

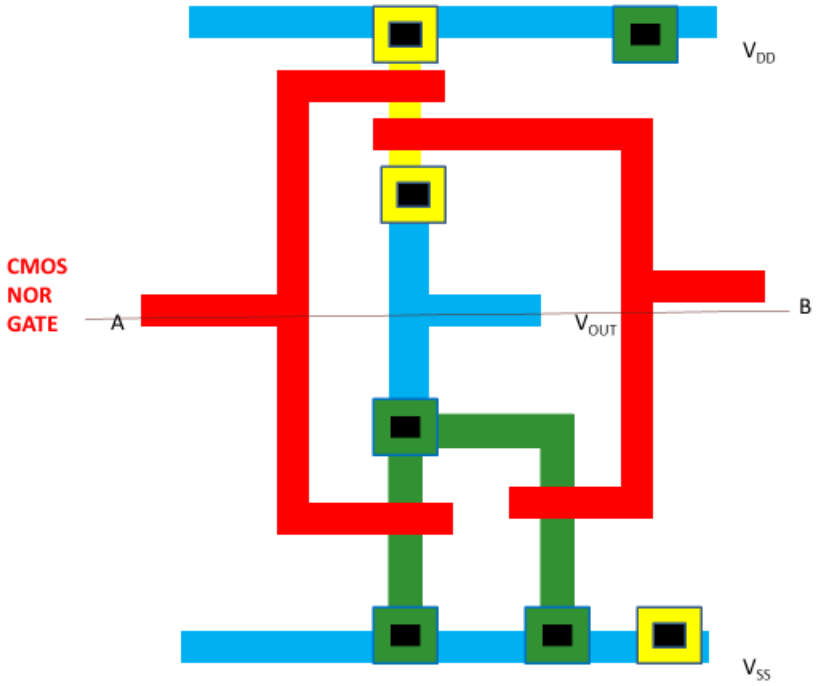

V_{DD}
NMOS INVERTER
V_{OUT}
A
V_{SS}


V_{DD}
NMOS NAND GATE
V_{OUT}
A
B
V_{SS}


V_{DD}
NMOS NOR GATE
V_{OUT}
B
A
V_{SS}


V_{DD}
CMOS INVERTER
A
V_{OUT}
V_{SS}



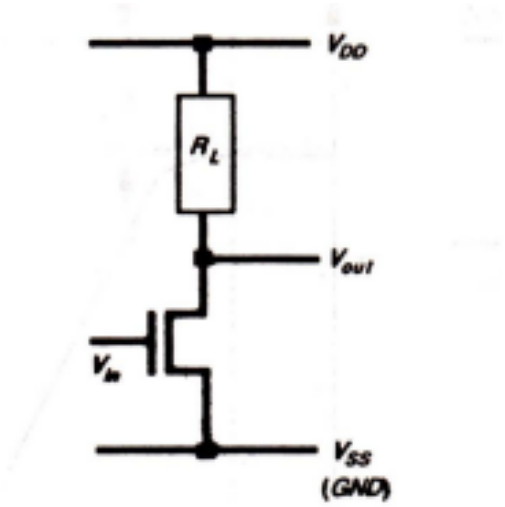


Alternate forms of Pull ups:

- **Load resistance R_L**

- **NMOS Depletion-mode transistor pull up**
- **NMOS Enhancement mode transistor pull up**
- **Complementary transistor pull up (CMOS)**

Load resistor R_L as pull up:

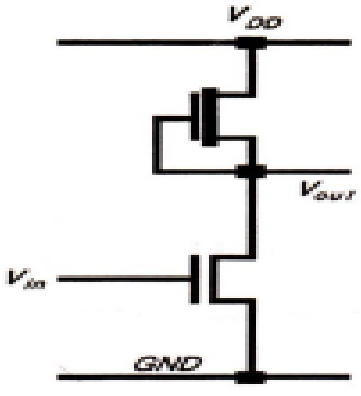


V_{in}	NMOS	V_{out}
$<V_{tn}$	OFF	V_{dd}
$>V_{tn}$	ON	> 0

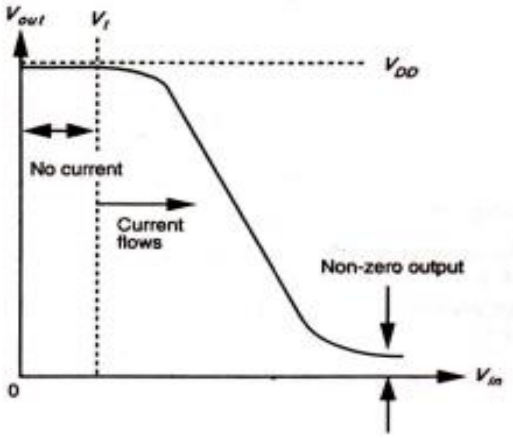
Limitations of resistive pull up:

- **Asymmetrical switching times.**
- **R_c & R_L should be low.**
  R_c – Large area of transistor.
  Increased power dissipation.
- **Large chip area.**
- **Resistance cannot be controlled.**

NMOS depletion mode transistor pull up:

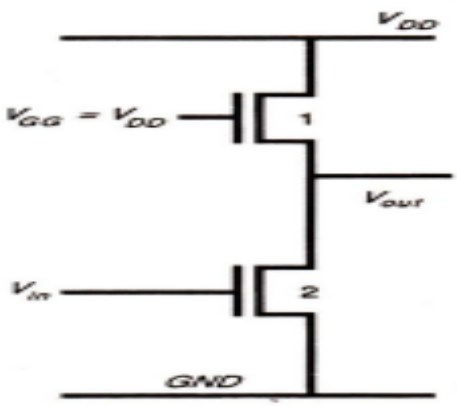


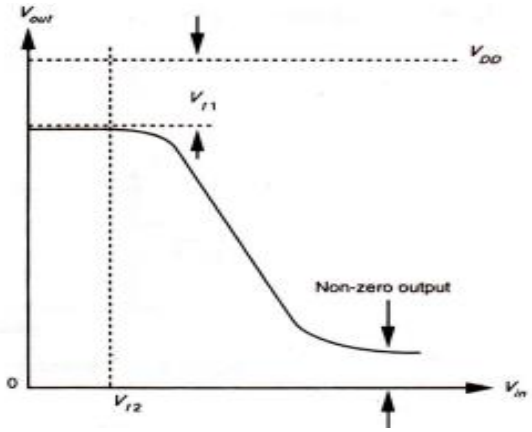
V_{in}	NMOS	V_{out}
$<V_{tn}$	OFF	V_{dd}
$>V_{tn}$	ON	> 0



- **High power dissipation – for logic 1 – rail to rail current**
- **Switching from logic 1 to logic 0 begins when V_{in} exceeds V_t of PD transistor.**
- **When switching the output from 1 to 0, the p.u. device is non-saturated initially and this presents lower resistance through which to charge capacitive loads .**
- **It produces strong high output level, but weak low output level.**

nMOS Enhancement-Mode Transistor as Pull up:





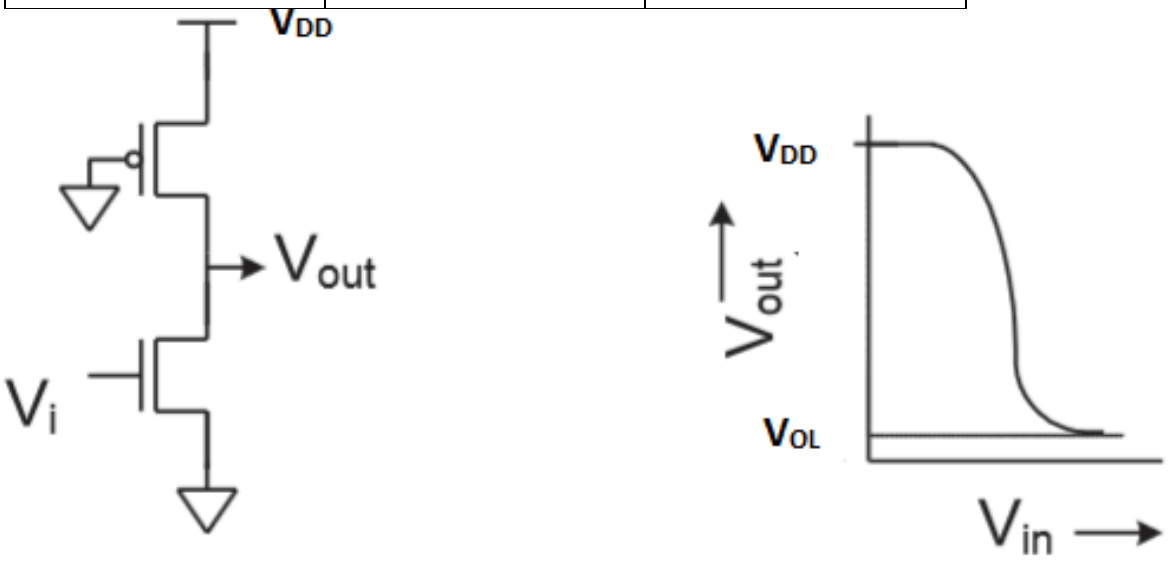
V_{in}	V_{out}	NMOS
0	$V_{DD} - V_{th}$	OFF
1	>0V	ON

Limitations of Enhancement NMOS:

- **High power dissipation – for logic 1 – rail to rail current**
- **The output is not ratioless, which leads to asymmetry in switching characteristics.**
- **It produces weak low and high output levels.**
- **VGG may be derived from a switching source, one phase of a clock, so that dissipation can be greatly reduced.**
- **If V_{GG} is higher than V_{DD} then an extra supply rail is required**

Complementary Transistor Pull Up (Pseudo NMOS):

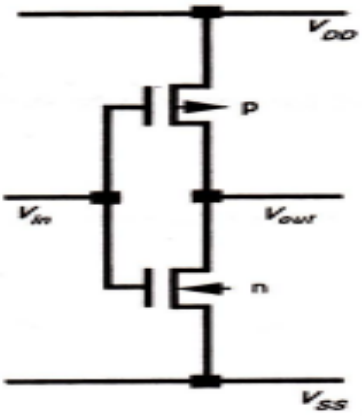
V_{in}	NMOS	V_{out}
0	OFF	V_{DD}
1	ON	>0V

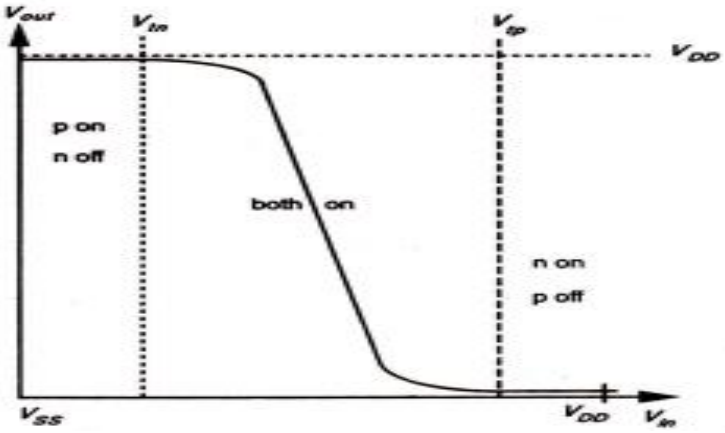


Limitations of Pseudo NMOS:

- The pull-up transistor always remains ON
- DC current flows when the pull-down device is ON.
- The low-level output is also not zero and is dependent on the β_n / β_p

Complementary Transistor Pull Up (CMOS):





V_{in}	NMOS	PMOS	V_{out}
0	OFF	ON	V_{DD}
1	ON	OFF	0

- **No current flow either for logical 0 or for logical 1 inputs.**
- **Full logical 1 and 0 levels are presented at the output.**
- **For devices of similar dimensions the p-channel is slower than the n-channel device.**