Code: 20A04303T

R20

B.Tech II Year II Semester (R20) Regular & Supplementary Examinations April/May 2024
**DIGITAL LOGIC DESIGN**
(Electronics & Communication Engineering)

Time: 3 hours                                                                                    Max. Marks: 70

## PART – A
### (Compulsory Question)
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1      Answer the following: (10 X 02 = 20 Marks)
  (a)  Convert $(615.25_8)$ to its hexadecimal equivalent.                                                 2M
  (b)  What are universal gates and why they are called as universal gates?                                2M
  (c)  Compare serial adder and parallel adder.                                                            2M
  (d)  What do you mean by K-map? Name it advantages and disadvantages?                                    2M
  (e)  Differentiate between Latch and flip flop.                                                          2M
  (f)  What is meant by race around condition in flip-flops?                                               2M
  (g)  What is FSM?                                                                                        2M
  (h)  What is State assignment?                                                                           2M
  (i)  Write the difference between PLA & PAL.                                                             2M
  (j)  Differentiate volatile and non-volatile memory.                                                     2M

## PART – B
### (Answer all the questions: 05 X 10 = 50 Marks)

2  (a)  Convert the following to the corresponding bases                                                   5M
        (i) $(343)_5 = ($  $)_6$ ; (ii)  $(7654)_8 = ($  $)_{10}$
        (iii) Simplify the following Boolean expression to a minimum number of literals ABC+A'B+ABC'
   (b)  State and prove the following Boolean laws:                                                        5M
        (i) Commutative, (ii) Associative, (iii) Distributive.
                                              **OR**
3  (a)  Perform the following arithmetic operation using l's complement method:                            5M
        (i) Add $(-19)_{10}$ $and$ $(29)_{10}$ ;   (ii) Add $(21)_{10}$ $and$ $(37)_{10}$
        (iii) Write the truth table and symbols of AND & OR gates.
   (b)  Simplify the following expression using Boolean algebra rule $\overline{A\bar{B} + \overline{ABC} + A(B + A\bar{B})}$.   5M

4  (a)  Simplify the Boolean expression, F = A' + AB + ABD' + AB'D' + C' using Four variable K-Map   5M
        and draw the logic diagram using AOI.
   (b)  Implement the following switching function using a Four input multiplexer                          5M
        F(A, B, C, D) = Σm ( 0, 1, 2, 4, 6, 9, 10, 13, 14).
                                              **OR**
5  (a)  Reduce the following function using K-Map.                                                         5M
        F(A, B, C, D, E) = Σm(1, 4, 8, 10, 11, 20, 22, 24, 25, 26) + d(0, 12, 16, 17).
   (b)  Design a 4-bit combinational logic to subtract one bit from the other. Draw the logic diagram   5M
        using NAND and NOR Gates.

6  (a)  Design 4-bit shift register using D flip-flops and explain its working with the help of timing   5M
        diagrams.
   (b)  With neat diagram explain the operation of 3-bit universal shift register.                        5M
                                              **OR**

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| 7 | (a) | Convert SR flip flop into JK Flip-Flop. Draw and explain its logic diagram. | 5M |
| | (b) | With neat diagram explain the operation of a 3-bit Ripple counter. | 5M |
| | | | |
| 8 | (a) | The reduced state table of a sequential machine has 12 rows. What is the minimum number of flip-flops needed to implement the machine? | 5M |
| | (b) | What is state reduction by partition method? Explain. | 5M |

**OR**

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| 9 | (a) | How many flipflops are needed to design an FSM with n states using binary encoding for state assignment? Explain FSM capabilities and limitations. | 5M |
| | (b) | What are the real-life examples of Mealy machines? Differentiate Moore and Mealy. | 5M |
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| 10 | (a) | Explain the functions and applications of PLAs in memory addressing and implement the following two Boolean functions with a PLA:<br>F1 (A, B, C) = $\sum$ (0, 1, 3, 5) and F2 (A, B, C) = $\sum$ (1, 2, 4, 7) | 5M |
| | (b) | Write Verilog module for a positive edge triggered flip flop with test bench. | 5M |

**OR**

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| 11 | (a) | Design PAL for a combinational circuit that squares a 3-bit number? | 5M |
| | (b) | Explain the basic Structure of CPLD and FPGA. | 5M |

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# R20

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B.Tech II Year II Semester (R20) Regular & Supplementary Examinations August/September 2023

## DIGITAL LOGIC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours                                                                                              Max. Marks: 70

## PART – A
(Compulsory Question)
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1        Answer the following: (10 X 02 = 20 Marks)
   (a)   Convert the following numbers with the given radix to decimal. (i) $(4433)_5$ (ii) $(1199)_{12}$.        2M
   (b)   What are the three methods of obtaining the 2's complement of a given binary number?        2M
   (c)   Multiply out and simplify to obtain a sum of products: (x' +y +z') (x' +z' +u) (y' +u').        2M
   (d)   State and prove the De-Morgan's laws.        2M
   (e)   What is meant by race around condition in flip-flops?        2M
   (f)   Why a multiplexer is called a data selector? Draw the 2x1 MUX.        2M
   (g)   Discuss about a serial-in, serial-out shift registers.        2M
   (h)   Draw the state diagram of modulo-4 up/down counter.        2M
   (i)   State the purpose of reducing the switching functions to minimal form.        2M
   (j)   Define full Subtractor.        2M


## PART – B
(Answer all the questions: 05 X 10 = 50 Marks)


2  (a)  Perform the subtraction using 1's complement method.        5M
        (i) 11010 – 10000.01, (ii) 11010 – 1101, (iii) 101 – 110000.
   (b)  How do you convert a gray number to binary? Generate a 4-bit gray code directly using the        5M
        mirror image property.
                                                **OR**
3  (a)  Convert the following numbers;        5M
        (i) $(10101100111.0101)_2$ to Base 10, (ii) $(153.513)_{10}$ to base 8.
   (b)  Convert the following to required form.        5M
        (i) $(163.789)_{10} = (\ )_8$, (ii) $(101101110001.00101)_2 = (\ )_{10}$, (iii) $(292)_{16} = (\ )_2$.


4  (a)  Simplify the following using K- map and implement the same using NAND gates. Y (A, B, C) =        5M
        $\sum$ (0, 2, 4, 5, 6, 7).
   (b)  Obtain the simplified expression in SOP form of:        5M
           F(a, b, c, d, e) = $\Sigma$(1, 2, 4, 7, 12, 14, 15, 24, 27, 29, 30, 31) using K-map.
                                                **OR**
5  (a)  Reduce the following expression to the simplest possible POS and SOP forms. F = $\sum$m (6, 8,        5M
        13, 18, 19, 25, 27, 29, 31) +d (2, 3, 11, 15, 17, 24, 28).
   (b)  State and prove consensus theorem? Solve the given expression using consensus theorem.        5M
        (i) AB + AC + BC +BC+ AB, (ii) (A + B)(A + C)(B + C)(A + D)(B + D).


6  (a)  Write the differences between ring counter to johnson counter.        5M
   (b)  Design a combinational circuit for a 2-bit magnitude comparator.        5M
                                                **OR**
7  (a)  Design a 4-bit ring counter.        5M
   (b)  Draw and design the decade counter.        5M


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| 8 | (a) | Write the capabilities and limitations of FSM. | 5M |
| | (b) | Convert a D flip flop into SR flip flop and JK flip flop. | 5M |

**OR**

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|---|---|---|---|
| 9 | (a) | Explain the types of FSM. | 5M |
| | (b) | Explain the mealy to more conversion with an example. | 5M |

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| 10 | (a) | Write the design of Sequential circuits using ROMs. | 5M |
| | (b) | Explain about (i) conditional operator, (ii) if-else statement in verilog. | 5M |

**OR**

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| 11 | (a) | Write the advantages of FPGAs. | 5M |
| | (b) | Explain the for loop using storage elements with CAD tools. | 5M |

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