UNIT-1

OPERATIONAL AMPLIFIER

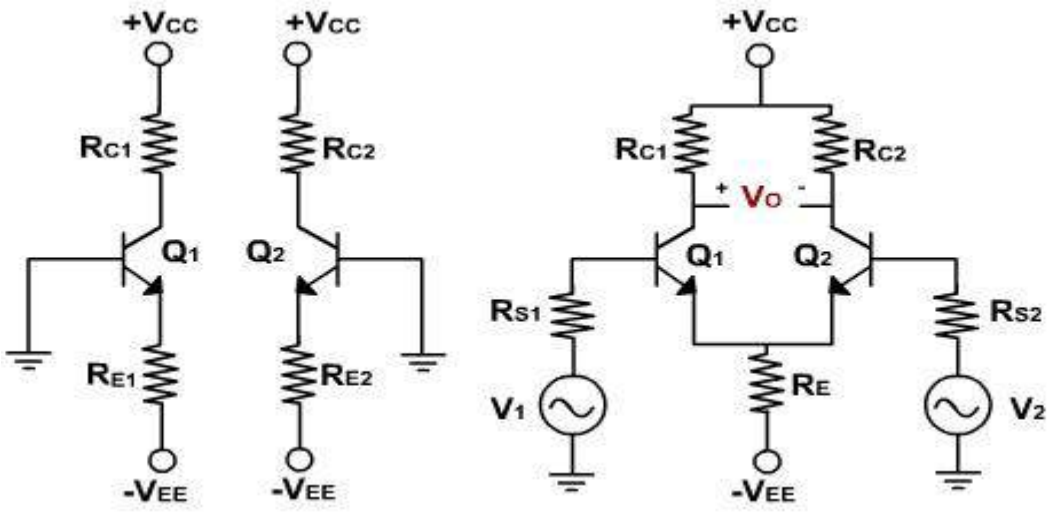
UNIT – I

Operational Amplifier: Introduction, Block diagram, Characteristics and Equivalent circuits ofan ideal op-amp, Various types of Operational Amplifiers and their applications, Power supplyconfigurations for OP-AMP applications, Inverting and non-inverting amplifier configurations.

The Practical op-amp: Introduction, Input offset voltage, Offset current, Thermal drift, Effect ofvariation in power supply voltage, common-mode rejection ratio, Slew rate and its Effect, PSRRand Gain bandwidth product, frequency limitations and compensations, transient response.

Differential amplifier: **Amplifier which amplifies the difference between two inputs.** The output signal of the differential amplifier is proportional to the difference between the two input signals.

Let us consider two emitter-biased circuits as shown



The two transistors Q_1 and Q_2 have identical characteristics. The resistances of the circuits are equal, i.e. $R_{E1} = R_{E2}$, $R_{C1} = R_{C2}$and the magnitude of $+V_{CC}$ is equal to the magnitude of $–V_{EE}$. These voltages are measured with respect to ground.

To make a differential amplifier, the two circuits are connected as shown above.The two $+V_{CC}$ and $–V_{EE}$ supply terminals are made common because they are same. The two emitters are also connected and the parallel combination of R_{E1} and R_{E2} is replaced by a resistance R_E. The two input signals v_1 & v_2 are applied at the base of Q_1 and at the base of Q_2. The output voltage is taken between two collectors. The collector resistances are equal and therefore denoted by $R_C = R_{C1} = R_{C2}$.

On account of symmetrical construction the circuit has low drift of I_{CBO} , V_{BE} &h_{fe} w.r.t temperature.

If a common input is applied to differential amplifier i.e $V_1 = V_2$ then the output is zero.

For a differential input, i.e $V_1 \neq V_2$,

One transistor is driven to higher conduction while the other is driven to lower conduction which results in differential voltage between two output terminals i.e proportional to the gain of the transistors.

Differential mode gain (A_d):

$$\mathbf{V_O = A_d\ (V_1 - V_2)}$$

$$\mathbf{V_O = A_d\ (V_d)}$$

$$\mathbf{V_O\ /V_d = A_d = \text{differential gain}}$$

If expressed in decibels

$$\mathbf{A_d\ (dB) = 20\ \log_{10} A_d}$$

Common mode gain (A_c):

$V_1 = V_2$,then $V_o = A_c\ (V_1 - V_2) = 0$

But the output of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs. Such an average level of the two input signals is called common mode signal(V_{cm}).

Common mode voltage $V_{cm} = (V_1+V_2) / 2$

Now output voltage $V_o = A_c V_{cm}$

Total voltage for any differential amplifier is

$Vo = A_d V_d + A_c V_{cm}$

CMMR(common mode rejection ratio):

The ability of a differential amplifier to reject common mode signal is expressed by ratio called CMRR.

It is defined as the ratio of differential voltage gain to common mode voltage gain.

CMRR= A_d/A_c(or) 20 log (A_d/A_c) dB

Differential amplifier circuit configurations.

Depending on number of inputs and the way the output is measured there are four differential amplifier configurations:

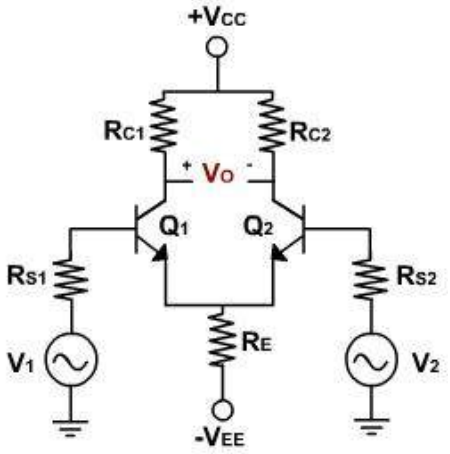
1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
3. Single input balanced output differential amplifier.
4. Single input unbalanced output differential amplifier.

- Balanced output: output is taken between two collectors (both the collectors are at the same dc potential w.r.t. ground)
- **Unbalanced output**: Output is taken between any one collector with respect to ground.

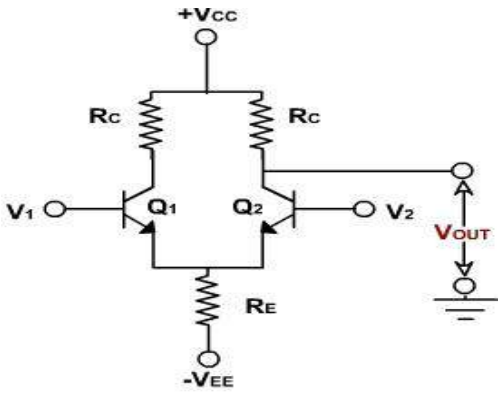
- Single input: Only one input is connected, other input grounded
- Dual input: Both inputs are applied

A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers.

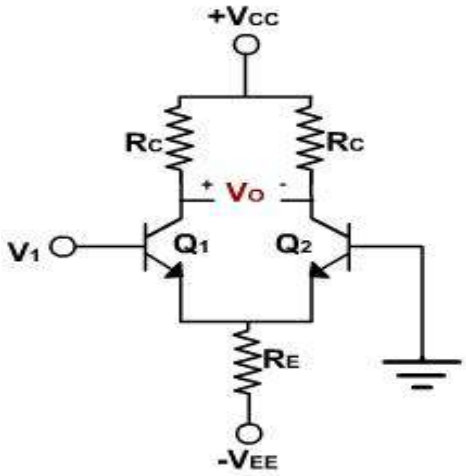
The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signals.



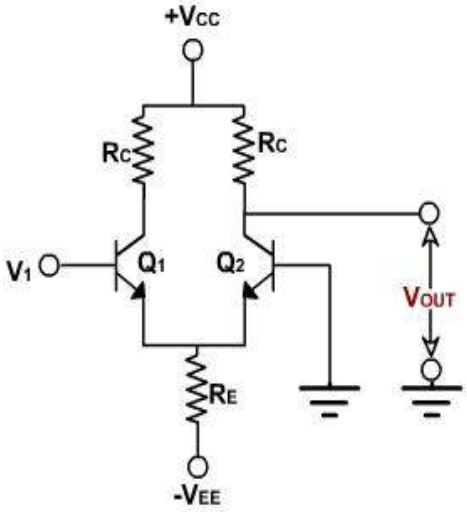
Dual input, balanced output differential amplifier



Dual input, unbalanced output differential amplifier



Single input, balanced output differential amplifier



Single input, unbalanced output differential amplifier

LEVEL TRANSLATOR:

A circuit which shifts the DC level of the input down to zero.

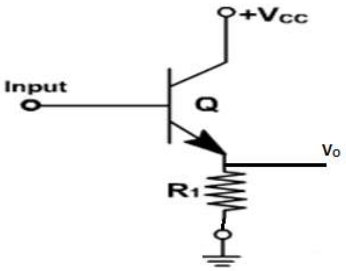
Features of level shifter:

- High input impedance & low output impedance(to avoid loading)
- Acts as buffer to isolate the high gain stages from output.

Simple level translator:Emitter follower

$V_O = V_i - V_{BE}$

$V_O - V_i = -V_{BE}$



If shift is not sufficient

$V_O = V_i - V_{BE} - IR_1$

$V_O - V_i = -(V_{BE} + IR_1)$

Limitation:

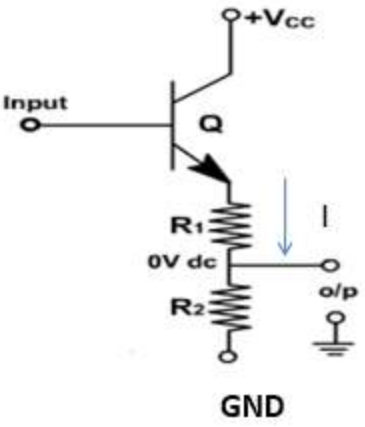
- **Even the signal gets attenuated by $R_2 / R_1 + R_2$**

$$I = \frac{V_E}{R_1 + R_2}$$

$$V_O = \frac{V_E}{R_1 + R_2} R_2$$

$$V_E = V_i - V_{BE}$$

$$V_{OUT} = \frac{V_i - V_{BE}}{R_1 + R_2} R_2$$



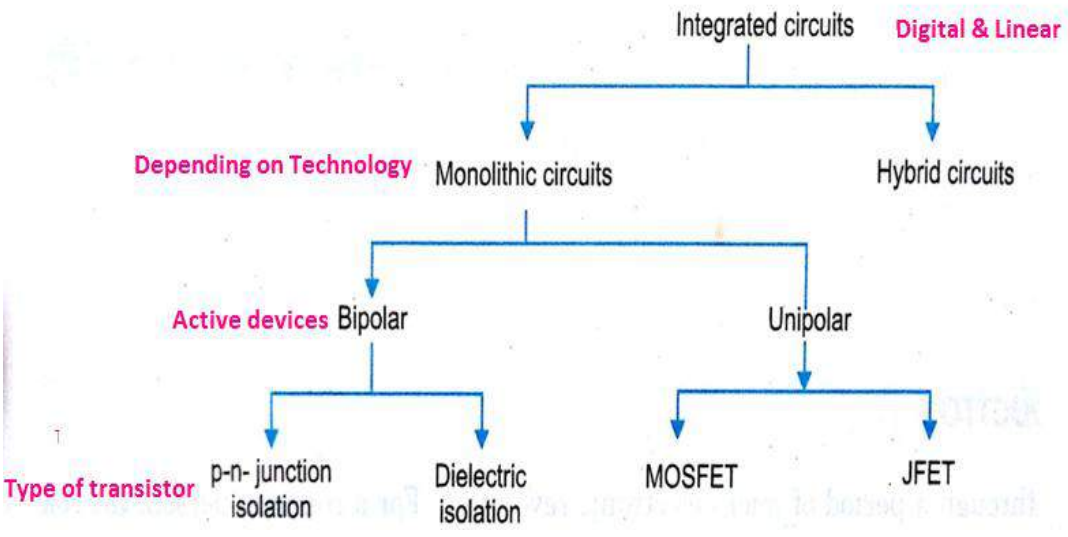
- **Increases the output impedance**

INTEGRATED CIRCUIT: A miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon.

Active components - transistors and diodes

Passive components - Resistors and capacitors.

Classification of ICs:



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Analog ICs:	Digital ICs:
ICs dealing with signals free to vary from zero to full power supply voltage. (Op- amp)	ICs dealing with signals restricted to values of zero and full supply voltage. (Micro processors)
Accurate control of Operating point	Accurate control is not needed
Requires additional components	Complete functional logic networks

Monolithic ICs	Hybrid ICs
Used in manufacturing identical circuits in large quantities	Separate component parts are attached to a ceramic substrate and interconnected by metallization
Low cost	Small quantities
More reliable	

ADVANTAGES OF INTEGRATED CIRCUITS:

- Miniaturization and hence increased equipment density.
- Cost reduction due to batch processing.
- Increased system reliability due to the elimination of soldered joints.
- Improved functional performance.
- Matched devices.
- Increased operating speeds.
- Reduction in power consumption

LEVELS OF INTEGRATION:

Depending on number of components on chip ICs are classified into the following.

Integration level	No of gates	No of transistors	Device
Small scale integration	**3 to 30**	**100**	**Logic gates**
MSI	**30 – 300**	**100-1000**	**Counters**
LSI	**300-3000**	**1000-20000**	**8 bit Microprocessor**
VLSI	**More than 3000**	**20000-1000000**	**32 bit microprocessor**
ULSI		**10^6 - 10^7**	
GSI		**>10^7**	

PACKAGE: A protective covering of chip

for easy handling

for assembling on PCBs

To protect from damage.

TYPES OF PACKAGES: There are three types of packages.

1. Dual in line package (DIP).
2. Metal can.
3. Flat package.

DIP Package: Chip is mounted in a plastic or ceramic case

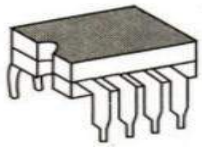
Available in 8, 12,14, 16 and 20.

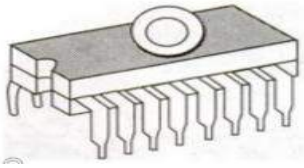
Advantages: Widely used

Can be mounted easily.

No need to bend the leads for mounting.

Uses: Experimentation / breadboarding purpose.





FLAT: Chip is mounted in a rectangular Ceramic case or plastic case

Pins extend through sides.

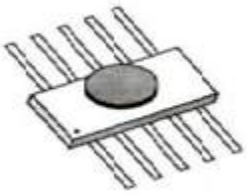
Available in 8,10,14,16 pins.

Advantages:

More reliable.

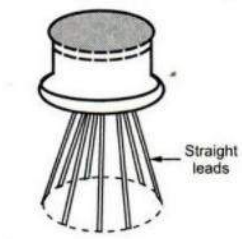
Light weight.

USES: Air borne applications.



METAL CAN: Metal or plastic case.

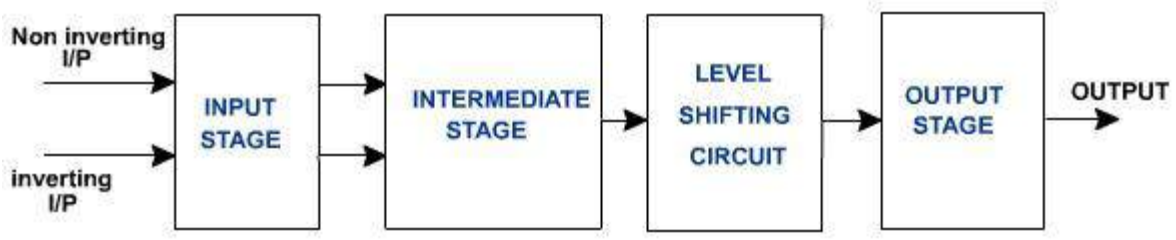
- 3,5,8,10,12 pins.
- Suited for Power amplifiers.(Heat dissipation)
- Allows use of external heat sinks.



OPERATIONAL AMPLIFIER:A direct coupled high gain amplifier which consists of one or more stages of differential amplifiers followed by a level translator and an output stage.

- Amplifies both DC and AC
- Performs many mathematical operations like addition, subtraction , multiplication and etc.

BLOCK DIAGRAM OF OP-AMP: Consists of one or more differential (OPAMP) amplifiers and followed by a level translator and an output stage..



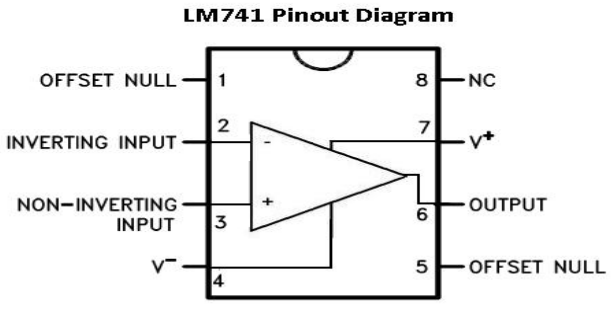
Input stage: It is a dual input balanced output differential amplifier. This stage provides most of the voltage gain of the amplifier and also establishes the input resistance of the OPAMP

Intermediate stage: It is a differential amplifier which is driven by the output of the first stage. This is usually dual input unbalanced output. Used for additional gain of the op-amp.

Level translator: Because direct coupling is used, the dc voltage level at the output of intermediate stage is well above ground potential. Therefore level shifting circuit is used to shift the dc level at the output downward to zero with respect to ground by using an emitter follower.

Output stage: It is a push pull complementary amplifier. The output stage increases the output voltage swing and raises the current supplying capability of the OPAMP. It also provides low output resistance.

Op-amp is available in 8 pin DIP package



Pin 1 & 5 offset null pins: These pins are used to nullify the output offset voltage by connecting a 10KΩ potentiometer across these pins.

Pin 2: Inverting input: This pin is used to apply an external input.

Pin 3: Non Inverting input: This pin is used to apply an external input.

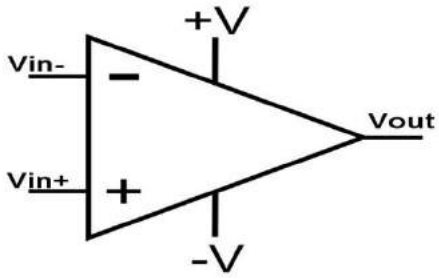
Pin 4 &7 : Negative supply & positive supply: These pins are used to bias the op-amp.

Pin 6: To measure the output.

Pin 8: No connection

SCHEMATIC SYMBOL OF OP-AMP:

A triangle with two inputs and one output. One input is inverting input and another is non inverting input.



IDEAL OP-AMP: It exhibits the following characteristics

- Infinite voltage gain A_d
- Infinite input resistance R_i, (so that almost any signal source can drive it and there is no loading of the input source).
- Zero output resistance R_O, (so that output can drive an infinite number of other devices).
- Zero output voltage when input voltage is zero.
- Infinite bandwidth (so that any frequency signal from 0 to infinite Hz can be amplified without attenuation.)
- Infinite common mode rejection ratio (so that the output common mode noise voltage is zero).
- Infinite slew rate, (so that output voltage changes occur simultaneously with input voltage changes.)

OP-AMP EQUIVALENT CIRCUIT:

A = Large signal voltage gain

V_{id} = Difference input voltage

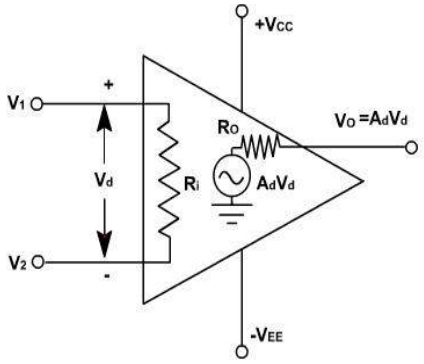
V_1 = Voltage at the non inverting terminal wrt ground.

V_2 = Voltage at the inverting terminal wrt ground.

$V_O = AV_{id} = A(V_1 – V_2)$ (equivalent Thevenin voltage source)

This equation indicates that the output voltage v_O is directly proportional to the algebraic difference between the two input voltages

R_i = Input impedance of OPAMP.
R_O = Thevenin equivalent impedance looking back into the terminal of an OPAMP



FEATURES OF IC 741 OP AMP:-

1. No frequency compensation required

2. Short circuit protection provided.

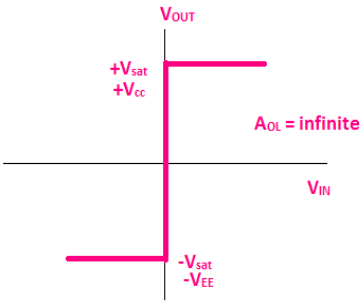
3. Offset voltage null capability

4. No latchup

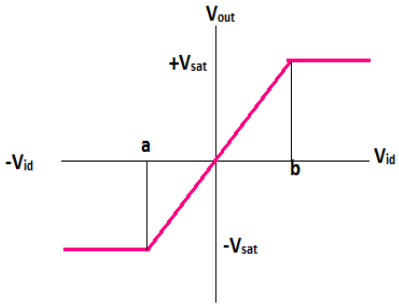
5. Large common mode and differential range.

VOLTAGE TRANSFER CURVE:

Graph plotted between output voltage V_o and difference input voltage V_{id}
Ideally the gain of the open loop op-amp is ∞.
$A_{OL} = V_o / V_{id} = \infty$
$V_{id} = V_o / \infty = 0$
For zero input the output is at saturated voltages because of infinite gain. Hence the voltage transfer curve is a vertical line.



Voltage transfer curve of practical op-amp:



The gain of the practical op-amp is not infinite hence for low input voltages the output is finite, for high voltages the output reaches saturated levels.

IDEAL	PRACTICAL
$V_{id} > 0, V_{out} = +V_{sat}$	$V_{id} > b, V_{out} = +V_{sat}$
$V_{id} < 0, V_{out} = -V_{sat}$	$V_{id} < a, V_{out} = -V_{sat}$

OPEN LOOP OPAMP CONFIGURATION:

Open loop: No connection (direct or indirect) exists between input and output.

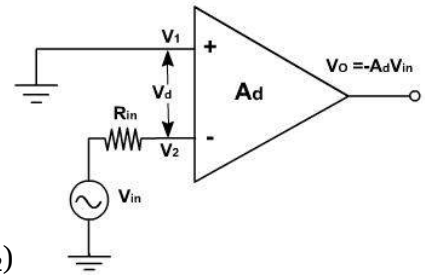
- Under open loop, op-amp acts as high gain amplifier.

There are three open loop configurations

- Inverting amplifier.
- Non inverting amplifier.
- Differential amplifier.

Inverting amplifier: Input is applied to inverting terminal and non inverting is grounded.

$V_1 = 0, V_2 = V_{in}$

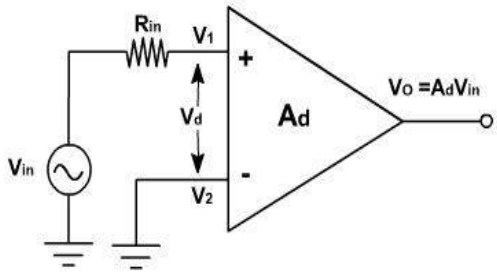


$V_{out} = A(V_1 - V_2)$

$= -A V_{in}$

- \- sign indicates 180^0 phase shift between input and output.

Non inverting amplifier: Input is applied to non inverting terminal and inverting is grounded.



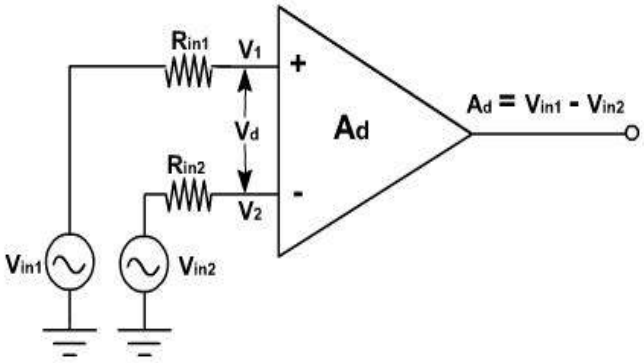
$V_1 = V_{in}, V_2 = 0$

$V_{out} = A(V_1 - V_2)$

$= A V_{in}$

- No phase shift between input and output.

Differential amplifier: Input is applied to both the input terminals.
Amplifies the difference of two inputs.



$V_1 = V_{in1}, V_2 = V_{in2}$

$V_{out} = A(V_1 - V_2)$

$= A (V_{in1} - V_{in2})$

- Output polarity depends on difference input polarity.

- For open loop configurations, mostly the output is $\pm V_{sar}$

PARAMETERS OF OP-AMP

Input offset Current: The difference between the currents into inverting and non-inverting terminals of a balanced amplifier.

$$I_{io} = | \quad I_{B1} - I_{B2} | = 200\eta A$$

Input Bias Current: The average of the current entering the input terminals of a balanced amplifier i.e.

$$I_B = (I_{B1} + I_{B2}) / 2 \ = 500\eta A.$$

Input offset voltage: The voltage that must be applied between the input terminals of an Op-amp to null the output.

$$V_{io} = 6mV$$

Differential Input Resistance: The equivalent resistance that can be measured at either the inverting or non-inverting input terminal with the other terminal grounded.

$$R_i = 2\ M\Omega$$

Input Capacitance: The equivalent capacitance that can be measured at either the inverting and noninverting terminal with respect to ground.

$C_i = 1.4$ pF

Common Mode Rejection Ratio : The ratio of the differential voltage gain A_d to the common mode voltage gain A_{CM}

$$CMRR = A_d / A_{CM} = 90\ dB$$

where $A_d = V_{od} / V_{id}$

$A_{CM} = V_{oCM} / V_{CM}$

- The ability of the differential amplifier to reject a common mode signal
- Higher the CMRR better the rejection.

Supply voltage Rejection Ratio: The ratio of the change in the input offset voltage to the corresponding change in power supply voltages.

$$SVRR = PSRR = \Delta V_{io} / \Delta V \ = 150\mu V/V$$

Large signal voltage gain: The ratio of output voltage to differential input.

A = output voltage/ differential input

= 2,00,000

Output voltage Swing: The maximum unclipped peak to peak output voltage that an OPAMP can produce.±13V

Output Resistance: The equivalent resistance that can be measured between the output terminal of the OPAMP and the ground.

$$R_O = 75\Omega$$

Output Short circuit Current : The short circuit current withstanding capability of Op-amp.

$$I_{SC} = 25mA.$$

Supply Current : The current drawn by the OPAMP from the supply.

$$I_S = 2.8\ mA$$

Power Consumption: Amount of quiescent power (v_{in}= 0V) that must be consumed by the OPAMP in order to operate properly.

$$P_C = 85mW$$

Gain Bandwidth Product: The bandwidth of the OPAMP when the open loop voltage gain is reduced to 1.

FEATURES OF 741 OP-AMP:

- Internally frequency compensated.
- Short circuit protection.
- Offset null capability.
- Large common mode and differential voltage ranges.
- Low power consumption.
- No latch up problem.
- Monolithic IC

COMPARISION BETWEEN IDEAL & PRACTICAL OP-AMP:

Parameter	Ideal Op-amp	Practical Op-amp
Input resistance	Infinity	Very high
Output resistance	Zero	Small finite
Bandwidth	Infinity	Very high
CMRR	Infinity	Very high
Slew rate	Infinity	Very high
Input offset voltage	Zero	Small finite
Voltage gain	Infinity	Very high

LIMITATIONS OF OPEN LOOP OP-AMP CONFIGURATION:

- Only the smaller signals having low frequency may be amplified.
- Open loop voltage gain varies with temperature and power supply.
- Bandwidth for open loop Op-amp is negligibly small.
- Not suitable for linear applications.

To overcome,

- Negative feedback is used.

FEEDBACK:

An output signal is fedback to the input either directly or via another network. The gain of the OPAMP can be controlled if fedback is introduced in the circuit

Depending on the way the output is fedback there are two types of feedback. They are

- **Positive feedback**:If the signal is fedback in phase with the input signal, the feedback is called positive feedback. In positive feedback the feedback signal aids the input signal. It is also known as regenerative feedback. Positive feedback is necessary in oscillator circuits.

- **Negative feedback:** If the signal feedback is of opposite polarity or out phase by 180° with respect to the input signal. Also known as degenerative feedback because it reduces the output voltage and,inturn,reduces the voltage gain. Used in amplifiers..

ADVANTAGES OF NEGATIVE FEEDBACK:

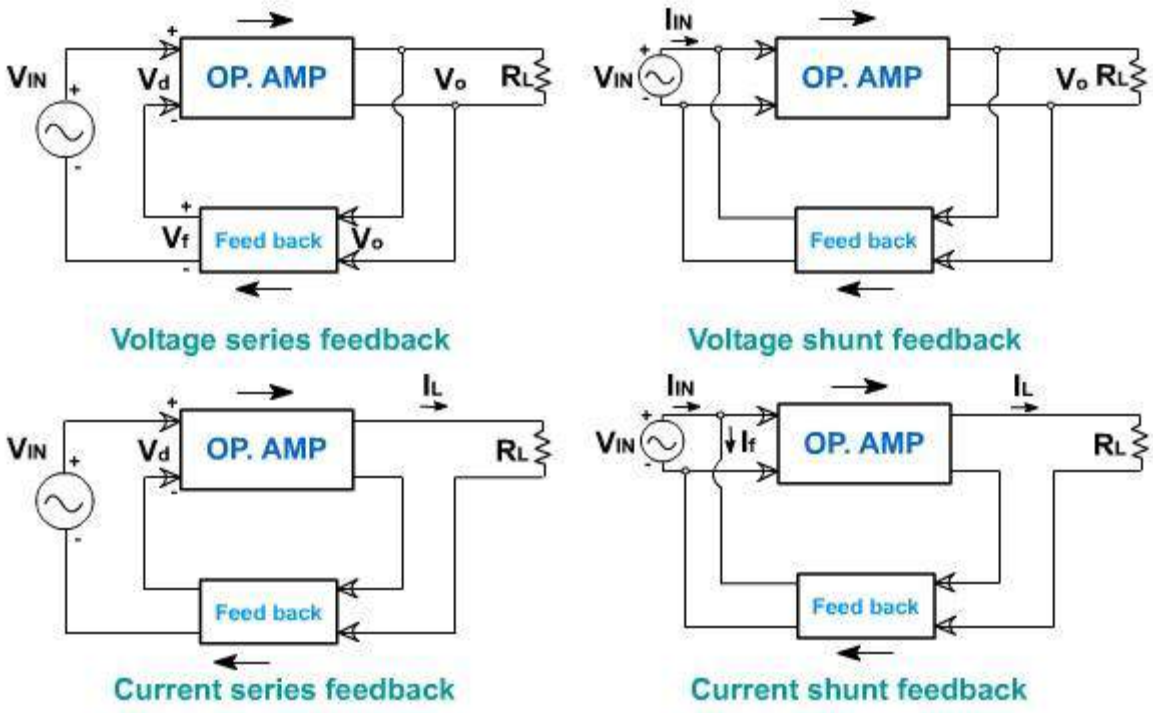
When used in amplifiers, negative feedback

- Stabilizes gain.
- Increases the bandwidth.
- Changes the input and output resistances.
- Decrease in harmonic distortion.
- Reduces the effect of input offset voltage.
- Reduces the effect of variations in temperature.

FEEDBACK AMPLIFIEROR CLOSED LOOP AMPLIFIER: An op-amp that uses feedback is called feedback amplifier.

It consists of two parts an op-amp and a feedback circuit. There are four ways to connect these two blocks.These connections are classified according to whether the voltage or current is feedback to the input in series or in parallel:

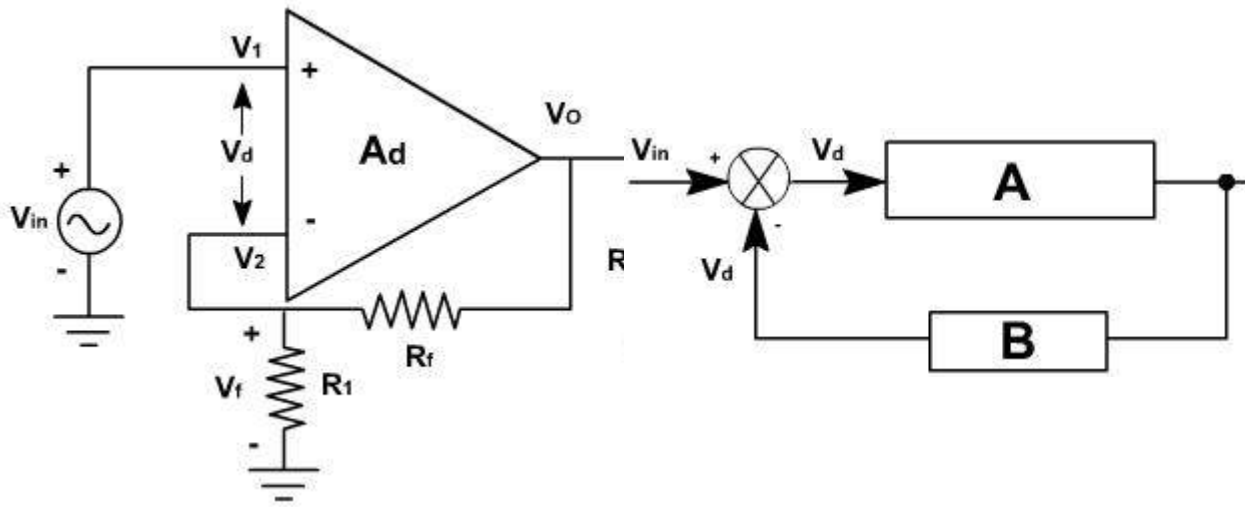
- Voltage – series feedback
- Voltage – shunt feedback
- Current – series feedback
- Current – shunt feedback



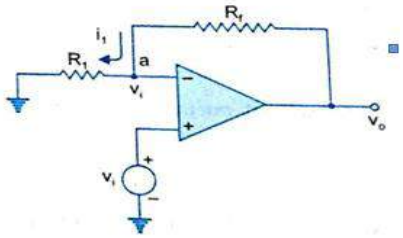
In all these circuits the signal direction is from input to output for OPAMP and output to input for feedback circuit. Only first two, feedback in circuits are important

VOLTAGE SERIES FEEDBACK AMPLIFIER (NON INVERTING AMPLIFIER):

The input signal drives the non-inverting input of an amplifier; a fraction of the output voltage is then fed back to the inverting input. The op-amp is represented by its symbol including its large signal voltage gain Ad or A, and the feedback circuit is composed of two resistors R_1 and R_F.



The voltage at non-inverting input terminal of an op-amp is approximately equal to that at the inverting input terminal provided that A_d is very large.



A = large signal voltage gain.

R_1, R_F = Feedback circuit.

Open loop voltage gain = $A = V_O / V_{id}$

Closed loop voltage gain = $A_F = V_O / V_{in}$

Gain of the feedback circuit = $\beta = V_F / V_O$

Negative feedback:

$V_{id} = V_{in} - V_f$

The feedback voltage always opposes the input.

Closed loop voltage gain:

$$A_F = \frac{V_O}{V_{In}}$$

$$V_O = A(V_1 - V_2)$$

$$V_1 = V_{in}$$

$$V_2 = V_f = \frac{V_O R_1}{R_1 + R_2}$$

$$V_O = A(V_{in} - \frac{V_O R_1}{R_1 + R_2})$$

$$V_O = \frac{A(V_{in}(R_1 + R_F) - R_1 V_O)}{(R_1 + R_F)}$$

$$V_O = AV_{in} - \frac{AR_1 V_O}{R_1 + R_F}$$

$$A_F = 1 + \frac{R_F}{R_1}$$

Limitation:

- The minimum gain achieved by non inverting configuration is 1.

Choose R_1 & R_F to be < than 1MΩ

Relation between A_F and β :

$$B = \frac{V_f}{V_O} = \frac{R_1}{R_1 + R_F}$$

$$A_F = \frac{1}{B}$$

$$A_F = \frac{A}{1 + AB}$$

II method to derive voltage gain:

$V_o = AV_{id}$

$V_{id} = \frac{V_o}{A}$

Since A is very large, $V_{id} = 0$

Therefore $V_1 = V_2$

$V_1 = V_{in}$

$V_2 = V_f = \frac{R_1 V_O}{R_1 + R_F}$

$V_{in} = \frac{R_1 V_O}{R_1 + R_F}$

$V_O / V_{in} = 1 + R_F / R_1$

Input resistance with feedback: $R_{if} = V_{in} / I_{in}$

$$R_{iF} = \frac{V_{in}}{i_{in}}$$

$$= \frac{V_{in}}{V_{id} / R_i}$$

but

$$v_{id} = \frac{v_o}{A} \qquad v_o = \frac{A}{1 + A\beta} v_{in}$$

$$R_{iF} = R_i \frac{v_{in}}{v_o / A}$$

$$= AR_i \frac{v_{in}}{Av_{in} / (1 + A\beta)}$$

$$= R_i (1 + A\beta)$$

R_i increases with feedback by (1+AB) times

Output resistance with feedback:

- Resistance seen looking back into the feedback amplifier from the output terminal.

- Output resistance is obtained by using Thevinins theorem for dependent sources. Reduce v_{in} to zero. Apply an external voltage v_o and then calculate the resulting current i_o.

$$R_{OF} = \frac{v_o}{i_o}$$

$$writing\ KCL\ at\ output\ node$$

$$i_o = i_a + i_b$$

$$\sin ce\ [(R_F + R_i) || R_i\ ] \square\ \ R_o\ \ and\ \ \ i_a \square\ \ i_b$$

$$therefore\ i_o \cong i_a$$

$$writing\ KVL\ at\ the\ output\ loop$$

$$v_o - R_o i_o - A v_{id} = 0$$

$$i_o = \frac{v_o - A v_{id}}{R_o}$$

$$v_{id} = v_1 - v_2$$

$$= 0 - v_f$$

$$= -\frac{R_1 v_o}{R_1 + R_F} = -Bv_o$$

$$i_o = \frac{v_o + ABv_o}{R_o}$$

$$substituting\ i_o$$

$$R_{oF} = \frac{v_o}{(v_o + ABv_o)/R_o}$$

$$= R_o / (1 + AB)$$

Output resistance decreases with feedback.

BANDWIDTH WITH FEEDBACK:

Bandwidth: Range of frequencies for which the gain remains constant.
Break frequency: Frequency at which the gain A is 3 dB down from its value at 0Hz.
Unity gain bandwidth: The frequency at which the gain equals 1.
For an op-amp with a single break frequency f_o , the gain bandwidth is constant, equal to the unity gain-bandwidth.
UGB = Af_o
A = open loop voltage gain
f_o = break frequency of an op-amp
UGB = $A_F f_F$
A_F = closed loop voltage gain
f_F = bandwidth with feedback

$Af_o = A_F f_F$

$f_F = Af_o / A_F$

For non inverting amplifier, with feedback

$A_F = A/(1+AB)$

$f_F = f_o (1+AB)$

Bandwidth increases with feedback

TOTAL OUTPUT OFFSET VOLTAGE:

Total output offset voltage With feedback = Total output offset voltage without feedback / 1+AB

$$V_{OOT} = \pm V_{sat} / (1+AB)$$

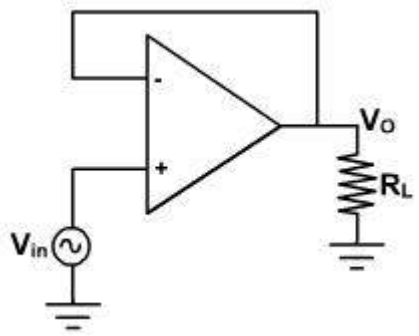
- Negative feedback reduces the effect of noise, variations in supply voltage, and changes on offset voltage with temperature.

Features of non inverting amplifier:

- Perfect voltage amplifier.
- Very high input impedance.
- Very low output impedance.
- Stable voltage gain.
- Large bandwidth.
- Very little output offset voltage.

VOLTAGE FOLLOWER:

When the non-inverting amplifier gives unity gain, it is called voltage follower because the output voltage is equal to the input voltage and in phase with the input voltage. In other words the output voltage follows the input voltage.



To obtain voltage follower, R_1 is open circuited and R_f is shorted in non inverting feedback amplifier.

$B = R_1 / (R_1 + R_F) = 1$
$A_F = 1/ B = 1$
$R_{iF} = (1+ AB) R_i = AR_i$ ($A >> 1$)
$F_F = Af_o$
$V_{OOT} = \pm V_{sat}/ A$

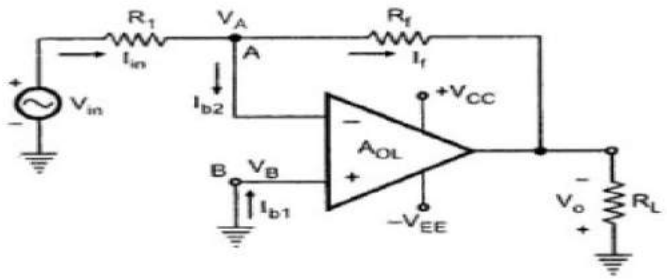
- Also called as non inverting buffer.

VOLTAGE SHUNT FEEDBACK AMPLIFIER (INVERTING AMPLIFIER):

Input drives the inverting terminal, and the amplified inverted signal is also applied to the inverting terminal via the feedback resistor R_F.

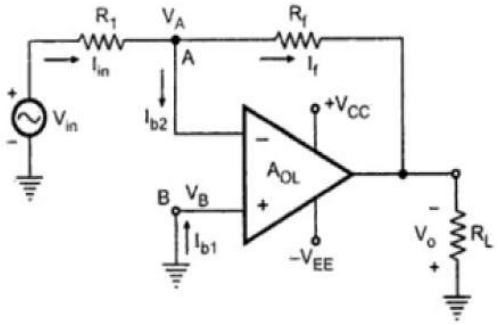
This arrangement forms a negative feedback because any increase in the inverting input causes a decrease in output.

Non inverting terminal is grounded. R_1 is connected in series with the input signal.



- The resistance R_f forms feedback from o/p to i/p
- Finite input impedance & A_{OL}
- Negative feedback is used.

- **Closed loop voltage gain:**
- Apply KCL at node 'A'



$$I_{in} = I_f + I_{b2} \quad \text{----(1)}$$

$$I_{in} \approx I_f \quad \text{----(2)}$$

$$\frac{V_{in} - V_A}{R_1} = \frac{V_A - V_0}{R_f} \quad \text{----(3)}$$

From equivalent circuit of op-amp we can write

$$V_0 = A_{OL}\, V_d = A_{OL}\,(V_1 - V_2) \quad \text{----(4)}$$

As $V_1 = 0$ V, $V_2 = V_A$

$$V_0 = -A_{OL}\, V_A$$

$$V_A = -\frac{V_o}{A_{OL}} \quad \text{----(5)}$$

Sub in eq(3)

$$\frac{V_{in} + \frac{V_o}{A_{OL}}}{R_1} = \frac{-V_0 + \frac{-V_o}{A_{OL}}}{R_f}$$

$$V_{in}\, R_f = -V_0 \left[\frac{R_1}{A_{OL}} + R_1 + \frac{R_f}{A_{OL}}\right] \quad \text{----(6)}$$

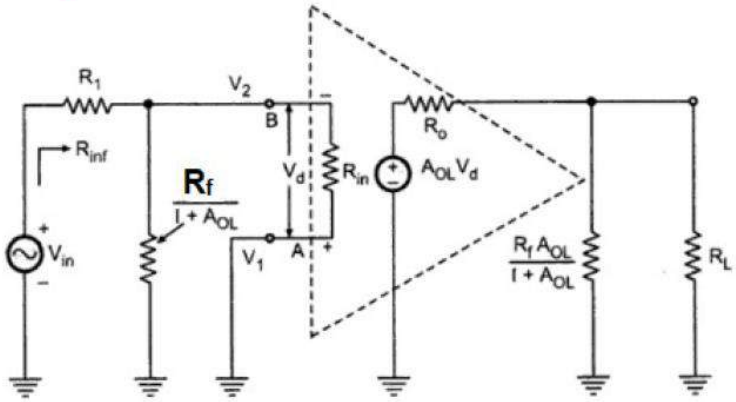
$$A_F = \frac{V_0}{V_{in}}$$

$$A_F = -\frac{A_{OL}\, R_f}{R_1 + R_f + A_{OL}\, R_f} \quad \text{----(7) (Practical)}$$

$$A_{OL}\, R_f \gg R_1 + R_f$$

$$A_F = -\frac{R_f}{R_1} \quad \text{(Ideal)}$$

Input Resistance with feedback:



- Equivalent circuit after applying millers theorem

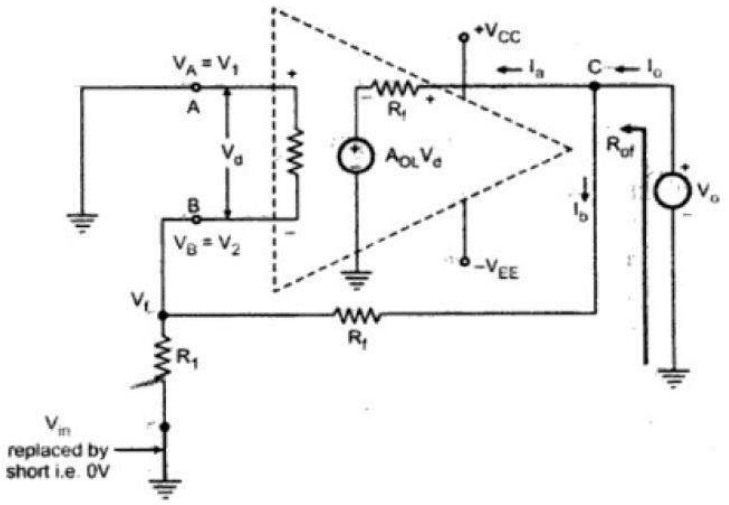
$$R_{inf} = R_1 + \left[\frac{R_f}{1+A_{OL}} \;||\; R_{in}\right]$$

$$R_{inf} = R_1 + \left[\frac{\left(\frac{R_f}{1+A_{OL}}\right) R_{in}}{\left(\frac{R_f}{1+A_{OL}}\right) + R_{in}}\right]$$

$$R_{inf} = R_1 + \frac{R_f\, R_{in}}{R_f + R_{in} + A_{OL} R_{in}} \quad \text{---- (9)}$$

- **For Ideal case AOL = ∞**
- **$R_{inf} \approx R_1$ ---- (10)**

output Resistance with feedback:



$$R_{0f} = \frac{V_0}{I_o}$$

- Apply KCL at node C
- $I_a + I_b = I_0$ ---- (11)
- $R_{in} \,||\, (R_1 + R_i) >> R_0$ ---- (12)
- As R_{in} is large, R_o is small
- $I_b << I_a$ ---- (13)
- $I_0 \approx I_a$
- Applying KCL to the output loop
- $V_0 - I_0 R_0 - A_{OL} V_d = 0$ as $I_a = I_0$

$$I_O = \frac{V_0 - A_{OL} V_d}{R_0} \quad \text{---- (14)}$$

- $V_d = V_1 - V_2 = V_A - V_B$
- Now the drop across the R_1 is V_f
- $V_d = 0 - V_f = -V_f$ ---- (15)

$$V_f = \frac{R_1 V_o}{R_1 + R_f}$$

But wkt $B = \frac{R_1}{R_1 + R_f}$

$V_f = B\,V_0$ ---- (16)

- Sub (16) in (15)
- $V_d = - BV_0$ ---- (17)
- Sub in (14)

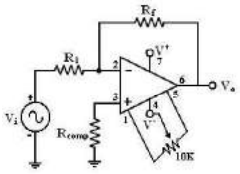
$$I_O = \frac{V_0 - A_{OL}(-B\,V_0)}{R_0}$$

$$I_O = \frac{V_0(1 + A_{OL}B)}{R_0} \quad \text{---- (18)}$$

$$R_{of} = \frac{V_0}{I_0} = \frac{R_0}{(1+A_{OL}B)} \quad \text{---- (19)}$$

Total output offset voltage:

- The total output offset voltage is the voltage produced at the output side due to the input bias current or input offset voltage (V_{ios})



- 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4.
- The position of the wipes is adjusted to nullify the offset voltage

Thermal drift:

- Bias current, offset current, and offset voltage change with temperature.
- A circuit carefully nullified at 25^0C may not remain same if temperature varies, therefore the change due to temp is referred as Thermal drift.

Contd..

$$\text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

ΔV_{ios} = Change in input offset voltage

ΔT = Change in temperature

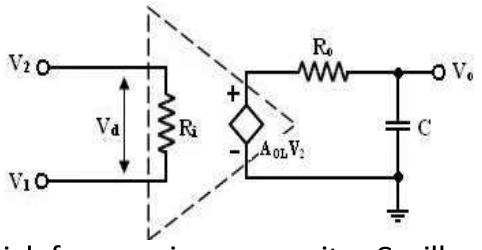
$$\text{Thermal drift in input bias current} = \frac{\Delta I_b}{\Delta T}$$

$$\text{Thermal drift in input offset current} = \frac{\Delta I_{ios}}{\Delta T}$$

Comparison of Ideal Practical op-amp Parameters

Sr. No	Parameter	Symbol	Ideal	Typical for 741 IC
1	Open loop voltage gain	A_{OL}	∞	2×10^5
2	Output impedance	Z_{out}	0	75 Ω
3	Input impedance	Z_{in}	∞	2 MΩ
4	Input offset current	I_{os}	0	20 nA
5	Input offset voltage	V_{os}	0	1 mV
6	Bandwidth	B.W	∞	1 MHz
7	CMRR	ρ	∞	90 dB
8	Slew rate	S	∞	0.5 V/μ sec
9	Input bias current	I_b	0	80 nA
10	PSRR	PSRR	0	30 μV/V

High Frequency op-amp equivalent circuit:



- In high frequencies, a capacitor C will get added to the output of our op-amp.

$$|A| = \frac{A_{OL}}{\sqrt{1+(f/f_1)^2}}$$

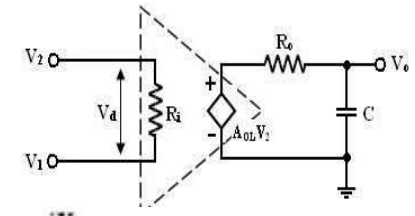
AC Characteristics:

- For small signal AC application of to Op-amp, we should know about the AC characteristics of op-amp such as:
  - Frequency response
  - Slew-Rate

Contd…

- **Frequency Response:**
  - It is the graph drawn between frequency and gain.
  - The variation in operating frequency will cause variations in gain magnitude and its phase angle.
  - At higher frequencies gain decreases.
  - Due to capacitance effect at the output of op-amp

Contd…



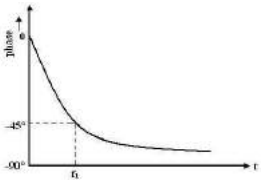
$$v_o = \frac{-jX_c}{R_o - jX_c} A_{OL} v_d$$

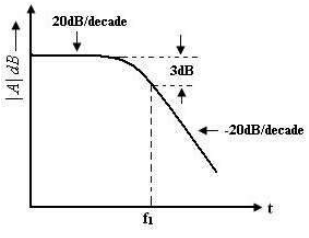
$$A = \frac{v_o}{v_d} = \frac{A_{OL}}{1 + j\,2\pi f R_o C}$$

$$A = \frac{A_{OL}}{1 + j(f/f_1)} \qquad f_1 = \frac{1}{2\pi R_o C}$$

$$|A| = \frac{A_{OL}}{\sqrt{1+(f/f_1)^2}} \qquad \phi = -\tan^{-1}(f/f1)$$

- For frequency f<< f_1 the magnitude of the gain is 20 log A_{OL} in dB.
- At frequency f = f_1 the gain in 3 dB down from the max value of A_{OL} in dB. This frequency f_1 is called **corner frequency**.
- For f>> f_1 the Gain roll-off at the rate off -20dB/decade.





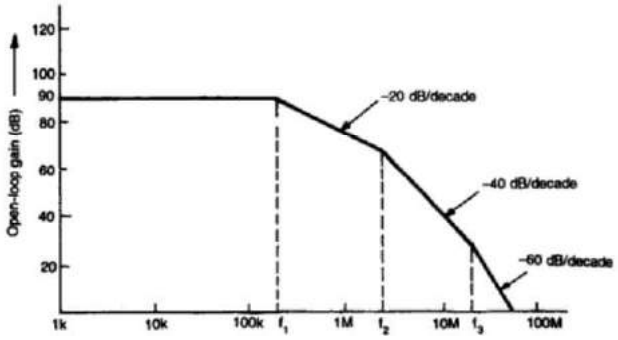
Contd…

If the op-amp operates with more than
One corner frequencies

$$A = \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)};\ 0 < f_1 < f_2 < f_3$$

$$A = \frac{A_{OL} \cdot \omega_1 \cdot \omega_2 \cdot \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$

Contd…



- Open loop gain verses frequency

Slew Rate:

- Another important frequency related parameter of an op-amp is the slew rate.
- Slew rate is the maximum rate of change of output voltage with respect to time.
- Specified in V/µs

Effect of slew rate:

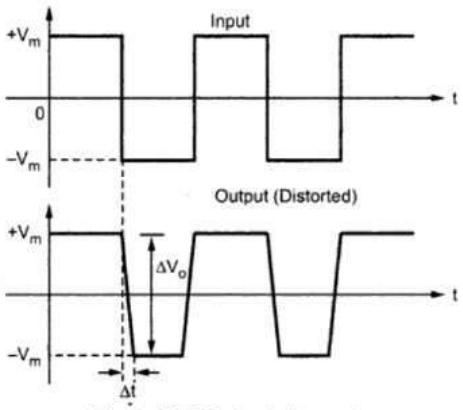


Fig. 2.40 Effect of slew rate

- **Reason for Slew rate:**
- There is usually a capacitor within or outside an op-amp to prevent oscillation.
- This capacitor which prevents the o/p voltage from fast changing input.
- The rate at which the voltage across the capacitor changes is given by

$$\frac{dV}{dt} = \frac{i}{C} \qquad i = C\frac{dV}{dt}$$

Contd…

dV/dt = I/C

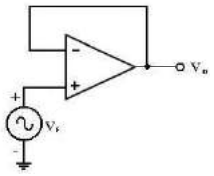
I -> Maximum amount furnished by the op-amp to capacitor C

slew rate of 741 IC is

$$SR = |dV/dt|_{max} = I_{max}/C .$$

Contd…

- For a sine wave input, the effect of slew rate can be calculated as consider voltage follower
- If $Vs = V_m \sin wt$
- then output $V_0 = Vm \sin wt$.



- The rate of change of output is given by
- $dV_0/dt = Vm\ w \cos wt.$

Contd…

•The max rate of change of output (when coswt =1)

$$SR = dV_0/dt\ |max = w\ Vm.$$

$$SR = 2\pi f\ Vm \quad V/s$$

•Thus the maximum frequency f_{max} at which we can obtain an un-distorted output volt of peak value Vm is given by

$$f_{max} = \frac{SR}{2\pi V_m}$$

•Where, f_{max} is the full power bandwidth.

Example - 1

- A 100 PF capacitor has a maximum charging current of 150 µA. What is the slew rate?

$$SR = \frac{I_{max}}{C} = \frac{150\ x\ 10^{-6}}{100\ x\ 10^{-12}} = 1.5\ V/\mu s$$

Example - 2

- An operational amplifier has a slew rate of 2 V / μs. If the peak output is 12 V, what is the power bandwidth?

$$f_{max} = \frac{SR}{2\pi V_m} = \frac{\frac{2}{10^{-6}}}{2\pi \, x \, 12} = 26.5 \text{ KHz}$$

Frequency compensation:

- The op-amp circuit with single break or corner frequency is inherently stable.
- Frequency compensation technique is used
  - To get larger band width with lower closed loop gain
  - To alter the response as per the requirement.
- There are 2 compensation techniques.
  1) External compensation
  2) Internal compensation

Frequency compensation:

1) external frequency compensation:

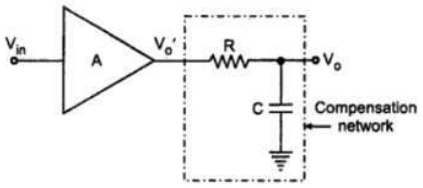
There are 2methods:

1. Dominant pole
2. Pole-zero compensation

Dominant pole compensation:

- Consider an op-amp with three break frequencies and with loop gain is A.

$$A = \frac{A_{OL}}{(1+j\frac{f}{f_1})(1+j\frac{f}{f_2})(1+j\frac{f}{f_3})}$$

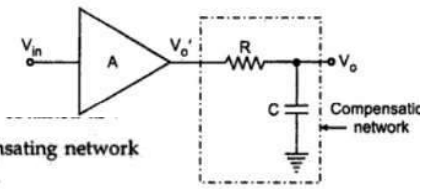


Contd..

- Dominant pole is introduced by adding a compensating network (R-C Network).
- The dominant pole means the pole with magnitude much smaller than the existing poles.
- The break frequency of the compensating network is the smallest compared to the existing break frequencies.

Contd..

- The transfer function of the compensating network can be obtained as:



A_1 = Transfer function of compensating network

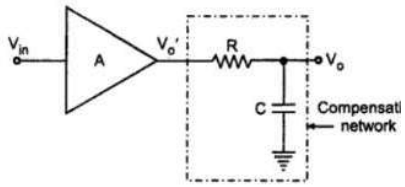
$$= \frac{V_o}{V_o'}$$

By the voltage divider rule applied to the network,

$$A_1 = \frac{V_o}{V_o'} = \frac{-jX_C}{R-jX_C}$$

Contd..

$$A_1 = \frac{1}{1+j\left(\frac{f}{f_d}\right)}$$



Hence, the compensated transfer function becomes

$$A' = AA_1$$

$$A' = \frac{A_{OL}}{(1+j\frac{f}{f_d})(1+j\frac{f}{f_1})(1+j\frac{f}{f_2})(1+j\frac{f}{f_3})}$$

Where fd < f1 < f2 < f3

Contd..

$$= \frac{-\frac{j}{2\pi f C}}{R-\frac{j}{2\pi f C}} = \frac{1}{\frac{R}{\left(-\frac{j}{2\pi f C}\right)}+1}$$

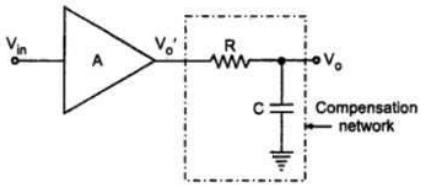
As $\frac{1}{-j} = +j$, we can write

$$A_1 = \frac{1}{1+j2\pi f R C}$$

Let $f_d = \frac{1}{2\pi R C}$

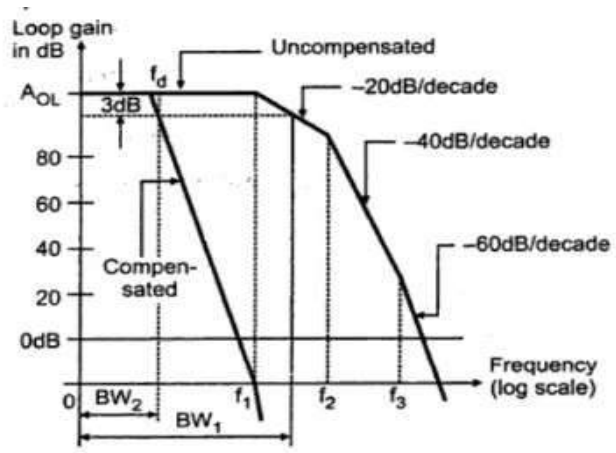
f_d = break frequency of the compensating network.

Contd..



- The value of R & C selected in such a way that the loop gain drops to 0 dB with a slope of -20 dB/dec
- At that frequency where the poles of uncompensated system contributes very small phase shift.

Contd..



Advantages:

- As the noise frequency components are outside the smaller bandwidth, the noise immunity of the system improves.
- Adjusting value of f_d, adequate phase margin and the stability of the system is assured.

Disadvantages:

- The bandwidth reduces drastically

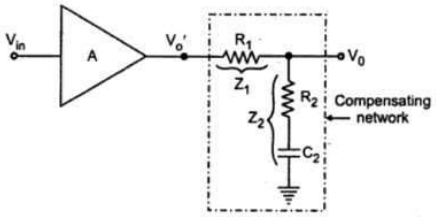
Pole-zero Compensation:

- Consider an op-amp with three break frequencies

$$A = \frac{A_{OL}}{(1+j\frac{f}{f_1})(1+j\frac{f}{f_2})(1+j\frac{f}{f_3})}$$

- The Transfer function is modified by adding a pole and a zero with the help of compensating network
- Zero added at high frequency
- Pole is added at lower frequency

Contd..



- The transfer function of compensating network is:

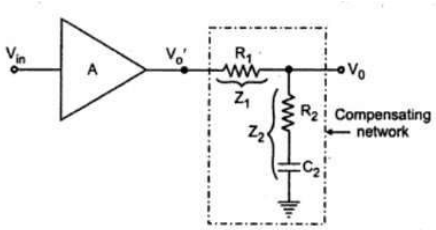
$$A_1 = \frac{V_0}{V_0'}$$

By the voltage divider rule,

$$A_1 = \frac{Z_1}{Z_1 + Z_2}$$

Contd..

- Where,
  - $Z_2 = R_2 - jXC_2$
  - $Z_1 = R_1$



$$A_1 = \frac{R_2 - jX_{C2}}{R_1 + R_2 - jX_{C2}} = \frac{R_2 - \frac{j}{2\pi f C_2}}{R_1 + R_2 - \frac{j}{2\pi f C_2}} = \frac{\frac{R_2}{\left[\frac{-j}{2\pi f C_2}\right]} + 1}{\frac{R_1 + R_2}{\left[\frac{-j}{2\pi f C_2}\right]} + 1}$$

Contd..

$$A_1 = \frac{1 + j2\pi f R_2 C_2}{1 + j2\pi f (R_1 + R_2) C_2}$$

Let,

$$f_1 = \frac{1}{2\pi R_2 C_2}$$

$$f_o = \frac{1}{2\pi (R_1 + R_2) C_2}$$

$$A_1 = \frac{1 + j\left(\frac{f}{f_1}\right)}{1 + j\left(\frac{f}{f_o}\right)}$$

Contd..

- The values of R_1. R_2 & C_2 are so selected to
- Break frequency for zero matches with the first corner frequency (f_1)
- Pole of the compensating network (at f_0) is selected to passes through 0 dB at second corner frequency.

Contd..

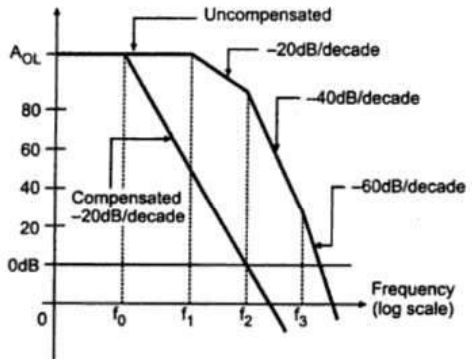
- The resultant loop gain becomes

$$A' = AA_1$$

$$= \frac{A_{OL}\left(1+j\frac{f}{f_1}\right)}{\left(1+j\frac{f}{f_0}\right)\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$$

- Where $0 < f_0 < f_1 < f_2 < f_3$
- 1st corner freq → f0 → Gain roll off -20 dB /Dec
- At f = f_1 → pole zero cancellation → -20 dB/ Dec
- R_1. R_2 & C_2 are selected such that the plot passes through 0 at f_2

Contd..



- **Advantage:** Compared to dominant pole compensation bandwidth increases.

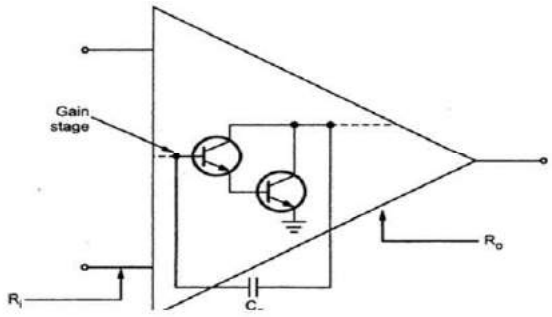
Internal Compensation Technique:

- In IC 741 op-amp, compensation provided internally.
- A capacitor from 10 to 30 pF fabricated between input and output stage.
- This type of compensation is also called Miller effect compensation.
- Such op-amps are called compensated op-amps.

Internal Compensation Technique:

- The Main drawback of dominant pole compensation is the reduction in the bandwidth.
- Capacitor value required is Large.
- These drawbacks are avoided by using Miller effect compensation.
- In miller effect a capacitor is connected in feedback path.

Contd..



- Darlington pair used in the output stage is show in above fig.
- Cc is the compensating capacitor.

Contd..

- The gain of the Darington stage is given by

$$a_2 = -G_{mc} R_o$$

Where G_{mc} = Transconductance of the stage

$$Z_{CM} = \frac{Z_{C_c}}{1+a_2}$$

Where $Z_{CM} = \frac{1}{j\omega C_M}$ and $Z_{C_c} = \frac{1}{j\omega C_c}$

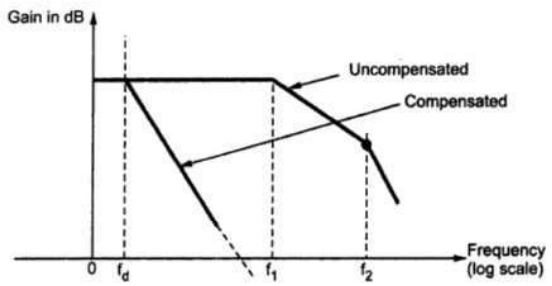
$$\frac{1}{j\omega C_M} = \frac{\frac{1}{j\omega C_c}}{(1+a_2)} \qquad C_M = (1 + a_2) C_c$$

Contd..

- The Cc gets multiplied by $(1+a_2)$, so practically small Cc values can be used.
- The Millers equivalent capacitance C_M forms a low pass RC section with input R_i, whose corner frequency is given by,

$$f_d = \frac{1}{2\pi C_M R_i}$$

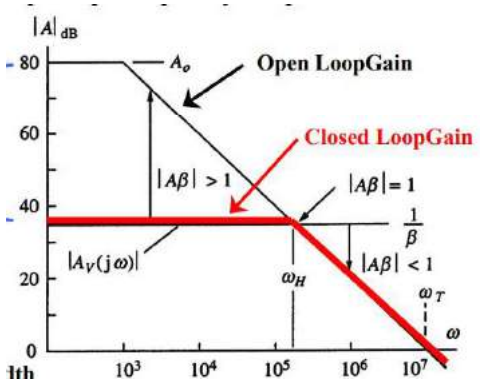
Contd..



- Miller compensation causes rearrangement of original poles and cause Pole Splitting.
- f_1 → Lowered & f_2 → raised.
- So , Bandwidth increases.

Closed loop op-amp frequency response:

$$A_F = \frac{A}{1 + AB}$$



- **FEATURES OF 741 OP-AMP:**
  - Internally frequency compensated.
  - Short circuit protection.
  - Offset null capability.
  - Large common mode and differential voltage ranges.
  - Low power consumption.
  - No latch up problem.
  - Monolithic IC

COMPARISION BETWEEN IDEAL & PRACTICAL OP-AMP:

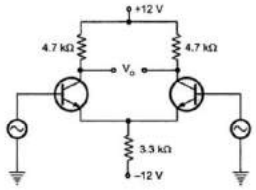
Parameter	Ideal Op-amp	Practical Op-amp
Input resistance	Infinity	Very high
Output resistance	Zero	Small finite
Bandwidth	Infinity	Very high
CMRR	Infinity	Very high
Slew rate	Infinity	Very high
Input offset voltage	Zero	Small finite
Voltage gain	Infinity	Very high

Applications of OP-AMPS

- Adders
- Subtractors
- Comparators
- Integrators & Differentiators
- Active filters
- Personal Computers

Problems:

1. Calculate the operating pint values for the circuit shown below.



$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} = \frac{12 - 0.7}{2 \times 3.3 \times 10^3} = 1.712 \text{ mA}$$

$$I_C = I_E = 1.712 \text{ mA} \quad I_{CQ} = 1.712 \text{ mA}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ}R_C$$

$$= 12 + 0.7 - 1.712 \times 10^{-3} \times 4.7 \times 10^3 = 4.653 \text{ V}.$$

∴Q point is (1.712 mA, 4.653 V).

Problems:

2 .The common mode input to a certain differential amplifier, having differential gain of 125 is 4 Sin 200 ∏ t. Determine the common mode output if CMRR is 60dB.

- 60 = 20 Log (Ad/Ac)
- Log (Ad/Ac) = 3
- (Ad/Ac) = 1000 wkt Ad = 125
- Ac = Ad/1000 = (125/1000) = 0.125
- V_{oc} = Ac Vc = 0.125(4 Sin 200 ∏ t) = **0.5 Sin (200∏t) V**

Problems:

3. An op-amp has a differential gain of 80dB and CMRR of 95dB. If V1 = 2uV and V2 =1.6uV, then calculate the differential and common mode output values.

- Ad in dB = 20 log Ad = 80
- Ad = 1×10^4
- CMRR in dB = 20 log CMRR

Problems:

- 95 = 20 log CMRR
- CMRR = 5.6234×10^4
- Differential output can be calculated as
- Vd = Ad (V1 – V2)
- = 1×10^4 (2-1.6) x 10^{-6}
- = 4mV

Problems:

- The common mode output can be calculated as,
- Vc = Ac(V1+V2)/2
- CMRR = Ad/Ac
- $5.6234 \times 10^4 = (1 \times 10^4) / Ac$
- Ac = 0.1778
- Vc = 0.1778 x (2+1.6)/ 2 x 10^{-6}
- Vc = 0.32uV