Code: 20A04504a

R20

B.Tech III Year I Semester (R20) Regular & Supplementary Examinations January 2024

COMPUTER ARCHITECTURE & ORGANIZATION

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a)	Write about register transfer notations.	2M
(b)	For what reason devices generate interrupts?	2M
(c)	List the four basic functions of the CPU.	2M
(d)	Write the address sequencing capabilities required in a control memory.	2M
(e)	Explain the conversion of octal number to hexadecimal number with an example.	2M
(f)	Design an Adder to add two 4-bit numbers.	2M
(g)	Explain significance of Memory hierarchy.	2M
(h)	Discuss about possible modes of data transfer.	2M
(i)	What is Parallel processing?	2M
(j)	Describe the need for inter processor communication.	2M

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

2 Briefly explain the input-output instructions. 10M

OR

3 Draw and explain the working of a bus system for four registers. 10M

4 Briefly explain logical and bit manipulation, shift instructions. 10M

OR

5 Explain the working of microprogram sequencer with a neat diagram. 10M

6 Show the step by step multiplication process using booth algorithm when the following binary numbers are multiplied (+15)*(-13). Assume 5-bit registers that hold signed numbers and draw the flow chart for the corresponding example. 10M

OR

7 Draw and explain the addition and subtraction of floating-point numbers. 10M

8 Construct an Associative memory page table with number of words equal to the number of blocks in the main memory. 10M

OR

9 Discuss about Set Associative mapping. 10M

10 Explain instruction pipeline with neat timing diagram. 10M

OR

11 Explain briefly about the characteristics of multiprocessors. 10M

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PART – A

(Compulsory Question)

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1		Answer the following: (10 X 02 = 20 Marks)	
	(a)	What is computer Architecture?	2M
	(b)	List the phases of instruction cycle.	2M
	(c)	List the address sequencing capabilities required in a control memory.	2M
	(d)	What are the fields in Instruction format?	2M
	(e)	Find (1001101 - 10101001) using 1's complement?	2M
	(f)	Multiply 10111 by 10011 using successive shift and add operations process.	2M
	(g)	Write any two differences that exist between Central computer and Peripherals.	2M
	(h)	What is Bootstrap Loader?	2M
	(i)	What is the Flynn's classification of computers?	2M
	(j)	Write a short note on synchronous bus.	2M

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

2		Distinguish between circular shift and arithmetic shift with proper example.	10M
		OR	
3		Explain memory reference instructions with an examples.	10M
4		Explain the design of micro programmed control unit in detail.	10M
		OR	
5	(a)	Explain three address instruction formats.	5M
	(b)	Explain Immediate and Register Indirect Addressing modes.	5M
6		Convert the following binary number into decimal & octal number: (i) $(00010.110)_2$ (ii) $(000.10110)_2$.	10M
		OR	
7		Discuss about Booth's multiplication algorithm.	10M
8		Distinguish between Isolated versus Memory Mapped I/O.	10M
		OR	
9		Explain different types of mapping functions in cache memory.	10M
10		Distinguish the characteristics of RISC and CISC.	10M
		OR	
11		What is multiprocessor system? Explain the advantages of multi processors over uniprocessors.	10M

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