

SEQUENTIAL LOGIC

Q1(a) Deduce the design procedure for sequential logic circuits?
To design any type of sequential logic circuit

use a common procedure:

Step ①:- From the given specification draw state diagram.

Step ②:- Draw state table from state diagram.

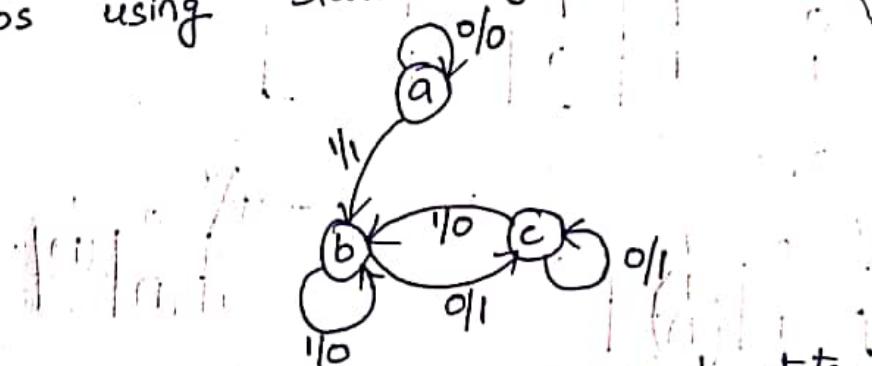
Step ③:- Reduce number of states using state reduction process.

Step ④:- Assign binary values to the states using state reduction process.

Step ⑤:- Derive state equations from reduced state table.

Step ⑥:- Draw logic diagram using state equations.

Example:- Design of sequential circuit using 'D' flip flops using state diagram.



From the state diagram represent state table

PS	I/P	NS	O/P
a	0	a	0
a	1	b	1
b	0	c	1
b	1	b	0
c	0	c	1
c	1	b	0

From the observation two states $b = c$.

Reduced state table becomes

PS	I/P	NS	O/P
a	0	a	0
a	1	b	1
b	0	b	1
b	1	b	0

For state assignment use condition $2^n \geq m$

$n = \text{no of binary bits}$

$m = \text{no of states}$

Here $m=2$. Then $n=1$ [only one binary bit].

$$a=0$$

$$b=1$$

state table becomes

PS	I/P	NS	O/P	flip-flop I/P
Q	x	Q _{n+1}	y	D
0	0	0	0	0
0	1	1	1	1
1	0	1	1	1
1	1	1	0	1

D is same as output (Q_{n+1})

State equations :-

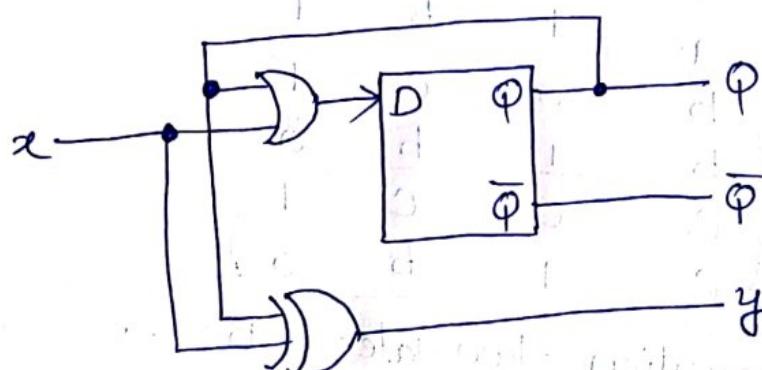
$$\text{For } D \Rightarrow Q'x \quad \begin{array}{|c|c|} \hline 0 & 1 \\ \hline 1 & 1 \\ \hline \end{array}$$

$$D = Q + x$$

$$\text{For } y \Rightarrow Q' \quad \begin{array}{|c|c|} \hline 0 & 1 \\ \hline 0 & 0 \\ \hline \end{array}$$

$$y = Q'x + Q'x' = Q \oplus x$$

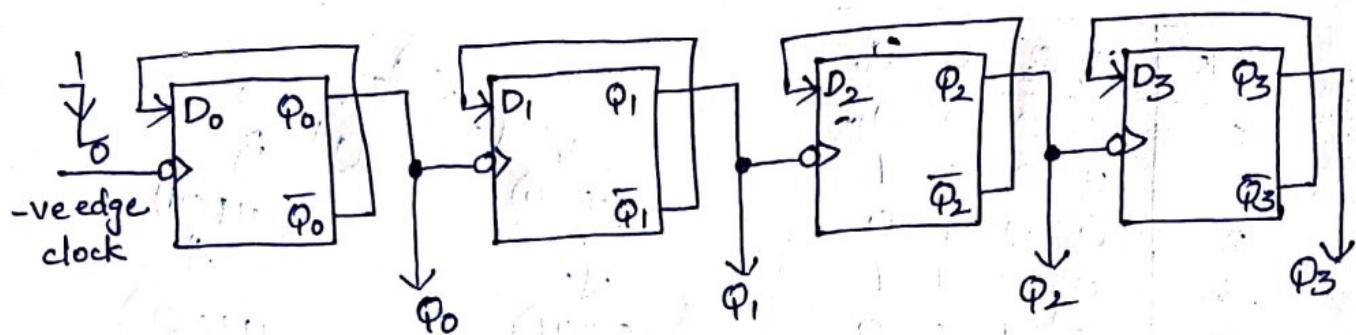
Logic diagram :-



①(b) Design a 4-bit ripple counter using D-flip-flops.

To design 4-bit ripple counter require 4 delay flip-flops.

Block diagram of counter:-



Operation:-

- * In ripple counter clock is applied for only first flip-flop directly.
- * Each flip-flop output act as clock input for next flip-flop.
- * Here using a -ve edge triggered clock, i.e., a transition from logic 1 to 0 can act as a proper clock.
- * In D-flip flop in the presence of proper clock output is same as input(D) & in the absence of clock output is no change condition (same as previous output).

CLK	D	O/P
0	0	NC
0	1	NC
1	0	0
1	1	1

- * In ripple counter (up counter) the initial state is always 0 i.e., (0000).
- * In circuit each flip-flop complemented output act as input(D) in each state.
- * For first clock pulse $\bar{Q}_0 = 1$ so $D_0 = 1$ then $Q_0 = 1$.
- * For second F-F output is due to 0 to 1 transition in Q_0 .

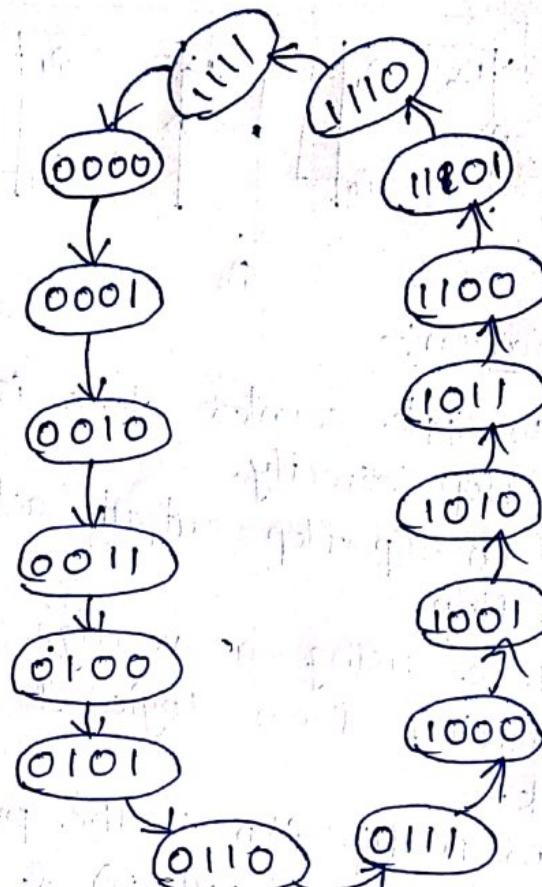
no change ($Q_1=0$). Due to 0 to 0 transition in Q_1 , output $Q_2=0$ & also $Q_3=0$.

* Like this by applying each clock pulse circuit can produce a 4-bit binary sequence.

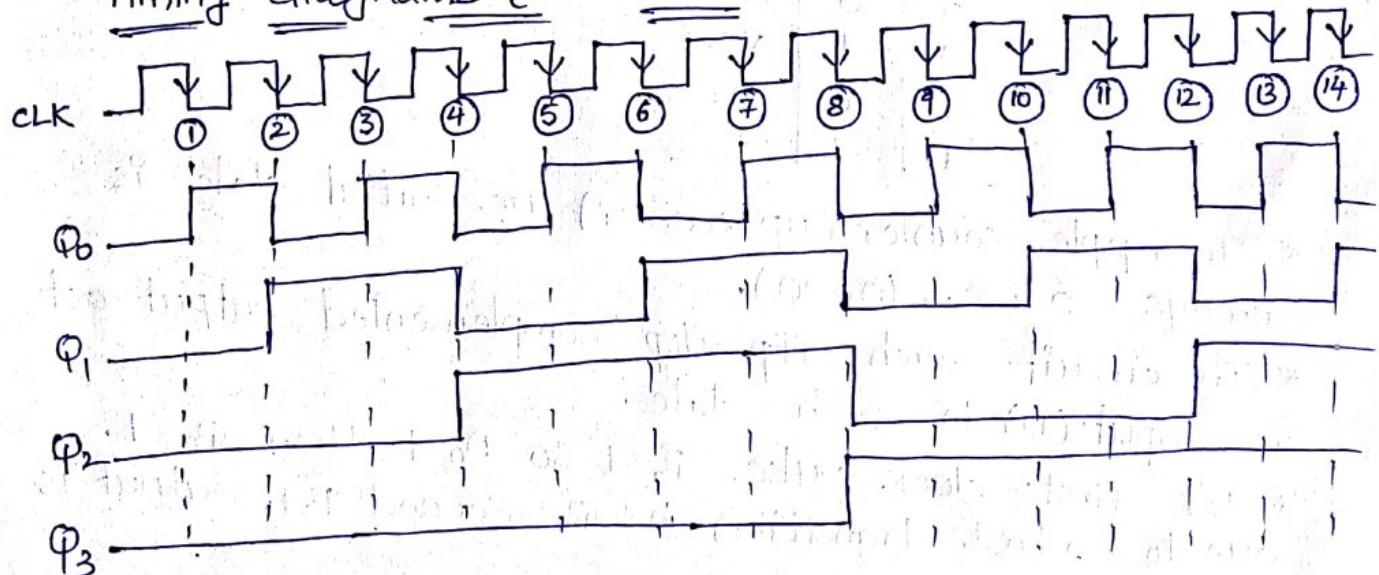
state table :-

state diagram :-

CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0



Timing diagrams (waveforms) :-



(2) Draw the circuit diagram of 4-bit ring counter using D flip flops & explain the operation with the help of bit pattern.

Ring Counter: A counter which can perform circular shift operation called ring counter.

→ To design 4-bit ring counter use 4 Delay flip flops.

→ A clock signal applied parallelly.

→ Output of one flip flop applied as input for next flip flop.

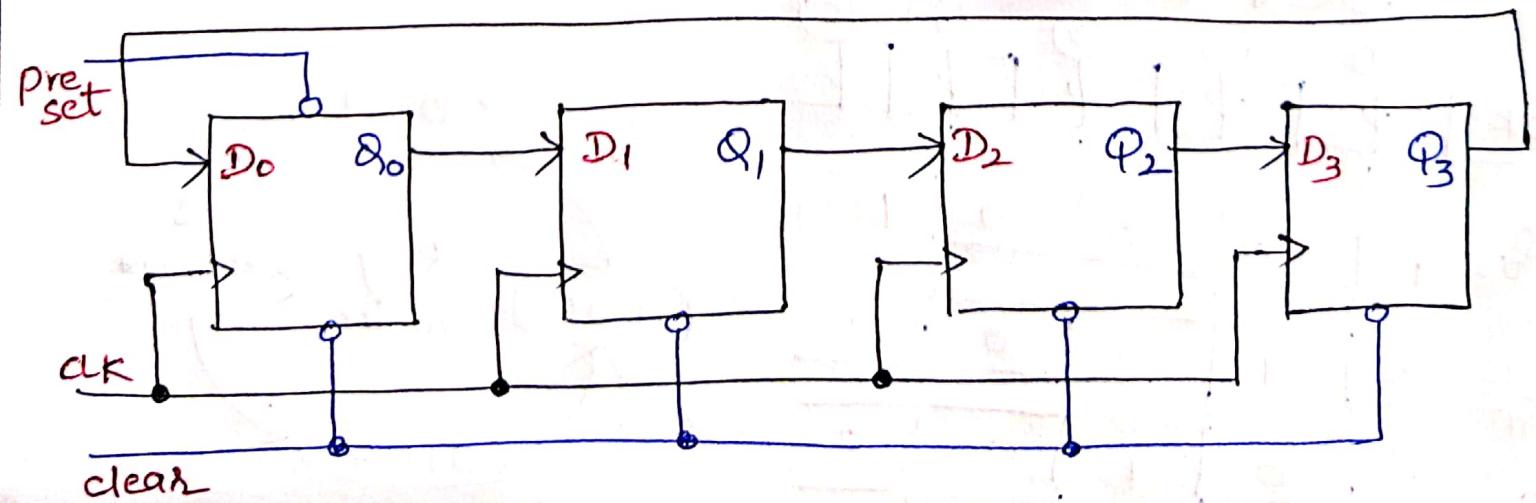
→ Last flip flop output applied as input for first flip flop.

→ i.e., it will shift the data circularly.

→ Use a clear input & preset input for first flip flop.

→ A preset followed by clear input set the first flip flop & remaining zero's.

→ 4-bit ring counter circuit diagram shown below.

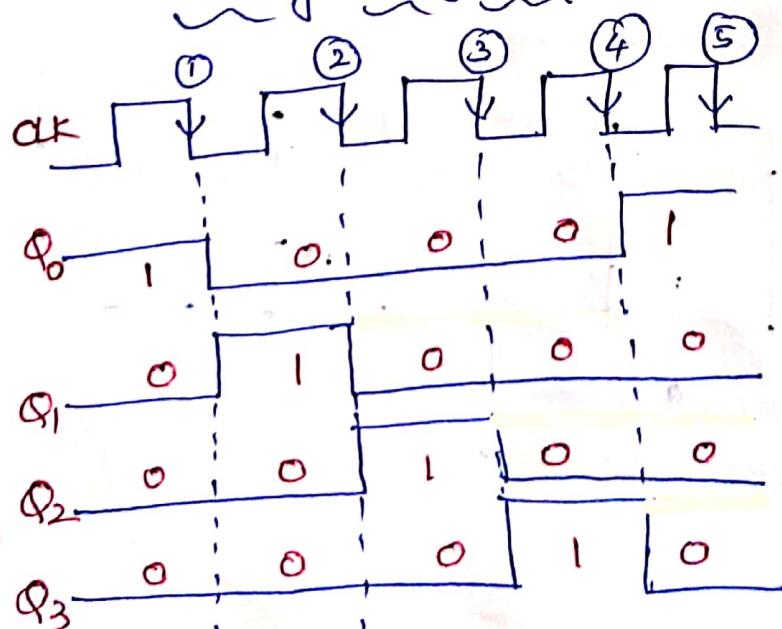


operations:-

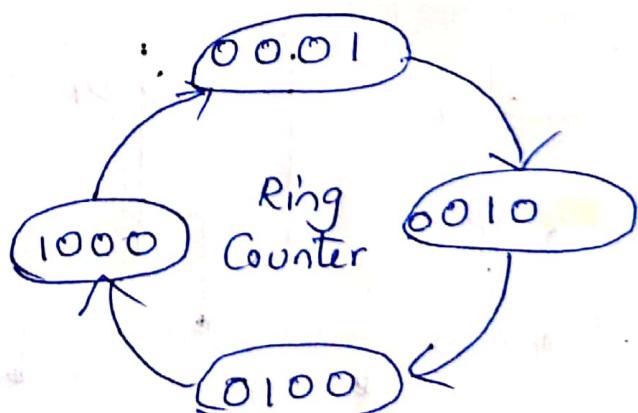
- In "D" -flip flop if we are applying proper clock signal output becomes same as input.
- Due to preset connection -for first flip flop & clear connection -for all flip flops initial state becomes $Q_3 Q_2 Q_1 Q_0 = 0001$.
- By applying every clock pulse internally data shifted towards left direction.
- 4-bit ring counter produces 4 unique states.

<u>state table</u>				
CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0
4	0	0	0	1

→ Timing diagram :-



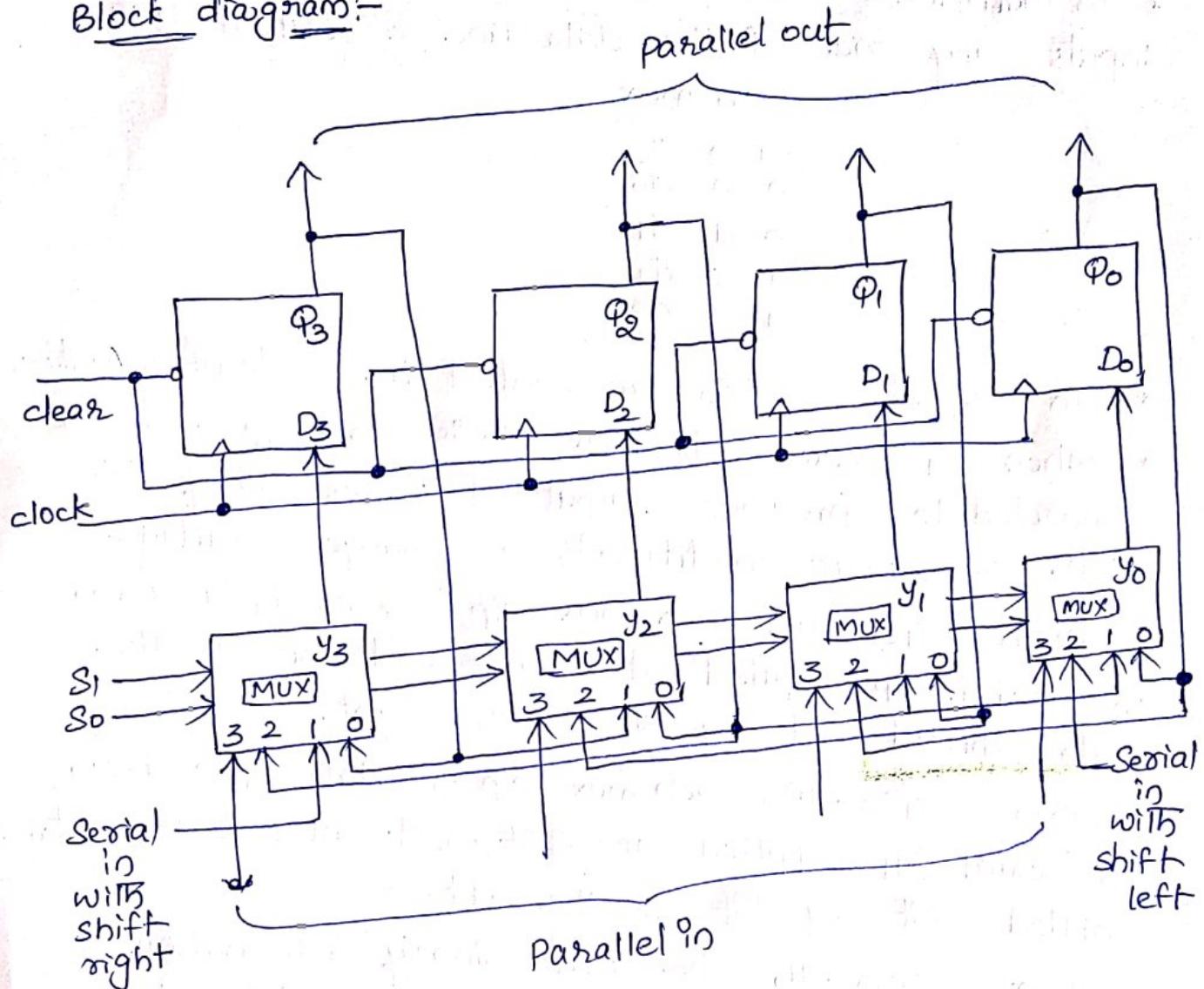
→ state diagram :-



③ Explain the operation of universal shift register.

Universal shift register:- A register which can perform bidirectional shift operations and having parallel load capability called universal shift register.

Block diagram:-



Truth table

Selection IP		operation
S_1	S_0	
0	0	No change
0	1	shift right operation with serial in
1	0	shift left with serial in
1	1	Parallel in Parallel out

Operation:-

- * It consists four D-flip-flops and four "4x1" mux.
- * The four multiplexers have two common selection inputs.
- * In multiplexer based on combination of selection inputs any one of the data line as output line.

In mux

S_1	S_0	y
0	0	d_0
0	1	d_1
1	0	d_2
1	1	d_3

- * In register $S_1 \& S_0$ can control the mode of operation.
- * When $S_1 S_0 = 00$; each mux o/p is data i/p '0' i.e., connected to previous output of corresponding flip-flop. So output condition is no change condition.
- * When $S_1 S_0 = 01$, each mux o/p is data i/p '1' i.e., the serial i/p applied at left most mux & the data shifted bit by bit to the right.
- * When $S_1 S_0 = 10$, each mux o/p is data i/p '2' i.e., the serial i/p applied at right most mux & the data shifted bit by bit to the left.
- * When $S_1 S_0 = 11$, the 4-bit binary information on the parallel input lines is transferred into the register and produce parallel output $[Q_3 Q_2 Q_1 Q_0]$ data-

(4) Design a mod-6 synchronous counter using JK flip-flops? With state table & k-map simplification.

↳ Mod-6 counter can produce total 6 states they are from 0 to 5.

↳ To design this require 3 flip flops.

↳ Each flip flop output assuming as Q_0, Q_1, Q_2

↳ State table of mod-6 counter

↳ Let present states are Q_0, Q_1, Q_2

Next states are $Q_0(t+1), Q_1(t+1), Q_2(t+1)$.

Present states			Next states			flip flop i/p's					
Q_2	Q_1	Q_0	Q_2 $(t+1)$	Q_1 $(t+1)$	Q_0 $(t+1)$	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	1
2	0	1	0	0	1	1	0	X	X	0	1
3	0	1	1	1	0	0	1	X	X	1	1
4	1	0	0	1	0	1	X	0	X	0	X
5	1	0	1	0	0	0	X	1	0	X	1

↳ flip flop inputs are produced based on excitation table

PS	NS	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

↳ simplified expressions for flip flop inputs are produced using k-map.

↳ For $J_2 \Rightarrow \Sigma m(3) + \Sigma d(4, 5, 6, 7)$

Q_1	Q_0	00	01	11	10
Q_2	0	0	1	1	0
	1	X ⁴	X ⁵	X ⁷	X ⁶

$$J_2 = Q_1 Q_0$$

↳ 6, 7 are don't cares in k-map because these are not using in table.

↳ So value may be either 0 or 1

For $k_2 = Em(5) + Ed(0,1,2,3,6,7)$

		$Q_1 Q_0$				
		00	01	11	10	
Q_2	0	x	x	x	x	
	1	1	x	x	x	

$$k_2 = Q_0$$

For $J_1 = Em(1) + Ed(2,3,6,7)$

		$Q_1 Q_0$				
		00	01	11	10	
Q_2	0	0	1	x	x	
	1	4	5	x	x	

$$J_1 = Q_2' Q_0$$

For $k_1 = Em(3) + Ed(0,1,4,5,6,7)$

		$Q_1 Q_0$				
		00	01	11	10	
Q_2	0	x	x	1	x	
	1	x	x	x	x	

$$k_1 = Q_0$$

For $J_0 = Em(0,2,4) + Ed(1,3,5,6,7)$

		$Q_1 Q_0$				
		00	01	11	10	
Q_2	0	1	x	x	1	
	1	1	x	x	x	

$$J_0 = 1$$

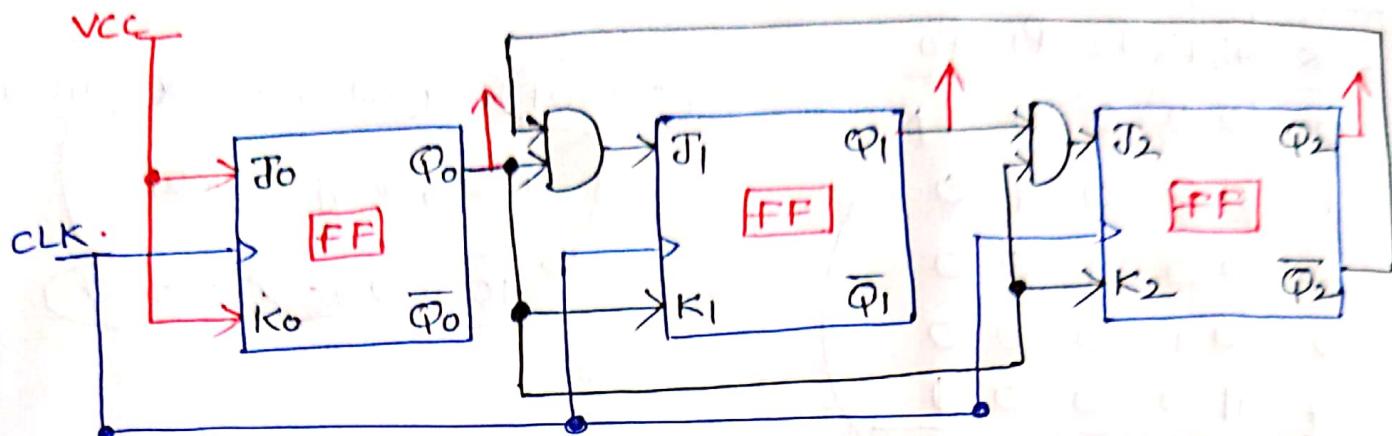
For $k_0 = Em(1,3,5) + Ed(0,2,4,6,7)$

		$Q_1 Q_0$				
		00	01	11	10	
Q_2	0	x	1	1	x	
	1	x	1	x	x	

$$k_0 = 1$$

To design mod-6 synchronous counter require
3 JK flip flops, 2 AND gates & common clock signal.

Design of mod-6 synchronous counter:

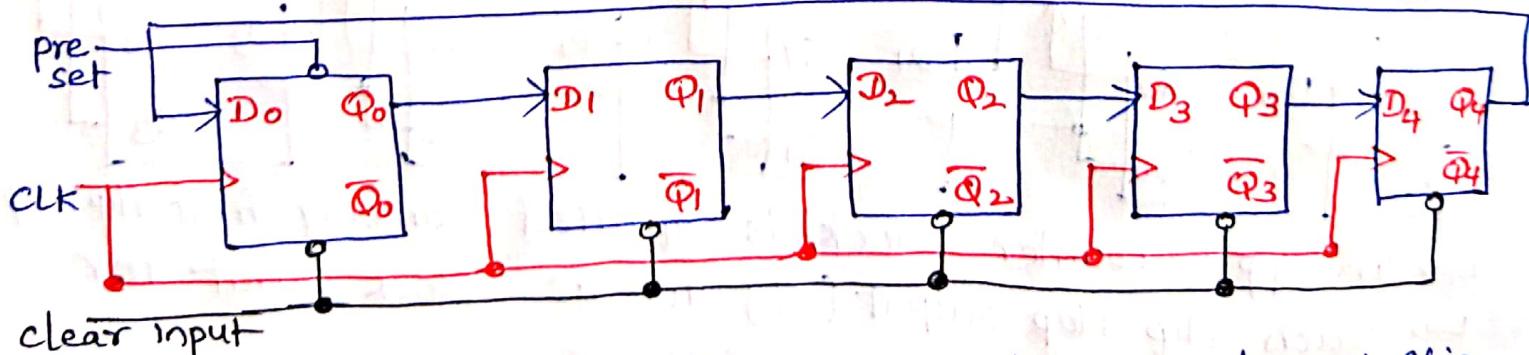


(5) (a) Design mod-5 ring counter using flip flops.

↪ A circular shift register act as ring counter.
↪ To design mod-5 ring counter require 5 flip flops.

↪ Use "D" flip flops to design.
↪ Use a common clock apply for ring counter.
↪ A common clock apply for next flip flop output as input for next flip flop, last flip flop output as first flip flop input.
↪ Use a preset input followed by clear to produce number of states in ring counter.

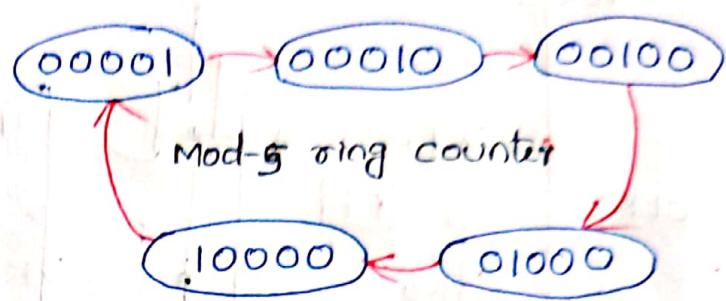
↪ Design:



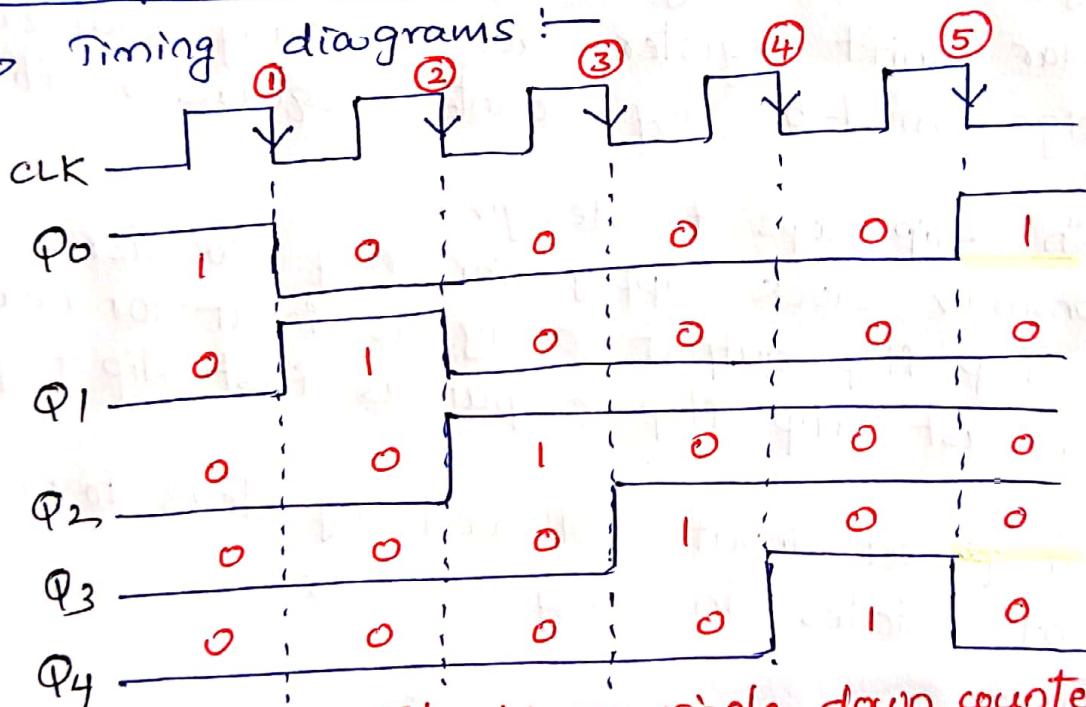
↪ By applying preset followed by clear input all flip flops are cleared except first flip flop.
↪ After each clock pulse internally shift the data bit by bit circularly [right left side)

↳ state table → ↳ state diagram!

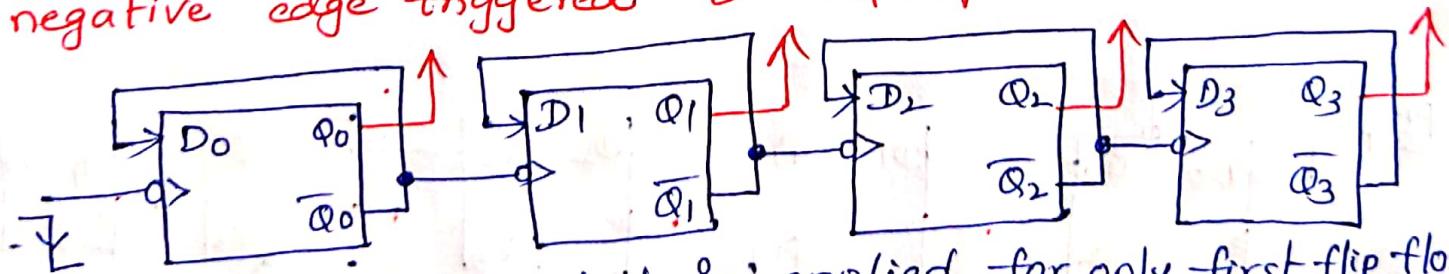
CLK	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
3	0	1	0	0	0
4	1	0	0	0	0
5	0	0	0	0	1



↳ Timing diagrams:



(b) Design a 4-bit binary ripple down counter using a negative edge triggered D flip flop.



↳ In ripple counter clock is applied for only first flip flop.
↳ Each flip flop output (\bar{Q}) act as clock input for next flip flop in down counter.

↳ Here using a -ve edge triggered clock i.e., a transition from logic 1 to logic 0 can act as a proper clock.

* In D flip-flop in the presence of proper clock output is same as input (D) & in the absence of clock output is no change condition.

CLK	D	O/P
0	0	NC
0	1	NC
1	0	0
1	1	1

* In ripple down counter the initial state is always $2^n - 1$; when $n = \text{no of flip-flops in a counter}$. Here $n=4$ then count = 15 i.e., 1111.

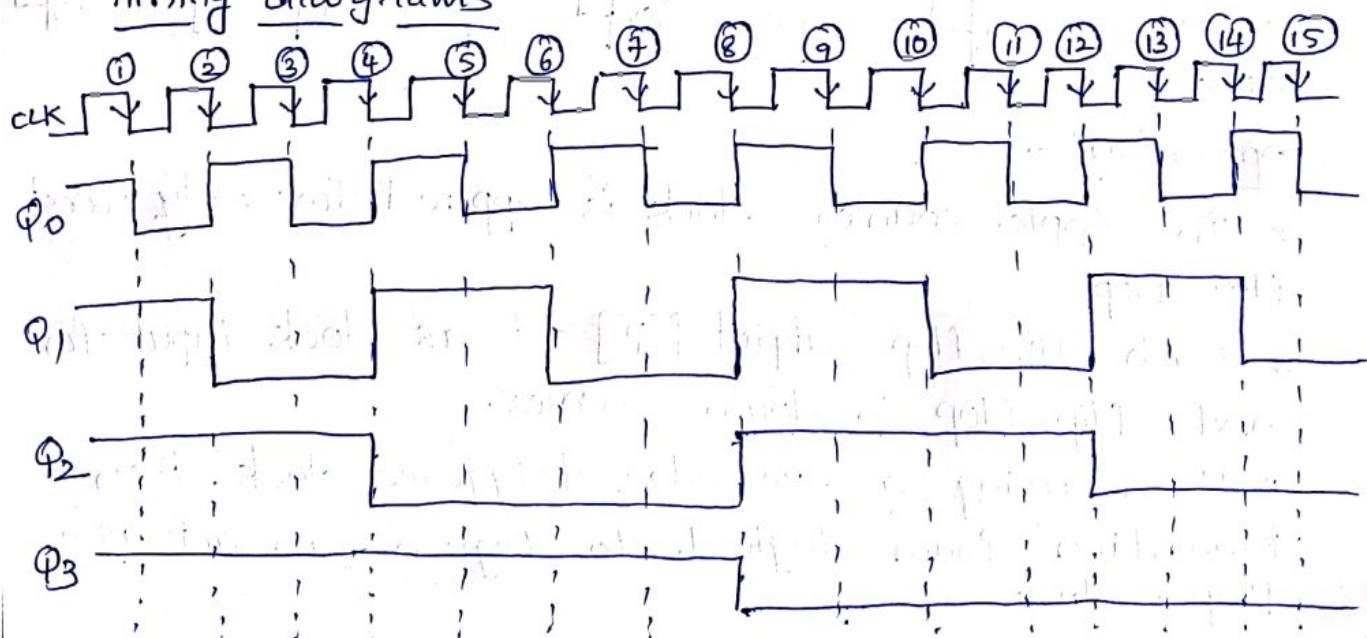
* In circuit each flip-flop complemented output act as input (D) in each state.

* In down counter by applying each clock pulse count is decremented by 1.

* For first clock pulse $\rightarrow \bar{Q}_0 = 0$ so $D_0 = 0$ then $Q_0 = 0$. due to 1 to 0 transition in Q_0 second F-F output is no change [$Q_1 = 1$]. Due to 1 to 1 transition in Q_1 output $Q_2 = 1$ & also $Q_3 = 1$.

* Like this by applying each clock pulse circuit can provide a 4-bit reverse binary sequence.

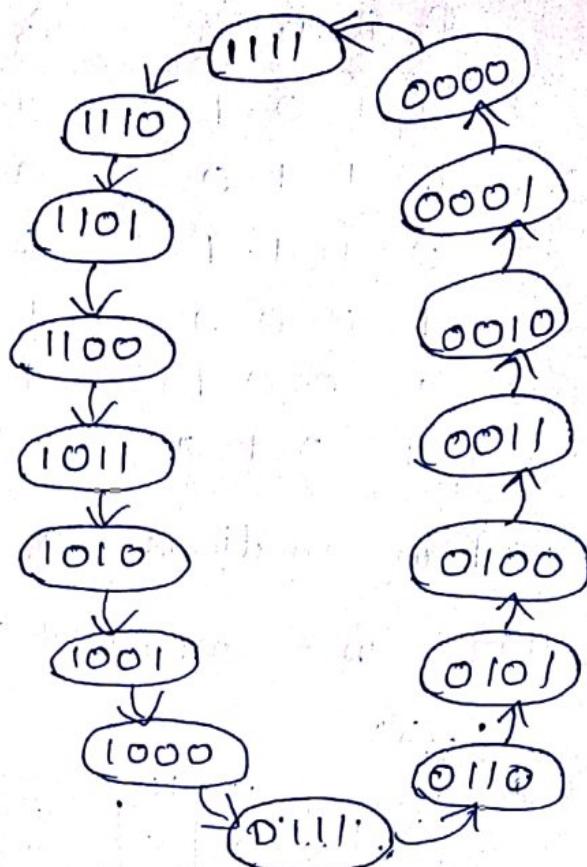
Timing diagrams



state table

CLK	Q ₃	Q ₂	Q ₁	Q ₀
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	0	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1
15	0	0	0	0
16	1	1	1	1

state diagram



⑥ @ Design a synchronous mod-6 counter with the following sequence: 5, 6, 7, 8, 9, 10, 5, ...

* Mod-6 counter can produce only 6 states.

* The sequence is 5, 6, 7, 8, 9, 10, 5, ...

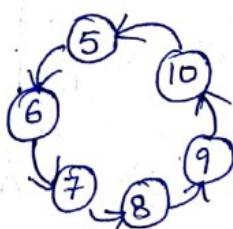
* In the sequence states are [0101, 0110, 0111, 1000, 1001, 1010].

* To design it require 4 flip-flops because of 4-bit.

* Use any type of flip-flops.

* We are using T type flip flops.

state diagram



CLK	T	O/P
1	0	NC
1	1	\bar{Q}_{n-1} (complement)

Excitation table for mod-6 counter

PS	NS	flip-flops
$Q_3\ Q_2\ Q_1\ Q_0$	$Q_3\ Q_2\ Q_1\ Q_0$	$T_D\ T_C\ T_B\ T_A$
0 1 0 1	0 1 1 0	0 0 1 1
0 1 1 0	0 1 1 1	0 0 0 1
0 1 1 1	1 0 0 0	1 1 1 1
1 0 0 0	1 0 0 1	0 0 0 1
1 0 0 1	1 0 1 0	0 0 1 1
1 0 1 0	0 1 0 1	1 1 1 1

Boolean equations for flip-flop inputs :-

$$\text{For } T_D = \sum m(7, 10) + d(0, 1, 2, 3, 4, 11, 12, 13, 14, 15)$$

$Q_3\ Q_2\ Q_1\ Q_0$	00	01	11	10
00	x	x	x	x
01	x		1	
11	x	x	x	x
10			x	1

$$T_D = \Phi_0\Phi_1 + \Phi_1\Phi_3$$

$$\text{For } T_C = \sum m(7, 10) + d(0, 1, 2, 3, 4, 11, 12, 13, 14, 15)$$

$$\therefore T_C = \Phi_0\Phi_1 + \Phi_1\Phi_3 \Rightarrow T_C = T_D$$

$$\text{For } T_B = \sum m(5, 7, 9, 10) + d(0, 1, 2, 3, 4, 11, 12, 13, 14, 15)$$

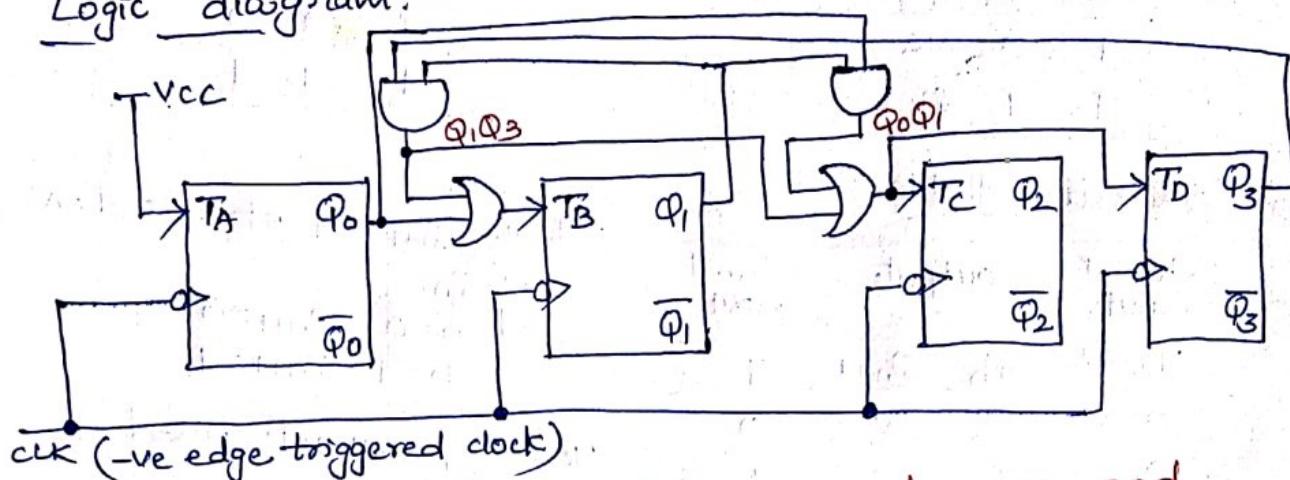
$Q_3\ Q_2\ Q_1\ Q_0$	00	01	11	10
00	x	x	x	x
01	x	1	1	
11	x	x	x	x
10	1	x	1	

$$T_B = \Phi_0 + \Phi_1\Phi_3$$

$$\text{For } T_A = \sum m(5, 6, 7, 8, 9, 10) + d(0, 1, 2, 3, 4, 11, 12, 13, 14, 15)$$

$Q_3 Q_2 Q_1 Q_0$	00 01	11 10	
00	X X	X X	$Q_3^1 \rightarrow Q_3$
01	X 1	1 1	$\Rightarrow Q_3^1 + Q_3 = 1$
11	X X	X X	$\Rightarrow T_A = 1$
10	1 1	X 1	

Logic diagram:



⑥ D Explain the difference between synchronous and asynchronous sequential circuits.

Asynchronous S.C

- * A circuit without clock input called asynchronous sequential circuit.
- * Basic elements are Latches.
- * Difficult to design.
- * Faster because no restriction to operate.
- * Low cost.
- * Use generally RS NAND / NOR latch to design asynchronous sequential circuit.

synchronous S.C

- * A circuit which can operate based on proper clock input called synchronous sequential circuit.
- * Basic elements are flip-flops.
- * Easier to design.
- * slower because of clock pulse.
- * High cost.
- * Use four types of flip-flops to design synchronous sequential circuit.
 - SR flip-flop
 - D flip-flop
 - JK flip-flop
 - T flip-flop

(7) A sequential circuit with two D flip-flops A & B, two inputs 'x' & 'y' and one output 'z' is specified by the following next state & output equation:

$$A(t+1) = x'y + xA$$

$$B(t+1) = x'B + xA$$

$$z = B$$

(i) Draw the logic diagram of the the circuit.

(ii) List the state table & draw the corresponding state diagram.

Given state equations are

$$\text{NS of first flip flop } A(t+1) = x'y + xA$$

$$\text{NS of second flip flop } B(t+1) = x'B + xA$$

$$\text{output } z = B$$

here A, B are present states

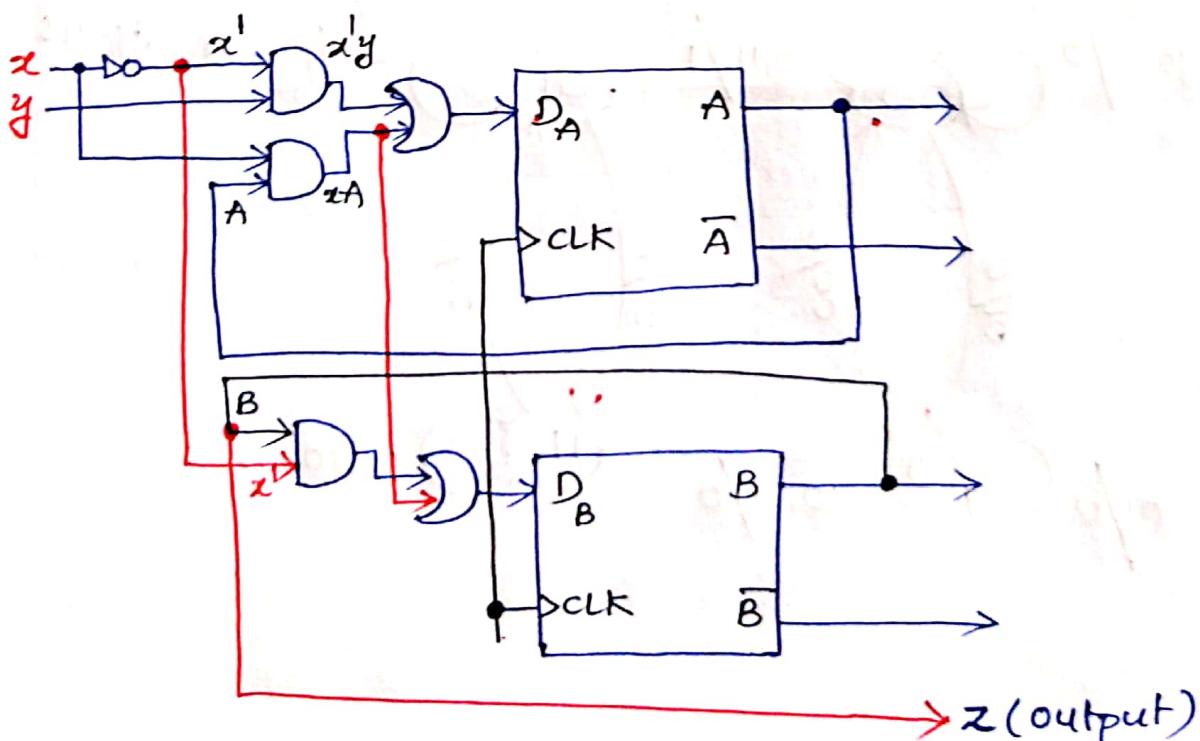
$A(t+1)$, $B(t+1)$ are next states

x & y are inputs

z is output.

(i) Logic diagram using two 'D' flip-flops.

In 'D' flip flop input D is same as next state.



(ii) state table :-

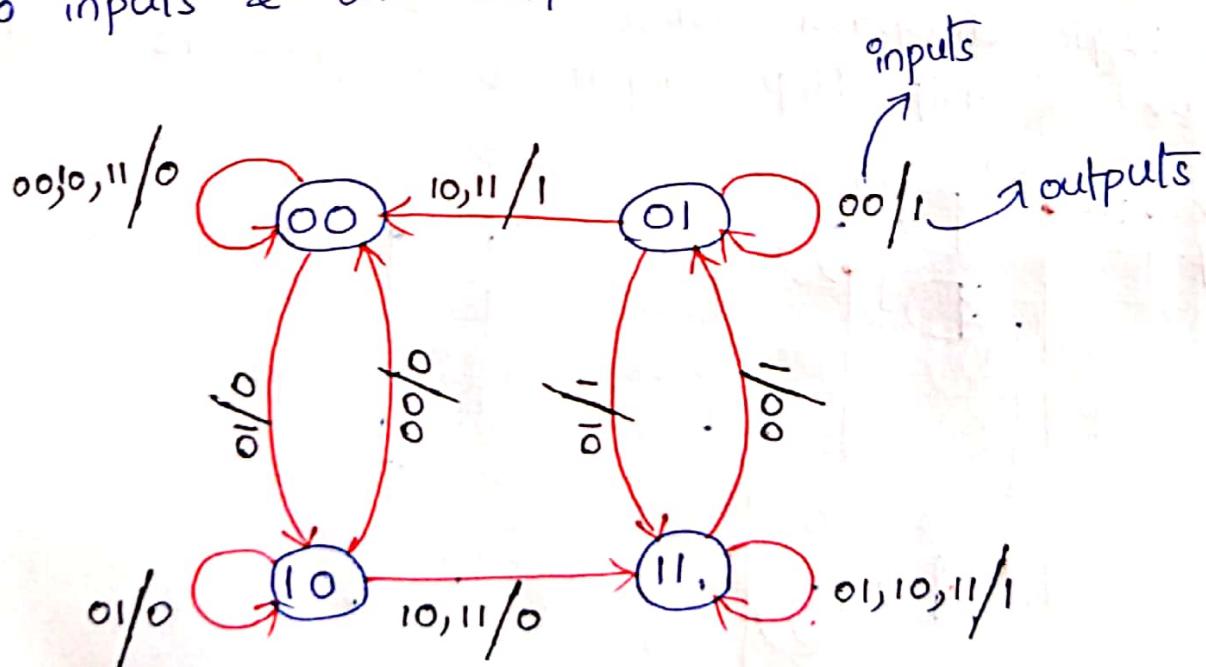
PS	I/P'S	NS	O/P			
A	B	X	Y	A(t+1)	B(t+1)	Z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

$$A(t+1) = \bar{x}y + xA$$

$$B(t+1) = \bar{x}B + xA$$

$$Z = B$$

state diagram with four states 00, 01, 10, 11; with two inputs & one output.



(B)(a) Draw the state diagram & state table of the binary serial adder & implement by using D flip-flop.

n-bit serial adder:-

- ↳ An adder which can perform addition operation bit by bit called serial adder.
- ↳ To perform n-bit addition it require only one full adder and one memory element.
- ↳ Memory element is used to store carry which is generated in previous operations.
- ↳ Use D flip-flop as memory element in serial adder.
- ↳ A combinational logic required to generate full adder circuit.

↳ Truth table for full adder is

A	B	C _{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\hookrightarrow \text{Sum} = \Sigma m(1, 2, 4, 7)$$

$$= A'B'C + A'BC' + AB'C' + ABC$$

$$= A[B \oplus C] + A[B \oplus C]' \Rightarrow A \oplus B \oplus C_{in}$$

$$\hookrightarrow \text{carry} = \Sigma m(3, 5, 6, 7)$$

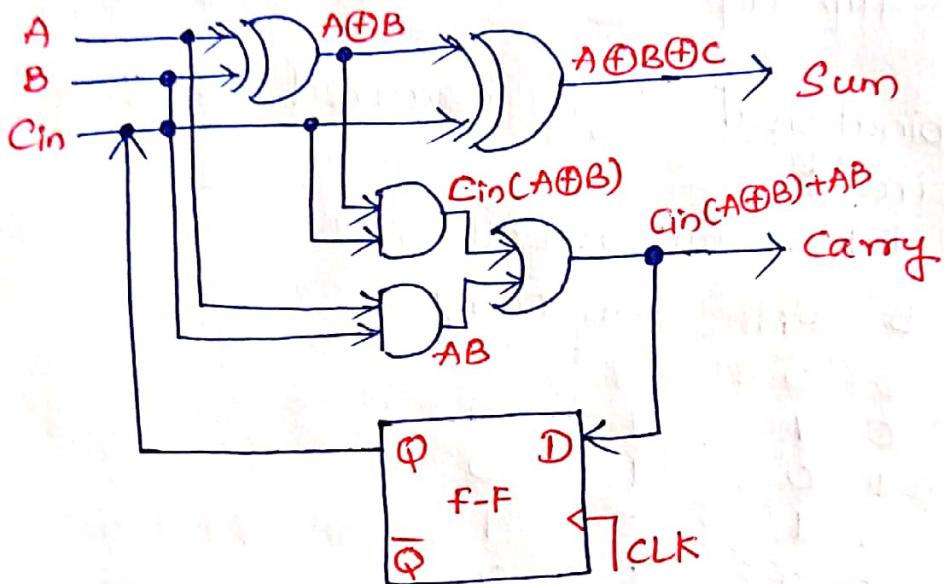
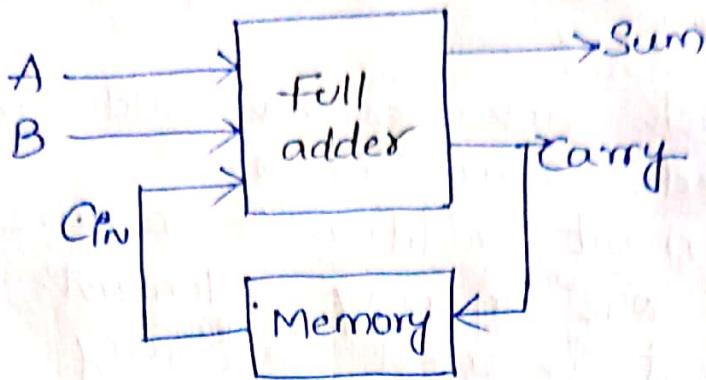
$$= A'BC + AB'C + ABC' + ABC$$

$$= C[A \oplus B] + AB[C \oplus C']$$

$$= C_{in}(A \oplus B) + AB$$

\hookrightarrow For full adder, require 2 EX-OR gates
2 AND gates
1 OR gate.

↳ Logic diagram of serial adder:-



(B)(b) Explain state reduction & state assignment with example?

State reduction:- A process of reducing number of states in a state table called state reduction process.
↳ By reducing number of states, required number of flip flops reduces & cost of the circuit reduces.

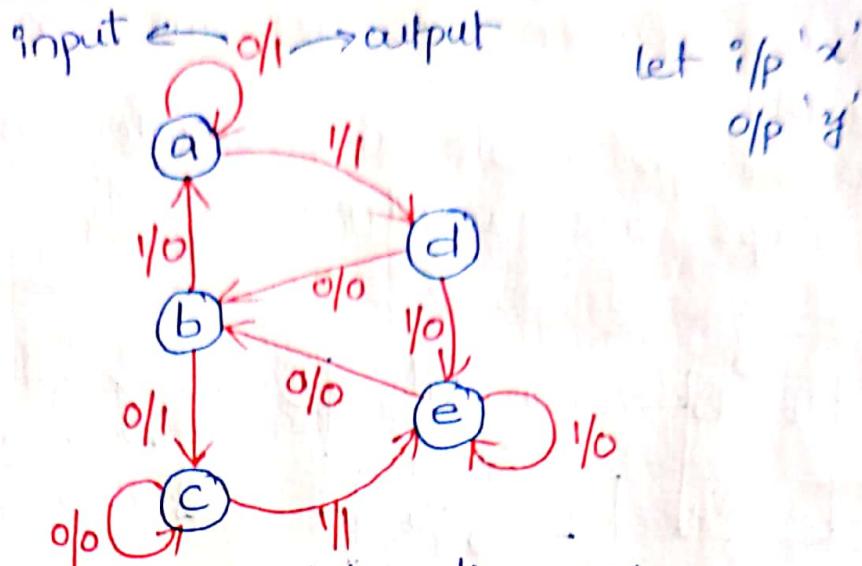
State Assignment:- A process of assigning binary values to number of states in a state table called state assignment process.

↳ Number of bits in each state based on condition

$$2^n \geq m$$

$n \rightarrow$ no of bits
 $m \rightarrow$ no of states

Example:- consider the state diagram



↳ Draw state table from state diagram.

PS	NS		O/P(y)	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	d	1	1
b	c	a	1	0
c	c	e	0	1
d	b	e	0	0
e	b	e	0	0

$d=e$

PS	NS		O/P(y)	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	d	1	1
b	c	a	1	0
c	c	d	0	1
d	b	d	0	0

↳ States d & e are equal because two states having same next states as well as outputs.

↳ Reduced state table has only 4 states.

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↳ Assign binary values for these 4 states.

$$\Rightarrow 2^n \geq m ; m=4$$

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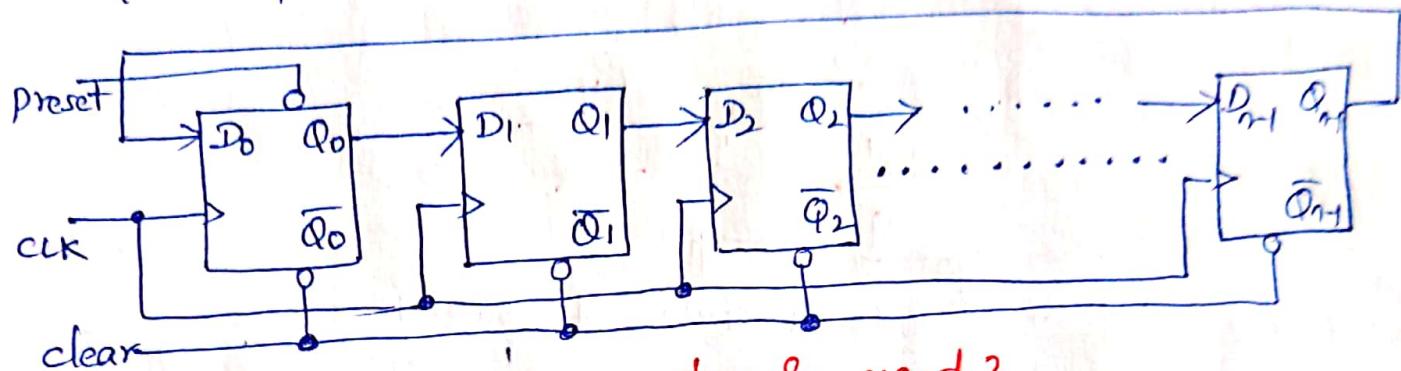
$\Rightarrow n=2$ use two binary bits in each state.

↳ Assign $00 \rightarrow a$
 $01 \rightarrow b$
 $10 \rightarrow c$
 $11 \rightarrow d$

↳ Then state table becomes

PS	NS		O/P	
	$x=0$	$x=1$	$x=0$	$x=1$
00	00	11	1	1
01	10	00	1	0
10	10	11	0	1
11	01	11	0	0

- (9) Draw the circuit of ring counter?
- A ring counter can perform circular shift operation internally.
 - To design n-bit ring counter "n" number of "D" flip flops are required.



- (10) Where the ripple counter is used?

- In frequency dividers
- In time measuring instruments
- In square wave generators
- In frequency measuring instruments

- (11) What is present state?

- The output of a flip flop is called as the state.
- The output of the flip flop before the clock pulse is applied called as present state.

- (12) What is next state?

- The output of the flip flop after the clock pulse is applied called as next state.

- (13) What is shift register?

- A device which can store more than one bit binary information temporarily called a register.
- A register not only can store the data & also shift the data bit by bit internally called shift registers.

- (14) What is state table?

- It is a truth table, which projects the relationship between present state & next state with respect to input & output variables.

(15) List the applications of shift registers?

- (1) Serial to parallel converters
- (2) Parallel to serial converters
- (3) To design ring & Johnson counters
- (4) In Time delay devices
- (5) Data storage devices.

(16) What is the difference between synchronous & Asynchronous counters?

Asynchronous counters

- ↳ Clock input is applied for only first flip flop.
- ↳ Also called ripple counter
- ↳ Output of each flip flop act as clock input for next flip flop.
- ↳ Slower than synchronous type counters.
- ↳ Less complexity at the time of design.
- ↳ Low cost.

Synchronous counters

- ↳ A common clock input is applied for each flip flop.
- ↳ Also called parallel counter.
- ↳ Output of each flip flop act as JK input for next flip flop.
- ↳ Faster than asynchronous type counters.
- ↳ High complexity at the time of design.
- ↳ High cost.

(17) What are the drawbacks of ripple counter?

- Ripple counters are slower because after producing output of one flip flop, next one will produce.
- Have to use only -ve edge triggered flip flop to produce number of states.

(18) Define synchronous & asynchronous sequential circuits?

Synchronous sequential circuit:

A sequential circuit, which can controlled by a clock signal called synchronous sequential circuit.

→ Use gated flip-flops to design it.

Asynchronous sequential circuit:-

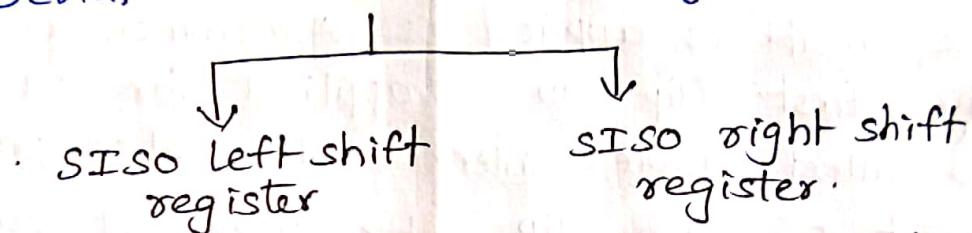
A sequential circuit, which can not be controlled by a clock signal called asynchronous sequential circuit.

→ Use latches to design it.

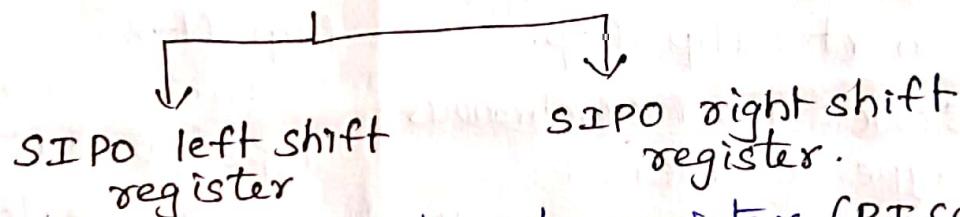
(19) List the types of shift registers.

→ Based on the data transfer & type of shift operation shift registers are classified into 4 types.

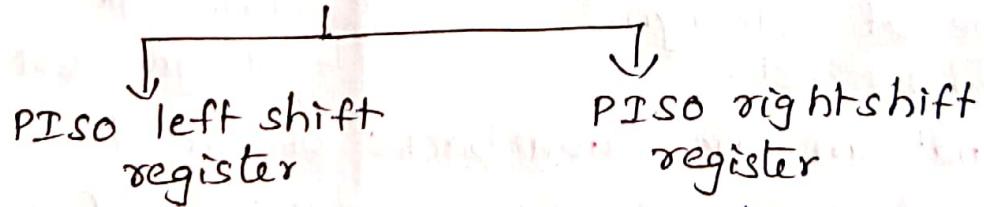
(1) Serial In Serial out register (SISO)



(2) Serial In Parallel out register (SIPO)



(3) Parallel In Serial out register (PISO)



(4) Parallel In Parallel out register (PIPO)

(20) What is the use of state reduction concept.

→ The process of reducing number of states in a state table called state reduction concept.

→ Uses:-
 (1) Number of flip-flops reduced in a circuit
 (2) Complexity of the circuit reduces
 (3) Cost of the circuit reduces

(21) List the elements of design style.

→ To design a digital circuit using software simulation use three elements.

- (1) Data flow style
- (2) Behavioural style
- (3) Structural style

(22) what is state assignment.

- A process of assigning binary values to the states in a state table called state assignment.
- Use the following condition to assign binary values

$$2^n \geq m$$

here n = no of bits in a binary value

m = no of states in a state table

(23) what is the difference between up & down counters?

Up Counter

- After each clock pulse, count value incremented by one.
- Initial count must be zero.
- Maximum count value is $2^n - 1$.
- In up counter use normal outputs of flip flops as clock input.

Down Counter

- After each clock pulse, count value decremented by one.
- Initial count is based on $2^n - 1$ value.
- It will reach zero.
- In down counter use complimented outputs of flip flops as clock input.

(24) List the advantages of having equivalent states.

If we have equivalent states in state table

- will reduce number of states
- will reduce number of flip flops
- will reduce complexity to design
- will reduce cost of the circuit.

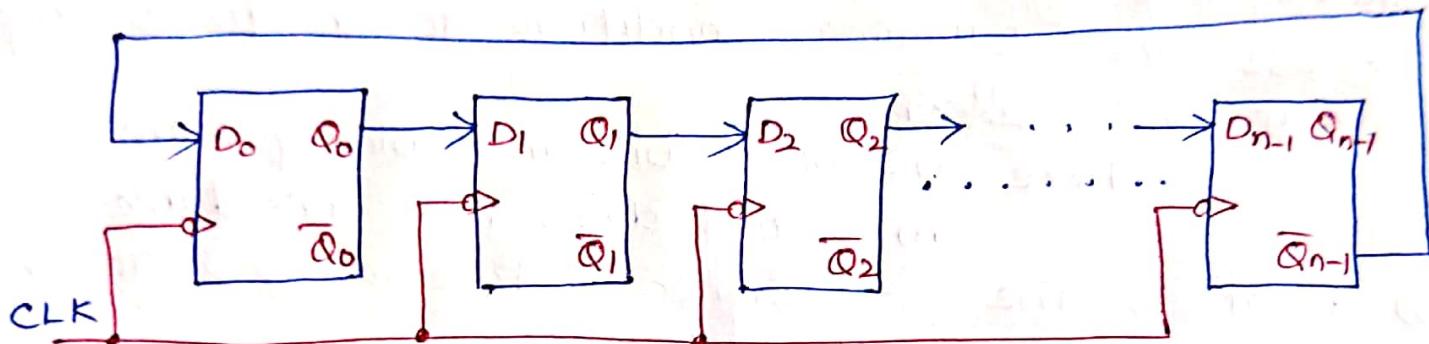
(25) What is the use of bidirectional shift register.

- A bidirectional shift register can shift the data bit by bit either in left or right operations.

→ So, we can use a single circuit to perform either left shift or right shift operations.

(26) Draw the circuit of Johnson counter.

→ To design n -bit Johnson counter use " n " number of "D" flip-flops.



(27) Define race free state assignment.

→ After state reduction, have to assign binary values to states.

→ Assigning binary values to states without race condition called race free state assignment.

→ i.e., only one bit changes at any given time when a state transition occurs in the state table. i.e., 4 states we have

$$\begin{array}{l} a = 00 \\ b = 01 \\ c = 11 \\ d = 10 \end{array} \quad \left. \begin{array}{l} \text{one bit changes occurred.} \end{array} \right\}$$

(28) What is the use of ASM chart.

Algorithmic State Machine — ASM charts are similar to flow charts

Uses:

- (1) To represent the flow of tasks to be performed in sequential circuits.
- (2) Easier to understand.
- (3) For large sequential circuits use ASM chart instead of state diagram.