

DIGITAL LOGIC FAMILIES

Introduction :-

→ Logic gates and memory devices are fabricated as Integrated Circuits (ICs) because the components used such as resistors, diodes, bipolar junction transistor and the insulated gate (IGFET) metal-oxide-semiconductor (MOS) transistors are the integral parts of the chip.

The various components are interconnected within the chip to form an electronic circuit during assembly. The ICs result in an increase in reliability and a reduction in weight and size.

Based on the IC fabrication technology, logic families are classified into two types

1. unipolar logic families.

2. Bipolar logic families

UNIPOLAR LOGIC FAMILIES

→ In unipolar logic families, unipolar device are the key element. MOSFET [metal oxide Semiconductor field effect transistor] is a only one type of charge carriers (i.e., either electrons (or) holes).

→ The examples of unipolar logic family include PMOS, NMOS, And CMOS.

BIPOLAR LOGIC FAMILIES :-

- The important elements of a bipolar ICs are Resistors, transistors, and diodes (Varactor diodes used as capacitor)
- Based on the two main operations of bipolar ICs, i.e., Saturated and non-Saturated bipolar logic families are classified into two types

1. Saturated logic and

2. Non Saturated logic

→ The following are the saturated bipolar logic families

1. Resistor-Transistor logic (RTL)

2. Direct-Coupled Transistor logic (DCTL)

3. Diode-Transistor Logic (DTL)

4. High Threshold Logic (HTL)

5. Transistor-Transistor logic (TTL)

6. Integrated Injection logic (I²L)

→ The following are the non-Saturated logic families

1. Schottky TTL

2. Emitter-Coupled logic (ECL)

4. TRANSISTOR-TRANSISTOR LOGIC :- (TTL)

→ The most commonly used saturating logic family

called the Transistor-Transistor logic (TTL or I²L) has the fastest switching speed which is comparable to other logic families that utilize saturated transistors.

→ The Series 54/74 TTL family has grown and evolved into four major divisions :

- i) standard ($SN5474$)
- ii) high-speed ($SN54H74H$)
- iii) low-power ($SN54L74L$)
- iv) Schottky-diode clamped ($SN54S74S$)
- v) low-power schottky ($SN54LS74LS$)

→ Although the high-speed and low-power series were designed for specific applications, all four families are compatible and are capable of interfacing directly with one another.

→ They have the following typical characteristics in common:

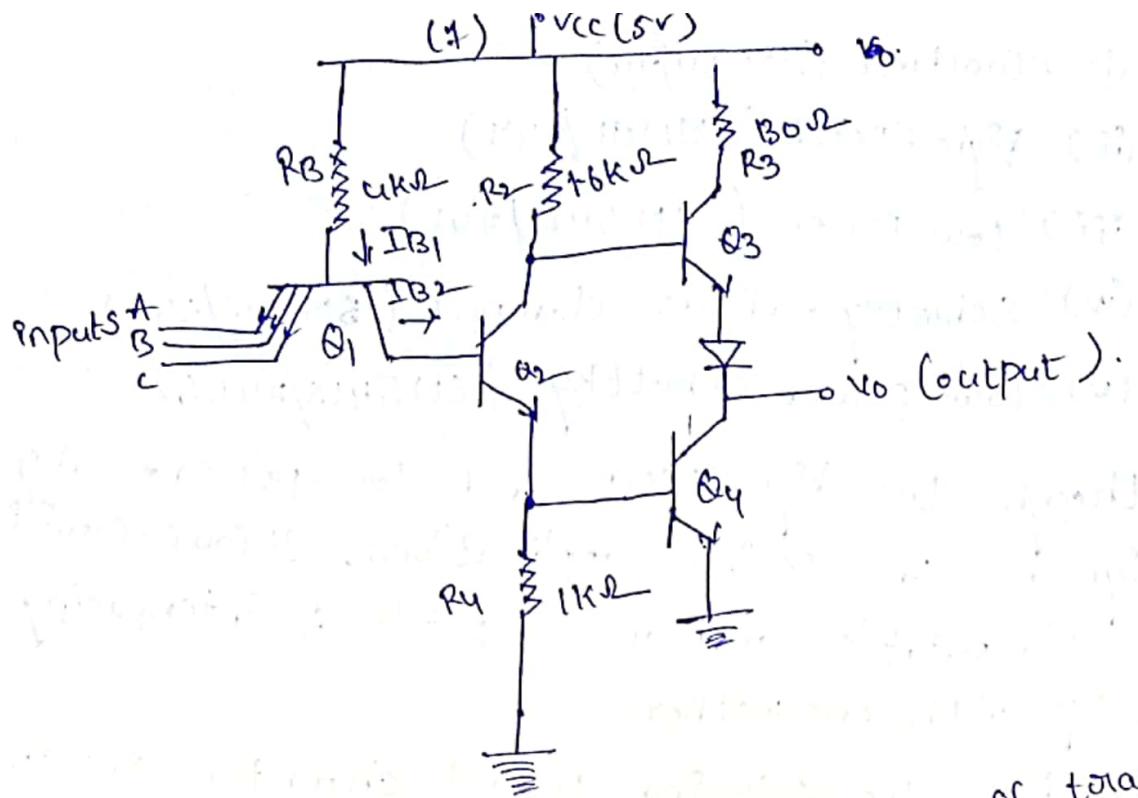
1. Supply voltage : $0.5\text{--}5.0\text{V}$
2. Logical o/p voltage : 0V to 0.4V
3. Logical o/p " : $2.4\text{--}5\text{V}$
4. Logical i/p " : 0V to 0.8V
5. Logical i/p " : $2.4\text{--}5\text{V}$ (input)
6. Noise immunity : 0.4V .

Operation of TTL :-

→ Transistor-Transistor logic will be operated by NAND gate.

→ The basic circuit of the TTL NAND gate is shown in below figure.

→ The TTL circuit uses a special single multi-emitter transistor that is fabricated with several emitters at its i/p.



- The o/p is taken from the collector of transistor Q_4 .
- Each Emitter of Q_1 act as a diode. Hence the overall ckt act like a 3-input NAND gate.
- When either (or) all inputs (A, B and C) are at $0V$ (logic 0) the corresponding emitter-base junction of Q_1 becomes forward biased. The value of R_B 's of Q_1 is selected so as to ensure that Q_1 is turned ON. The value I_{B2} flowing through the base of " Q_2 " reduces the potential at the base of Q_2 and hence transistors Q_2 and Q_4 are off so that the o/p voltage is at V_{CC} . (logic 1)
- When if all the ips are high (logic 1), the emitter base junction of Q_1 is reverse-biased so that it has no base current. Hence Q_1 is OFF.

- However its collector-base junction is forward biased supplying current I_{B2} to Q_2 . The current I_{B2} will be sufficiently large to activate saturate "Q₂" and hence Q₃ and Q₄ transistors are "ON".
- hence the o/p of the collector is low (logic 0).

OPEN COLLECTOR OUTPUT :-

- The open - collector TTL gate needs an external resistor that must be connected b/w the collector of a pull-down transistor and the supply voltage for proper operation.
- The TTL NAND gate with open-collector o/p is obtained by removing the following components : transistor Q₃, diode D₁ and resistor R₃ of fig. TTL NAND.
- The resulting open collector TTL NAND gate is shown in below figure

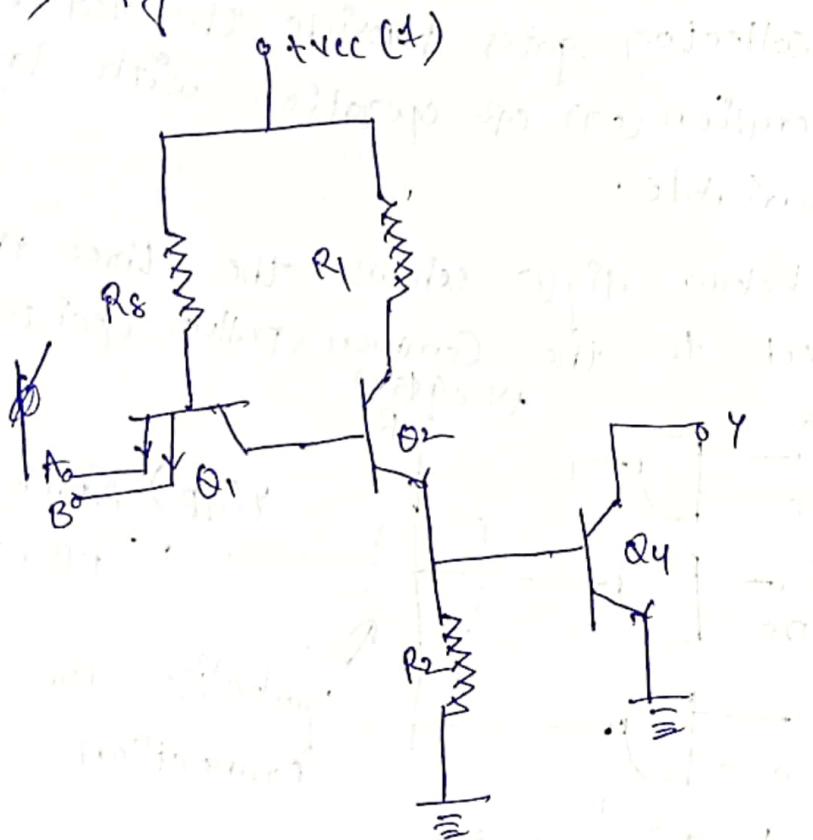
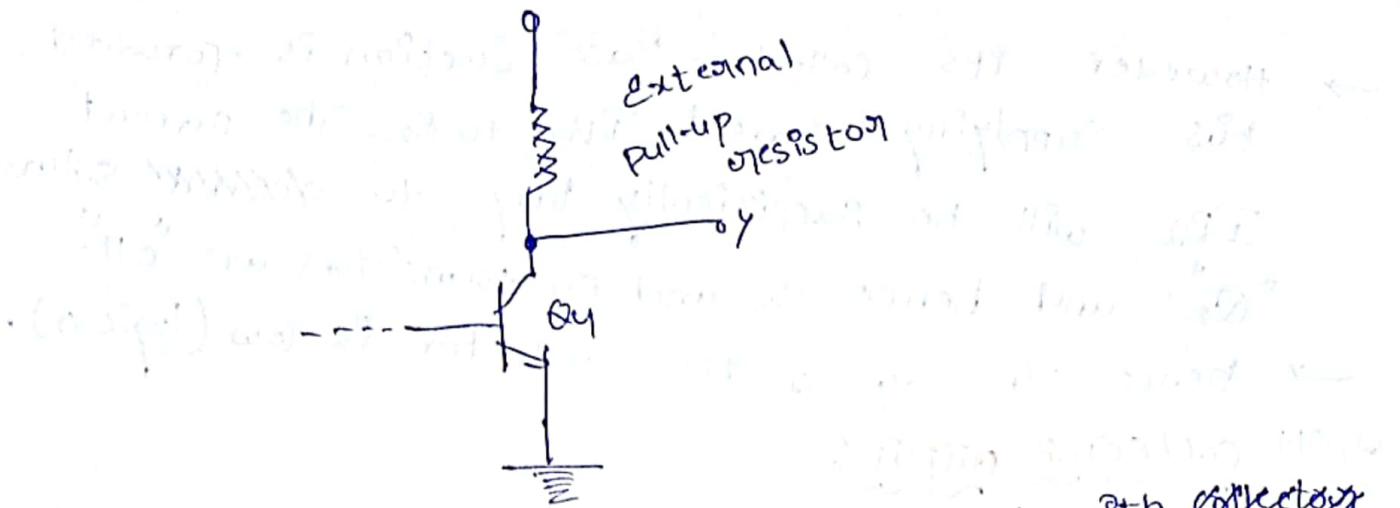


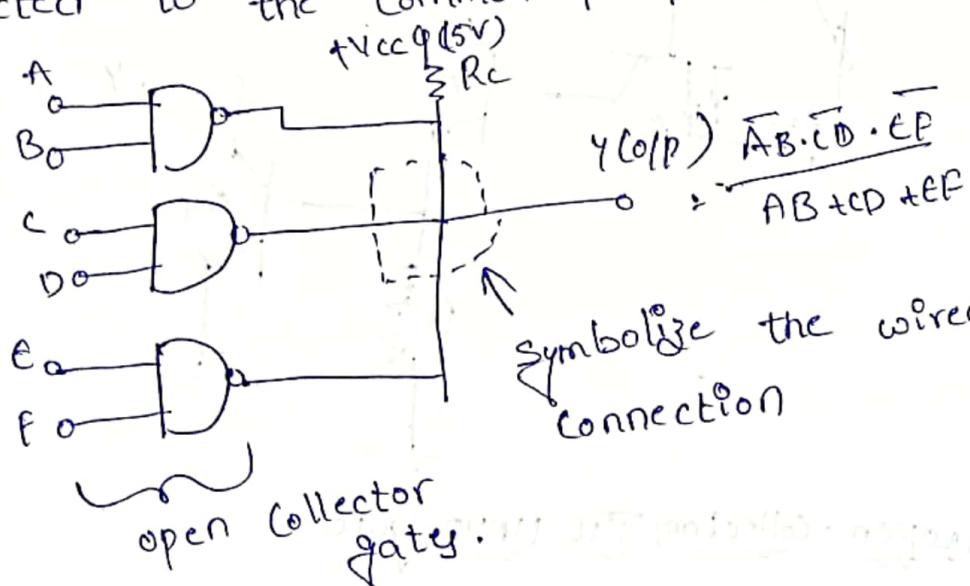
fig: open - collector TTL NAND gate



fig(b) :- open collector o/p with collector
external pull-up resistor

- As the collector of Q_1 is open, this open collector gate will not work properly unless an external pull-up resistor is connected to it as shown in fig(b).
- The o/p is taken at the collector of transistor Q_1 . A high voltage level will appear at the o/p in the HIGH state.
- Open-collector gates provide the versatility of wire AND-operation (or) OR-operation with large no. of logic variable.

→ The below fig(c) shows the three devices connected to the common pullup resistor.



symbolize the wired AND connection

- This has the advantage of combining the o/p of the three devices without using final OR gate (or AND gate).
- This is very useful when many devices are wired-ORed together.
- The main disadvantage of the open collector gate is that switching time delay is increased because the pull-up resistance is few k Ω , which results in a relatively long-time constant when its compmultipli-
cd by the stray o/p capacitance.
- The slow switching speed of the TTL devices become worse when the o/p goes from low to high.
- The o/p charge produces relatively slow exponential rise b/w the low and high state.
- Also the circuit is more sensitive to noise at the o/p.

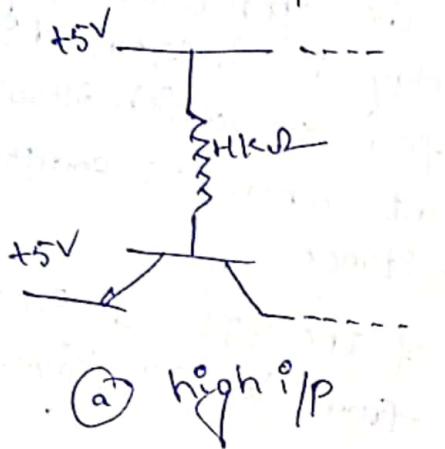
Current Source and Current Sink logic :-

- When the output of a gate is "HIGH", thereby providing current to the input of the gate being driven, the output is said to act as current source.
- For a TTL circuit, the maximum current drawn by an i/p from high o/p is 10mA.
- When o/p of a TTL gate goes Low, it must be capable of sinking current drawn from gate o/p's which are driven low. The driver then operates as current sink.

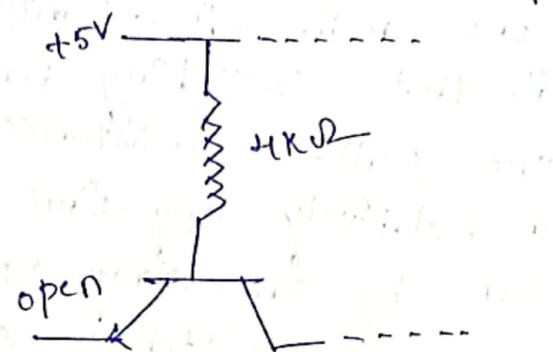
→ When one of its input is low, a current of 1.6mA flows out of the device. Thus

$$I_{IL(\max)} = -1.6\text{mA} \quad \text{and} \quad I_{IH(\max)} = 1.6\text{mA}$$

→ Here, the +ve sign indicates that the current flows out of the device. Refers to below figure



(a) high i/p



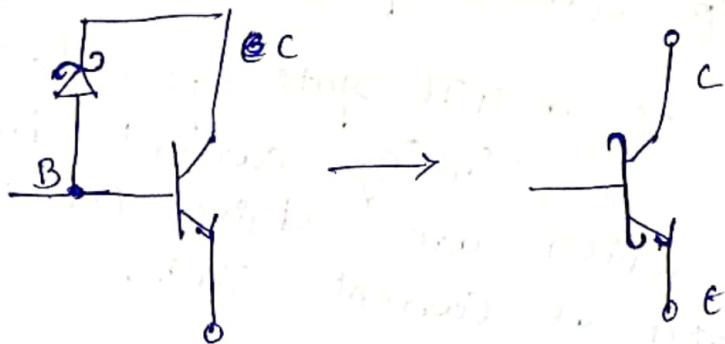
(b) floating TTL i/p
equivalent high i/p.

SCHOTTKY TTL :-

→ In standard TTL circuit the propagation time is more. This increase the time delay is mainly due to the increased the turned off time.

→ To overcome this difficulty schottky transistors are used instead of conventional transistors.

→ A schottky transistor is nothing but a conventional bipolar transistor with a schottky diode connected between its base and collector terminals.



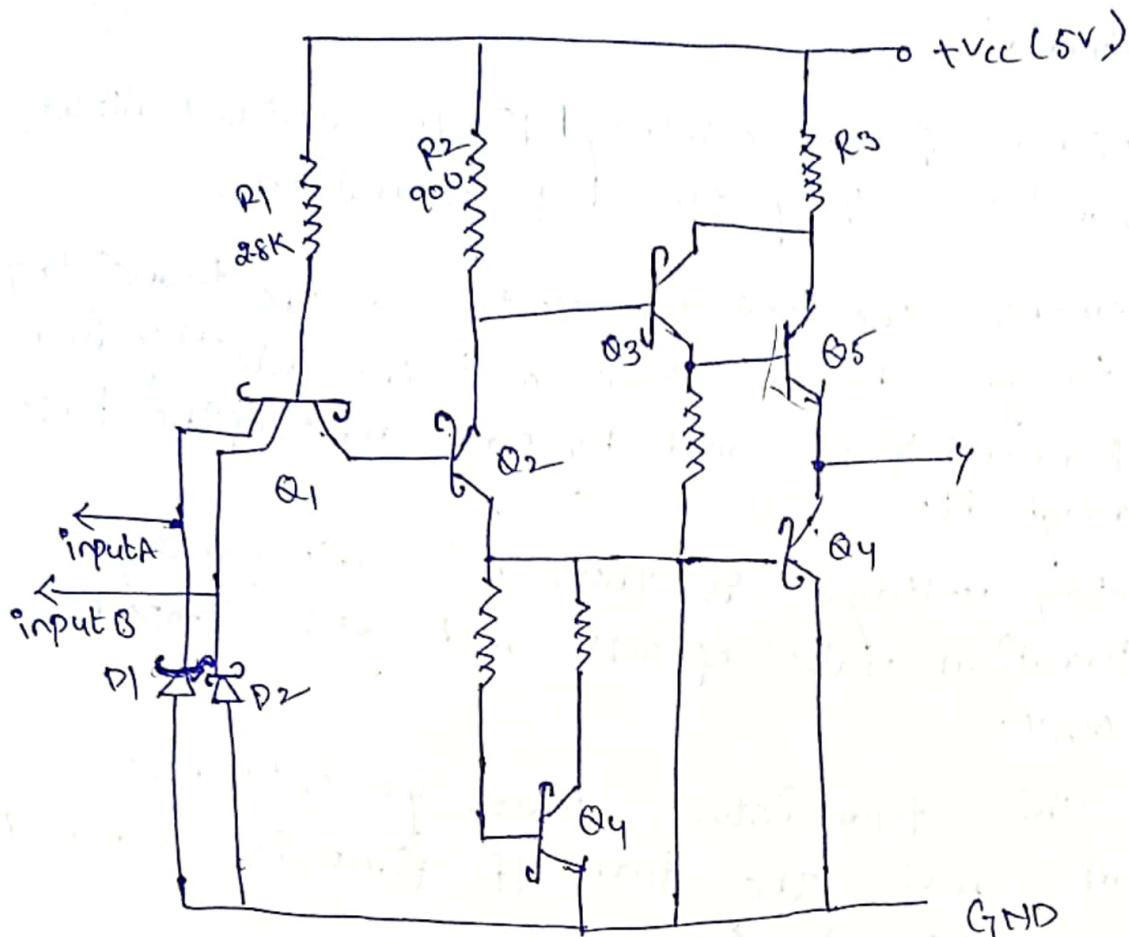
- The schottky diode with its metal-semiconductor junction not only is faster but also offers a lower forward voltage drop of $0.4V$ as against $0.7V$ for p-n junction diode for the same value of forward current.
- The presence of a schottky diode does not allow the transistor to go to deep saturation.
- The moment the collector voltage of the transistor tends to go below about $0.3V$ the schottky diode become forward bias and bypass part of the base current through it.
- The collector voltage is thus not allowed to go to the saturation value of $0.7V$ and gets clamped around $0.3V$.
- Due to this transistor do not go into the saturation and the turn off time is decreased.

Schottky TTL NAND gate :-

- Here Diodes D₁ and D₂ are clamping diodes which protects inputs A and B from taking any negative voltage.
- When A or B or both inputs are at level 0, base-emitter junction of Q₁ becomes forward biased.
- Due to this no current passes through base of Q₂ so it remains off and since base of Q₂ and Q₃ are connected with Q₂ they also remains

OFF.

- At the same time sufficient current is provided to base of Q_3 so it becomes ON and also switching ON Q_5 , so a closed switch is provided and the o/p $Y=1$.



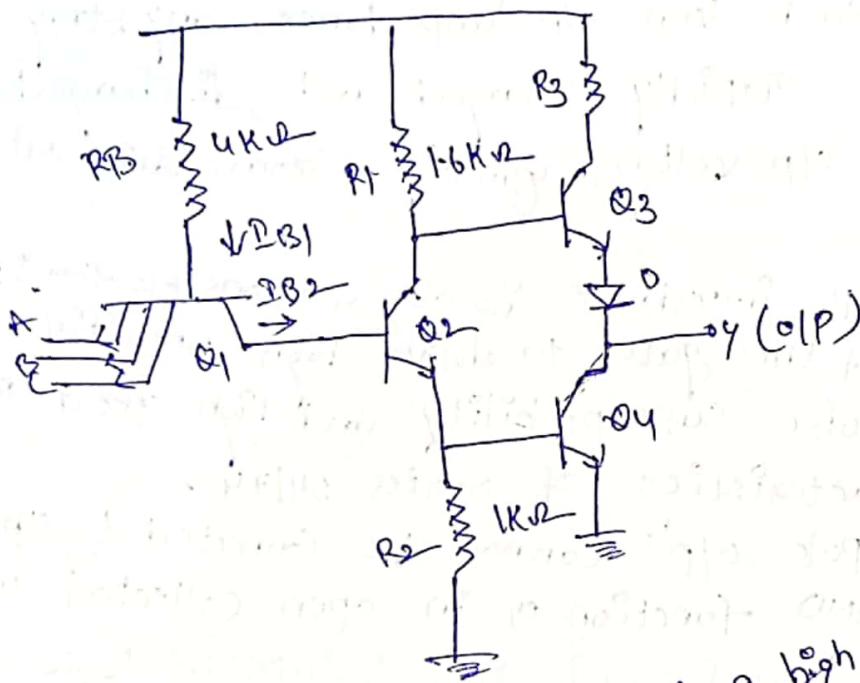
- Now when both the inputs are logic 1 the base Emitter function of Q_1 becomes reverse biased and current passes through base of Q_2 , so it becomes ON and also it makes transistor Q_3 and Q_4 ON.
- Due to this Q_3 does not get sufficient voltage so no current passes through its base hence it remains OFF and also makes Q_5 OFF.

$$t = \tau_C \quad (6)$$

TTL with active pull up :-

→ The circuit of TTL NAND gate is shown in below figure shows it work

→ The totem pole o/p is the standard o/p of a TTL gate and is specifically designed to reduce the propagation delay in the circuit and to provide sufficient o/p power for high-fan-out.



- The o/p of the circuit is a high voltage level when Q3 is ON (or) a low voltage level when Q4 is ON.
- The circuit designed in such a way that both Q3 and Q4 can never be ON at the same time. When either Q4 (or) Q3 conducts, the o/p impedance is low and hence the totem pole o/p of standard TTL circuit can not be connected to any other o/p without causing a serious loading.

Problem.

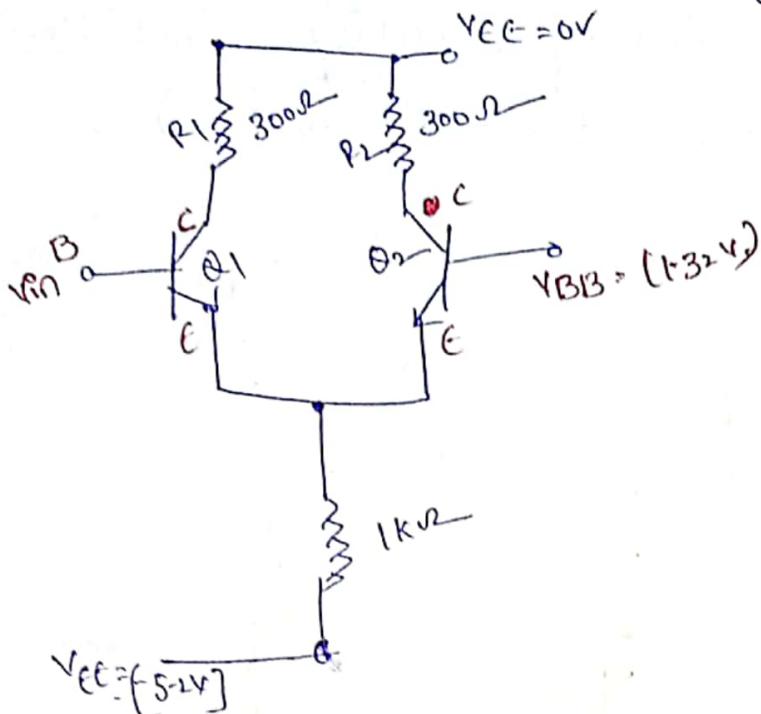
- This loading problem can be eliminated by a modified TTL circuit called a Tri-state TTL ckt
- The totem pole o/p configuration has the advantage of low o/p impedance in both logical states.
- When Q₃ is conducting, the o/p impedance is around 7Ω; when Q₄ is conducting the o/p impedance is only 1Ω.
- Because of such low o/p impedance, any stray o/p capacitance is rapidly charged and discharged, thereby changing the o/p voltage quickly from the state to the other.
- This lower o/p impedance is also responsible for the capability of the gate to drive high capacitive loads, for low-noise susceptibility and high speed performance characteristics of scopes 54174.
- The totem pole o/p's cannot be connected together to form an AND function by an open collector o/p.

Emitter Coupled logic [ECL] - Non-Saturated logic family :-

- Emitter Coupled logic is a current mode logic (CML) non-saturated digital logic family, which eliminates the turn-off delay of saturated transistors by operating in the active mode.
- The propagation delay time of a typical ECL gate is ins.
- The basic ckt of Emitter Coupled logic is a differential

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Amplifier as shown in below figure.

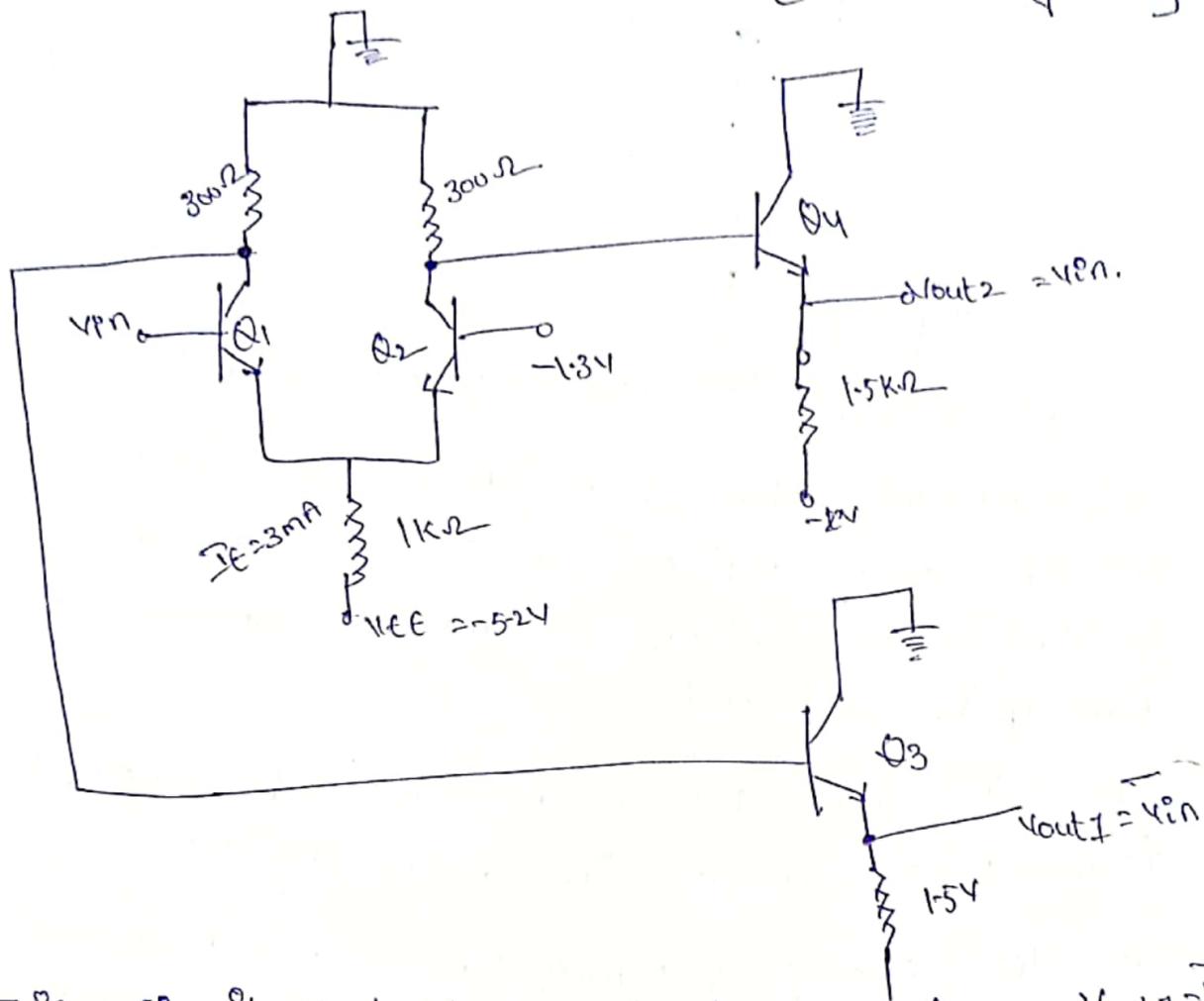


- The power supply line can be noise and spiky
- In addition the transistors are operated in the cut-off and active regions, so transistors do not go into the saturation and as result turn off time off is reduced.
- In this logic power dissipation is more as the transistors operate in active region.
- The Vee Supply produces the a fixed current I_F which remains around $3mA$ during normal operation.
- This Current is allowed flow through Q_1 or Q_2 depending on the voltage level at V_{in} .
- This Current Switches b/w the collectors Q_1 and Q_2 by V_{in} b/w its two logic levels of
 1. logic 0 for $-1.7V$ for logic "0" ECL
 2. $-0.8V$ for logic 1 for ECL.

→ The o/p voltage levels are made equal to the input logic level by connecting V_{C1} and V_{C2} to the Emitter follower stages (Q_3 and Q_4)

ECL Inverter -

$-1.7V \rightarrow \text{logic 0}$
 $-0.8V \rightarrow \text{logic 1}$.



→ This circuit produces low Complementary o/p; $V_{out1} = \overline{V_{in}}$ and $V_{out2} = V_{in}$.

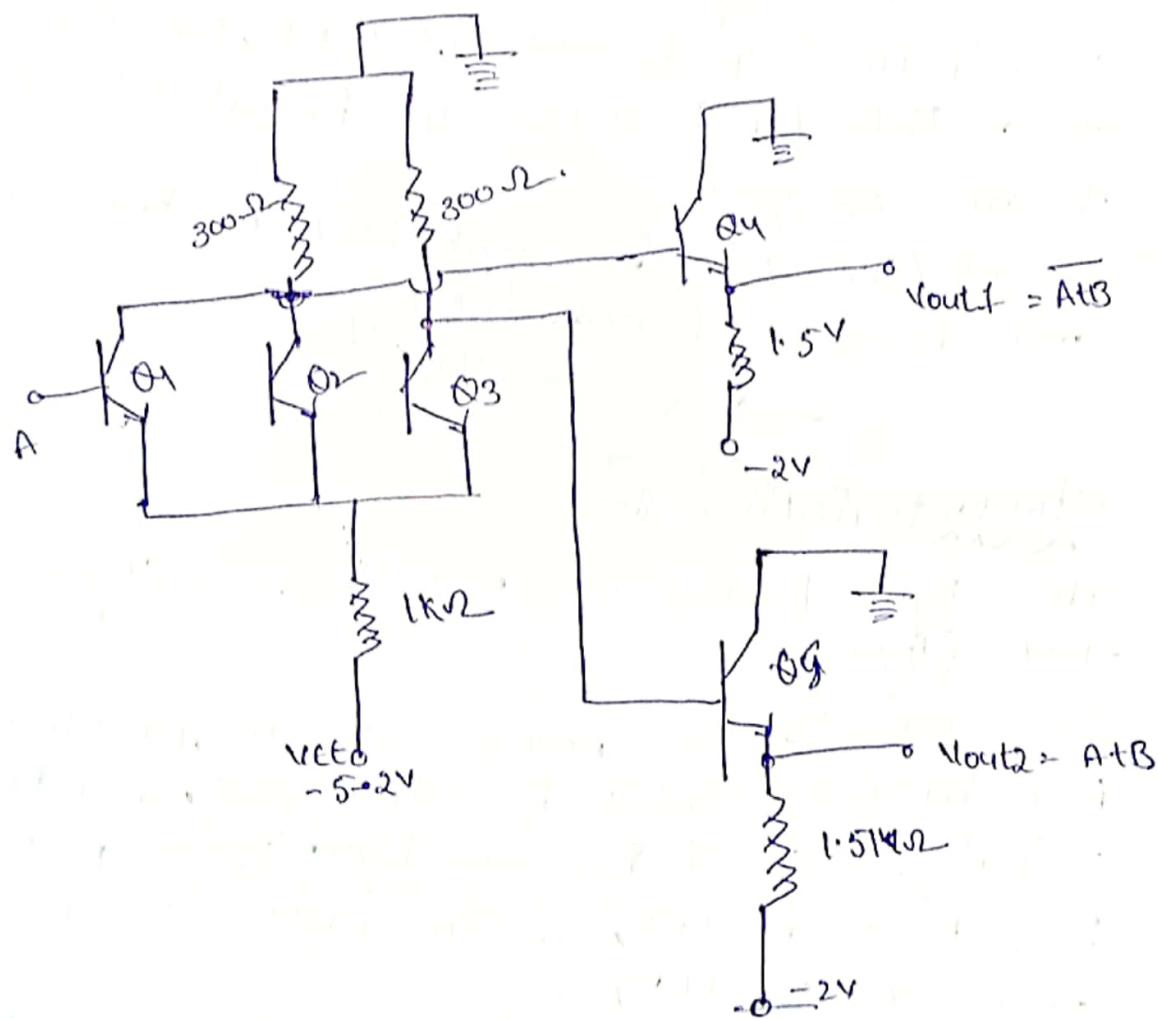
→ logic 0 = $-1.7V$ Then Q_1 is OFF. Q_3 is ON then
 $V_{out1} = 1$, $V_{out2} = 0$.

→ logic 1 = $-0.8V$ then Q_1 is ON Q_2 is OFF

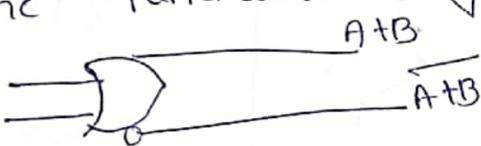
V_{in}	$V_{out,2} = V_{AFB}$	$V_{out,1} = V_{AFB}$
0	0 : 1	0
1	0	0 : 1

ECL OR/NOR Gate :-

→ By connecting one more transistor "Q" in parallel with "Q₁", as shown in below fig 8, the circuit becomes a two-p/p ECL OR/NOR gate with inputs A and B.



- If both input A and B are low, then both transistors Q and Q₁ are in the off state while transistor Q₂ is in the active region and its collector is in a low state.
- If either A and (or) B are HIGH, then according either transistor Q (or) Q₁ conducts and Q₂ is in the off state, resulting in HIGH state at its collector.
- Transistor Q₃ and Q₄ provide the necessary d.c. shift for voltage correction.
- Thus, if the o/p is taken at V_{out1}, the circuit act as a NOR gate; if the o/p is taken V_{out2} it act as an OR gate.
- This OR/NOR gate is symbolised in below figure and is the fundamental gate.



ECL Characteristics :-

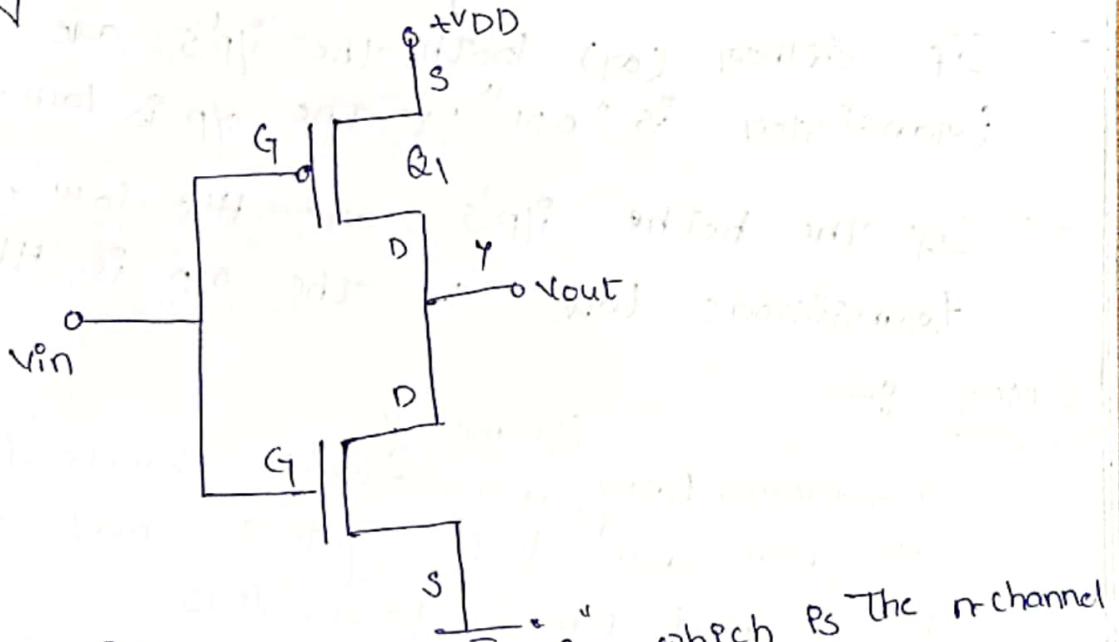
1. The logic levels are normally -0.8V (logic 1) and -1.7V (logic 0).
2. The transistors never saturate i.e. storage delay in ECL circuit is eliminated, and hence switching speed is very high. Typical propagation delay time is 4ns, which makes ECL faster than advanced Schottky TTL.
3. Because of the low noise margin, 1250-milli-volt, ECL circuit are not reliable in heavy industrial environments.

→ CMOS logic circuits excel PMOS and NMOS logic circuits in a no. of features like extremely small d.c power dissipation, Enhanced noise immunity, high fan-out capability and ease of interfacing.

- The source terminal of the p-MOS -channel device is at V_DO, and the source terminal of the n-channel device is ground.
- CMOS Circuits are used both in logic circuits and memory device.

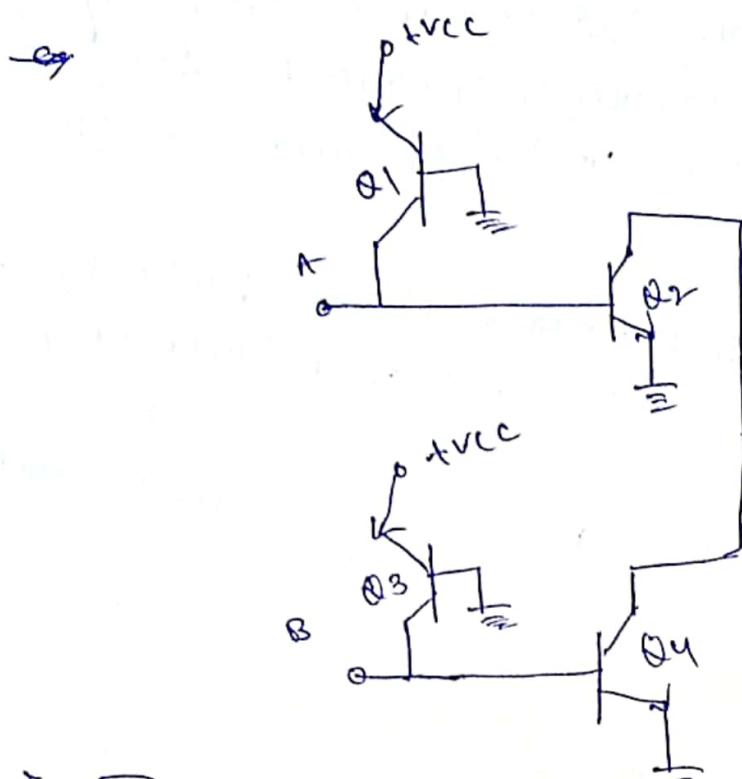
CMOS Inverter :-

- The basic CMOS Inverter Connection is shown in the below figure



- The driver is transistor $\equiv Q_1$ which is the n-channel and (p-mos channel device) act as the load
- The source of p-channel device is

I²L NOR gate :-



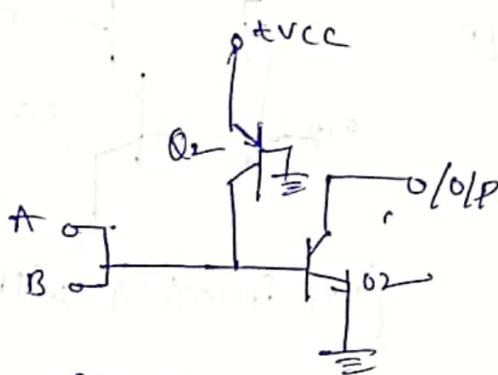
- In this open connection two inverter with their o/p connected together
- If either (or) both the o/p's are HIGH . Then Q1 transistor is "ON" so the o/p is low.
- If the both o/p's are low , both the o/p transistors low so the o/p is HIGH .

CMOS :-

- Complementary metal-oxide semiconductor, CMOS is symmetric logic gates made using both PMOS and NMOS transistors.
- The basic gates employ both p- and n-channel enhancement mode complementary symmetry MOSFET.
- The power consumption of CMOS under static conditions is extremely low .

- (8)
- As a Constant Current is drawn by the differential amplifier even during transition from one state to another state.
 - Because of the active mode of operation of the differential amplifier, there is no storage delay in switching between ON and OFF states of the transistors in the differential pair. *(not wrong)*
 - → OFF and o/p is HIGH
 - If the i/p is HIGH, the injected current flows into the base of "Q₂" turning it ON and making the output is low.

I²L NAND gate

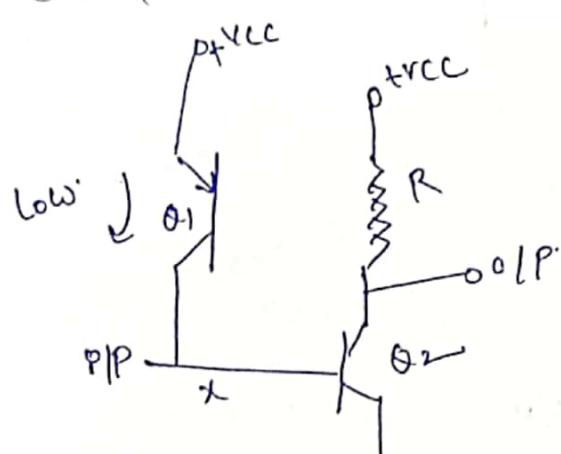


- if either input A or i/p B (or both i/p's A & B are low), the injected current flows into those p/p Q₂ to remains off so the o/p is HIGH.
- If the both i/p's are HIGH, the injected current to Q₂ making the o/p low. Thus NAND operation is performed.

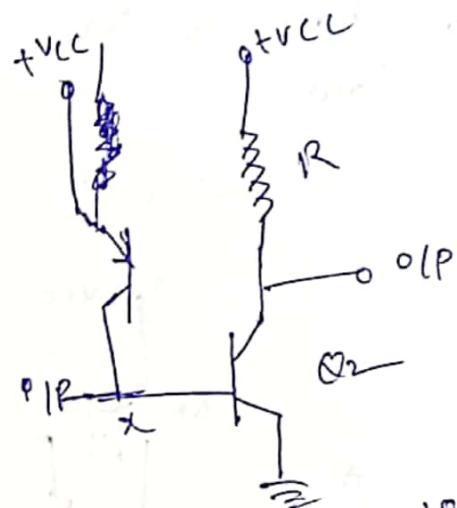
Integrated Injection logic [I²L (or) I²L] :-

- I²L is a new LSI technology technique also called merged Transistor logic.
- I²L logic gate are constructed using bipolar transition only.
- Due to the absence of resistors it's possible to integrate a large no. of gates on a single package. Their power consumption is low.

I²L INVERTER :-



{ I²L inverter with low o/P }



{ I²L inverter with high }

- Q₁ is called current injection transistor because when its emitter is connected to an external power source, it can supply current to the base of Q₂.
- Q₁ ~~seen~~ serving as a constant current source that injects current into node "o/P".
- A low o/P is a current sink, when the PIP is low, the injected current flows into the o/P, thus Q₂ is

- The gates of the two devices are connected together as a common input.

Operation :-

- When V_{in} is low, Q_2 is off, but Q_1 is on. This means the output voltage is high.
- On the other hand, when V_{in} is high, Q_2 is on and Q_1 is off.
- In this case, the output voltage is low. Since the output voltage is always opposite in phase to the i/p voltage, the circuit act as the inverter.

V_{in}	Pmos	Nmos	V_{out}
0	ON	OFF	1
1	OFF	ON	0

Interfacing CMOS with TTL :-

- Interfacing means connecting the outputs of one circuit (or) system to the i/p's of another ckt (or) system that may have different electrical characteristics.
- when two circuits have different electrical characteristics direct connection can not be made. In such cases driver and load circuits are connected through interface circuit.
- Its function is to take the drivers o/p signal and condition it. So that it is compatible with requirements of the load.



- One must consider following important points while interfacing two circuits (or) systems.
 - The driver op must st satisfy the voltage and current requirements of the load circuit
- ➢ The driver and load circuit may require different power supplies. In such cases the o/p of both ckt must swing b/w its specified voltage ranges.

→ TTL Driving CMOS :-

- Here TTL is a driver circuit and CMOS is a load circuit.
- The two circuits are from different logic families with different electrical characteristics, therefore we must check that the driving device can meet the current and voltage requirements of the load device.

	CMOS		TTL
I _{TH(max)}	400B	74HC/HCT	74
I _{IL(max)}	1mA	1mA	40mA
I _{OH(max)}	0.6mA	4mA	1.6mA
I _{OL(max)}	0.4mA	4mA	16mA
			8mA
			0.4mA
			2mA
			2mA
			20mA

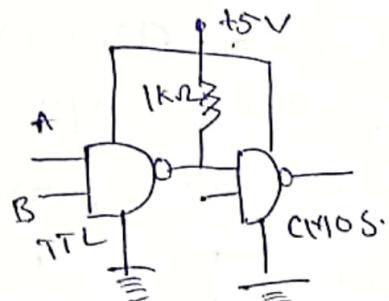
Table ① :- I_{IP} and o/p currents for standard device with supply voltage 5V.

-P001 CMOS 4000B	FOR TTL
$V_{IH(\min)} > 3.5V$	$V_{IL(\min)} > 2.0V$
$V_{IL(\max)} > 1.5V$	$V_{IL(\max)} = 0.8V$
$V_{OH(\min)} = 1.95V$	$I_{IH(\max)} = 40mA$
$V_{OL(\max)} = 0.95V$	$I_{IL(\max)} = 1.6mA$
$I_{OH(\max)} = 0.1mA$	$V_{OH(\min)} = 2.4V$
$I_{OL(\max)} = 0.4mA$	$V_{OL(\max)} = 0.4V$

Table (2)

- Table (2) indicates that the input current values for CMOS are extremely low compared with the o/p current capabilities of any TTL series. Thus, TTL has no problem meeting the CMOS input current requirements.
- But when we compare the TTL o/p voltages with the CMOS o/p voltage requirements we find that :-

✓ $V_{OH(\min)}$ for TTL $\ll V_{IH(\min)}$ for CMOS, for these situations TTL o/p must be raised to an acceptable level - for CMOS.



TTL driving CMOS using External pull-up resistors.

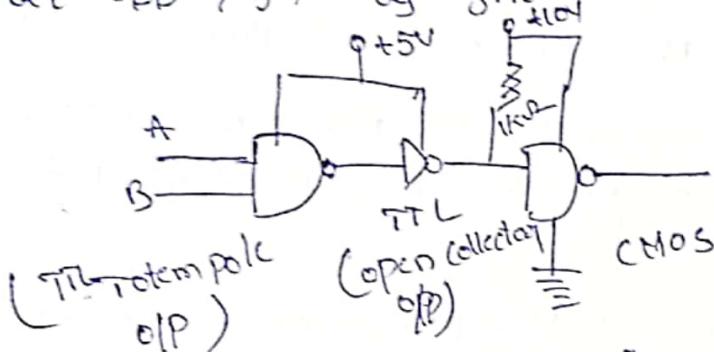
- In this figure, let the pull up resistor causes the TTL o/p to rise to approximately 5V in the HIGH state, thereby providing an adequate CMOS o/p voltage level.

Q) > TTL Driving HIGH voltage CMOS :-

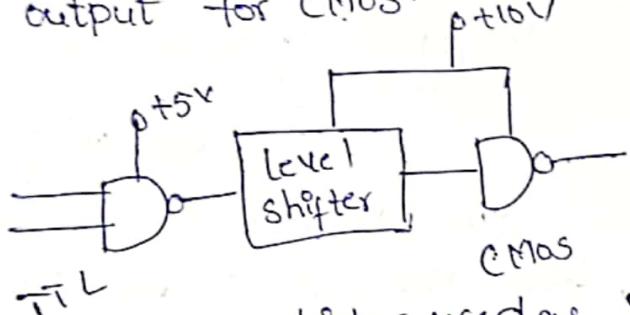
→ When the output of TTL circuit is operating with VDD greater than 5V, the situation becomes more difficult.

→ The output of many TTL devices cannot be operated at more than 5V. In such cases some alternative arrangement we made. Two of them are discussed below :-

> when the TTL op/p cannot be pulled up to VDD, one can use open collector buffer as an interface between totem pole TTL op/p and CMOS operating at VDD > 5V as shown in below figure.



→ The second alternative is to use level shifter circuit. This is a CMOS chip that is designed to take a low-voltage I/P and translate it to high voltage output for CMOS.



level shifter used as interface circuit.

CMOS Driving TTL :-

CMOS driving TTL in the high state :-

- Above voltage parameters shows that CMOS o/p's can easily supply enough voltage (V_{OH}) to satisfy TTL i/p requirements in the HIGH state (V_{IH})
- The parameters also show that the CMOS o/p's can supply more than enough (I_{OH}) to meet the TTL i/p current requirements (I_{IH}). Thus no special consideration is required for CMOS driving TTL in the HIGH state.

CMOS o/p TTL i/p

$$V_{O(H)(max)} = 4.9V \quad V_{I(H)(max)} = 2V$$

$$V_{O(L)(max)} = 0.1V \quad V_{I(L)(max)} = 0.84$$

$$I_{O(H)(max)} = 0.4mA \quad I_{I(H)(max)} = 40mA$$

$$I_{O(L)(max)} = 0.4mA \quad I_{I(L)(max)} = 11.6mA$$

CMOS driving TTL in low state :-

- The parameters in table ② show that CMOS o/p voltage (V_{OL}) satisfy TTL i/p requirement in the low state (V_{IL})
- However, the current requirements, in the low state are not satisfied the TTL i/p has a relatively high i/p current in low state (1.6mA) and CMOS o/p current at low state (I_{OL}) is not sufficient to drive even one i/p of TTL.

- In such situations some type of interface circuit is needed b/w the CMOS and TTL devices shown below

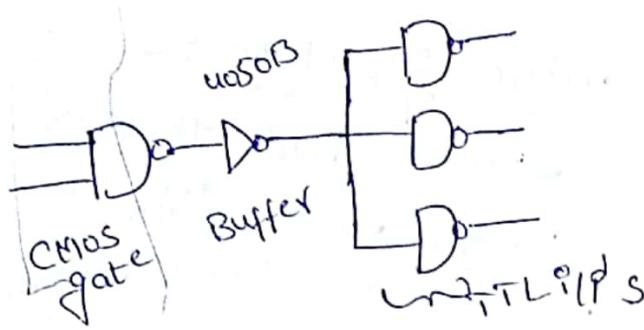


fig :- CMOS driving TTL in low state using buffer.

HIGH voltage CMOS driving TTL :-

- Some IC manufacturers have provided several full TTL device that can withstand 15V voltages as high as 15V.
- These devices can be driven directly from CMOS outputs operating at $V_{DD} = 5V$.
- However, most TTL I/P's cannot handle more than 7V, and so interface is necessary if they are to be driven from high-voltage CMOS. In such situations "voltage level translators" are used. They convert the high voltage I/P to a 5V I/P that can be connected to TTL.

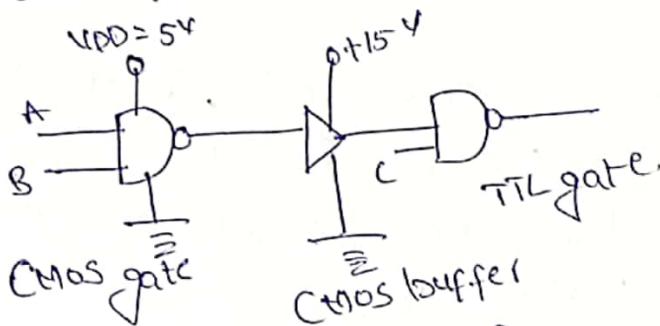


fig :- level translation using CMOS buffer.

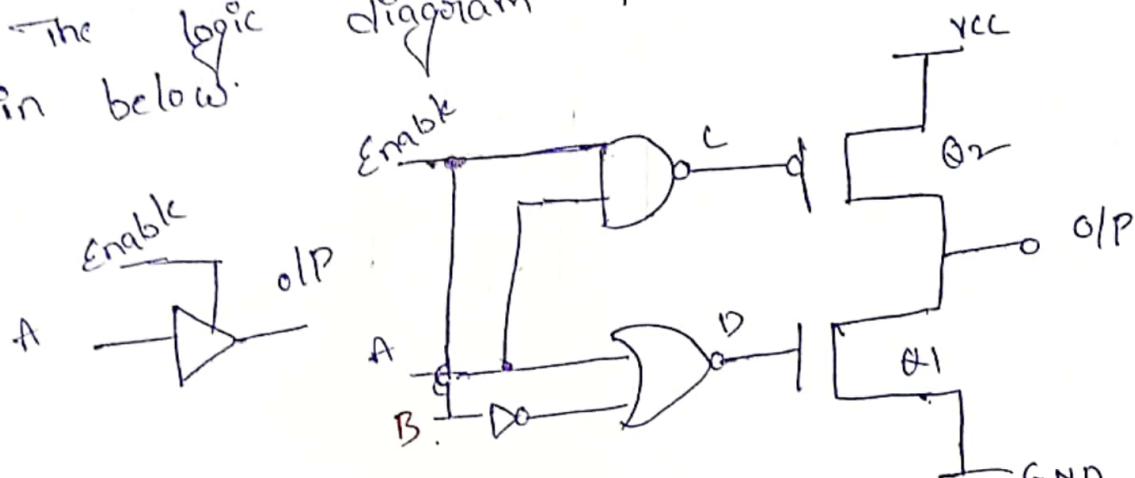
- The above fig. can be used to perform level translation between 15V and 5V.

CMOS CONFIGURATIONS :-

TRI-STATE LOGIC :-

→ The tri-state o/p combines the advantages of the totem pole & open collector ckt's.

- When the enable ip is low the device is enabled for normal logic operation.
- When enable is high both Q_1 and Q_2 are in the high state.
- The logic diagram for tri-state logic is shown in below.



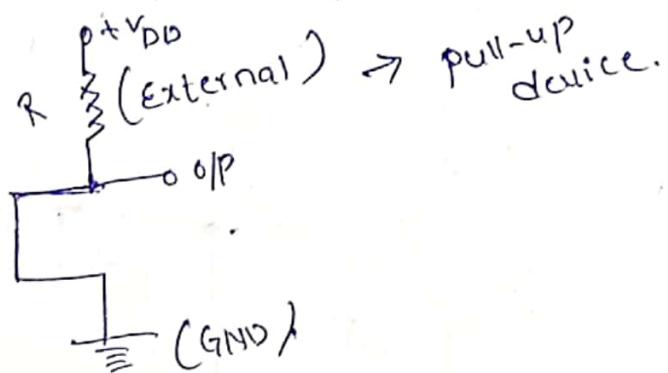
CMOS tri-state logic diagram

→ Truth table for CMOS tri-state logic is shown in below figure.

En	A	B	C	D	Q_1	Q_2	O/P
L	L	H	H	L	OFF	OFF	H-Z
L	H	H	H	L	OFF	OFF	H-Z
H	L	L	H	H	ON	OFF	L
H	H	W	H	H	OFF	ON	H

OPEN DRAIN OUTPUTS :-

- The term open drain means that the drain terminal of the output transistor is unconnected and must be connected externally to VDD through a load.
- An open-drain o/p ckt is a single n-channel MOSFET as shown in below figure.
- It is used to produce a high o/p state.



4.14 Characteristics of CMOS

The first CMOS logic series was produced by RCA and is known as the 4000 series, which was later developed by other manufacturers. At present, several manufacturers have developed a CMOS series which is pin-for-pin compatible with TTL. This is the 74C00 series and it contains devices that have the same pin assignments and logic operations as their TTL counterparts. Any device in the 74C00 series works over a temperature range of -40°C to $+85^{\circ}\text{C}$, which is sufficient for most commercial applications. The 54C00 series works over a temperature range of -55°C to 125°C and is useful for military applications. The 74HC00 series of devices has the advantage of higher speed.

Power dissipation Under static conditions (i.e. when the output is constant), the power consumed by a CMOS gate is extremely small (in nanowatts). When a CMOS output changes from the LOW state to the HIGH state (or vice versa), the average power dissipation increases. This is due to the fact that during a transition between states, both MOSFETs conduct for a small period of time. This leads to a spike in the supply current.

Therefore, during the transition, the drain current becomes appreciable. Moreover, any stray capacitance across the output has to be charged before the output voltage can change. This capacitive charging draws additional current from the supply, thereby increasing the instantaneous power dissipation.

The average power dissipation of a CMOS device whose output is continuously changing is called the *active power dissipation*. This power dissipation per gate increases with frequency and supply voltage. The power consumption of a CMOS gate is around 10mW in the MHz region. Thus, CMOS loses its advantages at higher frequencies.

Propagation delay time The propagation delay of a standard CMOS gate ranges from 25 to 150ns, with the exact value depending on the power supply voltage and other factors. A CMOS NAND gate typically has a propagation delay time of about 25ns when $V_{DD} = 10\text{V}$, and 50ns when $V_{DD} = 5\text{V}$.

Voltage levels CMOS can be operated over a supply voltage range of 3V to 15V. A supply voltage of 9V to 12V can be used to obtain the overall best performance of a CMOS gate in respect of high speed and noise immunity. When CMOS is being used with TTL, the V_{DD} supply voltage is made 5V so that the voltage levels of the two families are the same.

Noise margin In CMOS series, the noise margin is typically about 45% of the supply voltage V_{DD} . They have the same noise margin in both HIGH and LOW states. A V_{DD} of 5V guarantees a 25V noise margin.

Floating inputs A floating TTL input is equivalent to a high input. If a CMOS input is floated, a possible noise problem is set up and there is excessive power dissipation. Therefore, it is necessary to connect all the input pins of the CMOS devices to some voltage level, preferably to ground or V_{DD} .

Sourcing and sinking When a standard CMOS driver output is LOW, the current from the CMOS load to the driver is only $1\mu A$. This indicates that the CMOS driver has to sink only $1\mu A$. Similarly, when the CMOS driver output is HIGH, the driver is sourcing $1\mu A$ to an input of the load gate. The worst case input currents for CMOS devices are:

$$I_H(\text{max}) = -1\mu A; \quad I_{HH}(\text{max}) = 1\mu A$$

$$I_{OL}(\text{max}) = 10\mu A; \quad I_{OH}(\text{max}) = -10\mu A$$

Fan-out The fan-out of CMOS gates depends on the type of load being connected. If a standard CMOS drives another standard CMOS, the fan-out can be calculated from the input and output currents of the standard CMOS gate given above.

$$\text{Considering low output state: } \frac{I_{OL,\text{max}}}{I_{H,\text{max}}} = \frac{10\mu A}{1\mu A} = 10$$

$$\text{Considering high output state: } \frac{I_{OH,\text{max}}}{I_{HH,\text{max}}} = \frac{10\mu A}{1\mu A} = 10$$

Therefore, 10 standard CMOS gates can be connected to the output of another standard CMOS gate. Thus, the fan-out of standard CMOS gate is 10.

4.3 Characteristics of Digital ICs

Some of the important parameters or properties of various logic families are listed as follows:

1. Speed of operation (Propagation delays)
2. Power dissipation
3. Fan-in
4. Fan-out
5. Noise immunity
6. Operating temperature
7. Power supply requirements

The comparison of performance of digital ICs may be made with reference to the above properties.

4.3.1 Speed of Operation

The speed of operation of an IC is expressed in terms of propagation delay. *Propagation delay* is defined as the time taken for the output of a gate to change after the inputs have changed.

A logic signal always experiences a delay in going through a circuit. The two propagation delay times shown in Fig. 4.1 are defined as follows:

t_{PLH} : It is the propagation delay time in going from logical LOW (0 state) to logical HIGH (1 state).

t_{PHL} : It is the propagation delay time in going from logical HIGH (1 state) to logical LOW (0 state).

It is evident that t_{PLH} is the delay in the *output* response as it goes from LOW state to a HIGH state, and vice versa for t_{PHL} . The delay times are measured between the 50% voltage levels of the input and output waveforms. In general, the two delays t_{PHL} and t_{PLH} are not necessarily equal and will vary depending on load conditions. The values of propagation times are a measure of the relative

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Therefore, during the transition, the drain current becomes appreciable. Moreover, any stray capacitance across the output has to be charged before the output voltage can change. This capacitive charging draws additional current from the supply, thereby increasing the instantaneous power dissipation.

The average power dissipation of a CMOS device whose output is continuously changing is called the *active power dissipation*. This power dissipation per gate increases with frequency and supply voltage. The power consumption of a CMOS gate is around 10mW in the MHz region. Thus,

Propagation delay time The propagation delay of a standard CMOS gate ranges from 25 to 150ns, with the exact value depending on the power supply voltage and other factors. A CMOS NAND gate typically has a propagation delay time of about 25ns when $V_{DD} = 10\text{V}$, and 50ns when $V_{DD} = 5\text{V}$.

Voltage levels CMOS can be operated over a supply voltage range of 3V to 15V. A supply voltage of 9V to 12V can be used to obtain the overall best performance of a CMOS gate in respect of high speed and noise immunity. When CMOS is being used with TTL, the V_{DD} supply voltage is made equal to that of TTL.

Noise margin In CMOS series, the noise margin is typically about 45% of the supply voltage V_{DD} . They have the same noise margin in both HIGH and LOW states. A V_{DD} of 5V guarantees a 25V noise margin.

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speed of logic circuits. The average of the above two propagation delays $(t_{PHL} + t_{PUL})/2$ is called average propagation delay and is used to rate the circuit. It is a function of the switching time of individual transistors or MOSFETs in the circuit.

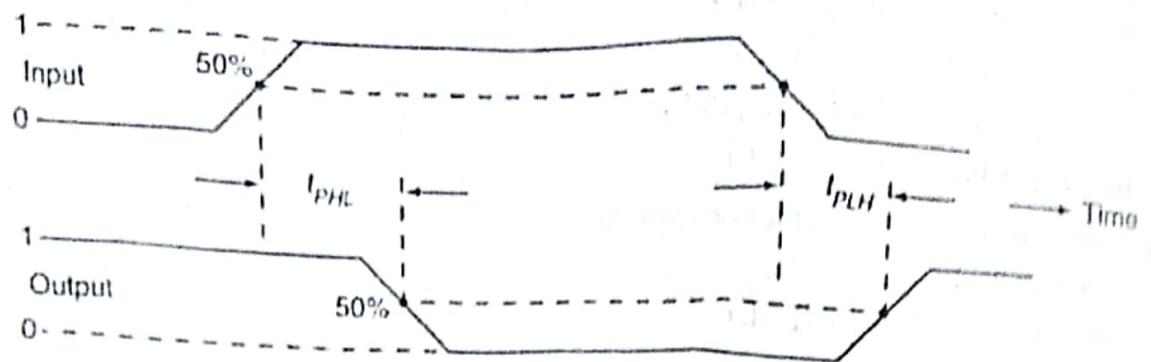


Fig. 4.1 Propagation delays

4.3.2 Power Dissipation

Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its inputs, and it is expressed in milliwatts or nanowatts. The d.c. or average power dissipation is the product of d.c. supply voltage and the mean current taken from that supply.

4.3.3 Fan-in

The fan-in of a gate is the number of inputs connected to the gate without any degradation in the voltage levels. For example, an eight-input gate requires one Unit Load (UL) per input. Its fan-in is 8. This parameter determines the functional capabilities of a logic circuit.

4.3.4 Fan-out

Fan-out is the maximum number of similar logic gates that a gate can drive without any degradation in voltage levels. Very often a gate will drive several other gates. Each driven gate requires a certain current which must be supplied by the driving gate. The driving gate must be capable of supplying this current while maintaining the required voltage level. In part, this is a function of the output impedance of the driving gate and the input impedance of the driven gates. Usually, in a given logic family, gates drive others of the same type. If their output impedance is low while their input impedance is high, then one gate can often drive many others.

4.3.5 Noise Immunity or Noise Margin

The term noise denotes an unwanted signal voltage, e.g., hum, transients and glitches.

Noise can sometimes cause the input voltage of a logic gate to drop below V_{IH} (min) or rise above V_{IL} (max), which leads to unreliable operation. Noise immunity is the maximum noise voltage that may appear at the input of a logic gate without changing the logical state of its output. A quantitative measure of noise immunity is called noise margin.

The difference between the operating input-logic voltage level and the threshold voltage is called the noise margin of the circuit. The manufacturer usually quotes the noise margin, which refers to the amplitude of the noise voltage that may cause the logic level to change. In the worst case, a TTL gate functions properly as long as the noise margin is kept less than 0.4V.

3.6 Operating Temperature

IC gates are semiconductor devices that are temperature-sensitive by nature. The operating temperature ranges for an IC vary from 0°C to $+70^{\circ}\text{C}$ for consumer and industrial applications and from -55°C to $+125^{\circ}\text{C}$ for military applications.

3.7 Power Supply Requirements

The amount of power and supply voltage required by an IC are the main parameters to be taken into consideration while choosing a proper power supply.

3.8 Current and Voltage Parameters

The following currents and voltages are very important in designing digital systems. The values given below are for TTL gates only.

High-level input voltage (V_{IH}) [$V_{in(1)}$] It is the minimum voltage level required for a logical 1 at an input. Its minimum value is 2V.

Low-level input voltage (V_{IL}) [$V_{in(0)}$] It is the maximum input voltage required for a logical 0 (LOW) at an input. Its maximum value is 0.8V.

High-level output voltage (V_{OH}) [$V_{out(1)}$] It is the minimum voltage required for a logical 1 state at the output. Its minimum value is 2.4V.

Low-level output voltage (V_{OL}) [$V_{out(0)}$] It is the maximum voltage available at the circuit's output corresponding to the logical 0 state. Its maximum value is 0.4V.

High-level input current (I_{IH}) [$I_{in(1)}$] The current that flows through an input when a specified high-level voltage is applied to that input.

Low-level input current (I_{IL}) [$I_{in(0)}$] The current that flows through an input when a specified low-level voltage is applied to that input.

High-level output current (I_{OH}) [$I_{out(1)}$] The current that flows from an output in the logical 1 state under specified load conditions.

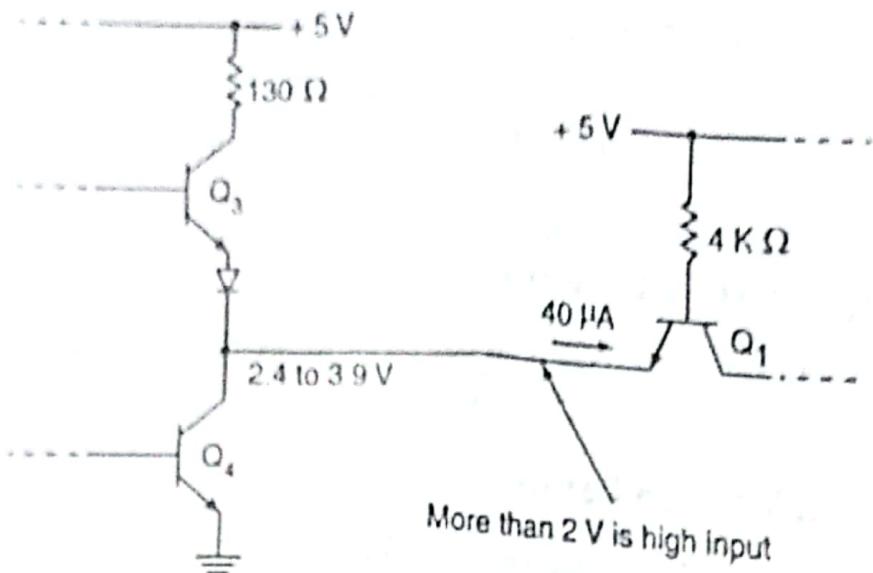
Low-level output current (I_{OL}) [$I_{out(0)}$] The current that flows from an output in the logical 0 state under specified load conditions.

4.4 Current-sourcing and Current-sinking Logic

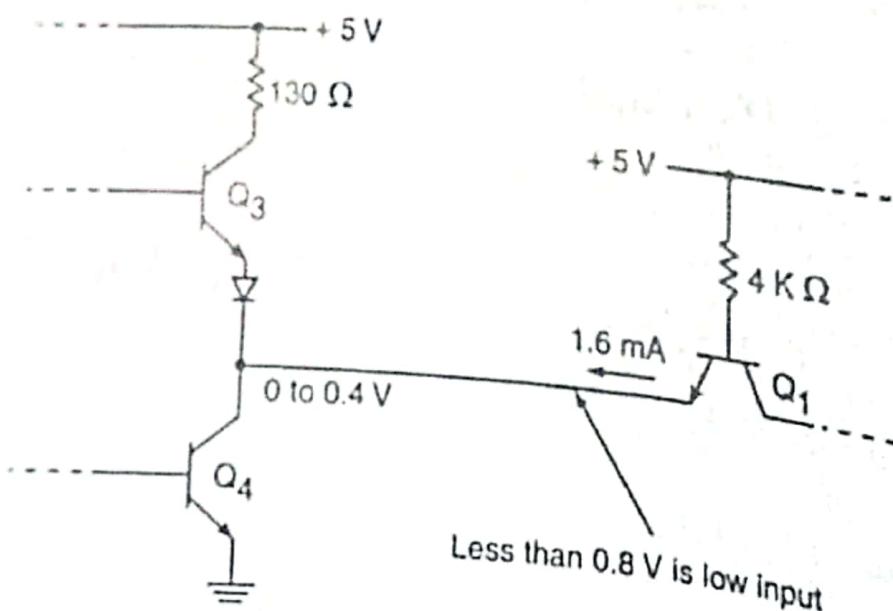
Logic families can be categorised depending upon the flow of current from the output of one logic circuit to the input of another. Current-sourcing and current-sinking logic gates are illustrated in Fig. 4.2(a) and (b) respectively.

When a standard TTL gate output is HIGH as shown in Fig. 4.2(a), a reverse emitter current of 40 mA flows from transistor Q_3 of driver gate to the emitter of transistor Q_1 of load gate, and hence Q_3 acts as a *current source*.

When a standard TTL gate output is LOW as shown in Fig. 4.2(b), an emitter current of 1.6 mA flows from the emitter of transistor Q_1 of load gate to the collector of transistor Q_4 of driver gate. As Q_4 is saturated, current flows through it to the ground, and hence Q_4 acts as a *current sink*.



(a) Current-sourcing



(b) Current-sinking

Fig. 4.2