

Basic Building Blocks of Analog IC Design

* Regions of operation of MOSFET:

There are three regions of operation in the MOSFET.

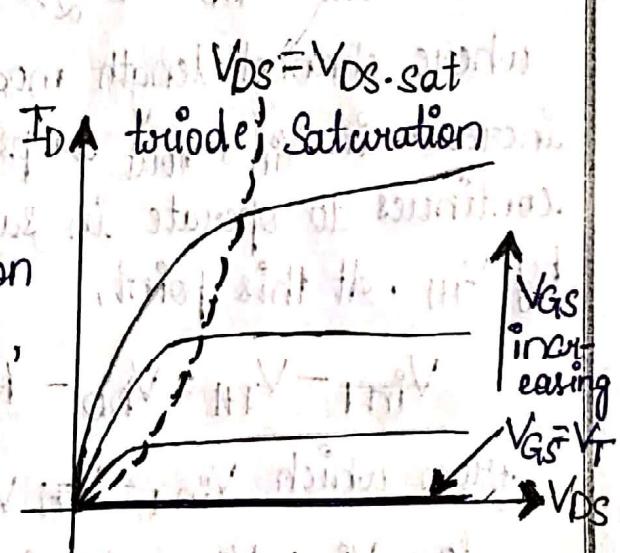
→ When $V_{GS} < V_T$, no conductive channel is present and $I_D = 0$, the cutoff region.

→ If $V_{GS} < V_T$ and $V_{DS} < V_{DS,sat}$, the device is in the triode region of operation. Increasing V_{DS} increases the lateral field in the channel, and hence the current. Increasing V_{GS} increases the transverse field and hence the inversion layer density, which also increases the current.

→ If $V_{GS} > V_T$ and $V_{DS} > V_{DS,sat}$, the device is in the saturation region of operation. Since the drain and channel density has become small, the current is much less dependent on V_{DS} , but is still dependent on V_{GS} , since increased V_{GS} still increases the inversion layer density.

MOSFET $I_D - V_{DS}$ Characteristic:

- For $V_{GS} < V_T$, $I_D = 0$
- As V_{DS} increases at a fixed V_{GS} , I_D increases in the triode region due to the increased lateral field, but at a decreasing rate since the inversion layer density is decreasing.
- Once pinchoff is reached, further V_{DS} increases only increase I_D due to saturation of the high field region.
- The device starts in triode, and moves into saturation



at higher V_{DS} .

* Single stage amplifier with resistive load:

Common-source stage with Resistive load:

A MOSFET converts changes in its gate-source voltage to a small-signal drain current, which can pass through a resistor to generate an output voltage. Shown in figure, the common-source stage performs such an operation. We study both the large-signal and the small-signal behavior of the circuit. Note that the input impedance of the circuit is very low at low frequencies.

If the input voltage increases from zero, M_1 is off and $V_{out} = V_{DD}$. As V_{in} approaches V_{TH} , M_1 begins to turn on, drawing current from R_D and lowering V_{out} . Transistor M_1 turns on the saturation regardless of the values of V_{DD} and R_D , and we have

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$

where channel-length modulation is neglected. With further increase in V_{in} , V_{out} drops more and the transistor continues to operate in saturation until V_{in} exceeds V_{out} by V_{TH} . At this point,

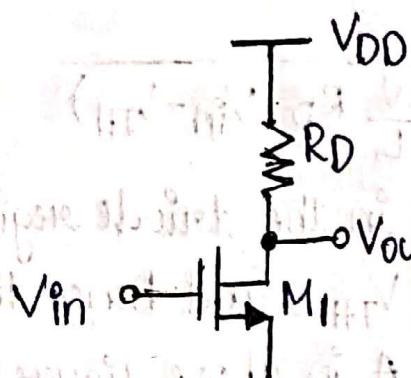
$$V_{in} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$

from which $V_{in} - V_{TH}$ and hence V_{out} can be calculated.

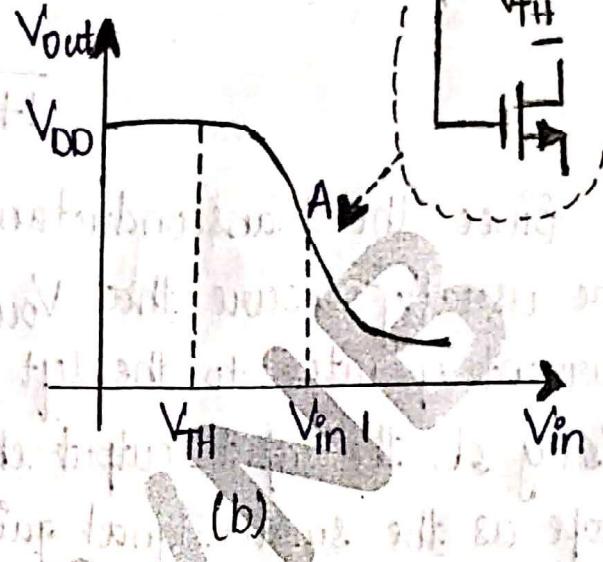
for $V_{in} > V_{in} 1$, M_1 is in the triode region:

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu n C_{ox} \frac{W}{L} [2(V_{in} - V_{TH})V_{out} - V_{out}^2]$$

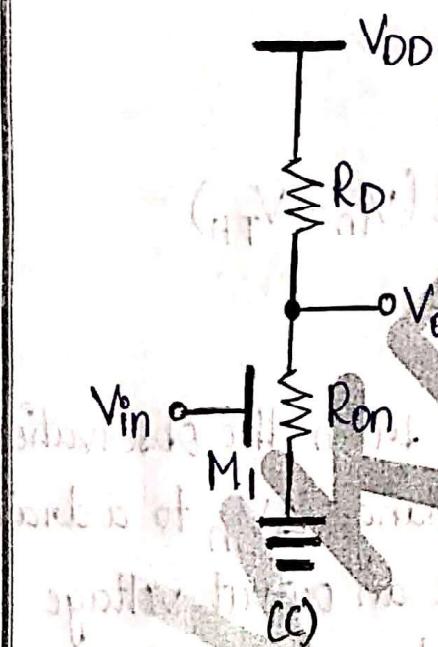
The common-source topology is identified as receiving the input at the gate and producing the output at the drain.



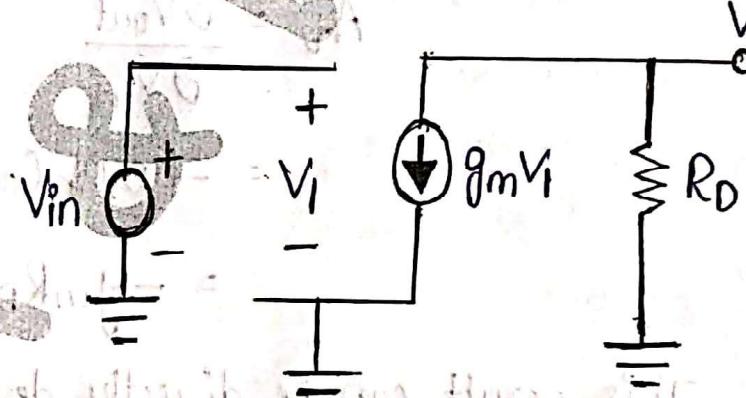
(a)



(b)



(c)



(d)

Figure : (a) Common-source stage, (b) input-output characteristic, (c) equivalent circuit in the deep triode region and (d) small-signal model for the saturation region.

If V_{in} is high enough to drive M_1 into the deep triode region, $V_{out} \ll \alpha(V_{in} - V_{TH})$, and from the equivalent

Circuit of above figure (c),

$$V_{out} = V_{DD} \frac{R_{on}}{R_{on} + R_D}$$

$$\approx \frac{V_{DD}}{1 + M_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})}$$

Since the transconductance drops in the triode region, we usually ensure that $V_{out} > V_{in} - V_{TH}$, and hence the current operates to the left of point A in above figure (b). Using as the input-output characteristic and viewing its slope as the small-signal gain, we have:

$$\begin{aligned} A_v &= \frac{\partial V_{out}}{\partial V_{in}} \\ &= -R_D M_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) \\ &= -g_m R_D \end{aligned}$$

This result can be directly derived from the observation that M_1 converts an input voltage change ΔV_{in} to a drain current change $g_m \Delta V_{in}$, and hence an output voltage change $-g_m R_D \Delta V_{in}$. The small-signal model of above figure (d) yields the same result: $V_{out} = -g_m V_I R_D = -g_m V_{in} R_D$.

Ans. 1. Neg. load. Damping. - Usual (C) for design.

selected goals will always result at chosen point in not fit
for obvious all cases have (A) and (B) and (C) will be missed.

* Single stage amplifier with diode connected load:

Common source stage with Diode-connected load:

In some CMOS technologies, it is difficult to fabricate resistors with tightly-controlled values or a reasonable physical size. Consequently, it is desirable to replace R_D with a MOS transistor.

A MOSFET can operate as a small-signal resistor if its gate and drain are shorted. Called a "diode-connected" device in analogy with its bipolar counterpart, this configuration exhibits small-signal behavior similar to that of two-terminal resistor. Note that the transistor is always in saturation because the drain and the gate have the same potential. Using the small-signal equivalent to obtain the impedance of the device, we write $V_I = V_X$ and $I_X = V_X / (\gamma_0 + g_m V_X)$. That is, the impedance of the diode is simply equal to $V_X / I_X = (1/g_m) \parallel \gamma_0 \approx 1/g_m$. If body effect exists, we can use the circuit to write $V_I = -V_X$, $V_{BS} = -V_X$, and

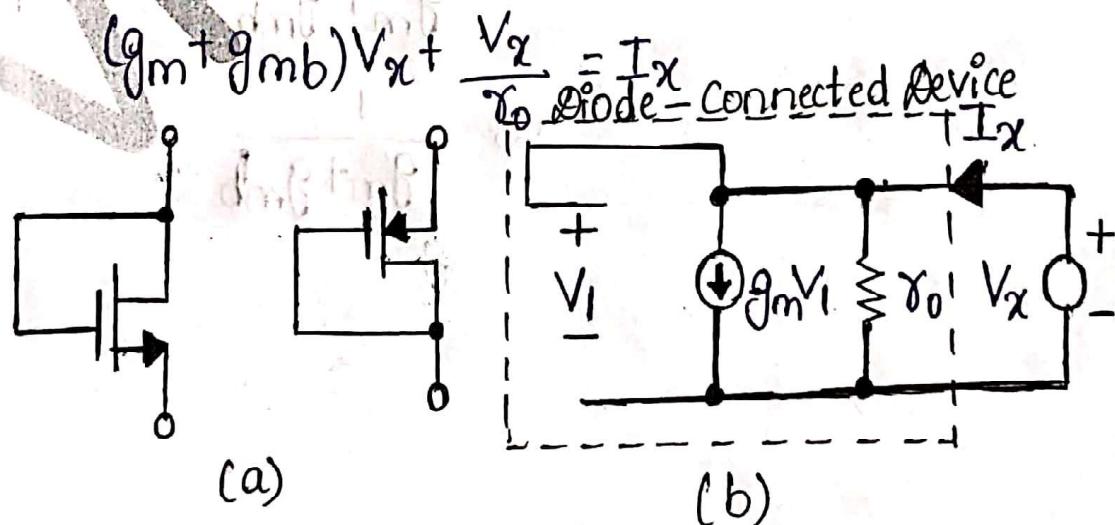


Figure : (a) Diode-connected NMOS and PMOS devices;
(b) small-signal equivalent circuit.

Common-Source Stage

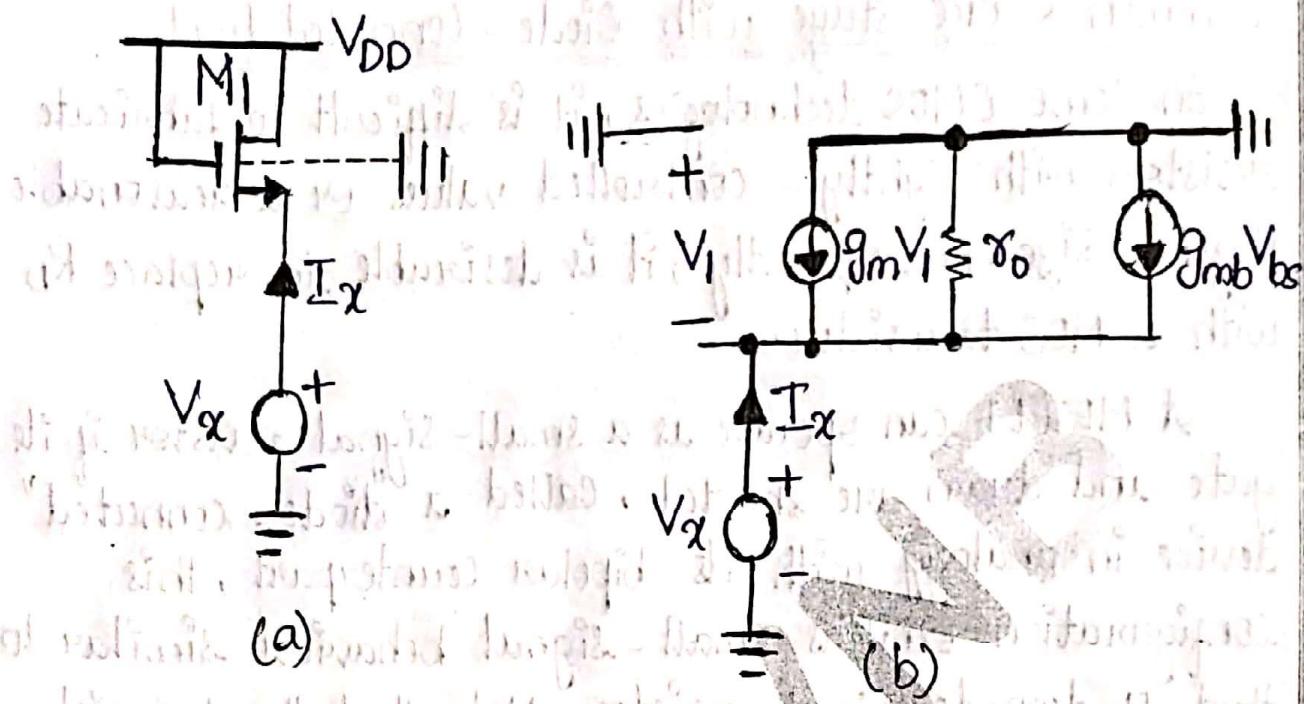


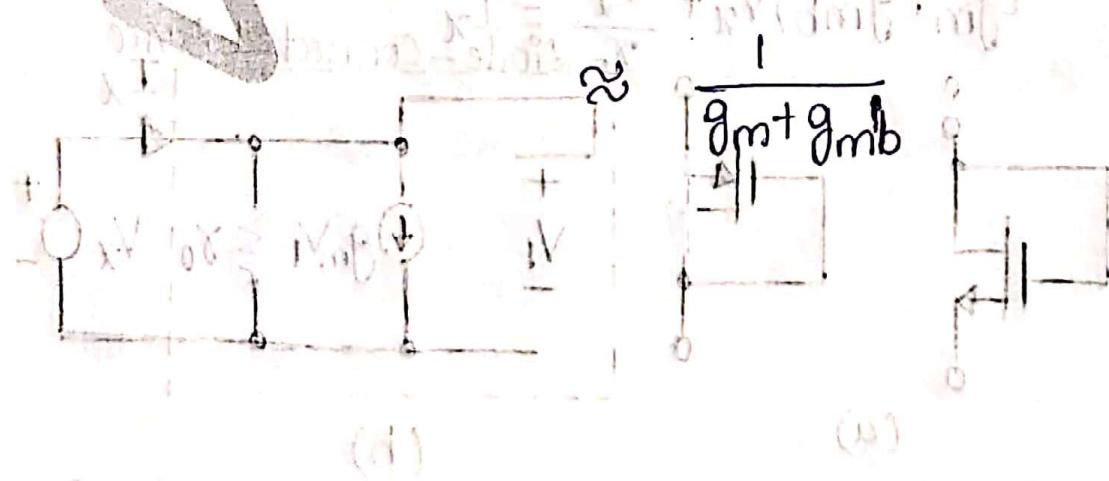
Figure: (a) arrangement for measuring the equivalent resistance of a diode-connected MOSFET; (b) small-signal equivalent circuit.

It follows that

$$\frac{V_x}{I_x} = \frac{1}{g_m + g_{mb} + r_o}$$

$$= \frac{1}{g_m + g_{mb}} \parallel r_o$$

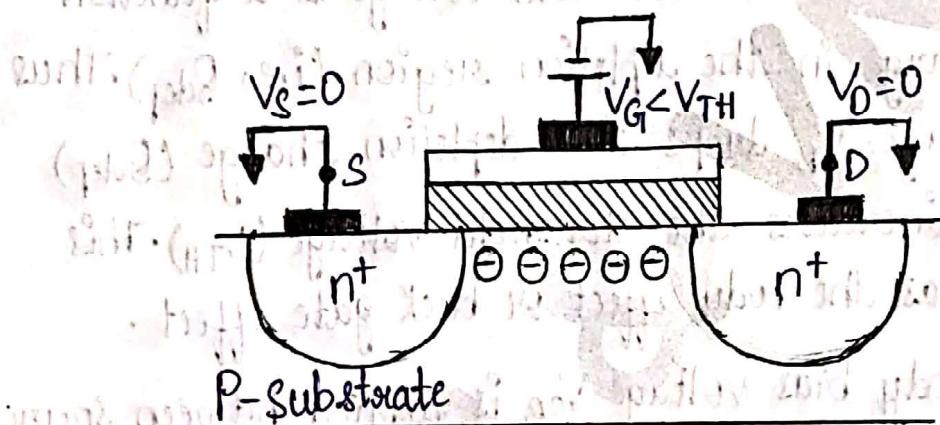
$$\approx \frac{1}{g_m + g_{mb}}$$



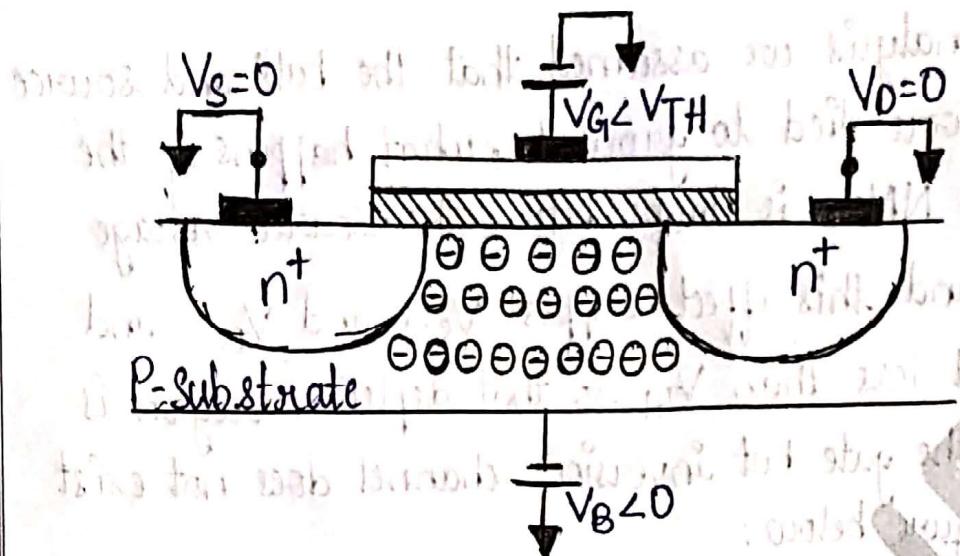
* Body Bias Effect:

In I-V analysis we assumed that the bulk and source of transistor were tied to ground, what happens if the bulk voltage of NMOS drops below the source voltage

To understand this effect suppose $V_S=0$ and $V_D=0$ and V_G is somewhat less than V_{TH} so that depletion region is formed under the gate but inversion channel does not exist as shown in figure below:



As V_B becomes more negative (i.e., $V_B < V_S$ where $V_S=0$) more holes are attracted to the substrate connection leaving a larger negatively charged ions behind i.e. the depletion region becomes wider as shown in figure below.



As we know that the threshold voltage is a function of the total charge in the depletion region (i.e., Q_{dep}). Thus as the body voltage V_B drops then depletion charge (Q_{dep}) increases which increases the threshold voltage (V_{TH}). This effect is called as the body effect or back gate effect.

When the body bias voltage V_{SB} is applied between source and body the surface potential required for strong inversion is increased and becomes $|2\phi_F + V_{SB}|$. The charge stored in the depletion region can now be expressed as :

$$Q_{dep} = \sqrt{2qN_A\epsilon_s|1 - 2\phi_F|/C_{ox}} \text{ (Volts)}$$

From the preceding discussions it is clear that V_{SB} has an impact on the threshold voltage.

Thus the threshold voltage with body bias can be expressed as :

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{1 - 2\phi_F} + V_{SB} \right) - \sqrt{1 - 2\phi_F} \quad \left(\gamma = \frac{\sqrt{2qN_A\epsilon_s}}{C_{ox}} \right)$$

Where V_{TH0} is given by equation discussed in above section
 γ = is the body effect coefficient.

* Biassing Styles:

Types of Biassing:

- Biassing by fixing V_{GS}
- Biassing by fixing V_G and connecting a Resistance in the source.
- Biassing Using a Drain-to-Gate feedback Resistor.
- Biassing Using a Constant - Current Source.

→ Biassing by fixing V_{GS} :

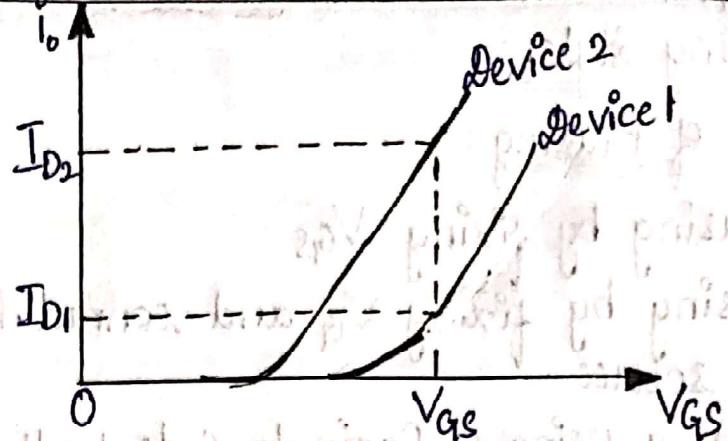
- The most common approach to biassing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required to provide the desired I_D .
- This Voltage is derived from the power supply voltage V_{DD} through the use of an appropriate voltage divider.
- Independent of how the voltage V_{GS} may be generated, this is not a good approach to biassing a MOSFET.

Because we know that,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

And the threshold voltage V_t , the oxide-capacitance C_{ox} , and transistor aspect ratio W/L vary widely among devices of same size and type.

- Biassing by fixing V_{GS} is not a good technique.
- Figure two I_D - V_{GS} characteristic curves representing extreme values in a batch of MOSFETs of the same type.
- For the fixed value of V_{GS} , the resultant spread in the values of the drain current can be substantial.



→ Biasing by fixing V_G and connecting a Resistance in the source:

- An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G , and connecting a resistance in the source lead, as shown in figure.

We can write,

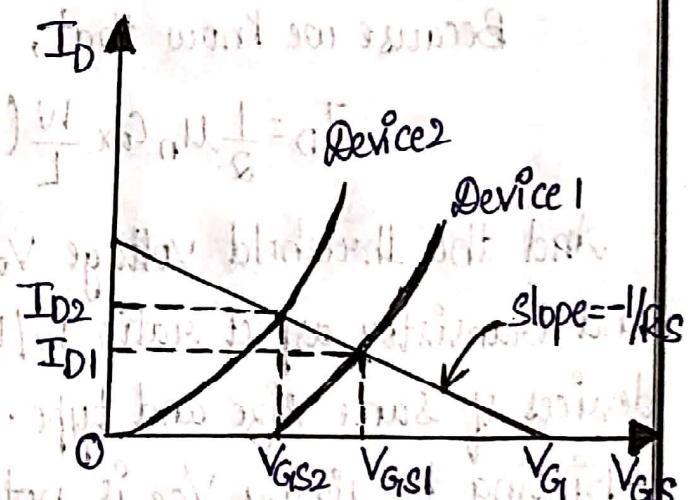
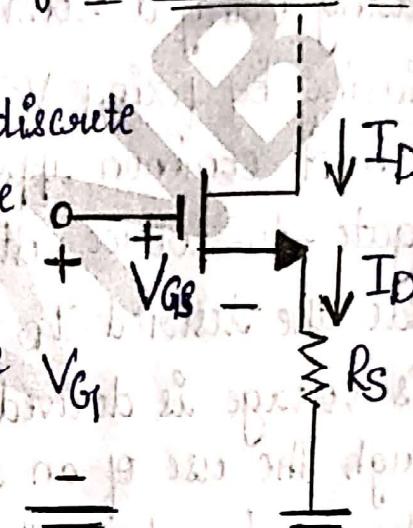
$$V_G = V_{GS} + R_S I_D$$

- If $V_G \gg V_{GS}$, I_D will be determined by the values of V_G and R_S .

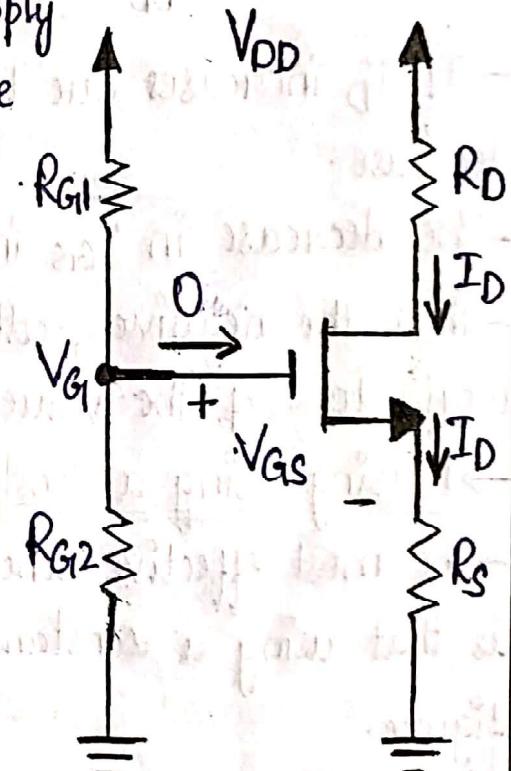
- If $V_G > V_{GS}$, resistor R_S provides negative feedback, which will stabilize the value of the bias current I_D .

- From equation, when I_D increases and V_G is constant, V_{GS} will decrease which will further decrease I_D .

- Thus the R_S works to keep I_D as constant as possible.



- This negative feedback action of R_s gives it the name degeneration resistance.
- Figure shows the $i_D - V_{GS}$ characteristics for two devices that represent the extremes of a batch of MOSFETs.
- A straight line that represents the constraint imposed by the bias circuit - namely.
- The intersection of this straight line with the $i_D - V_{GS}$ characteristic curve provides the coordinates (I_D and V_{GS}) of the bias point.
- In this case, the variability obtained in I_D is much smaller. Also, note that the variability decreases as V_G and R_s are made larger.
- Practical implementation using a single supply:
- The circuit utilizes one power-supply V_{DD} and derives V_G through a voltage divider (R_{G1}, R_{G2}).
- Since $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (in the MΩ range), allowing the MOSFET to present a large input resistance to a signal source.



→ Biasing Using a Drain-to-Gate feedback Resistor:

- A simple and effective biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in figure.

- Here the large feedback resistance R_G (Usually in the $M\Omega$ range) forces the dc voltage at the gate to be equal to that at the drain (because $I_{G_s}=0$).

Thus we can write

$$V_{G_s} = V_{D_s} = V_{DD} - R_D I_D$$

which can be rewritten in the form

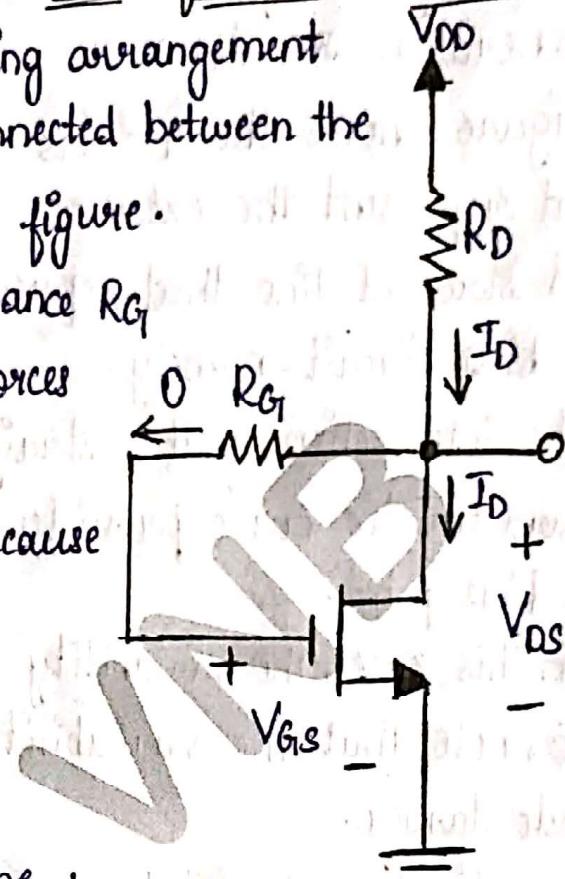
$$V_{DD} = V_{G_s} + R_D I_D$$

- If I_D increases due to any reason, then V_{G_s} must decrease.
- The decrease in V_{G_s} in turn causes a decrease in I_D .
- Thus the negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.

→ Biasing Using a Constant-Current Source:

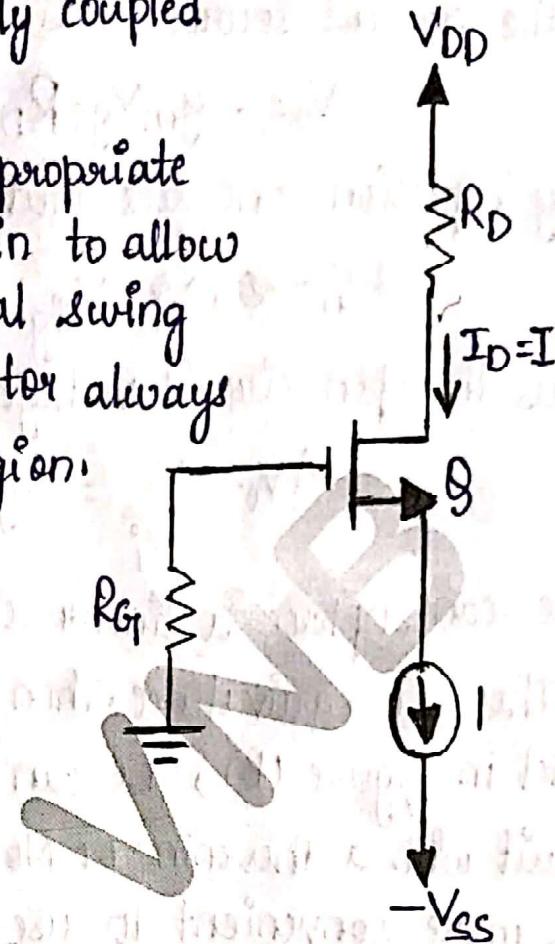
- The most effective scheme for biasing a MOSFET amplifier is that using a constant-current source, as shown in figure.

- Here R_G (Usually in $M\Omega$ range) establishes a dc ground at the gate and presents a large resistance to an input signal



Source that can be capacitively coupled to the gate.

Resistor R_D establishes an appropriate dc voltage at the drain to allow for the required output signal swing while ensuring that the transistor always remains in the saturation region.



* Common-Source (CS) Amplifier:

The common-source (CS) amplifier for MOSFET is the analogue of the common-emitter amplifier for BJT. Its popularity arises from its high gain, and that by cascading a number of them, larger amplification of the signal can be achieved.

Characteristic parameters of the CS amplifier:

Figure (a) shows the small-signal model for the common-source amplifier. Here, R_D is considered part of the amplifier and is the resistance that one measures between the drain and the ground. The small-signal model can be replaced by its hybrid- π model as shown in figure (b). Then the current induced in the output port is $i = -g_m V_{GS}$ as indicated.

by the current source. Thus

$$V_o = -g_m V_{gs} R_D$$

By inspection, one sees that

$$R_{in} = \infty, V_i^o = V_{sig}, V_{gs} = V_i^o$$

Thus the open-circuit voltage gain is

$$A V_o = \frac{V_o}{V_i^o} = -g_m R_D$$

~~One can replace a linear circuit driven by a source by its Thevenin equivalence. Then from the equivalent-circuit model in figure (b), one can replace the output part of the circuit with a Thevenin or Norton equivalence. In this case, it is more convenient to use the Norton equivalence. To find the Norton equivalence resistance, one sets $V_i^o = 0$, which will make the current source an open circuit with zero current. And by the test-current method, the output resistance is~~

$$R_o = R_D$$

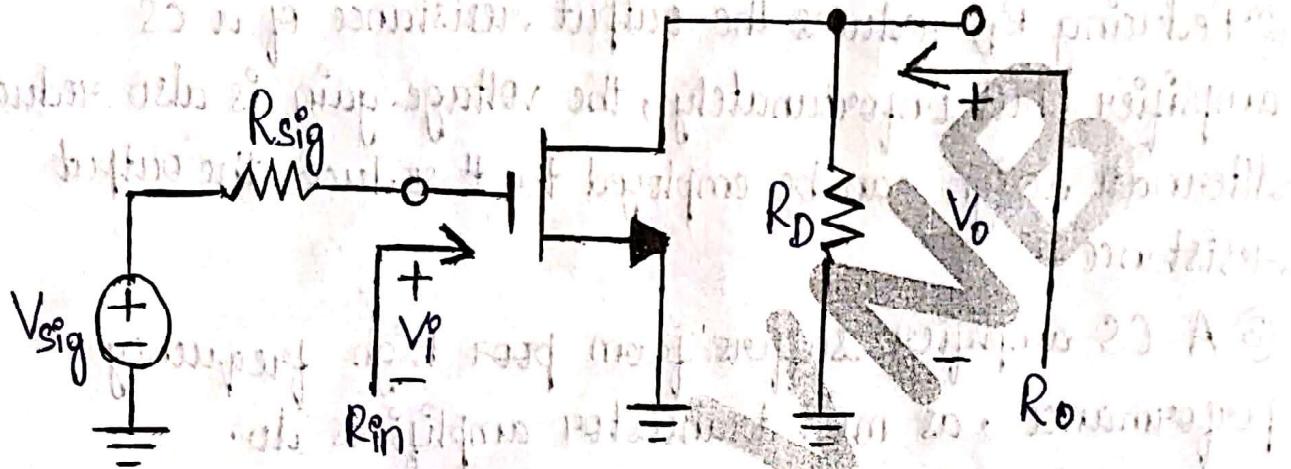
~~If now, a load resistor, R_L is connected to the output across R_D , then the voltage gain proper (also called terminal voltage gain), by the voltage divider formula, is~~

$$A_V = A V_o \cdot \frac{R_L}{R_L + R_o} = -g_m \frac{R_D R_L}{R_L + R_D} = -g_m (R_D || R_L)$$

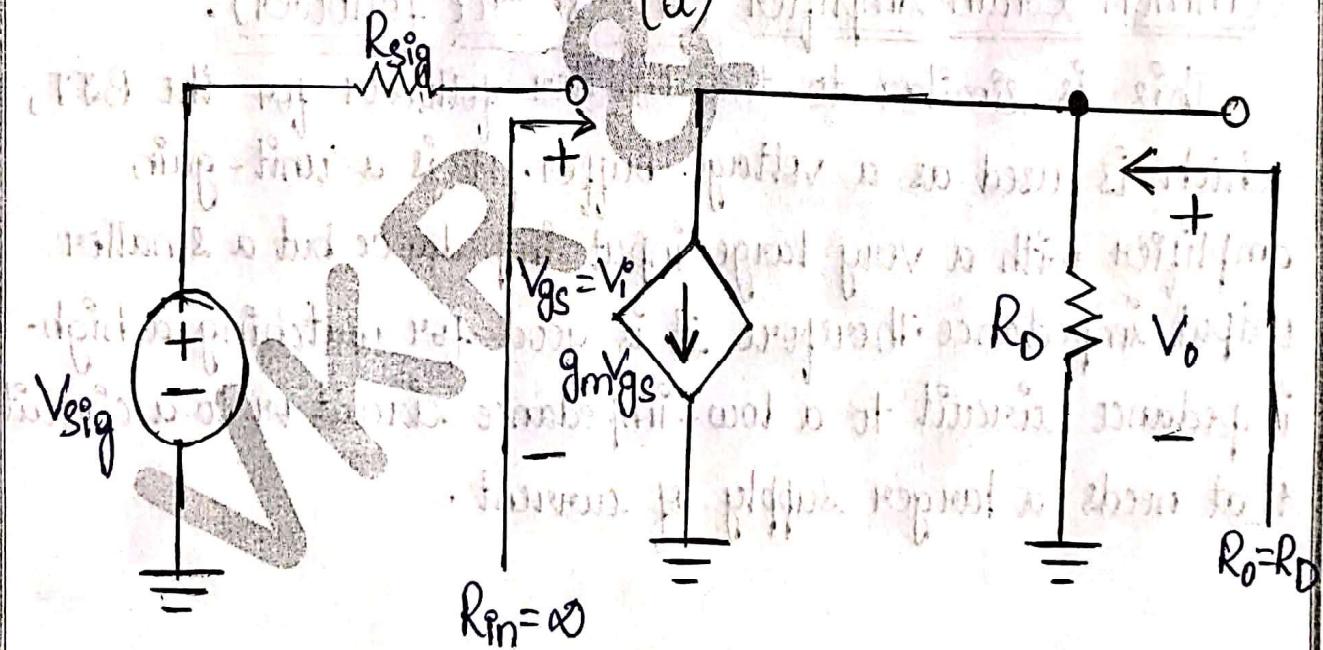
From the fact that $R_{in} = \infty$, then $V_i^o = V_{sig}$. The overall

Voltage gain, G_V , is the same as the voltage gain proper, A_V , namely

$$G_V = \frac{V_o}{V_{sig}} = -g_m (R_D / R_L)$$



(a)



(b)

Figure: (a) Small-signal model for a common-source amplifier. (b) The hybrid- Π model for the common-source amplifier.

Final Remarks on CS amplifier:

- ① The CS amplifiers has infinite input impedance (draws NO current at DC), and a moderately high output resistance (easier to match for maximum power transfer), and a high voltage gain (a desirable feature of an amplifier).
- ② Reducing R_D reduces the output resistance of a CS amplifier, but unfortunately, the voltage gain is also reduced. Alternate design can be employed to reduce the output resistance.
- ③ A CS amplifier suffers from poor high frequency performance, as most transistor amplifiers do.

* Common Drain Amplifier (The source follower):

This is similar to the emitter follower for the BJT, which is used as a voltage buffer. It is a unit-gain amplifier with a very large input impedance but a smaller output impedance. Therefore it is good for matching a high-impedance circuit to a low-impedance circuit or to a circuit that needs a larger supply of current.

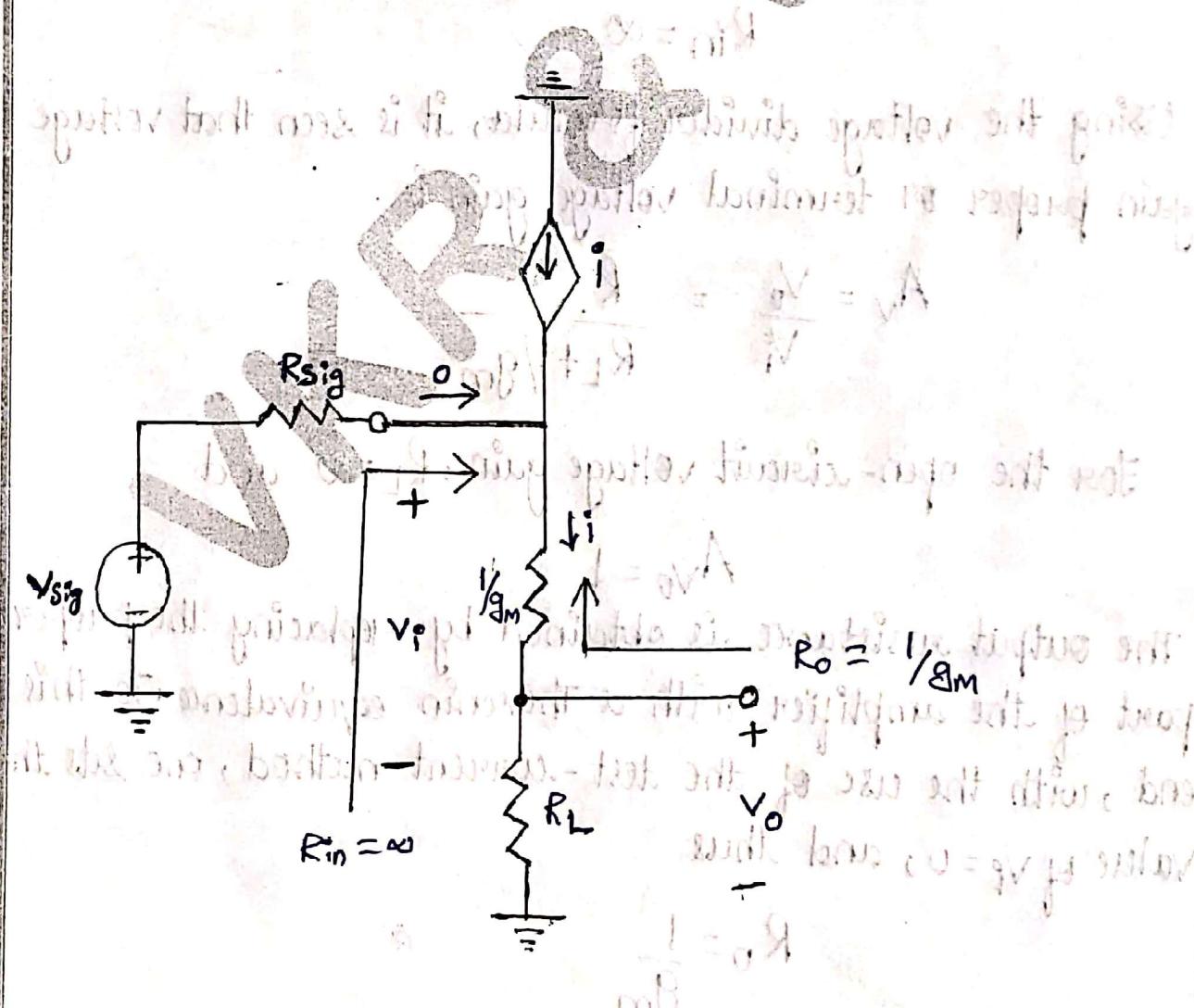
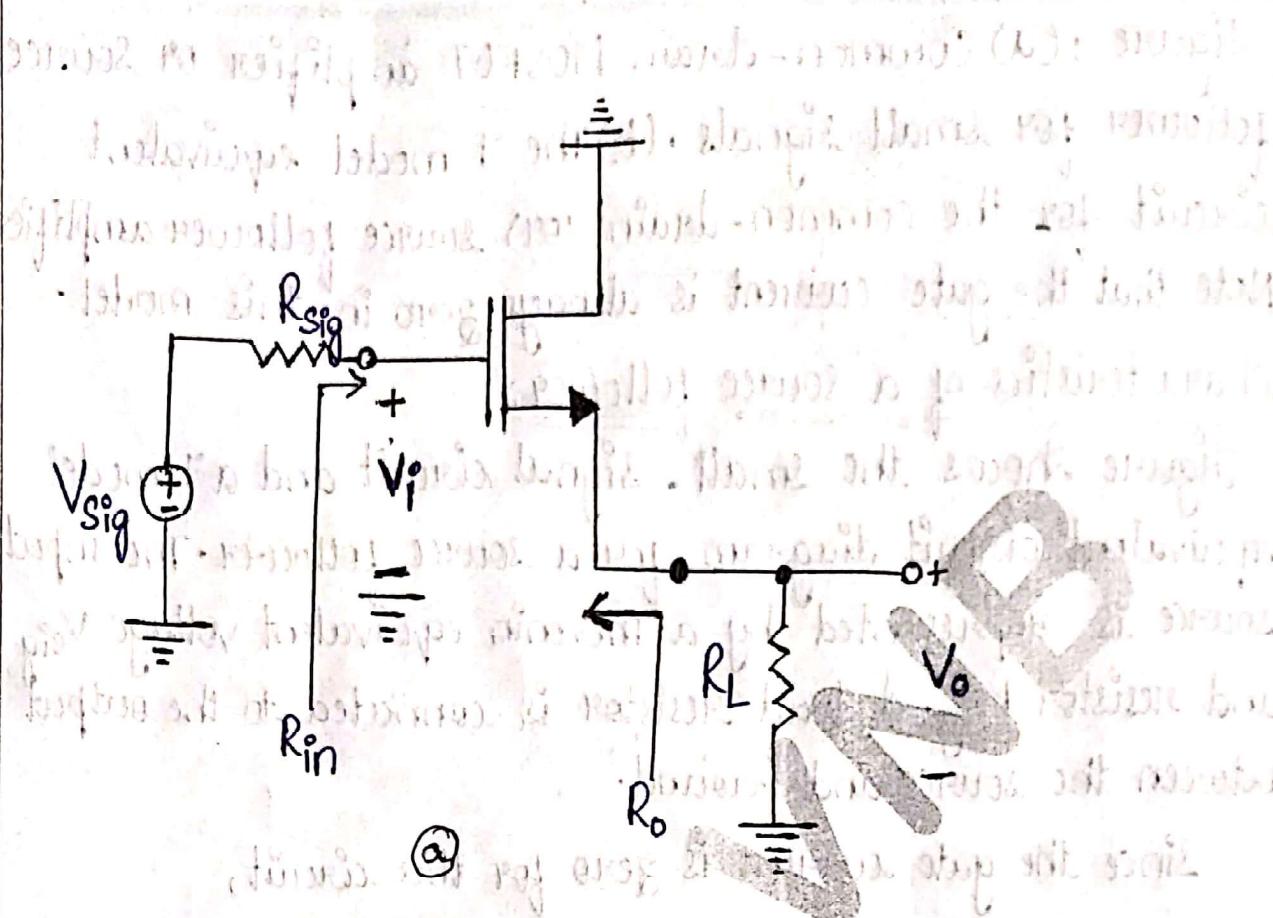


figure : (a) Common-drain MOSFET amplifier or source follower for small signals . (b) The T model equivalent circuit for the common-drain (or) source follower amplifier . Note that the gate current is always zero in this model .

Characteristics of a source follower :

Figure shows the small - signal circuit and a T-model equivalent circuit diagram for a source follower . The input source is represented by a Thevenin equivalent voltage V_{sig} and resistor R_{sig} . A load resistor is connected to the output between the source and ground .

Since the gate current is zero for this circuit ,

$$R_{\text{in}} = \infty$$

Using the voltage divider formula , it is seen that voltage gain proper or terminal voltage gain is .

$$A_V = \frac{V_o}{V_i} = \frac{R_L}{R_L + 1/g_m}$$

For the open-circuit voltage gain , $R_L = \infty$ and

$$A_{V0} = 1$$

The output resistance is obtained by replacing the proper part of the amplifier with a Thevenin equivalence . To this end , with the use of the test-current-method , one sets the value of $V_i = 0$, and thus

$$R_o = \frac{1}{g_m}$$

Because of the infinite input impedance R_{in} , then $v_i = v_{sig}$, and the overall voltage gain G_V (also called the total voltage gain) is the same as the voltage gain proper A_V (also called terminal voltage gain).

$$G_V = A_V = \frac{R_L}{R_L + 1/g_m}$$

Since $1/g_m$ is typically small, with large R_L , the gain is less than unity, but is close to unity. Hence, this is a source follower, because the source voltage follows the input voltage, but yet, it can provide a larger current to the output than the input current.

* Common Gate Amplifier:

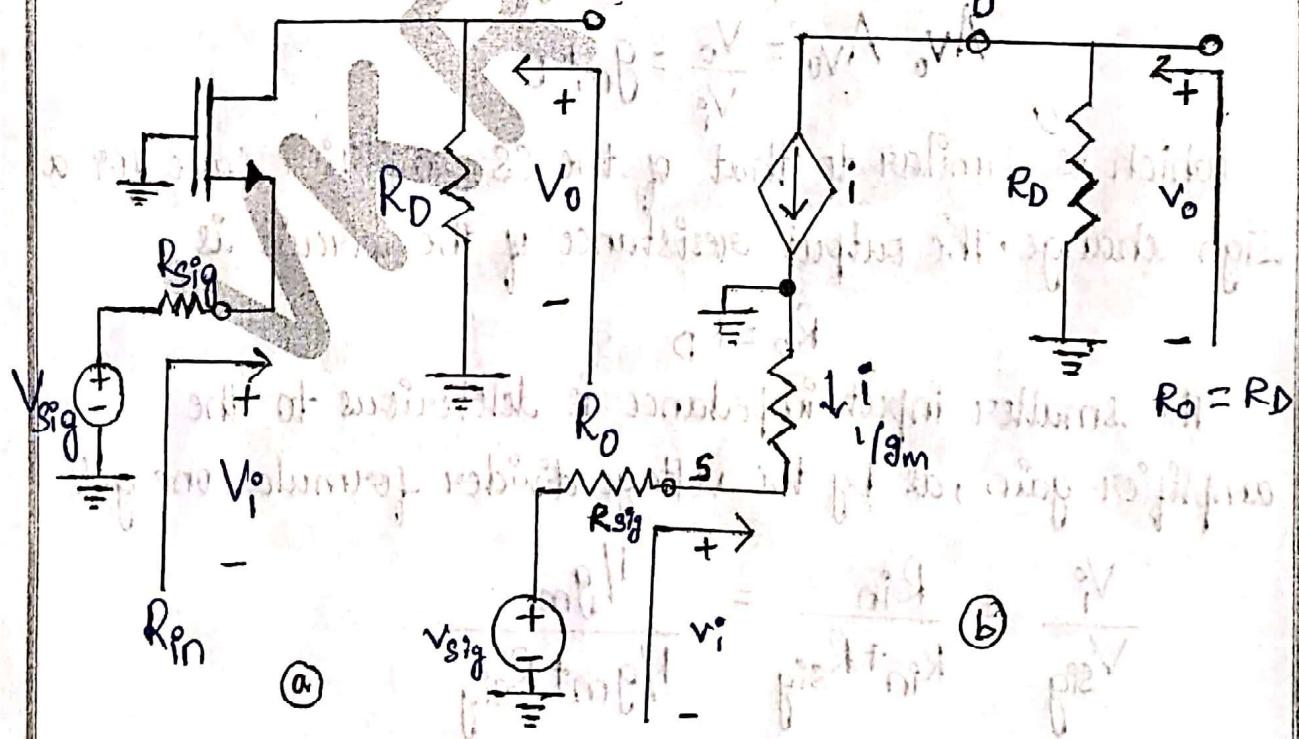


Figure: (a) Small-signal model for a common-gate amplifier. (b) The T model equivalent circuit for the common-gate amplifier. Note that the gate current is always zero in the T model.

The small-signal and a T-model equivalent-circuit common-gate (CG) amplifier is shown in figure. By inspection, the input resistance R_{in} is given by

$$R_{in} = \frac{1}{g_m}$$

which is typically a few hundred ohms, a low input impedance. The output voltage is

$$V_o = -i R_D, \text{ where } i = -\frac{V_i}{1/g_m} = -g_m V_i$$

Hence the open-circuit voltage gain is

$$A_{vo} = \frac{V_o}{V_i} = g_m R_D$$

which is similar to that of the CS amplifier save for a sign change. The output resistance of the circuit is

$$R_o = R_D$$

The smaller input impedance is deleterious to the amplifier gain, as by the voltage divider formula, one gets

$$\frac{V_i}{V_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{1/g_m}{1/g_m + R_{sig}}$$

meaning that the V_i is attenuated compared to V_{sig} , since

R_{sig} is typically larger than $1/g_m$:

When a load resistor R_L is connected to the output, the voltage gain proper is then

$$A_v = g_m R_D \parallel R_L$$

Thus the overall voltage gain is

$$G_V = \frac{1/g_m}{R_{sig} + 1/g_m} g_m (R_D \parallel R_L) = \frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$$

As the input impedance is low, it is good for matching sources with a low input impedance due to the maximum power theorem, but it draws more current, implying high power consumption from the signal source.

Summary of the CG amplifier:

- ① The CG amplifier has a low ~~but~~ input resistance $1/g_m$. This is undesirable as it will draw large current when driven by a voltage input.
- ② The voltage gain of the CG amplifier can be made similar in magnitude to that of the CS amplifier if $R_D \parallel R_L$ can be made large compared to $R_{sig} + 1/g_m$.
- ③ The output resistance can be made large since $R_o = R_D$.
- ④ The CG amplifier has good high frequency performance as shall be shown later.

* Current Sources and Sinks:

Current sources and current sinks form one of the most important components in analog circuits. When a source of current flows from the highest positive potential (V_{DD}) into a load it is designated a current source while when the source of current flows from the load to the ground, it is designated a current sink. A schematic of a current source and a current sink is shown in figure.

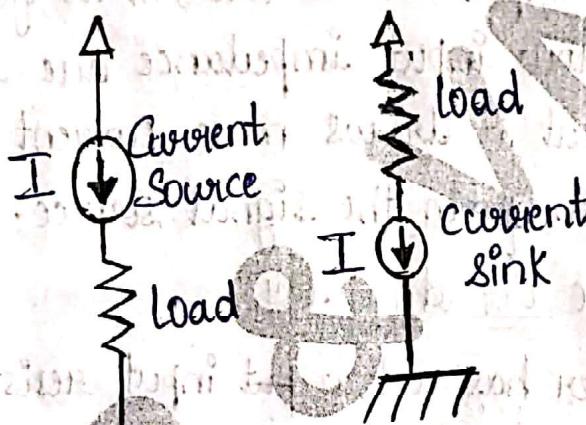
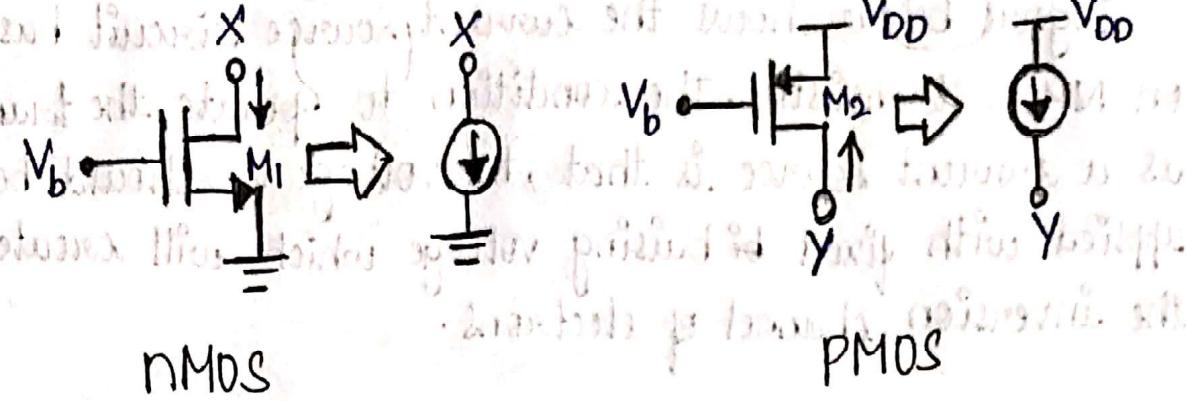


Figure Definition of Current Source and Sink.

A MOSFET behaves as a current source when it is operating in the saturation region. An NMOSFET NMOSFET draws current current from a point to ground ("sink current"), whereas a PMOSFET draws current from V_{DD} to a point ("source current").

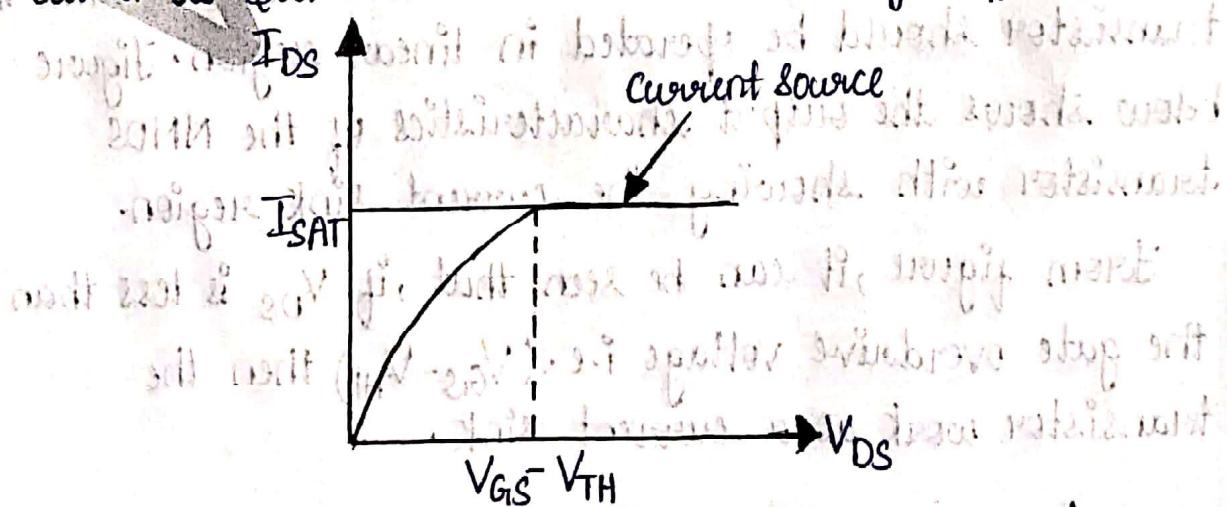


Current sources:

In order to use the MOSFET as a current source, we will have to operate it in saturation region.

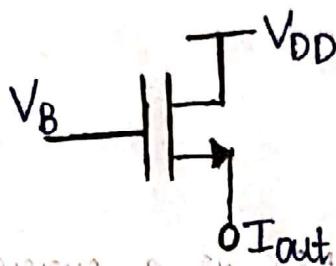
According to the output characteristics of the MOSFET, the current in the saturation region is constant. Therefore if we operate the MOSFET in saturation region it will work as a current source.

From figure it can be seen that, if V_{DS} is greater than the gate overdrive voltage i.e. $(V_{GS} - V_{TH})$ then the drain current flowing through the device is constant. This current is called as saturation current denoted by I_{SAT} .



Output characteristics of NMOS transistors as current source

Figure below shows the current source circuit based on NMOS transistor. The condition to operate the transistor as a current source is that, the voltage V_B should be applied with fixed biasing voltage which will create the inversion channel of electrons.



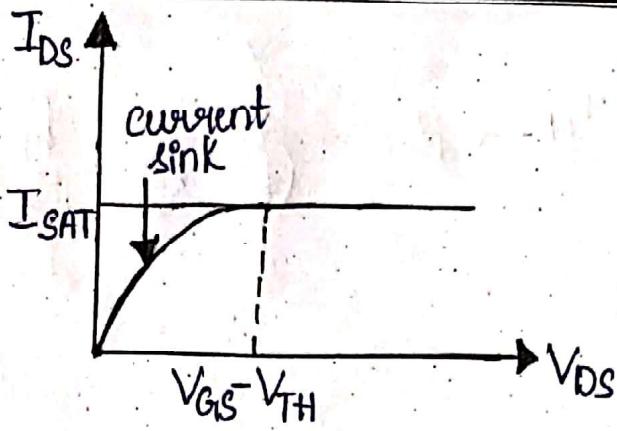
NMOS current source

Once the inversion is created then the current will flow through the device and will act as a current source when V_{DD} is greater than the gate overdrive voltage. The important application of current source is it can work as a load resistor in amplifier circuits with larger load resistance value.

Current sink:

In order to work the transistor as a current sink the transistor should be operated in linear region. Figure below shows the output characteristics of the NMOS transistor with showing the current sink region.

From figure, it can be seen that, if V_{DS} is less than the gate overdrive voltage i.e. $(V_{GS} - V_{TH})$ then the transistor work as a current sink.



Output characteristics of NMOS transistor as current sink.

Figure shows the current sink circuit based on NMOS transistor. The condition to operate the transistor as a current sink is that, the voltage V_B should be applied with fixed biasing voltage and the drain voltage applied to the transistor should be less than the gate overdrive voltage ($V_{GS} - V_{TH}$):

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Modeling of Transistor (or) MOSFET Modeling

The device models describe the terminal behavior of a device in terms of current-voltage (I-V), capacitance-voltage (C-V) characteristics, and the carrier transport process which takes place within the device. These models thus reflect device behavior in all regions of operation of the device. It is convenient to divide these models into two categories: (1) physical device models, and (2) equivalent circuit models. Physical device models are based on a careful definition of device geometry, doping profile, carrier transport equations (*semiconductor equations*) and material characteristics. These models can be used to predict both terminal characteristics and transport phenomenon. Modern MOS VLSI devices, due to their small size (micron and submicron), require two- or three-dimensional solutions of the coupled semiconductor equations which can be solved only by numerical methods. These so called numerical *device simulators* provide detailed insight into the physical aspect of device operation and can predict the characteristics of new devices. For this reason they are mostly used to study device physics and device design. Several public domain and commercial software packages are now available for device analysis and simulation; the most well known among them are MINIMOS, PISCES, FIELDAY, CADDETH. Since device simulators are computationally intensive and require large amount of computer memory, they are not suitable for circuit simulation.

Due to the 2-D and 3-D nature of the physical effects governing electrical behavior of VLSI MOS transistors, it is very difficult to obtain a closed form analytical formulation which is valid in all operating regions of interest. However, *one can still obtain closed form analytical models, based on device physics, that are generally valid only over a limited region of device operation*. Despite this limitation, such models are frequently used for circuit simulators because of ease of computation.

Equivalent circuit models describe electrical properties of the device by connecting electrical circuit elements in such a way that the model emulates the electrical terminal behavior of the device. These models are thus based on the device characteristics; the circuit elements of this model are derived either from closed form analytical function or using an empirical approach. These models are often used in circuit simulators to represent device characteristics because of the ease of evaluation; the circuit simulator SPICE exclusively uses equivalent circuit models. For semiconductor devices the equivalent circuit model elements are highly nonlinear and element values are strongly dependent on DC bias, frequency, signal level and temperature.

Therefore, in addition to having separate DC and AC circuit models, it is generally necessary to distinguish between the small-signal and large-signal (transient) models. Thus in general we require three types of circuit models—DC, transient and AC—corresponding to three basic types of circuit analysis:

- A DC model is a *static model* that evaluates the device current for a fixed voltage, not varying with time. Thus in a DC model dynamic effects such as time delay arising from the presence of energy-storage elements (capacitors and inductors) are ignored. This model is used to calculate quiescent operating points of a circuit.²
- A transient model is a *large-signal dynamic model* which evaluates the device current when the applied voltage is varying with time. It is called a large-signal model because no restrictions are placed on the magnitude of the applied voltage. This model is required for the time domain analysis. In this case current is the sum of both DC and transient currents arising from the charging or discharging of device storage elements, usually capacitances.
- An AC model is a *small-signal model* which evaluates the current when the variation in the applied voltage is so small that the resulting small current variations can be expressed using linear relations. The small-signal linear model can usually be obtained very easily and systematically from the DC model of the device. Since AC model is used for the frequency-domain analysis, it should take into account energy-storage elements and the frequency dependent effects of the transistor.

The MOSFET model we will be concerned with contains only capacitances as the storage elements and not the inductors. The latter are important only at very high frequencies (GHz range). For the transistor model to be used in a circuit simulator, the following requirements should be satisfied:

- The model should be *accurate* so that it simulates actual transistor behavior over all regions of operation of interest. An accuracy of about 5% between the experimental device current (and capacitances) and the model is generally sufficient for circuit modeling work.
- During transient analysis, calculation of transistor current is carried out thousands of time, therefore, it is imperative that the model be both *computationally efficient*, and accurate. Thus, the model needs not only to be accurate but *simple* too; there is always a trade-off between accuracy and simplicity.
- In order to avoid any nonconvergence problems in the simulator, the

² The points (nodal voltages and branch currents) about which the circuit operates are termed *quiescent points* (Q-points) or *bias points*. Accurate Q-points are critical for the design and simulation of transient and AC response.

mathematical equations representing the device model must be continuous, with continuous first derivatives (which are required by the Newton–Raphson algorithm), although not necessarily in a strict mathematical sense. The degree of discontinuity, if present, must be so small that the resulting errors can be absorbed by the overall simulation program error tolerances.

- In MOS VLSI circuit design devices of different lengths and widths are used, therefore, it is desirable that a single model should fit all device sizes used in actual design practice.

Clearly, any choice of the model must be based on compromises between the accuracy of the model in predicting device characteristics over the operating range of interest and the computational efficiency of simulating large circuits. As the size and the complexity of modern circuits increases, the choice of appropriate models becomes more critical. For this reason a hierarchy of models of different levels of accuracy are normally available in a circuit simulator so that designers can choose a model best suited to their potential application. For example, Berkeley SPICE has four different levels of MOSFET models. The combined requirements of computational efficiency and available memory restrict the device models for circuit simulators into the following three categories.

Analytical Models. There are basically two types of analytical models where model equations are directly derived from device physics. One type of model is based on surface potential analysis, often called *charge sheet models*. These models are inherently continuous in all regions of operation of the device. The current can be accurately determined using these models, but the equations themselves are complex, involving transcendental expressions, and often require iterations just to compute the surface potential for a given bias condition. They are thus not very suitable for VLSI circuit simulation, although recently they have been used for simulation of small circuits. The second type of analytical model is the result of applying various approximations to the semiconductor equations, based upon decisions as to which physical phenomena dominate. Thus, different equations are required to represent different regions of operation of the device. Such models represent first order device behavior fairly accurately, and higher order effects are normally accounted for through the introduction of physical and empirical parameters. These models are usually referred to as *semi-empirical analytical models*. *Practically all the models used in today's circuit simulators fall into this category, and range from simple to more complex models.* These are the type of models which are covered in this book. The advantage of these models are that they do describe the relationship between the physical process and geometry structure on the one hand and

electrical behavior on the other, so that with some minor changes in the process, electrical behavior can still be predicted. However, the disadvantage is that they are technology dependent and takes considerable time to develop the model. Furthermore, effects resulting from new device structures often require minor or major modification of the existing model and may even require a new model.

Table Lookup Model. In a table lookup model the device current data are stored for different bias points and device geometries in a tabular form. Generally some sort of interpolation scheme is used to obtain the current values which are not stored. This data base is collected from experimental devices or generated from device level simulators like MINIMOS/PISCES. In another approach, instead of directly storing the device current I_{ds} , the coefficient of some mathematical functions like cubic splines are precalculated from original I_{ds} data for different bias and geometry. It is the coefficients of this function which are then stored in a tabular form, and are later used to compute the currents and conductances required by the simulator. This approach increases model evaluation speed and reduces storage. *These types of models have the advantage that they are technology independent and can be developed in a shorter time compared to physical models.* The disadvantage of this approach is that it gives no physical insight into device behavior. The model validity outside the data range is uncertain, and if accuracy is required storage is still a problem.

It should be pointed out that table lookup models are generally used for device DC models. For transient and AC models, we still use analytical models because the charges associated with different device terminals are difficult to measure. The charges can be calculated from terminal capacitances, but even the capacitance measurements for VLSI devices are difficult to carryout. We will not cover the table lookup model and the interested reader should look into the references cited.

Empirical Model. In an empirical model, the model equations representing device characteristics are purely of the curve fitting type and are thus not based on device physics. The only advantage of this type of model is that it requires small data storage as compared to table look models and model development time is shorter compared to other modeling approaches. The disadvantage is that this approach is not technology independent. *Purely empirical models are seldom used in circuit simulators,* although empirical (or curve fitting) parameters are often included in physical models to describe 2 or 3-D device behavior.