

* UNIT - 4 *

* Memory Organization :

Memory organization consists of

i, Basic Term of memory.

ii, Basic memory operation.

i) Basic Term of memory :

The basic term regarding the memory are given below

Memory :

Memory is the portion of a system for storing binary data in large quantities. Semiconductor memories consists of arrays of storage elements that are generally either Latches (or) Capacitor units of binary data:

1. The smallest unit of binary data is bit
2. 8 bit unit is called a byte.
3. The byte can be split into two 4-bit units called "nibble".
4. A complete unit of information is called "word", generally consists of one (or) more bytes.

Capacity :

Capacity of memory is defined as how many bits can be stored in a particular memory. Suppose that we have a memory which can store 1024×8 bits. This represents the total capacity of memory. When the capacity is expressed in this way, the first number (1024) is the number of words and the second number (8) is the number of bits per word.

Address :

Address is a number that identifies the location of a word in memory. Each word has a unique address in the memory system. For example a small memory consists of 16 words having a specific address by a 4-bit ($2^4 = 16$) number ranging from 0000 - 1111.

Read operation:

The binary data word reads the content in a memory location during the Read operation.

Write operation:

A binary data word is placed in a specific memory location during the write operation. It is also referred to as a store operation.

Volatile memory:

Any type of memory requires some power to store the binary information. All information are lost when the power is removed.

Non-volatile memory:

The contents of memory is not lost even when the power is removed from the memory. These types of memory are called non-volatile memory.

Random Access memory (RAM):

We can access the data randomly from any location of memory. This is known as random access memory. The access time of each content is same for all the locations and also it reduces the access time.

Read write memory:

A memory in which it is possible to read from or written into a specified location is called read-write memory.

Read only memory (Rom):

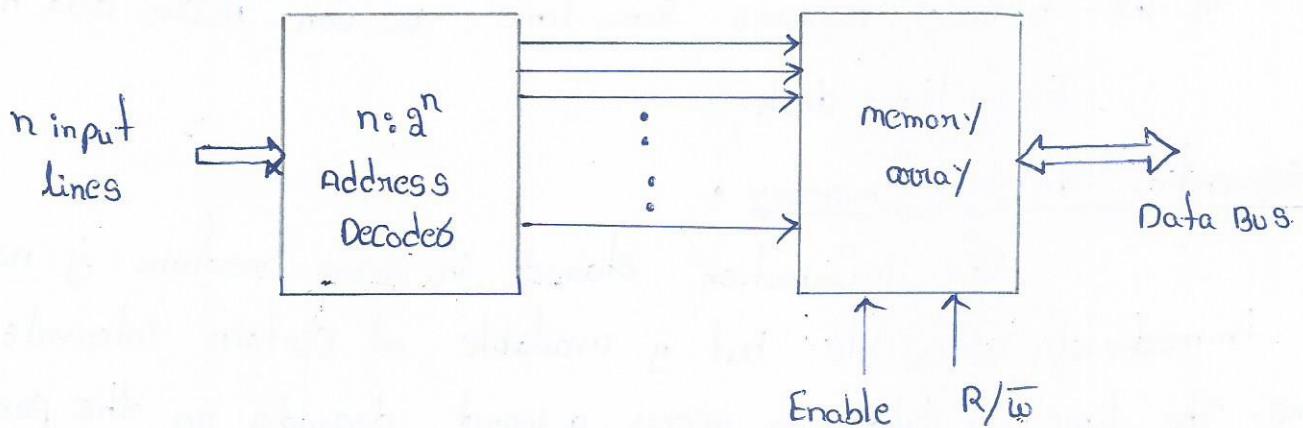
A memory that can be read only from a specific location in the memory.

ii) Basic memory operation:

Based on different types of memory, the internal memory operation is varied. Since memory stores the binary data, data must be placed into the memory and the data must be copied from the memory when data processing is required.

The write operation is to place the memory content into the specified location and the read operation is copying the content from specified location.

A memory to perform the read or write operation the block diagram is shown in fig ①. The data are read during a read operation and the data are stored during a write operation. A set of lines called "Bus" are used for read or write operations. An address is selected by placing a binary code representing the address bus. The address is on a set of lines, called address bus and address bus is the unidirectional bus. The number of address lines depends on the capacity of memory. The 6 bit address code can select (2^6) 64 locations.



Write operation: fig ①: Block diagram of Basic memory operation.

The following steps are followed to write contents in a memory. We can perform the write operation, when the R/W control input is low.

1. The address decoder decodes the address for specified location based on the given input of decoder.

- a. Data is placed on the data bus.
3. The data is written in the above specified location when the memory chip receives the write signal.

Read operation :

we can perform the read operation, when the R/W control input is HIGH.

1. Address decoder decodes a specified memory location based on the input of decoder.
2. The read command is sent to memory.
3. Contents of a specified location is placed on the data bus.

* Classification of Semiconductor memories :

In General the memory is classified in two types based on their mode of access of a memory system.

1. Random ACCESS memory
2. Sequential ACCESS memory.

1. Random ACCESS memory :

The word of data reading or writing from or to the memory requires same time. we can access data Randomly.

Ex: Hard disk.

2. Sequential ACCESS memory :

The information stored in some medium is not immediately accessible but is available at certain intervals of time. The time it takes to access a word depends on the position of the word with respect the reading head position : therefore the access time is variable.

Ex: magnetic tape.

Figure ① shows the classification of memory.

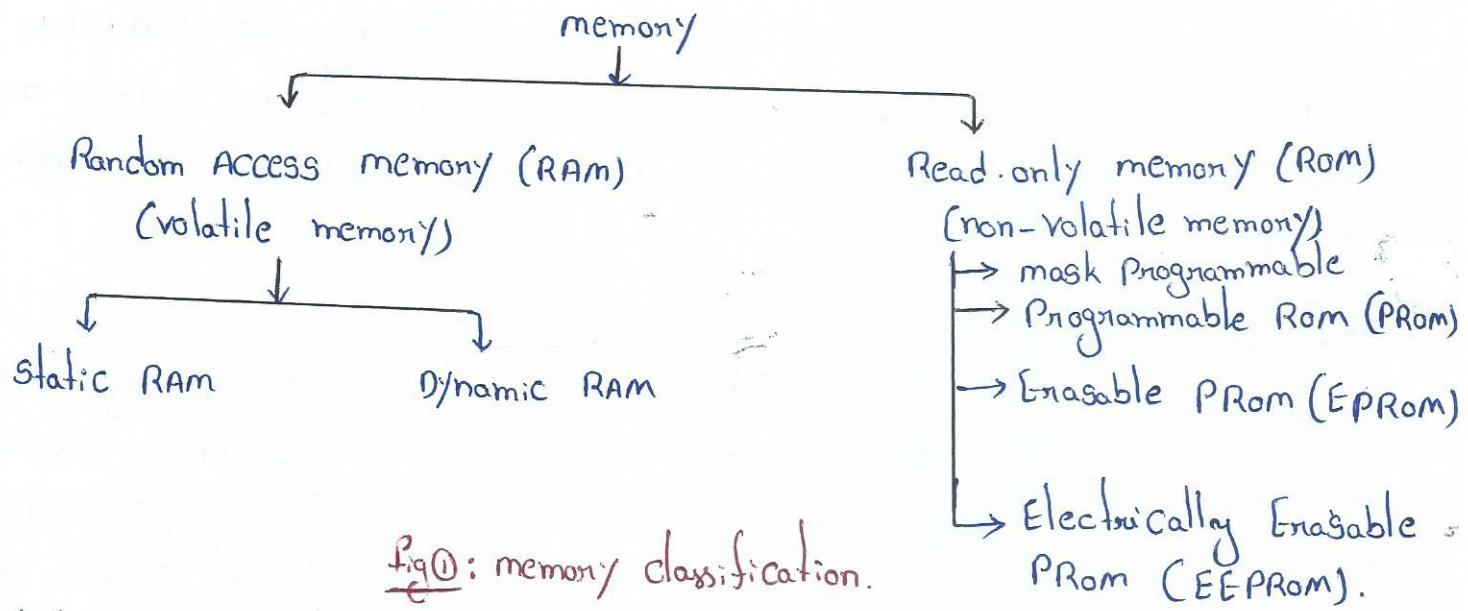


Fig ①: memory classification.

static RAM:

It consists of internal latches that store the binary information. The stored information remains valid as long as power is applied to the unit.

Dynamic RAM (DRAM):

The Dynamic RAM stores the binary information in the form of electric charge on capacitors. The capacitors are provided inside the chip by MOS transistors. The stored charge on the capacitors tends to discharge with time and the capacitors must be periodically recharge by refreshing the dynamic memory.

Classification of

* Read only memory (Rom):

It is a non-volatile memory, which retains the data even when power is removed from this memory. Programs and data that cannot be altered are stored in Rom. The required paths in a Rom may be programmed in four different ways.

1. mask Programming

2. Programmable Read only memory (PROM)

3. Erasable PROM (EPROM)

4. Electrically Erasable PROM (EEPROM)

5. Electronically Alterable Programmable Read-only memory (EAPROM)

1. mask Programming :

It is done by Company during the fabrication process of the unit. The procedure for fabricating a ROM requires that the customer fills out the truth table he wishes the ROM to satisfy.

2. Programmable Read only memory (PROM) :

PROM contain all the fuses intact giving all 1's in the bits of the stored words. The fuses in the PROM are blown by application of high voltage pulse to the device through a special pin. A blown fuse defines binary 0 state and an intact fuse give a binary 1 state. This allows the user to program the PROM by using a special instruments called PROM programmer.

3. Erasable PROM (EPROM) :

In a PROM or ROM pattern once fixed is permanent & can not be altered. Once bit pattern has been established, the unit must be discarded if the bit pattern is to be changed. The EPROM can be restructured to the initial state even though it has been programmed previously.

EPROM is placed under a special ultra-violet light for a given period of time, all the data are erased. After erased, the EPROM returns to its initial state and can be programmed to a new set of values.

4. Electrically Erasable PROM (EEPROM) :

It is similar to EPROM except that the previously programmed connections can be erased with an electrical signal instead of ultraviolet light. The advantage is that device can be erased without removing it from its socket.

5. Electronically Alterable PROM (EAPROM) :

EAPROM stands for Electronically Alterable Programmable Read-only memory. It is a type of PROM whose contents can be changed. It acts as a non-volatile storage device, and its individual bits can be re-programmed during the course of system operation.

* Read only memory (Rom) :

Rom is essentially a memory device in which permanent binary information is stored.

* The binary information must be specified by the designer and is embedded in the unit to form the required interconnections. Once the pattern is established, it stays with in the unit when power is turned off and on again. Hence, Rom is a non volatile memory.

* Programs and data which are stored in Rom cannot be altered.

* Rom can perform only the read operation. This means that suitable binary information is already stored inside memory and can be read at any time & can't be altered by writing.

Block diagram of Rom is shown in below figure.

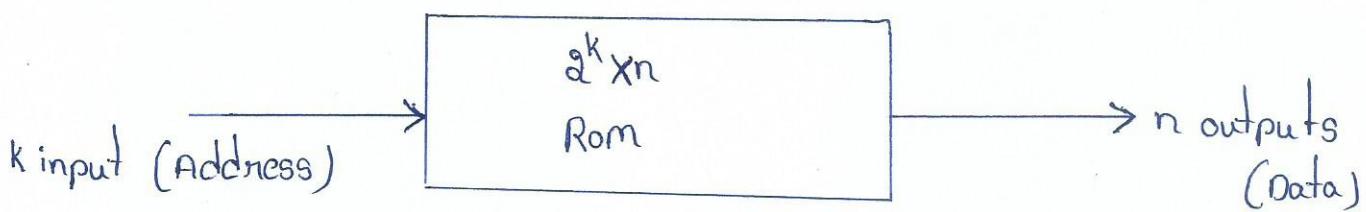


Fig: Rom Block diagram.

- ⇒ It contains of k inputs and n-outputs.
- ⇒ The Inputs provide the address for memory & the outputs give the data bits of the stored word that is selected by the address.
- ⇒ k address input lines are need to specify 2^k words.
- ⇒ Rom does not have data inputs, because it does not have a write data.

Types of Rom:

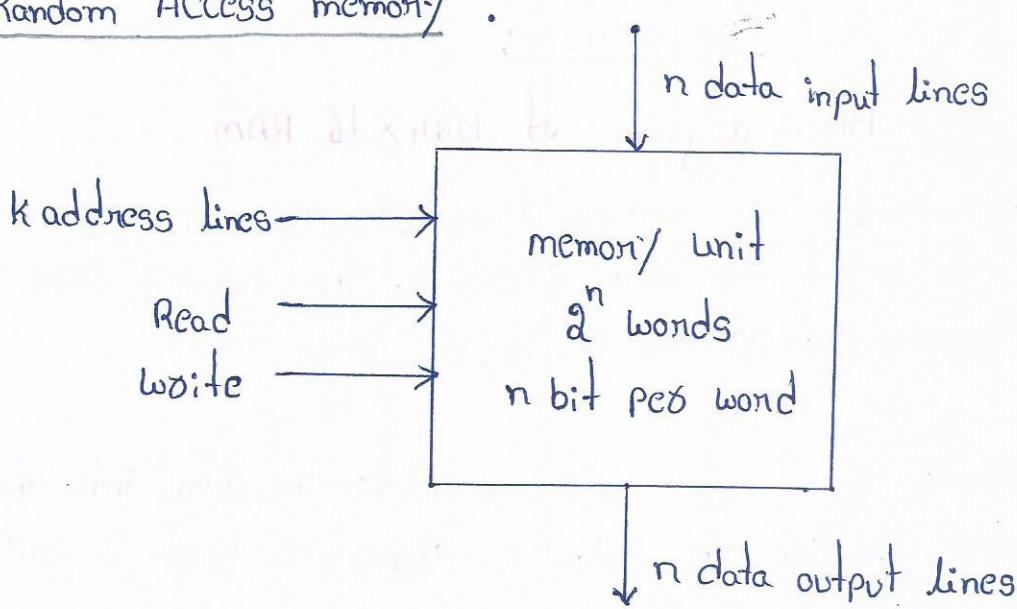
The process of entering information in a Rom is known as "Programming".

Depending upon Programming Process Employed, the Roms are Categorized as follows.

[Refer Back side]
(Types)

* RAM (Random Access memory) :

A memory unit is collection of storage cells together with associated circuits needed to transfer information in and out of the memory device. The time it takes to transfer information to or from any desired location is always same, Hence it is called as "Random Access memory".



fig①: Block diagram of RAM.

The Block diagram of memory unit is shown in fig①. The n data input lines provide the information to be stored in memory & the n data output lines supply the information out of the memory. The k-address lines specify the particular word chosen among the many available memory location.

The two Control Signals write & Read are used to transfer the data into the memory and the Read data from the memory.

The memory unit specified by the number of words it contains and the number of bits in each word. Address lines is used to select one particular word. Each word in memory is assigned an identification number called address, starting from 0 to 2^k, where k is the number bits in the address lines. Fig ② shows the block diagram of a 1024x16 memory.

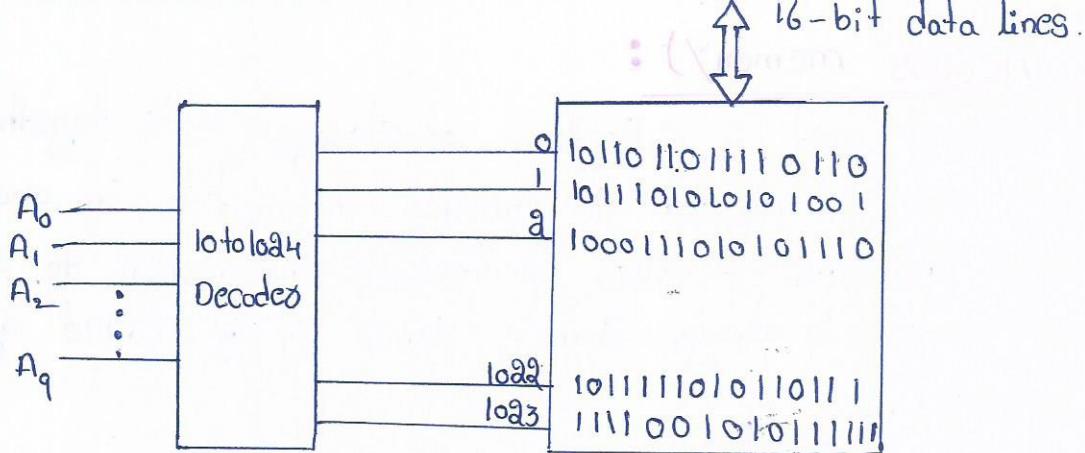


Fig ②: Block diagram of 1024×16 RAM

A decoder accepts the address lines ($A_9, A_8, \dots, A_1, A_0$) & provides the paths needed to select the word specified. The memory size varies from 1024 words requiring an address of $10 (2^{10})$ bits.

Write operation:

The write signal is used to write the data into the specified memory location. The following steps are used to write the data.

1. Apply the binary address of the desired word to the address lines.
2. Apply the data bits that must be stored in memory to the data input lines.
3. Activate the write input. The data is written in the specified memory location after activating the write signal.

Read operation:

The Read operation is the process of Reading data from the specified memory location. The following steps are used to read the data.

1. Apply the binary address of the desired word to the address lines.
2. Activate the read input. Now the required data is available in the data line.

The memory unit will then take the bits from the word that has been selected by the address and apply them to the o/p data lines. The Content of the selected word does not change after Reading.

The memory enable (on chip select) is used to select the particular memory chip in a multichip implementation of a large memory. When the memory enable is inactive, the memory chip is not selected and no operation is performed. When the memory enable i/p is active, the Read/write input determines the operation to be performed as shown in Table ①.

Table ①: Control i/p's of memory chip.

Enable	R/ \bar{W}	memory operation
0	X	none
1	0	write to selected word
1	1	Read from selected word

Timing waveform :

The operation of the memory unit is controlled by an external device such as Central processing unit (CPU). The CPU is synchronized by its own clock but the memory does not employ an internal clock. Instead, its Read & write operations are specified by clock cycle time of a memory is the time required to complete a write operation. The CPU must provide the memory control signal in such a way as to synchronize its internal operations with the Read & write operation of memory. This means that the access time & cycle time of the memory must be within a time equal to a fixed number of CPU clock cycles.

Write cycle :

Fig ③ shows the write cycle timing diagram for a CPU with 50MHz clock & a memory with 50ns maximum cycle time. Fig ③ write cycle requires three 25ns cycles T_1 , T_2 & T_3 . For a write operation, the CPU must provide the address & i/p data to the memory.

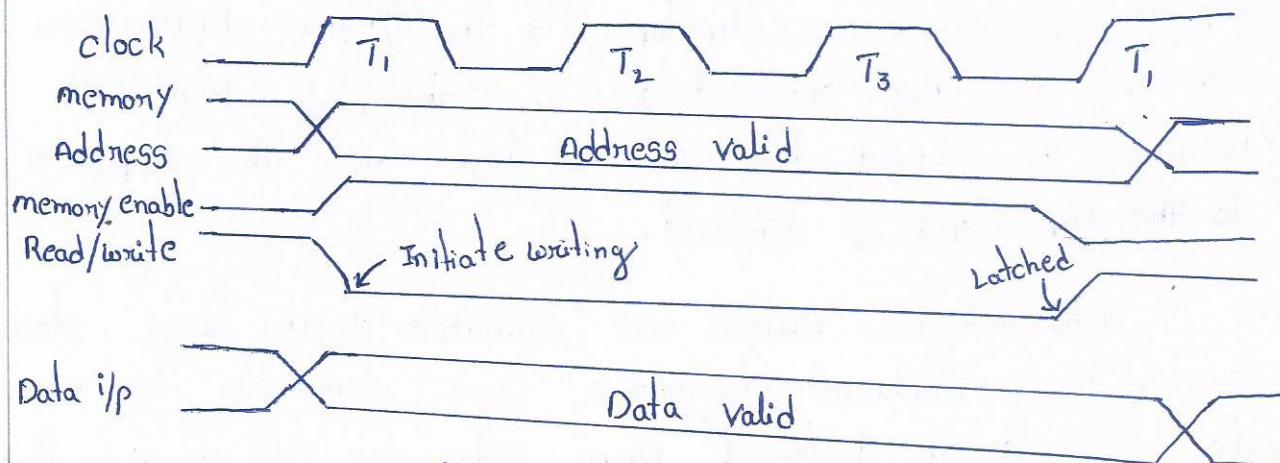


Fig ③: memory write cycle.

The memory enable signal changes to the high level & the Read/write signal goes to the low level to indicate a write operation. These two signals must be active for the period of 50ns. The address & data signals must remain stable for a short time after the control signals are deactivated. At the completion of the third clock cycle, the memory write operation is completed & the CPU can access the data from the corresponding memory location.

Read Cycle :

Fig ④ shows the Read cycle. In this operation the required address for the memory is provided by the CPU. The memory enable & Read/write must be in their high level of Read operation. The memory places the data of the word selected by the address into the output data lines within a 50 ns interval from the time that the memory enable is activated.

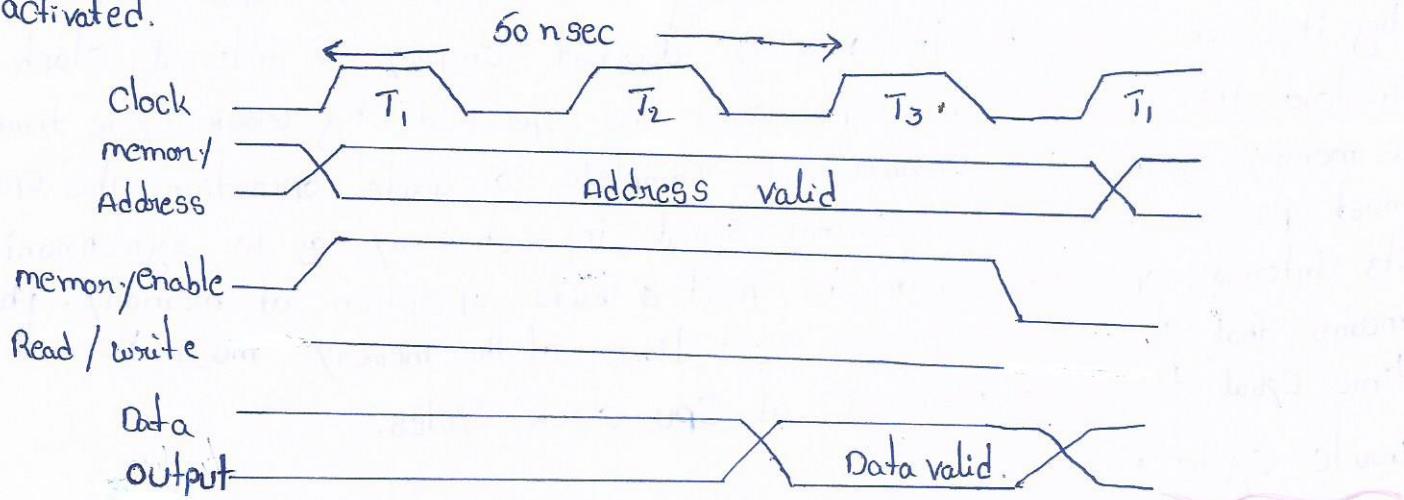


fig ④ : Read cycle.

Types of RAM:

Semiconductor RAMs may be static or dynamic. The static RAM employs bipolar or MOS flipflops, & the dynamic RAM uses MOSFETs & capacitors that store data. In either case, RAMs are volatile because the stored data will be lost once the DC power applied to the flip-flops is removed.

Semiconductor RAMs are available with large storage capacities & have replaced magnetic core memories in most of computer circuits. The different RAM categories are shown in Fig ①.

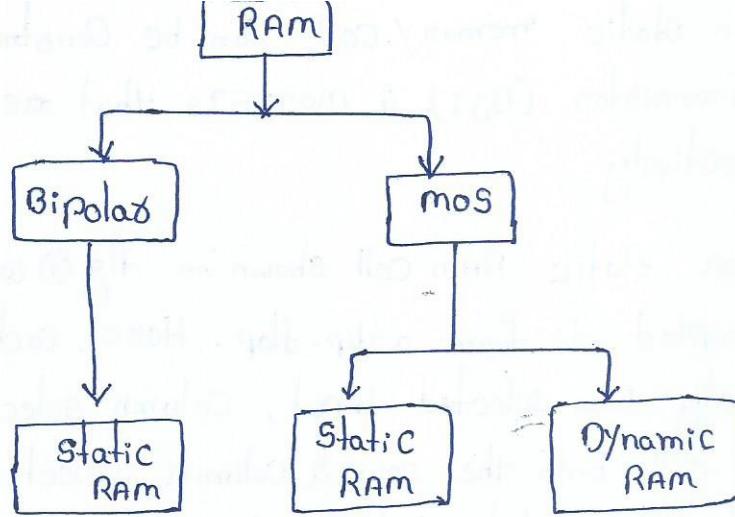


fig ① : The RAM family.

Static RAM :

A static RAM essentially contains an array of flip-flops, one for each stored bit. Data written into a flip-flop remains stored as long as d.c power is maintained. The memory capacity of a static RAM varies from 64 bits to 1 mega bit.

static RAM cell :

The logic diagram of a static RAM cell is shown in fig ②. The cell (or a group of cells) is selected by HIGH values on the Row & Column lines. The input data bit (1 or 0) is written into the cell by setting the flip-flop for a 1 & resulting the flip-flop for a 0 when the READ/WRITE line is Low (i.e., write). When the READ/WRITE line is HIGH, the flip-flop is unaffected. It means that the stored bit (data) is gated to the data out line.

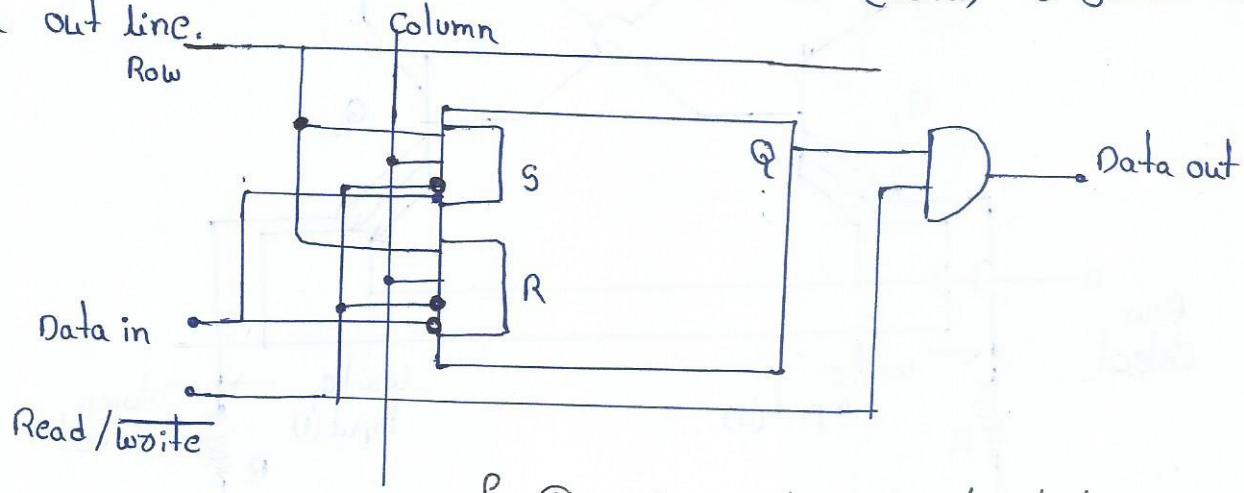
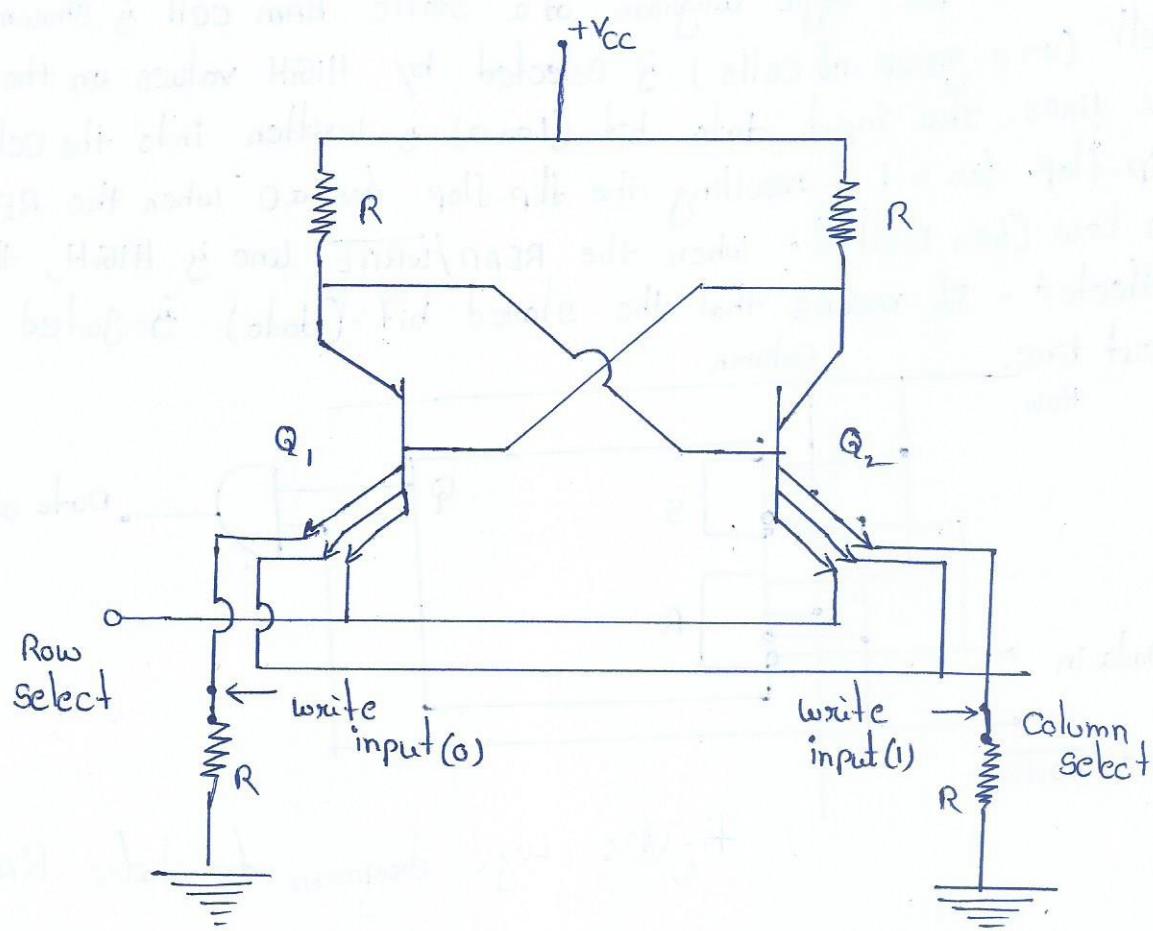


fig ② : Logic diagram of static RAM cell.

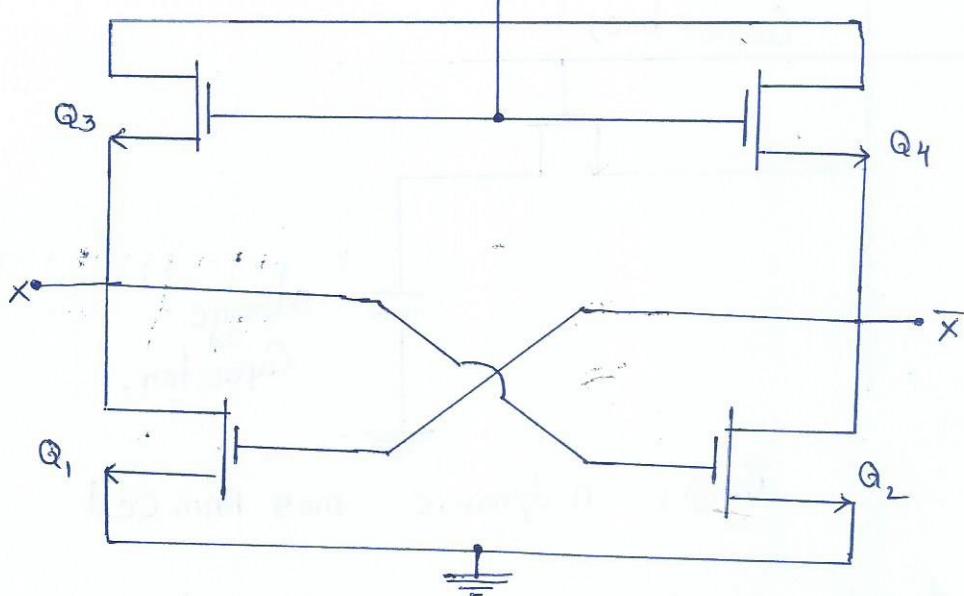
The flip-flop in static memory cell can be constructed using Bipolar Junction Transistor (BJT) & MOSFETs that are shown in fig ③(a) and (b) respectively.

In a bipolar static RAM cell shown in fig ③(a), two BJTs Q₁ & Q₂ are cross-coupled to form a flip-flop. Here, each transistor has three emitters, namely Row select input, Column select input, & write input. To select the cell, both the row & column select lines must be held HIGH. When selected, a data bit can be stored in the cell (write operation) or the content of the cell can be read (Read operation). If either row or column select lines is low, then the memory cell is disabled.

In a mos static RAM cell shown in Fig 3) (b), Q_1 & Q_2 act like switches while Q_3 & Q_4 act as active load resistors. The transistor Q_1 conducts & Q_2 is cut off or vice versa. As a static RAM uses a flip-flop as the basic memory cell, it consists of thousands of flip-flops.



@ Using bipolar transistor.



(b) Using MOS transistor.

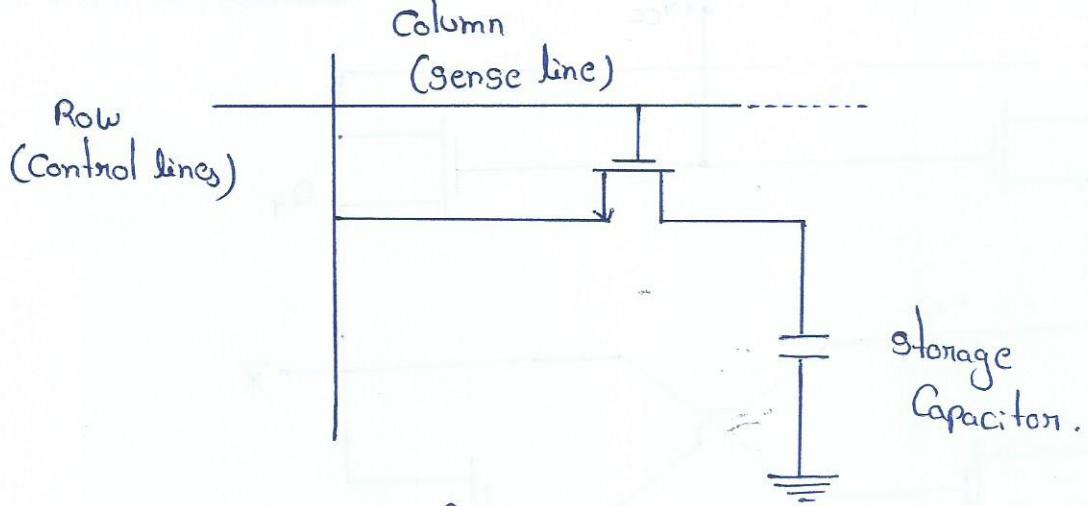
Fig ③ : static RAM cell.

Dynamic RAM (DRAM) :

The Dynamic Random Access memory (DRAM) is the lowest cost, high density Random Access memory available. Nowadays, Computers use DRAM for main memory storage with the memory sizes ranging from 16 to 256 mega bytes.

The DRAM stores its binary information in the form of electric charges on Capacitors. Data are stored by charge on every Capacitor, which must be recharged or refreshed thousand of times every second in order to retain the storage charge. These memory devices makes use of an integrated mos Capacitor as basic memory cell instead of a flip-flop.

The Advantage of this cell is that it allows very large memory arrays to be constructed on a chip at a lower cost per bit than in static memories. The disadvantage is that the mos Capacitor can't hold the stored charge over an extended period of time & it has to be refreshed every few milliseconds. This requires more circuitry & complicates the design problem. static RAMs are similar than dynamic RAMs.



Fig(4): A dynamic mos Ram cell

The typical dynamic RAM cell consisting of a single MOSFET & a capacitor is shown in Fig(4). A dynamic RAM consists of an array of such memory cells. In this type of cell, the transistor acts as a switch. The memory cell also requires MOSFETs for READ & WRITE gating to operate the cell. Data input is connected for storage by a WRITE Control signal.

The Dynamic RAM offers reduced power consumption & large storage capacity in a single memory chip. With the availability of such high packing density memory IC's, the capacity of memory will continue to grow.

* Programmable Logic devices :
These are used to implement specified logic functions.

A Programmable logic device (PLD) is an electronic component used to build Reconfigurable digital circuits. Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture. Before the PLD can be used in a circuit it must be programmed, that is reconfigured".

Advantages :

1. Easily Configurable by the individual user for specific applications.
2. PLDs can be reprogrammed within seconds. Hence gives more flexibility to design.
3. Reprogramming also makes it possible to accept modifications in the previous design.
4. Cheap in cost, less space & power required.
5. Highly reliable & easy to test.

All these advantages make PLDs very popular in digital circuit design.

Classifications of PLD's :

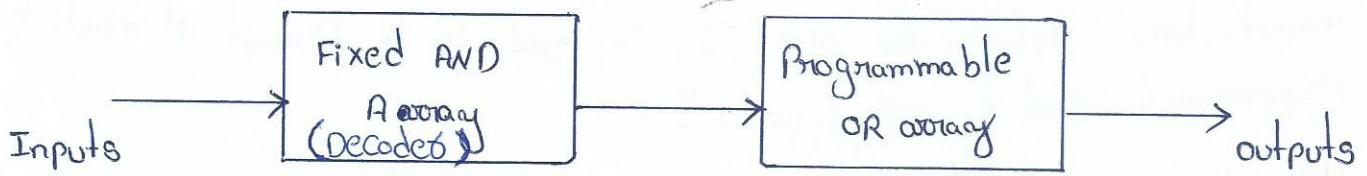
According to programming architecture, complexity, flexibility, PLD's are classified as.

1. PROM → Programmable ROM.
2. PLA → Programmable Logic Array
3. PAL → Programmable Array Logic
4. FPGA → Field Programmable Gate Array
5. CPLD → Complex " Logic Devices.

* PROM : (Programmable Read-only-memory) :

PROM has a fixed AND array Constructed as a decoder & a programmable OR array.

- * The AND Gates are programmed to provide the product terms for the boolean functions, which are logically summed in each OR Gate.



(a) Programmable Rom.

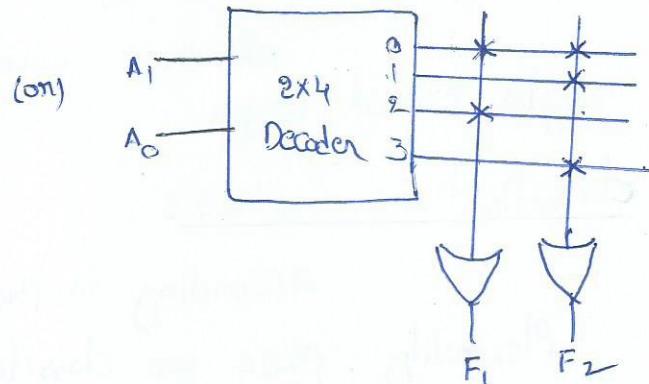
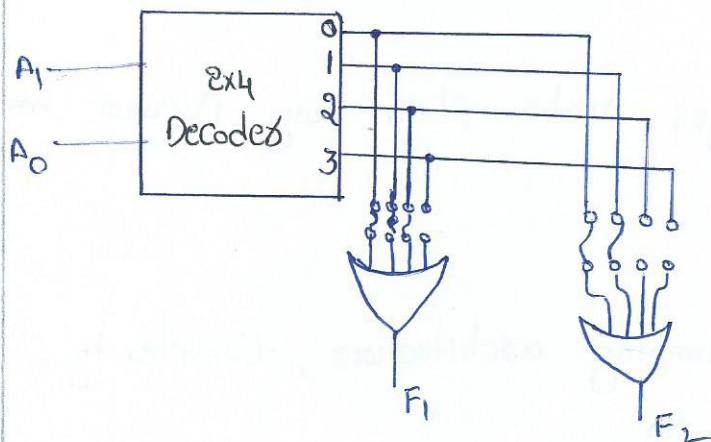
Example:

- ① Realize two o/p's F_1 and F_2 using a 4×2 PROM/Rom.

$$F_1(A_1, A_0) = \Sigma m(0, 2)$$

$$F_2(A_1, A_0) = \Sigma m(0, 1, 3)$$

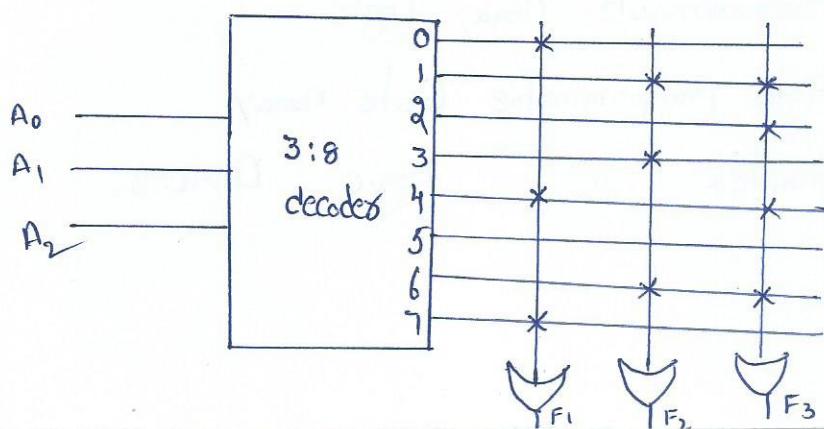
Sol: The functions F_1, F_2 have two variables. we use a 2×4 Decoder.



- ② Realize the following functions using a PROM of size

$$8 \times 3 \quad F_1 = \Sigma m(0, 4, 7), \quad F_2 = \Sigma m(1, 3, 6), \quad F_3 = \Sigma m(1, 2, 4, 6).$$

Sol:



$$F_1(A_0, A_1, A_2) = \Sigma m(0, 4, 7)$$

$$F_2(A_0, A_1, A_2) = \Sigma m(1, 3, 6)$$

$$F_3(A_0, A_1, A_2) = \Sigma m(1, 2, 4, 6)$$

3. Design a Combinational logic circuit using a PROM. The circuit accepts 3-bit binary number and generates its equivalent Ex-3 Code.

Sol:

Truth table:

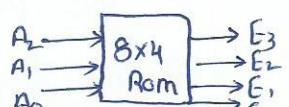
Inputs			outputs			
C	B	A	E_3	E_2	E_1	E_0
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	1	0

$$E_0 = \Sigma m(0, 2, 4, 6)$$

$$E_1 = \Sigma m(0, 3, 4, 7)$$

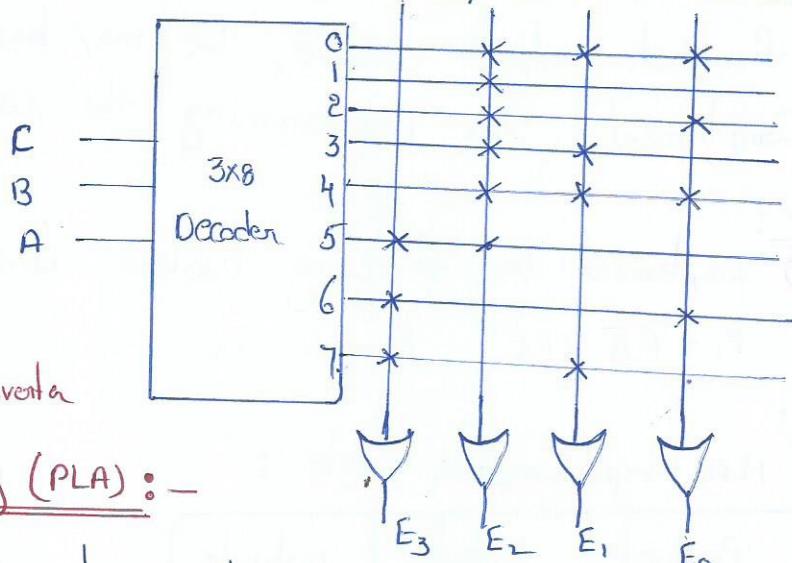
$$E_2 = \Sigma m(1, 2, 3, 4)$$

$$E_3 = \Sigma m(5, 6, 7)$$



(Block diagram)

Implementation of Binary to Ex-3 Code Converter using PROM.



Q. Implement a BCD to Gray Code Converter using PROM?

* Programmable Logic Array (PLA):-

The PLA does not provide full decoding of the variables and does not generate all the minterms.

The decoder is replaced by an array of AND Gates that can be programmed to generate any product term of the input variables. The product terms are then connected to OR Gates to provide the sum of products for the required Boolean functions.

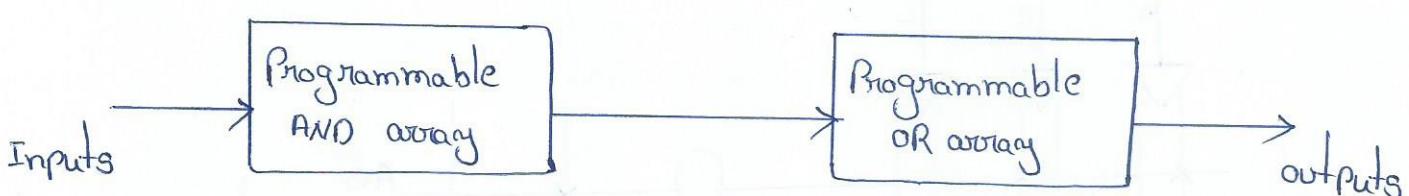


Fig 1: PLA

PLA has Programmable AND array and Programmable OR array.

PLA Programming Table :

The fuse map of a PLA can be specified in a

Tabular form.

- ⇒ The PLA Programming table consists of 3 sections
- ⇒ The first section lists the Product terms numerically.
- ⇒ The second " specifies the required paths between i/p's & AND Gates.
- ⇒ The third " the paths between the AND and OR Gates
for each output variable, we may have a T (for true) or C (for Complement) for Programming the XOR Gate.

Ex:

① Implement the following boolean functions using PLA

$$F_1 = A\bar{B} + AC \quad F_2 = AC + BC$$

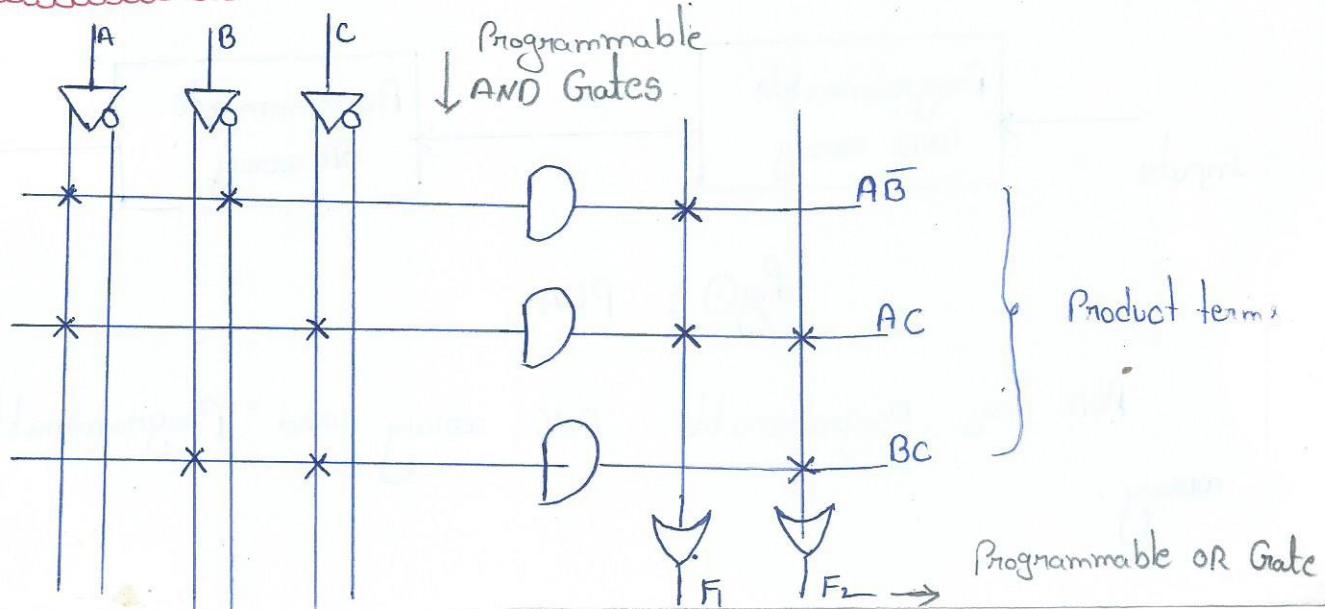
Sol:

PLA Programmable Table :

Product Terms	Inputs			outputs	
	A	B	C	F_1	F_2
$A\bar{B}$	1	0	-	1	-
AC	1	-	1	1	1
BC	-	1	1	-	1

✗ → indicates fuse.

Programmable PLA:



→ ② Implement the following boolean function with a PLA

$$F_1 = \Sigma m(1, 3, 7)$$

$$F_2 = \Sigma m(5, 6, 7)$$

Sol: Determine the simplified Boolean function Expression by using 3 variable K-map. Consider the three variables A, B, C.

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}		1		
A		1	1	

$$F_1 = \bar{B}C + AC$$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}		1		
A		1	1	1

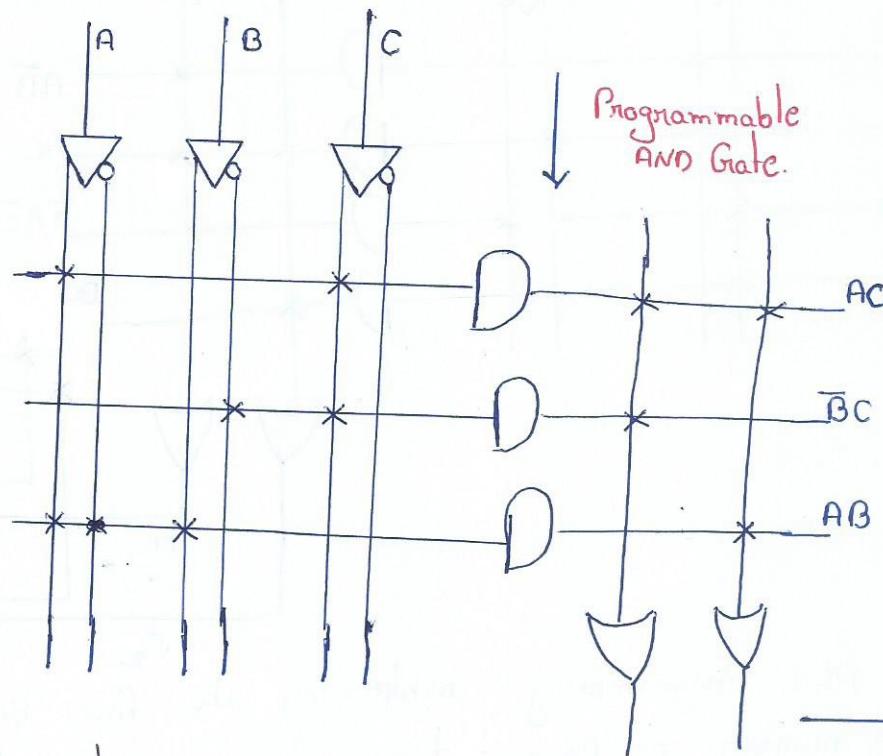
$$F_2 = AC + AB$$

Programmable Table:

Product term	Inputs			outputs	
	A	B	C	F_1	F_2
AC	1	-	1	1	1
$\bar{B}C$	-	0	1	1	-
AB	1	1	-	-	1

Implementation of

The Programmed PLA:



Programmable AND Gate.

Programmable OR Gate.

③ → A Combinational logic circuit has 4 inputs and two outputs F_1 & F_2 . The output F_1 gives high output when the input Combinational is greater than or equal to 1001, otherwise low o/p. The output F_2 give high output when the input Combinational is less than 1001 otherwise the output F_2 is low. by using PLA

→ ④ A Combinational logic Circuit is defined by the function. in PLA

$$F_1 = A\bar{B} + AC + \bar{A}\bar{B}\bar{C}$$

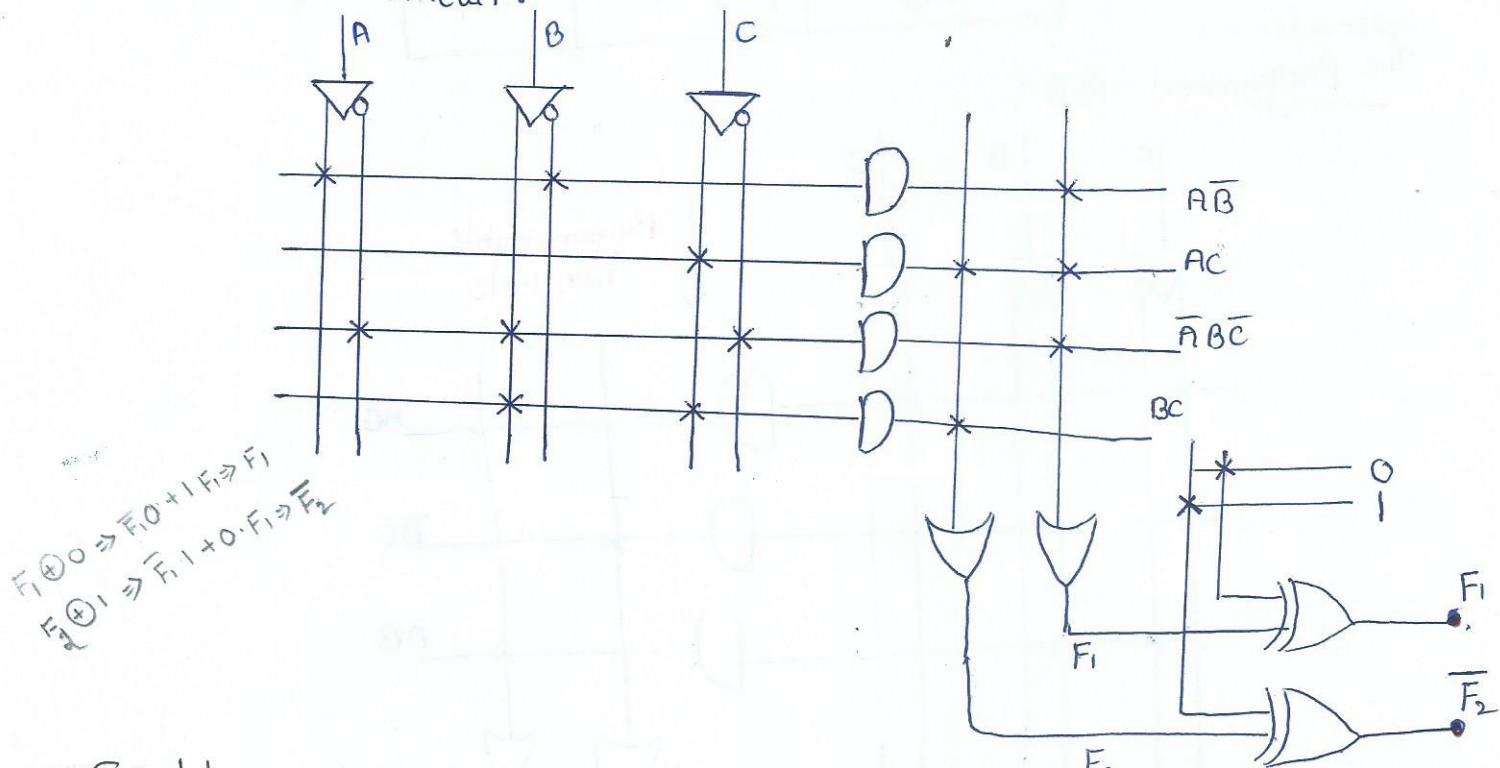
$$F_2 = \overline{AC + BC}$$

Sol: The circuit function is defined by Boolean function, so we can construct a program table directly.

Programmable table:

Product term	Inputs			outputs	
	A	B	C	F_1	F_2
$A\bar{B}$	1	0	-	1	-
AC	1	-	1	1	1
$\bar{A}\bar{B}\bar{C}$	0	1	0	1	-
BC	-	1	1	-	1

Programmable PLA: The function F_2 is inverted, hence we do the modification in the output circuit.



→ ⑤ Tabulate the PLA Programming table for the four Boolean functions & minimize the number of product term.

$$A(x,y,z) = \Sigma(1,2,4,6)$$

$$B(x,y,z) = \Sigma(0,1,6,7)$$

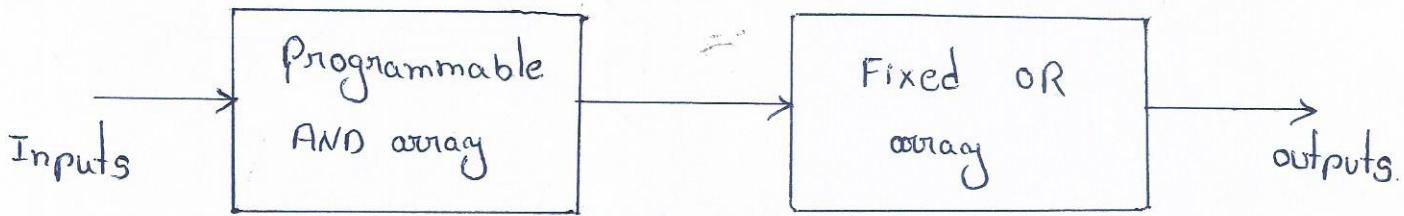
$$C(x,y,z) = \Sigma(2,6)$$

$$D(x,y,z) = \Sigma(1,2,3,5,7)$$

→ ⑥ List the PLA Programming table for the BCD to Excess-3 Code Converter and implement in PLA.

* Programmable Array Logic (PAL) :

The PAL is a specific type of PLD. The PAL is a Programmable logic device with a fixed OR array & a Programmable AND array. Because only the AND Gates are programmable, the PAL is easier to program, but is not as flexible as the PLA.



Example :

fig: Block diagram of PAL

i) Implement the Given function in PAL

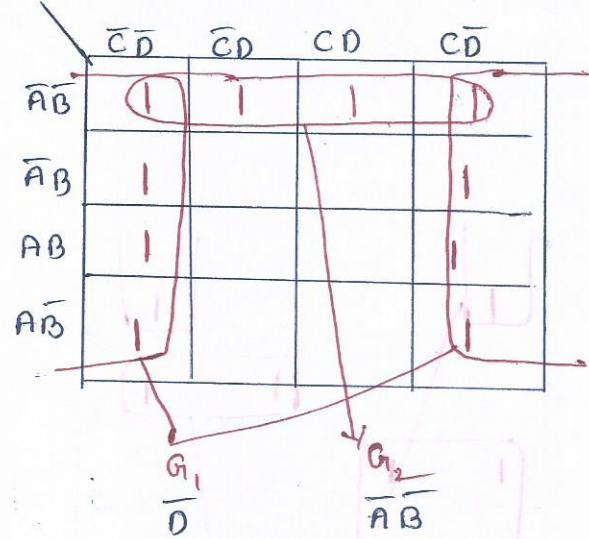
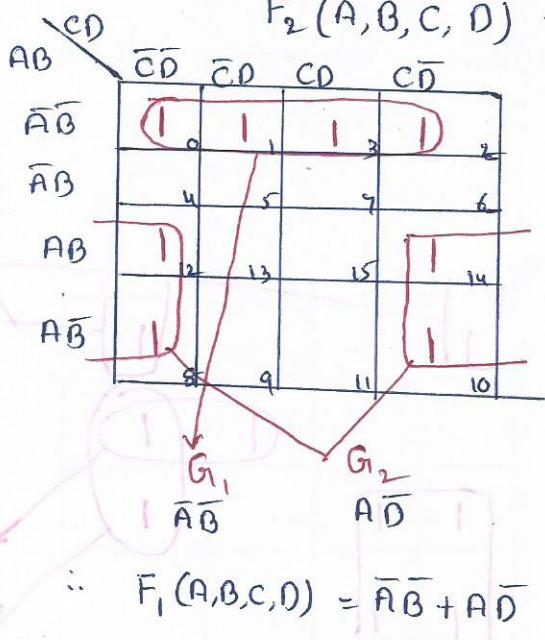
$$F_1 = \sum m(0, 1, 2, 3, 8, 10, 12, 14), F_2 = \sum m(0, 1, 2, 3, 4, 6, 8, 10, 12, 14).$$

Sol:

K-map Simplification:

$$F_1(A, B, C, D) = \sum m(0, 1, 2, 3, 8, 10, 12, 14)$$

$$F_2(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 6, 8, 10, 12, 14)$$



Programmable Table of PAL:

Product term	Inputs A B CD	Outputs
$\bar{A}\bar{B}$	1	0 0 --
$A\bar{D}$	2	1 - - 0
\bar{D}	3	- - - 0
$\bar{A}\bar{B}$	4	0 0 - -

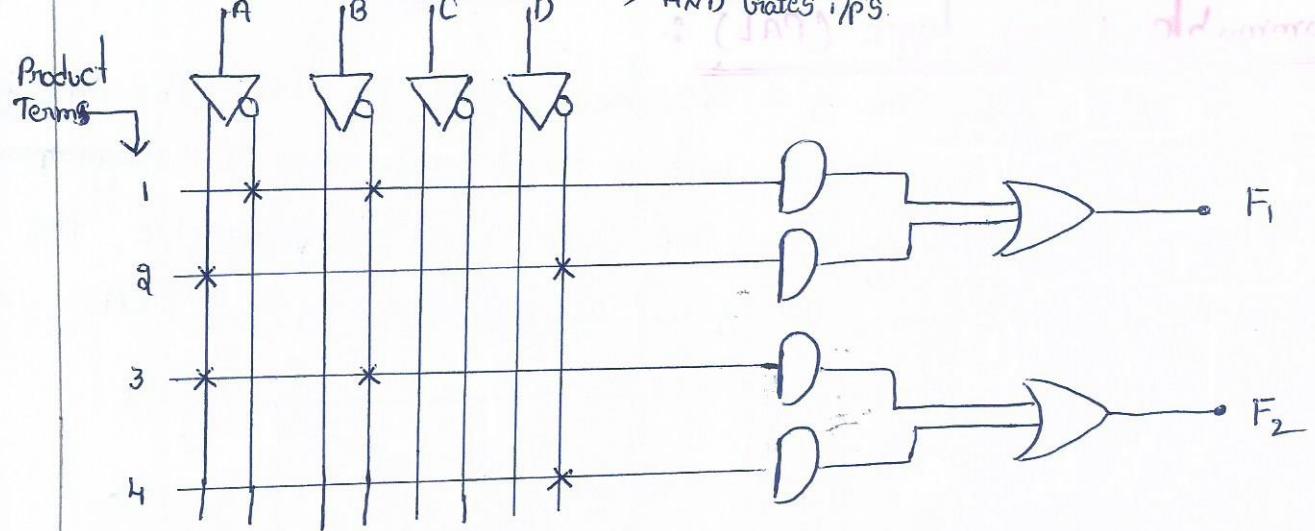


fig: Fuse map for PAL.

2) Implement the given function in PAL

$$A(w, x, y, z) = \Sigma m(0, 2, 6, 7, 8, 9, 12, 13)$$

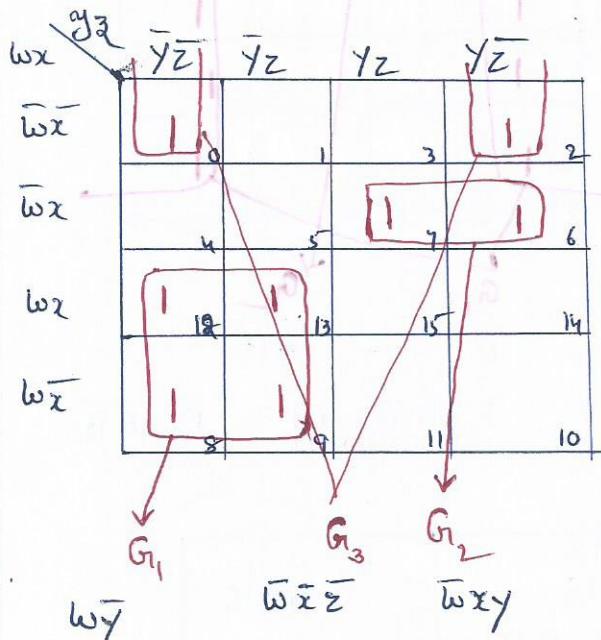
$$B(w, x, y, z) = \Sigma m(0, 2, 6, 7, 8, 9, 12, 13, 14)$$

$$C(w, x, y, z) = \Sigma m(1, 3, 4, 6, 10, 12, 13)$$

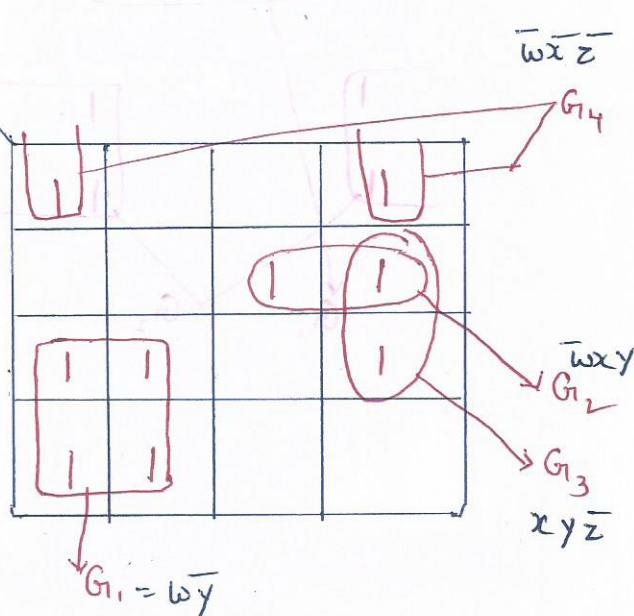
$$D(w, x, y, z) = \Sigma m(1, 3, 4, 6, 9, 12, 14)$$

Sol: Let us simplified the four functions by using k-map.

Expression for A:

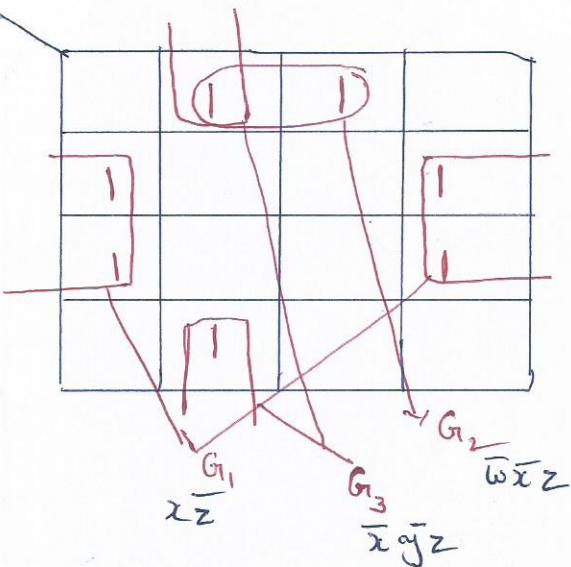
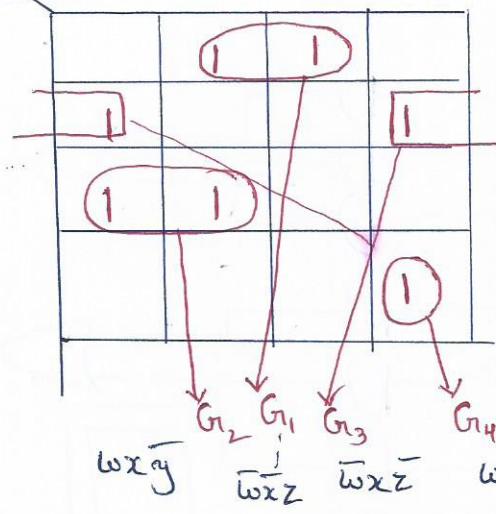


$$A(w, x, y, z) = w\bar{y} + \bar{w}\bar{x}\bar{z} + \bar{w}x\bar{y}$$



$$B(w, x, y, z) = w\bar{y} + \bar{w}xy + xy\bar{z} + \bar{w}\bar{x}\bar{z}$$

$$B(w, x, y, z) = A + xy\bar{z}$$



$$C(w, x, y, z) = \bar{w}\bar{x}z + w\bar{x}\bar{y} + \bar{w}x\bar{z} + w\bar{x}yz$$

$$D(w, x, y, z) = x\bar{z} + \bar{x}\bar{y}z + \bar{w}\bar{x}z$$

Programmable Table of PAL:

$$A = w\bar{y} + \bar{w}\bar{x}\bar{z} + \bar{w}xy$$

$$B = A + xy\bar{z}$$

$$C = \bar{w}\bar{x}z + w\bar{x}\bar{y} + \bar{w}x\bar{z} + w\bar{x}yz$$

$$D = x\bar{z} + \bar{x}\bar{y}z + \bar{w}\bar{x}z$$

Product term	Inputs $w \quad x \quad y \quad z \quad A$	outputs $A \quad B \quad C \quad D$
$w\bar{y}$	1 - 0 - -	
$\bar{w}\bar{x}\bar{z}$	0 0 - 0 -	
$\bar{w}xy$	0 1 1 - -	$A = w\bar{y} + \bar{w}\bar{x}\bar{z} + \bar{w}xy$
A	- - - - 1	
$xy\bar{z}$	- 1 1 0 -	$B = A + xy\bar{z}$
$\bar{w}\bar{x}z$	0 0 - 1 -	
$w\bar{x}\bar{y}$	1 1 0 - -	
$\bar{w}x\bar{z}$	0 1 - 0 -	$C = \bar{w}\bar{x}z + w\bar{x}\bar{y} + \bar{w}x\bar{z} + w\bar{x}yz$
$w\bar{x}yz$	1 0 1 0 -	
$x\bar{z}$	- 1 - 0 -	
$\bar{x}\bar{y}z$	- 0 0 1 -	$D = x\bar{z} + \bar{x}\bar{y}z + \bar{w}\bar{x}z$
$\bar{w}\bar{x}z$	0 0 - 1 -	

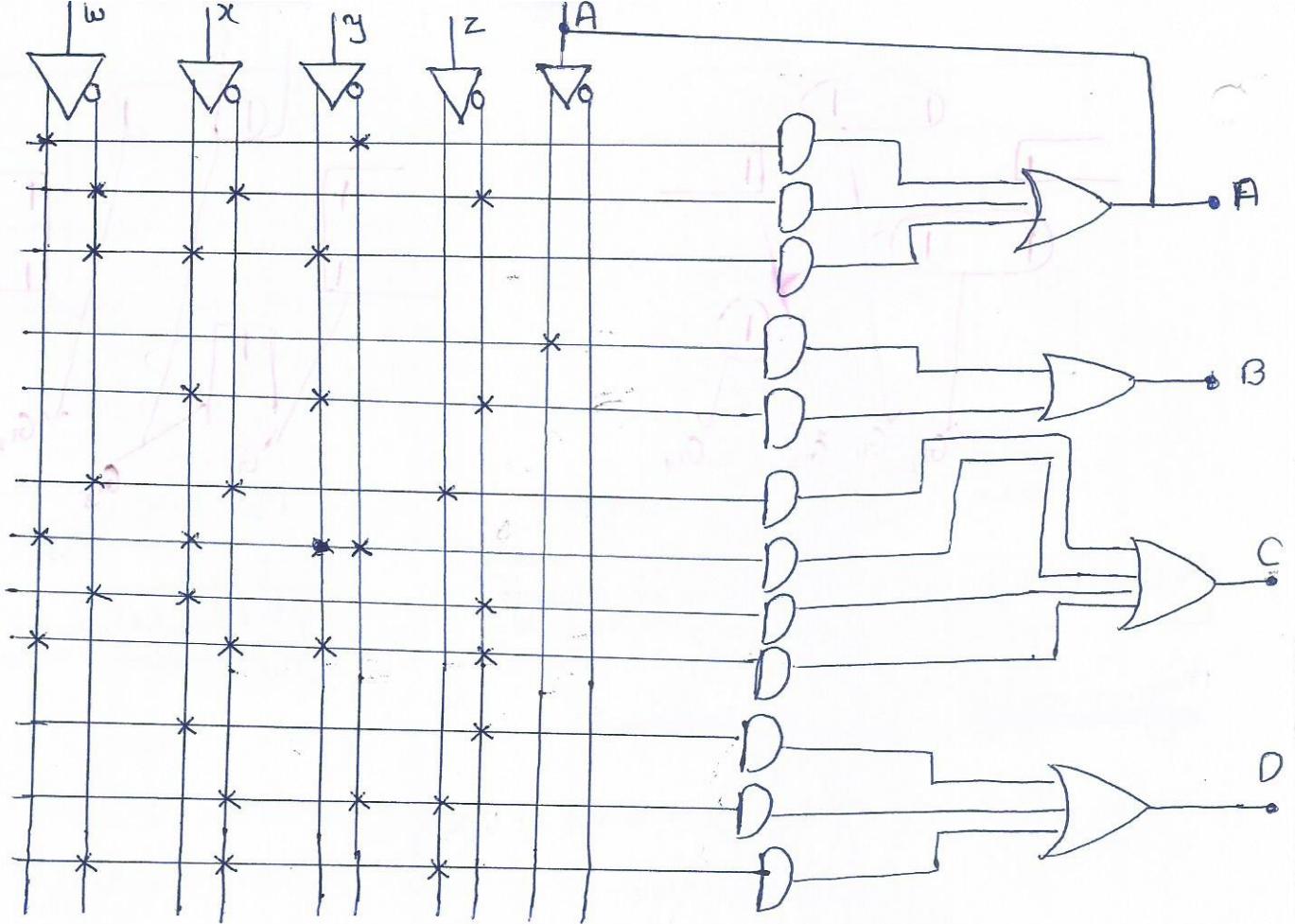


fig: Fuse map for PAL.

3. Implement the following Boolean function using PAL

$$w(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13)$$

$$x(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13, 14)$$

$$y(A, B, C, D) = \sum m(2, 3, 8, 9, 10, 12, 13)$$

$$z(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 12, 14).$$

4. Implement the following Boolean function using PAL

$$A(x, y, z) = \sum m(1, 2, 4, 6)$$

$$B(x, y, z) = \sum m(0, 1, 6, 7)$$

$$C(x, y, z) = \sum m(2, 6)$$

$$(y\bar{z} + \bar{y}\bar{z} + \bar{x}\bar{z})$$

$$\bar{x}\bar{y} + xy$$

$$y\bar{z}$$

5. Implement the following Boolean function by using PAL.

$$F_1(a, b, c) = \sum m(0, 1, 3, 4)$$

$$\bar{a}\bar{c} + \bar{b}\bar{c}$$

$$F_2(a, b, c) = \sum m(1, 2, 3, 4, 5).$$

$$ab + \bar{a}c + \bar{a}\bar{b}$$

* Memory decoding : The memory IC used in a digital system is selected or enabled only for the range of addresses assigned to it and this process is called memory decoding. The memory IC is disabled for the range of addresses that are not assigned to it.

In addition to requiring storage components in a memory unit there is a need for decoding circuits to select the memory word specified by the input Address.

An example of two-dimensional coincident decoding arrangement is shown in fig below, which shows a more efficient decoding scheme that is used in large memories.

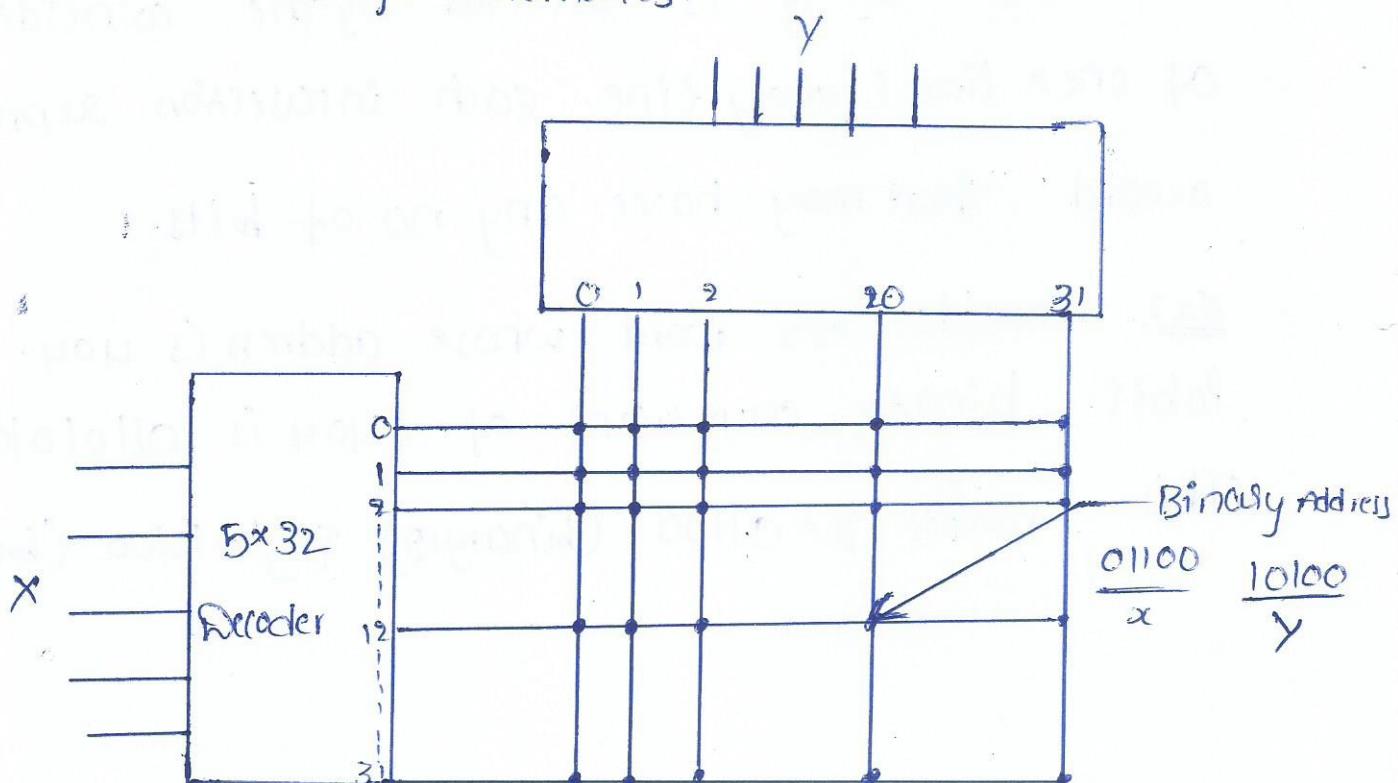


fig: 2-D decoding structure for 1k word memory

A decoder with k -inputs & 2^k outputs requires 2^k AND gates with k inputs per gate. The total no. of gates & no. of i/p's per gate can be reduced by

employing two decoders in a 2-D selection scheme.

The basic idea of 2D decoding is to arrange the memory cells in an array that is close as possible to square. Here two $k/2$ input decoder's are used instead of one k -input decoder one decoder performs the row selection & other the column selection in a 2-D matrix configuration.

Here using a single 10×1024 decoder we use two 5×32 decoders. The 5 most significant bits of the address go to i/P_x & 5 LSB go to i/P_y . Each word in the memory array is selected by the coincidence of one line & one y line. Each intersection represents a word that may have any no. of bits.

Ex: Consider the word whose address is 404. The 10bit binary equivalent of 404 is 011010100. This makes $x = 01100$ (binary₁₂) & $y = 10100$ (binary₂₀).