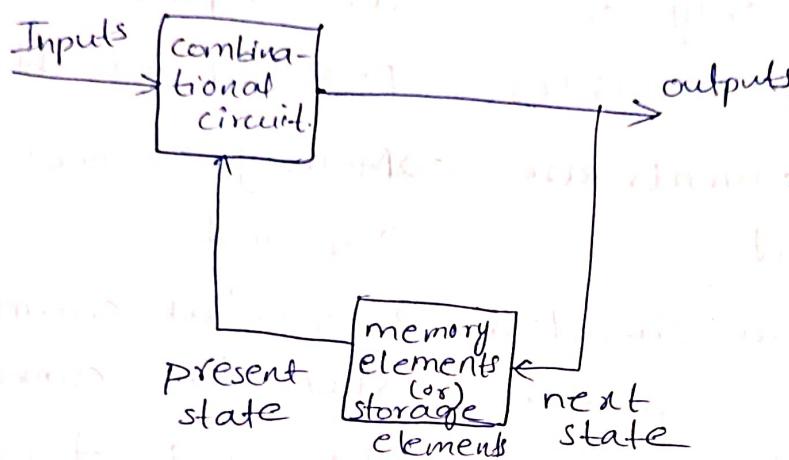


Sequential logic circuits-3

Sequential Circuits:- Sequential ckt's are one type of digital circuits whose outputs depends upon present inputs as well as previous inputs.

Ex:- counters, Registers.



• Block diagram of sequential circuit.

- ⇒ Sequential ckt consists of combinational circuit to which storage elements are connected to form a feedback path. The storage elements storing binary information.
- ⇒ The information stored in memory elements at any given time defines the present state of the sequential circuit.
- ⇒ The present state and external inputs determines the output and the next state of the sequential circuit.
- ⇒ Thus, we can specify the sequential circuit by a time sequence of external inputs, internal states and outputs.

~~Combinational~~ Comparison b/w combinational and Sequential circuits:-

Combinational	Sequential.
⇒ In a combinational ccts the output variables at any instant of time are dependent only on present ilp variables.	⇒ In sequential circuits, the output variables at any instant of time are dependent only on past ilp variables.
⇒ Memory elements are not required.	⇒ Memory elements are required.
⇒ Combinational circuits are faster than sequential	⇒ Sequential circuits. are slower than combinational
⇒ easy to design Ex:- parallel adders, encoders, decoder etc.	⇒ difficult to design. Ex:- counters, shift registers, serial address, sequence generators etc.

Classification of Sequential circuits:-

The sequential circuits can be classified depending on the timing of their signals. They are.

(1) Synchronous sequential circuit.

(2) Asynchronous sequential circuit.

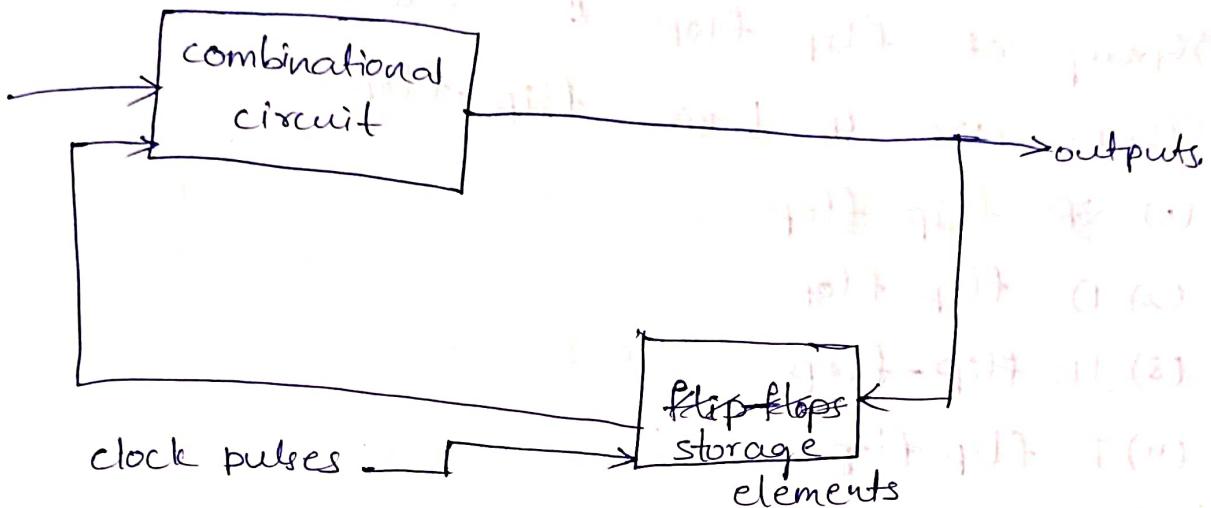
(1) Synchronous Sequential circuit:-

In synchronous sequential circuit signals affect the memory elements only at discrete instant of time.

⇒ Synchronous sequential circuits that are clo-

pulses to control storage elements are called clocked sequential circuits.

In synchronous / clocked sequential circuits, clocked flip-flops are used as memory elements, which change their individual states with the clock.



* Block diagram of synchronous clocked sequential circuit

2) Asynchronous sequential circuits:-

In Asynchronous sequential circuit signals can affect the memory elements at every instant of time.

Storage elements:-

The storage elements / memory elements used in sequential circuits are latches and flip-flops.

Latches:-

Latches are used to store 1-bit information. Latches are the basic circuits from which all flip-flops are constructed. Latches are 2 types:

(1) SR latch (2) D-Latch.

Flip-flops:-

Flip-flops are basic building blocks of sequential circuits.

⇒ Flip-flops are memory elements which are capable of storing '1 bit information'.

⇒ Flip-flops are also called as Bistable element as the two states 0 & 1 are stable.

⇒ Group of flip-flop is called as 'Registers'.

⇒ There are 4 basic flip-flops.

(1) SR flip flop

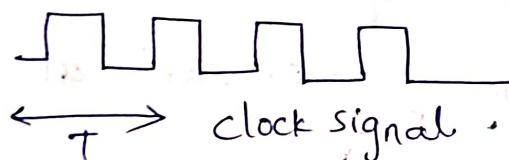
(2) D flip-flop

(3) JK flip-flop

(4) T flip flop

Clock:-

It decides the time of input. Clock is nothing but a signal which is having of duty cycles.



Triggering of clock:-

Clock having two types of triggering.

(1) Level triggering

(2) edge triggering.

⇒ Latches having level triggering

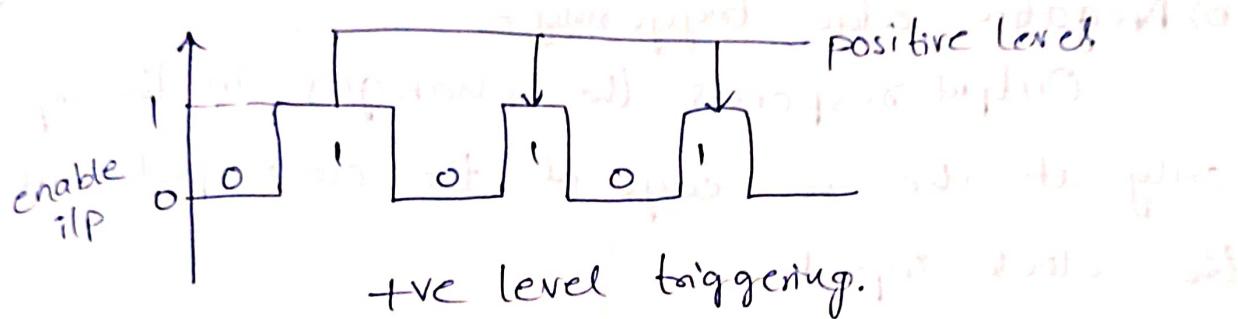
⇒ flipflops having edge triggering.

1) Level triggering:-

In level triggering, the o/p state is changed according to active level maintained at the enable input. There are two types of level triggered latches.

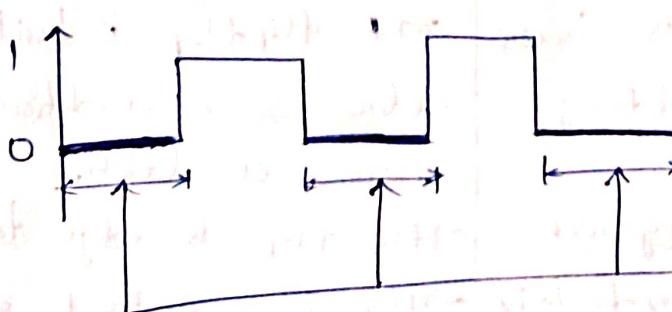
a) Positive level triggered:-

The output of latch responds to the input changes only when its enable is put as 1 and clock is active at high position.



b) Negative level triggered:-

The output of latch responds to the i/p changes only when its enable input is 0 (low) and clock is active at low position.



-ve level triggering.

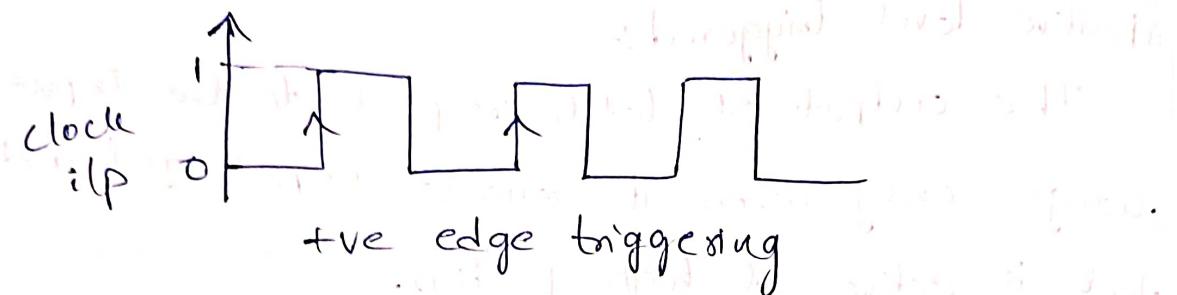
2) Edge triggering:-

In the edge triggering, the o/p responds to the changes in the output only at the +ve or -ve edge of the clock pulse at clock input. There

are two types of edge triggering:-

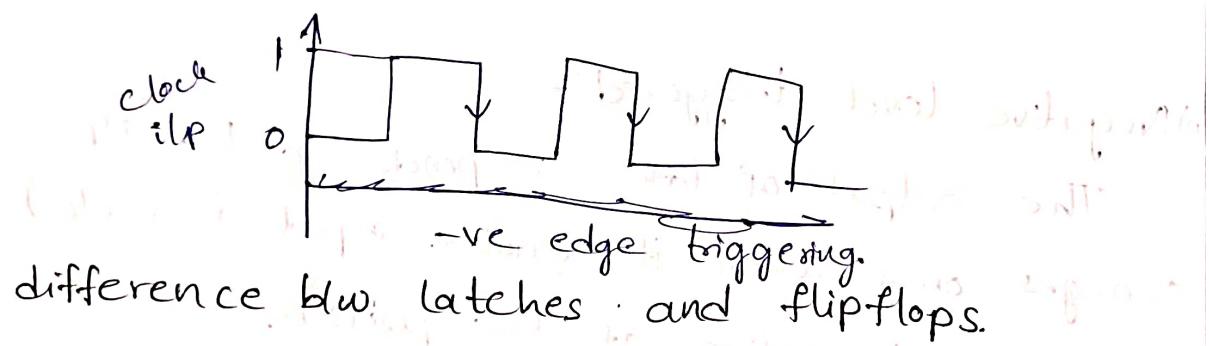
a) Positive edge triggering:-

Output responds to the changes in the input only at the positive edge (from 0 to 1) of the clock pulse at the clock input.



b) Negative edge triggering:-

Output responds to the changes in the input only at the -ve edge of the clock pulses at the clock input.



difference b/w latches and flip-flops.

latch

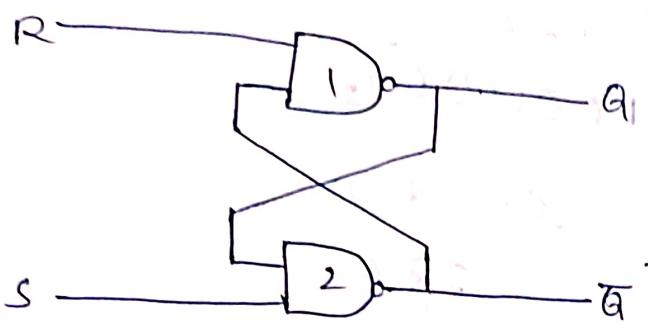
- ⇒ A simple latch is basic for flip-flop building
- ⇒ Latch is level triggered
- ⇒ The latch dp responds to ilp until active level is maintained at the enable ilp.
- ⇒ storage elements that operate with signal levels referred as latches

flip flop

- ⇒ A flip flop is built by connecting some additional components around a latch.
- ⇒ flip flop is edge triggered
- ⇒ flip flop output responds to ilp only at the specified edges of clock pulse.
- ⇒ storage elements controlled by clock transition are referred as flip-flop.

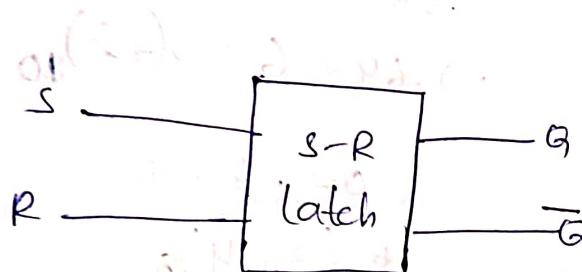
S-R Latch using NAND gate -

S-R Latch is the simplest type of flip-flop. The logic diagram for S-R latch using NAND gate is shown below.



A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

Symbol of S-R latch:-

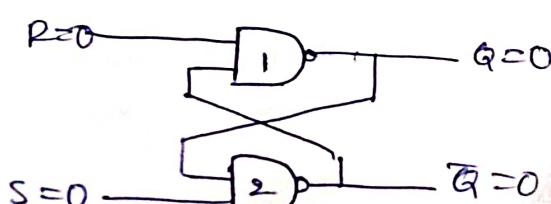


Truth table:-

R	S	Q	\bar{Q}	state
0	0	X	X	forbidden (invalid)
0	1	1	0	set
1	0	0	1	Reset
1	1	N.C.	N.C.	no change

Ex-1,

When $S=0$, $R=0$



→ both the inputs of NAND gate is 'zero'. So it is invalid.

~~D - B:~~

$$\begin{array}{r} \cancel{D-B:} \\ 2 \mid 32 \\ 2 \mid 16 \\ 2 \mid 8 \\ 2 \mid 4 \\ 2 \mid 2 \\ 1 \end{array}$$

$$(100000)_2$$

$$\begin{array}{r} \cancel{D-B:} \\ 2 \mid 76 \\ 2 \mid 38 \\ 2 \mid 19 \\ 2 \mid 9 \\ 2 \mid 4 \\ 2 \mid 2 \\ 1 \end{array}$$

$$(1001100)_2$$

~~D - 04~~

$$\begin{array}{r} \cancel{D-04} \\ 8 \mid 60 \\ 8 \mid 7 \\ 1 \end{array}$$

$$(74)_8$$

B-dec:

$$\begin{array}{cccc} 0 & 0 & 0 & 1 \\ | & | & | & | \\ 1 & 1 & 1 & 1 \\ \cancel{1} & \cancel{1} & \cancel{1} & \cancel{1} \\ = 0 & (1)_{10} \end{array}$$

Oct-dec:

$$\begin{array}{r} 8 \cdot 8^3 + 8 \cdot 8^2 + 8 \cdot 8^1 + 8 \cdot 8^0 \\ \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \\ 8 \cdot 8 + 8 \cdot 8 + 8 \cdot 8 + 8 \cdot 1 \\ \Rightarrow 64 + 64 = (72)_{10} \end{array}$$

Bin-Hex:

$$\begin{array}{r} 0000001110111 \\ \hline 1 \quad 6 \quad 2 \quad 8 \\ 0 \quad 7 \quad 7 \quad 11 \\ (077)_{16} \end{array}$$

Oct-bin:

$$(364)_8$$

$$(011110100)_2$$

$$(542)_8$$

$$(101100010)_2$$

hexa-bin:

$$\begin{array}{c} A \quad C \quad B \\ | \quad | \quad | \\ 10 \quad 12 \quad 11 \end{array}$$

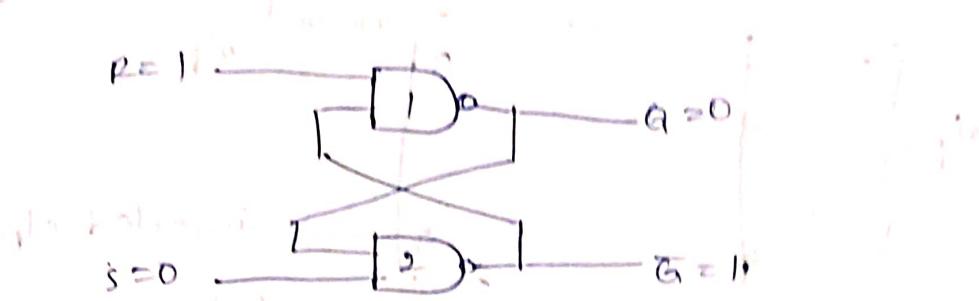
$$(101011001011)_2$$

$$(214)_{16}$$

$$(001000010100)_2$$

Case-2:
when

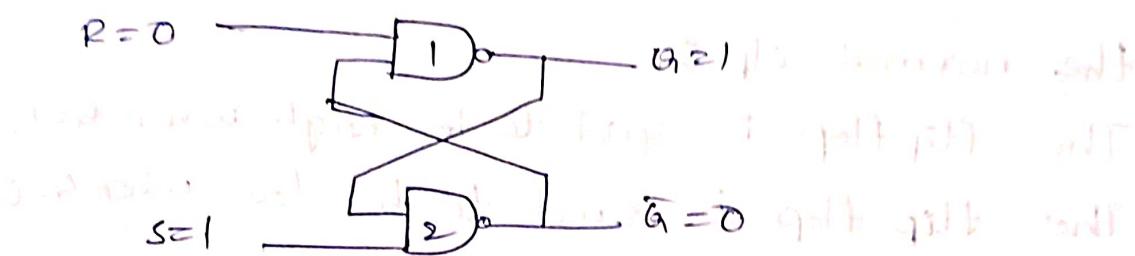
$$s=0 \& R=1$$



In this case, the o/p of '1' NAND gate is '0' and '2' NAND gate is '1'.

Case-3:

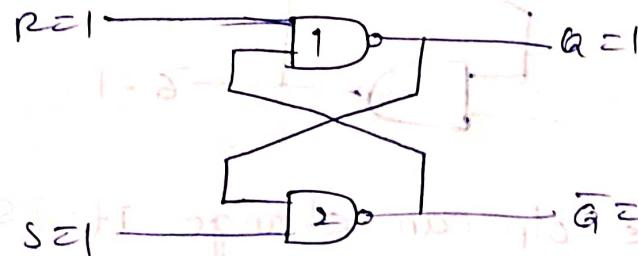
$$\text{when } s=1, R=0$$



In this case, the o/p of '1' NAND gate is '1' & '2' NAND gate is '0'.

Case-4:

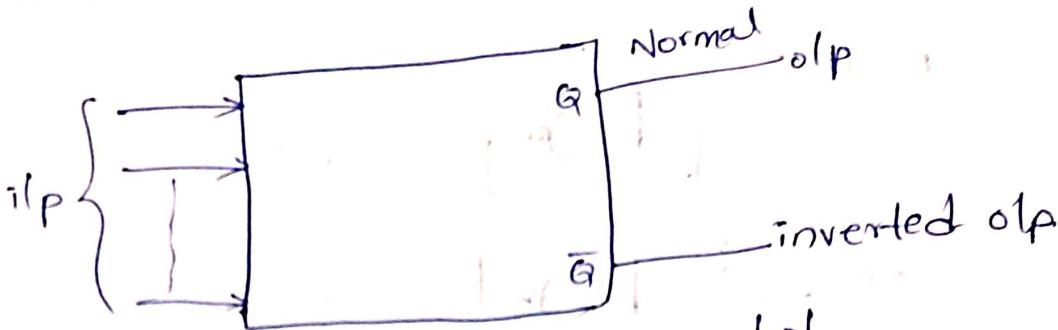
$$\text{when } s=1, R=1$$



In this case, the o/p of '1' NAND gate is '1' & '2' NAND gate is '1'.

Latches has no effect on o/p of the slave Q & G will remain same with No change.

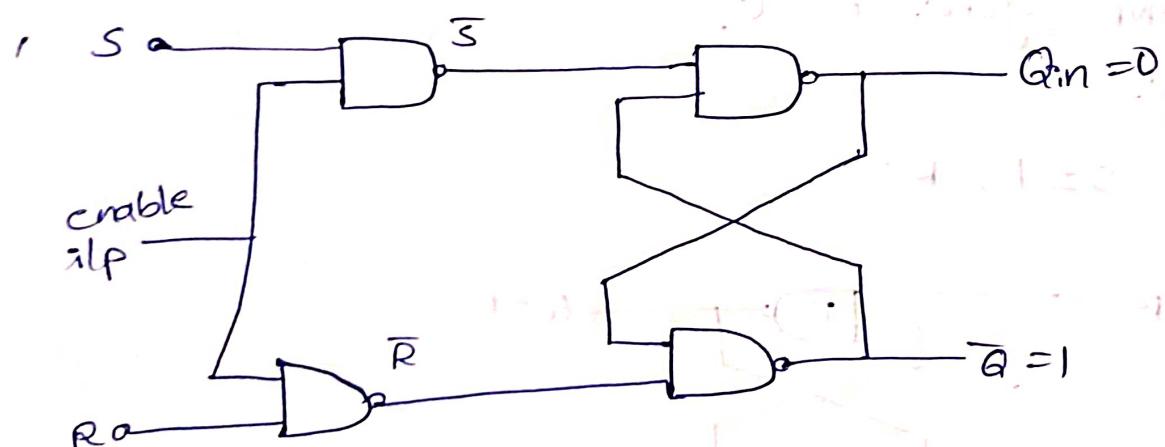
Structure of the flip-flop



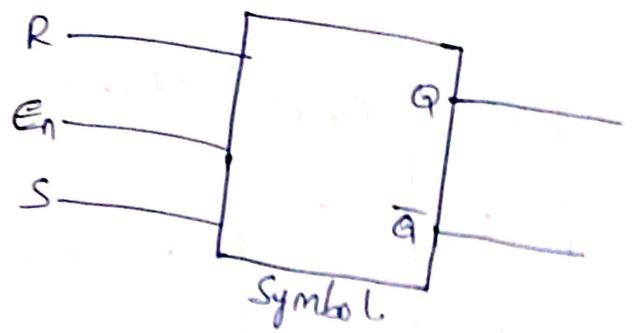
General flip-flop symbol.

- ⇒ The flip-flop has two output states labelled as Q & \bar{Q} . The Q is the normal output & \bar{Q} is the inverted output of the flip-flop.
- ⇒ The state of the flip-flop always refers to the normal o/p Q .
- ⇒ The flip flop is said to be high when $Q=1$.
- ⇒ The flip flop is said to be low when $Q=0$.

Clocked SR flip-flop



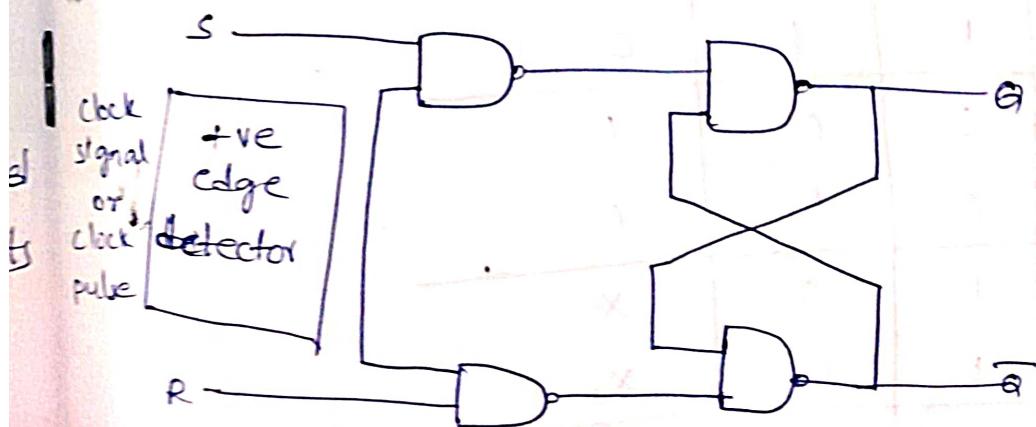
- ⇒ In the latch, the o/p can change its state at any time with the ilp condition.
- ⇒ The latch is called Asynchronous latch.
- ⇒ The gated S-R latch is also called as clocked S-R latch or synchronous S-R latch, because its o/p is controlled by the ilp or clocked.



Truth table:-

E_n	S	R	Q_n	Q_{n+1}	state
0	X	X	1	1	no change
0	X	X	0	0	
1	0	0	0	0	
1	0	0	1	1	no change
1	0	1	0	0	
1	0	1	1	1	Reset
1	1	0	0	1	
1	1	0	1	1	set
1	1	1	0	*	indeterminant
1	1	1	1	X	invalid

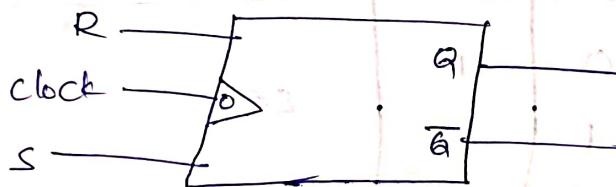
SR flip-flop using NAND Gates with +ve edge triggering:-



Truth table:-

CP	S	R	Q _n	Q _{n+1}	state
↑	0	0	0	0	no change
↑	0	0	1	1	
↑	0	1	{0}	0	reset
↑	0	1	{1}	0	
↑	1	0	0	1	set
↑	1	0	1	1	
↑	1	1	0	x	invalid
↑	1	1	1	x	
0	x	x	0	0	no change
0	x	x	1	1	

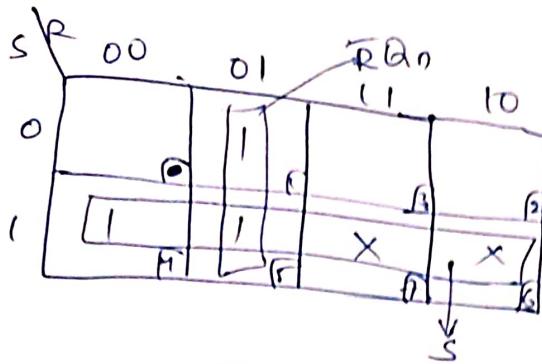
Symbol:-



Characteristic table:-

S	R	Q _n	Q _{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

Characteristic eqⁿ by using k-map
 $\Sigma M(1,4,5) + \Sigma d(6,7)$



$$Q_{n+1} = S + \bar{R} Q_n$$

excitation table:-

Q _n	Q _{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

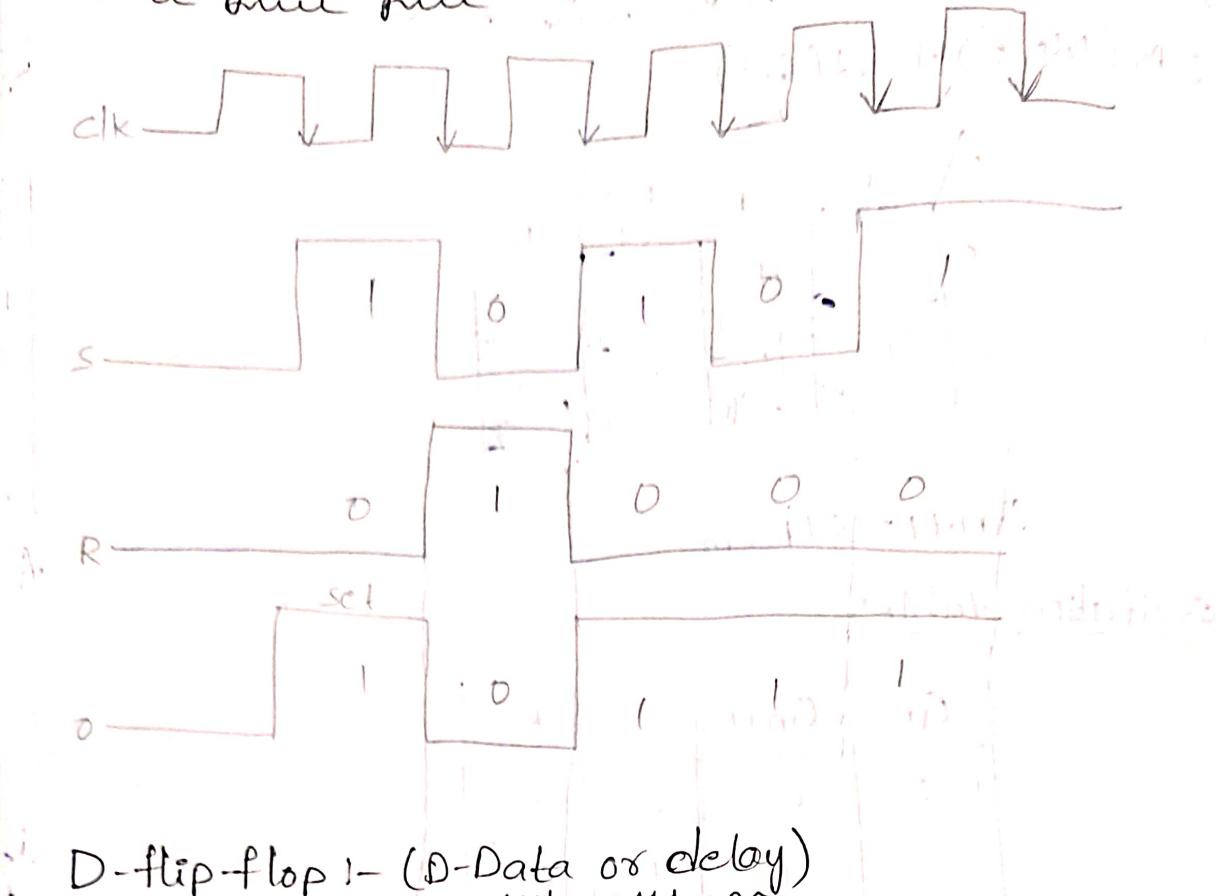
⇒ Draw the timing diagram of output for the inputs $S=10101$; $R=01000$, SR flipflop when triggering R is applied.

Truth table:-

S	R	Q _n	state
0	0	NC	NC
0	1	0	preset
1	0	1	set
1	1	x	invalid

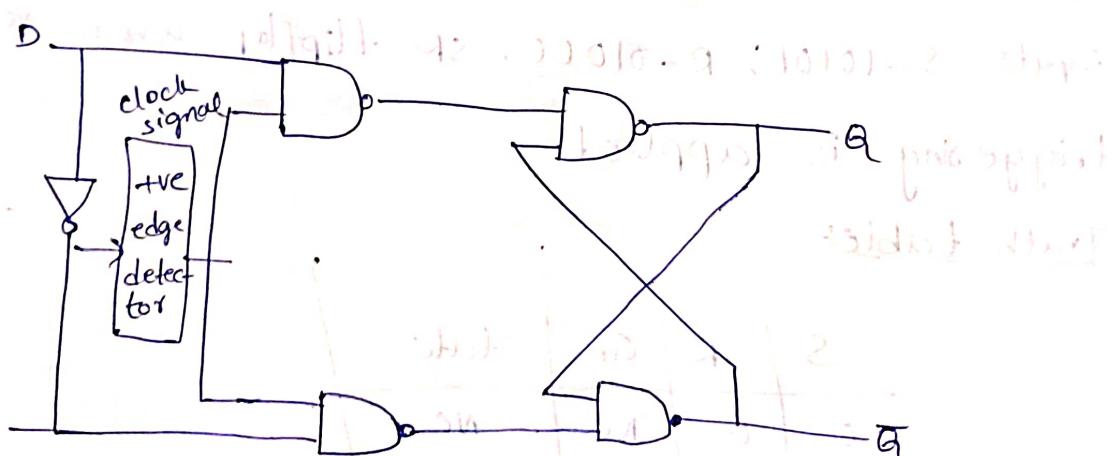
$S = 10101$ $R = 01000$

Timing diagram:-

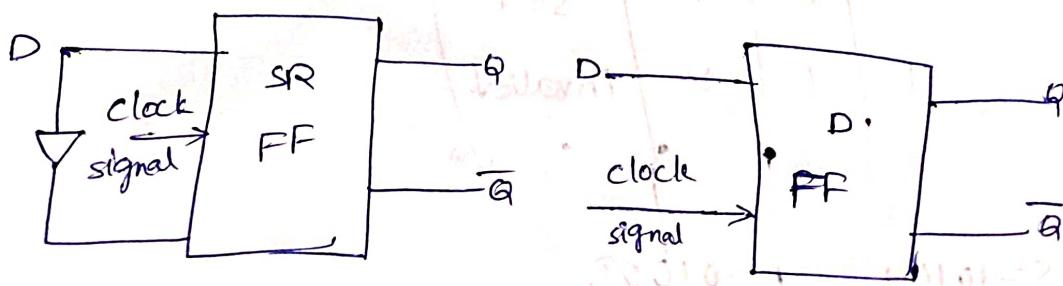


D-flip-flop :- (D-Data or delay)

In D-flip-flop we are using an SR flip-flop with complemented inputs, the logic diagram for D flip-flop is shown in the below figure.



Symbol-



truth table:-

clk	D	Qn	Qn+1	state
↑	0	0	0	reset
↑	0	1	0	
↑	1	0	1	
↑	1	1	1	set
0	x	0	0	
0	x	1	1	no change

excitation table:-

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

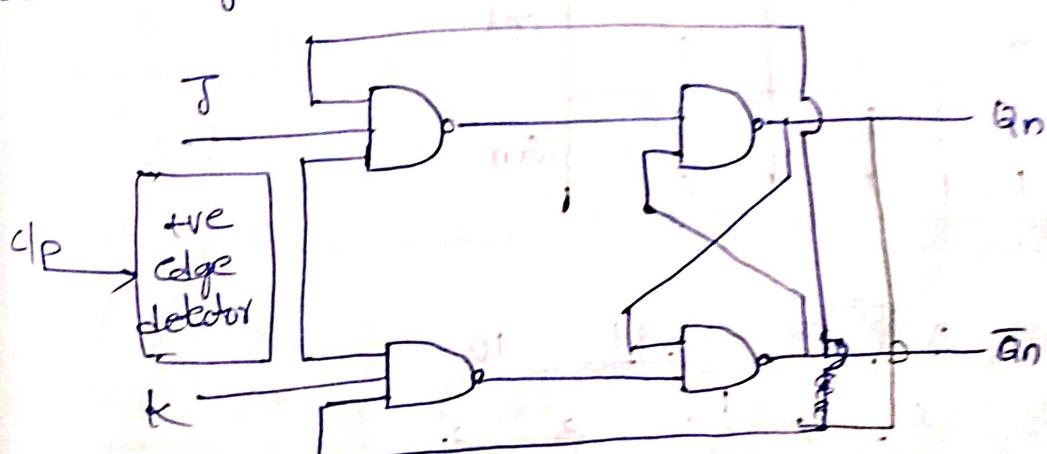
characteristic eqn :-

$$Q_{n+1} = \Sigma(2,3)$$

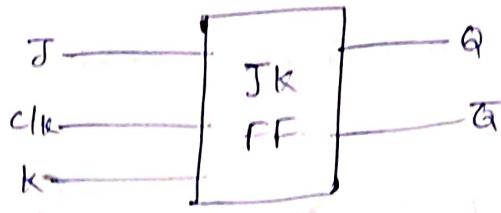
Qn	0	1
D	0	
0	0	
1	1	1
1	1	1

$$Q_{n+1} = D$$

JK flip-flop:
 In SR flip-flop when S=1 and R=1, we are getting an indeterminant state to eliminate these indeterminate state we are going for JK flip-flop. The logic circuit is JK flip-flop as in below figure.



Symbol:-



Truth-table:-

Cp	J	K	Qn	Qn+1	state
↑	0	0	0	0	no change $Q_{n+1} = Q_n$
↑	0	0	1	1	
↑	0	1	0	0	reset $Q_{n+1} = 0$
↑	0	1	1	0	
↑	1	0	0	1	set $Q_{n+1} > 1$
↑	1	0	1	1	
↑	1	1	0	1	Toggle (Race around condition)
↑	1	1	1	0	
0	x	x	0	1	
0	x	x	0	1	no change

Characteristic table of JK flip-flop:-

J	K	Qn	Qn+1	
0	0	0	0	
0	0	1	1	no change
0	1	0	0	
0	1	1	0	reset
1	0	0	1	
1	0	1	1	set
1	1	0	1	
1	1	1	0	\bar{Q}_n

J	K	Qn	Qn+1
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

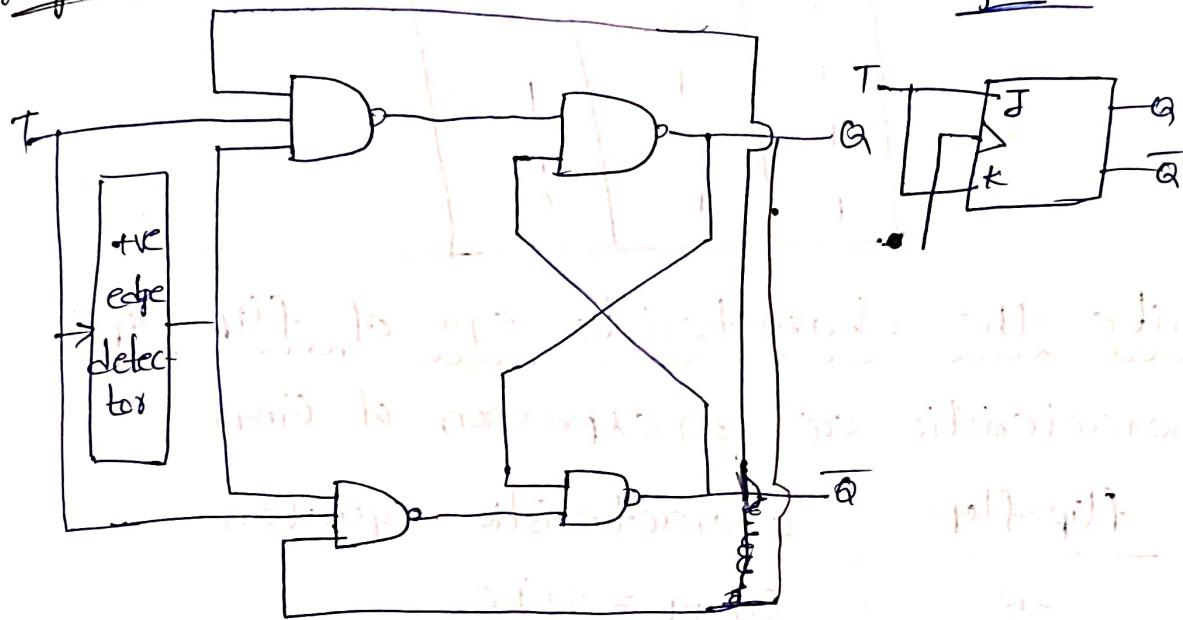
$$Q_{n+1} = J\bar{Q}_n + KQ_n$$

Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

+ Flip-flop or Toggle flip-flop :-
logic circuit :-

Symbol :-



Truth table :-

CP	T	Q_n	Q_{n+1}	state
↑	0	0	0	no change
↑	0	1	1	
↑	1	0	1	Toggle
↑	1	1	0	
0	X	0	0	no change
0	X	1	1	

Characteristic Table:-

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

T	Q_n	0	1
0	0	0	1
1	1	1	0

$$Q_{n+1} = T\bar{Q}_n + TQ_n \\ = T \oplus Q_n$$

Excitation table:-

	Q_n	Q_{n+1}	T
	0	0	0
	0	1	1
	1	0	1
	1	1	0

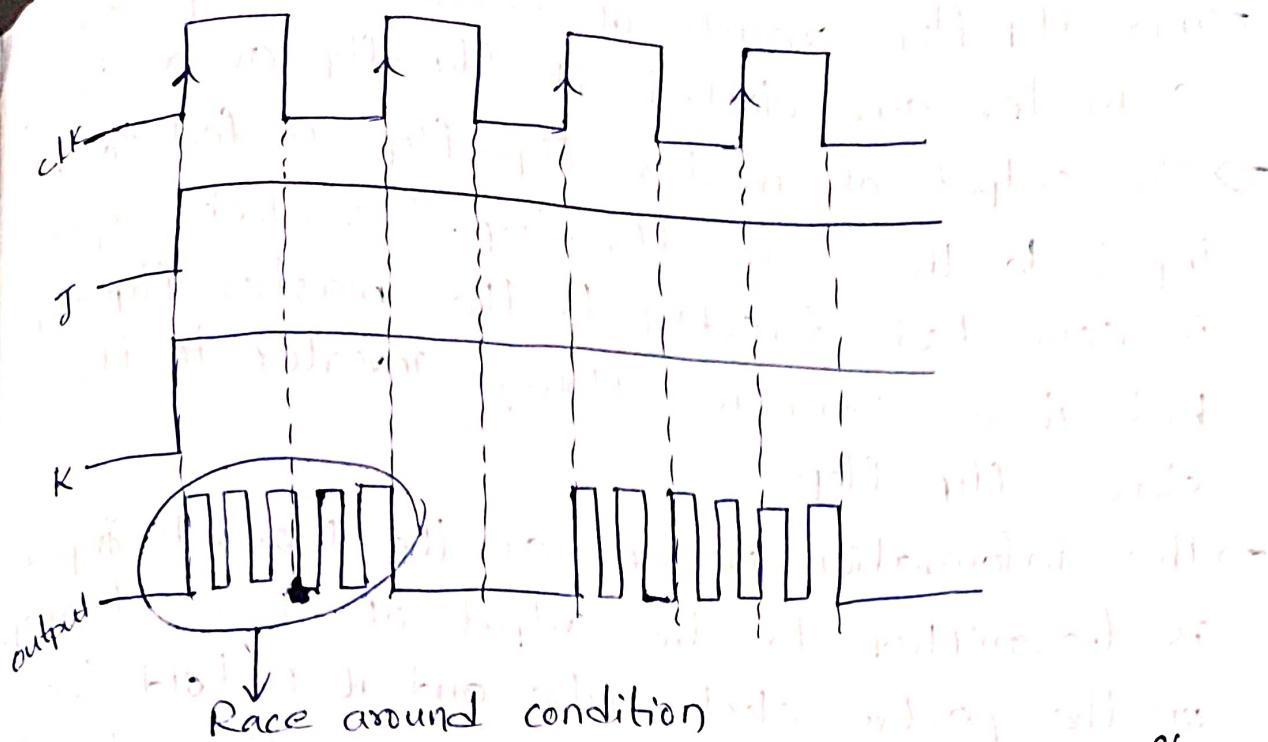
Write the characteristic eqn of flip-flops.

Characteristic eqn (or) expression of Q_{n+1} .

flip-flop	characteristic equation
SR	$Q_{n+1} = S + \bar{R}Q_n$
D	$Q_{n+1} = D$
JK	$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$
J	$Q_{n+1} = JQ_n + \bar{T}Q_n$ (or) $J \oplus Q_n$

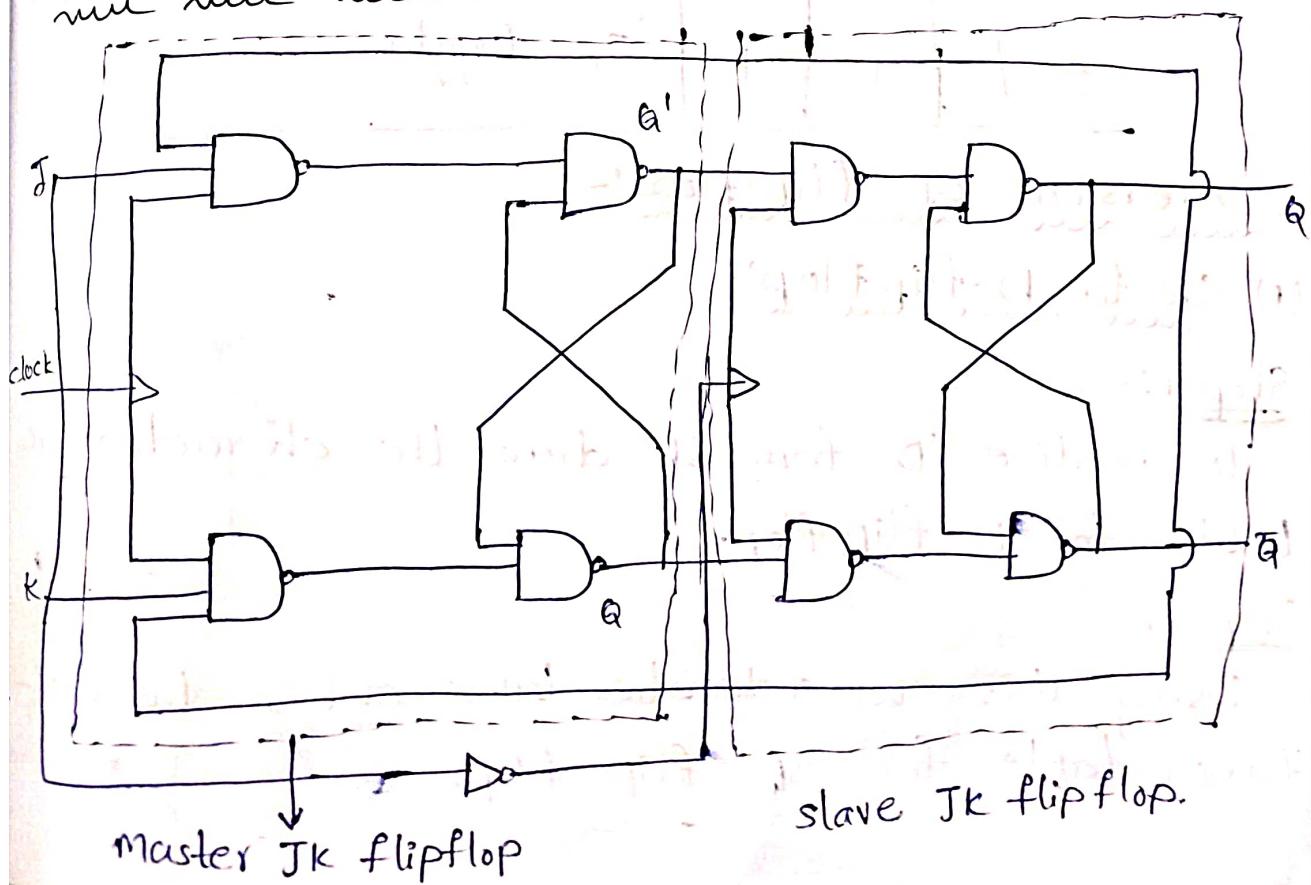
Race around condition in JK flip-flop:-

In JK flip-flop, when $J=K=1$, the output toggles continuously changes from 0 to 1 (or) from 1 to 0.
 From 0 to 1 is suffered as Race around condition.



- ⇒ For eliminating Race around condition in JK flip-flop, we can keep $t_p < \Delta t$. (propagation delay)
- ⇒ Apply the -ve edge triggering clock.
- ⇒ A more practical method for overcoming this difficulty is the use of Master slave (MS) configuration.

Master-slave JK flip-flop:-



- ⇒ MS flip flop consists of clocked JK flip-flop as a Master and clocked JK flip-flop as a slave.
- ⇒ The output of master flip-flop is fed to an input to the slave flip-flop. The clock signal is connected directly to the master flip-flop but it is connected through inverter to the slave flip-flop.
- ⇒ The information present at the J and K inputs is transmitted to the output of master flip-flop on the positive clock pulse and it is held there until the -ve clock pulse occurs after which it is allowed to pass through the output of slave flip-flop.

<u>Truth Table</u>	<u>clk</u>	<u>J</u>	<u>K</u>	<u>Q_{n+1}</u>
	0	0		Q_n (no change)
	0	1		0 (reset)
	1	0		1 (set)
	1	1		$\overline{Q_n}$ Toggle

Conversions of flip-flops:-

(i) SR to D-flip flop:-

Step-1:-

To realise 'D' from 'SR' draw the characteristic table for D flip-flop.

Step-2:-

Using this characteristic table obtain the excitation table for SR flip-flop.

Step-3:-
Obtain the equations for S & R in terms of D & $Q(n)$ (Present state).

Step-4:-
from the above obtained eqn's realise 'D' from SR.

Step-5:- D characteristic table

D	$Q(n)$	$Q(n+1)$
0	0	0
0	1	0
1	0	1
1	1	1

Step-6:- Excitation Table of SR.

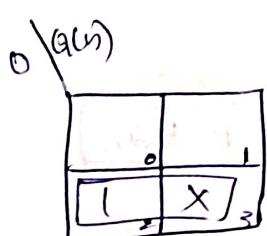
D	$Q(n)$	$Q(n+1)$	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

Characteristic table of D.

$Q(n)$	$Q(n+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

for reference.

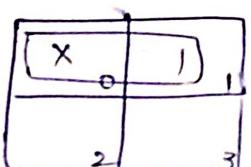
* $S = \sum m(2) + \sum d(3)$



$$S = D(n) \\ \begin{array}{r} 0 \\ 1 \\ 1 \\ \hline D \end{array}$$

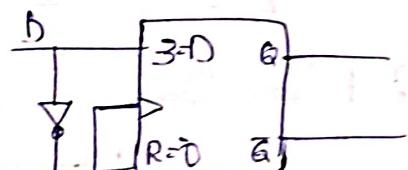
$$S = D.$$

* $R = \sum d(0) + \sum l(1)$



$$R = \overline{Q(n)} \\ \begin{array}{r} 0 \\ 1 \\ \hline \overline{Q(n)} \end{array}$$

$$R = \overline{Q(n)}$$



Graphic symbol

(2) SR to JK flip-flop

Step-1:-

= JK flip-flop characteristic table & from this
excitation table. \rightarrow characteristic Table of JK.

J	K	Q _n	Q _{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

\rightarrow excitation Table of SR.

$$S = \sum m(4,6) + \sum d(1,5)$$

		JK Q _n				
		00	01	11	10	
		0	0	1	3	2
		1	1	1	0	1

$$\begin{array}{r} \text{JKQ}_n \\ G_1 \Rightarrow 100 \\ 110 \\ \hline J\bar{Q}_n \end{array}$$

$$S = J\bar{Q}_n$$

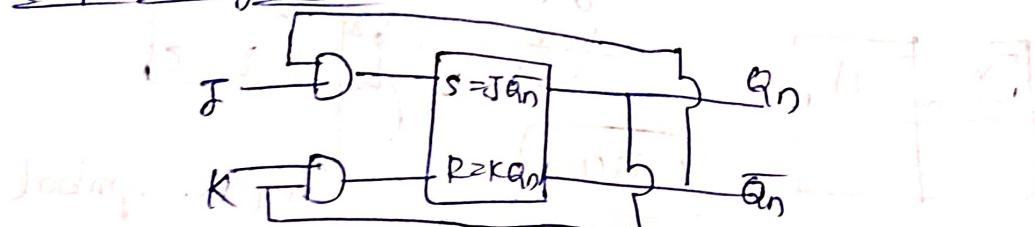
$$R = \sum m(3,7) + \sum d(0,2)$$

		JK Q _n				
		00	01	11	10	
		0	0	1	3	2
		1	1	1	0	1

$$\begin{array}{r} \text{JKQ}_n \\ G_1 \Rightarrow 011 \\ 111 \\ \hline K\bar{Q}_n \end{array}$$

$$R = K\bar{Q}_n$$

Graphic symbol:-



to T flip-flop:- characteristic table of T.

T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

Excitation table of SR

$$S = \sum d(1) + \sum (2)$$

ST	$Q(n)$
0	0 X 1
1	① 2 3

$$G_n = \sum (2)$$

$$\begin{matrix} T \\ Q(n) \\ 1 \\ 0 \\ \hline TQ_n \end{matrix}$$

$$S = TQ_n$$

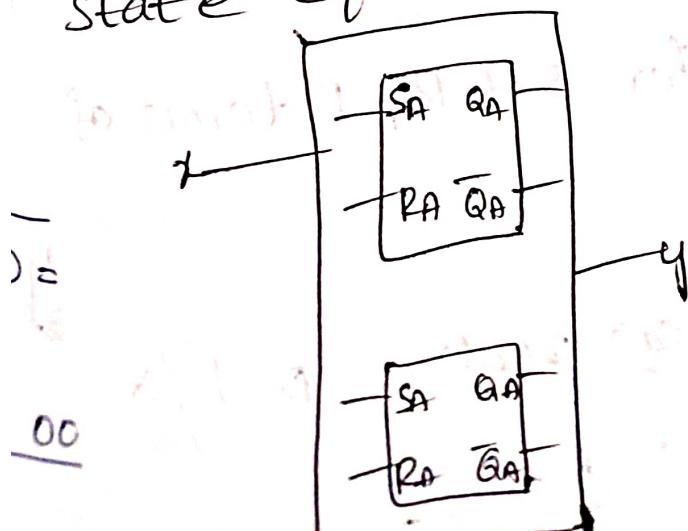
$$R = \sum d(0) + \sum (3)$$

$$G_1 = \sum (3)$$

$$TQ_n + Q_n \rightarrow R = TQ_n$$

$$\begin{matrix} 1 \\ 0 \\ \hline TQ_n \end{matrix}$$

⇒ Remaining conversions are also same procedure
 Introduction to state Table, state diagram &
 state equation.



The circuit have input & and output y.

stable state
 (same as truth table).

- By using stable state we can know the connection b/w input & output y .
- It tells the relation b/w present state, next state and o/p depending upon 'x' next state will change.

Stable state:-

present state	x input	next state	y output
Q_A	Q_B	Q_A^+ Q_B^+	
let us assume 0	0	1 0	1 0
assume 0	1	0 1	0 1

~~Conversions of flip-flops:-~~

(1) SR to D flip flop:-

Step-1:-

To realise D from SR draw the characteristic table for D flip flop.

Step-2:-

Using this characteristic table obtain the excitation table for SR flip flop.

Step-3:-

Obtain the equation for S & R in terms of D & Q(n) (present state)

Step-4:-

From the above obtained eq" realise D-P

(2) SR to JK flip-flop

Step-1:-

= JK flip-flop characteristic table & from this sp. excitation table. \rightarrow characteristic Table of JK.

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

\rightarrow excitation Table of SR.

$$S = \sum m(4,6) + \sum d(1,5)$$

		JKQ _n				
		00	01	11	10	
		0	0	1	3	2
J	K	4	5	7	6	

$$G_1 \Rightarrow \begin{array}{r} 100 \\ 110 \\ \hline JQ_n \end{array}$$

$$S = J\bar{Q}_n$$

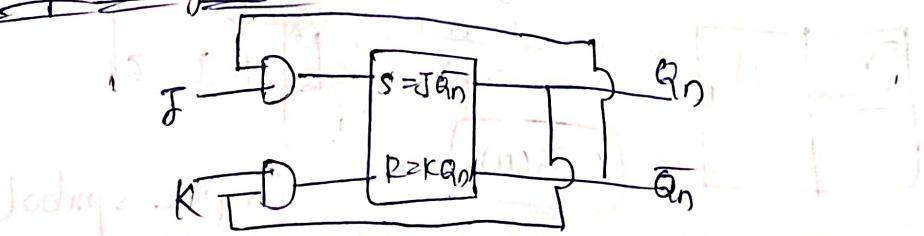
$$R = \sum m(3,7) + \sum d(0,2)$$

		JKQ _n				
		00	01	11	10	
		0	0	1	3	2
J	K	4	5	7	6	

$$G_1 \Rightarrow \begin{array}{r} 101 \\ 111 \\ \hline KQ_n \end{array}$$

$$R = KQ_n$$

Graphic symbol:-



Conversions of flip-flops

D flip-flop to SR flip-flop:-

Step-1:- S.R characteristic Table

S	R	Q _n	Q _{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

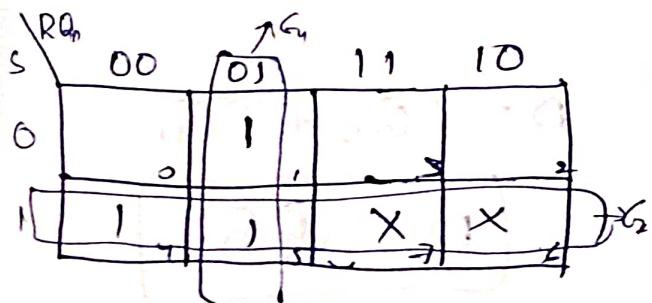
Step-2:- Excitation table of D.

S	R	Q _n	Q _{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	X	X
1	1	1	X	X

Q _n	Q _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

D excitation table:

$$D = \sum_{B} (1, 4, 5) + \sum_{d} (6, 7)$$



$$\therefore D = S + \overline{R} Q_n$$

$$G_1 = \begin{array}{l} S \quad R \quad Q_n \\ \hline 0 & 0 & 1 \\ 1 & 0 & 1 \end{array}$$

$$G_1 = (1, 5)$$

$$G_2 = (4, 5, 6, 7)$$

$$G_2 = \begin{array}{l} S \quad R \quad Q_n \\ \hline 1 & 0 & 0 \\ 1 & 0 & 1 \\ 1 & 0 & 0 \\ 1 & 1 & 1 \end{array}$$

$$G_2 = (S)$$

D flip-flop to JK flip-flop:-

J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

$$D = \sum_m (1, 4, 5, 6)$$

$$G_1 = J K Q_n$$

$$0, 0, 1.$$

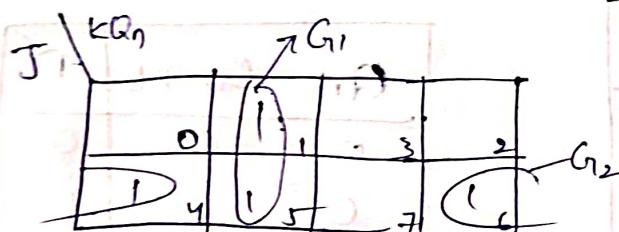
$$\underline{1, 0, 1}$$

$$\underline{\underline{E} Q_n}$$

$$G_1 = \sum_m (1, 5)$$

$$G_2 = (4, 6)$$

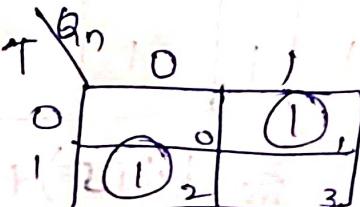
$$G_2 = \begin{array}{l} J K Q_n \\ 1 0 0 \\ \hline 1 1 0 \\ J Q_n \end{array}$$



D flip-flop to T flip-flop:-

T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

$$D = \sum_m (1, 2)$$



$$D = T Q_n + T \bar{Q}_n$$

$$D = T \oplus Q_n$$

(c) JK to SR flip flop:-

S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	X	X
1	1	1	X	X	X

$$J = \sum_m (4) + \sum_s (1, 3, 5, 6, 7)$$

$$K = \sum_m (3) + \sum_s (0, 2, 4, 6, 7)$$

F

$G_1 : (4, 5, 6, 7)$

S	R	Q_n	00	01	11	10
0	0	0	0	X	1	3
1	0	1	1	X	X	X

$\rightarrow G_1$

S	R	Q_n	00	01	11	10
0	0	0	0	1	3	2
1	0	1	1	X	X	X

$\rightarrow Q_1$

S	R	Q_n	00	01	11	10
0	0	0	0	1	3	X
1	0	1	1	X	X	X

$\rightarrow G_2$

S	R	Q_n	00	01	11	10
0	0	0	0	1	3	2
1	0	1	1	X	X	X

$\rightarrow Q_2$

S	R	Q_n
1	0	0
1	0	1
1	1	1

$$\boxed{J = S}$$

$$G_2 : (2, 3, 6, 7)$$

S	R	Q_n
0	1	0
0	1	1
1	1	0

$$\boxed{K = R}$$

$$\therefore J = S \text{ & } K = R$$

JK flip flop to D flip flop:- $J = \sum_m (2) + \sum_s (1, 3)$

D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

D	Q_n	Q_{n+1}
0	0	1
1	1	X

$$G_1 : (2, 3)$$

$$D \cdot Q_n$$

$$1 \cdot 0$$

$$1 \cdot 1$$

$$\frac{D}{D}$$

$$\therefore J = D$$

$$k = \sum_m (1) + \sum_d (0, 1) \quad G_1 = (0, 1) \Rightarrow \begin{array}{r} D \quad Q_n \\ 0 \quad 0 \\ 0 \quad 1 \\ \hline \bar{D} \end{array}$$

D	Q_n	0	1
0	\boxed{x}	0	1
1	x	2	2

$\therefore k = 5$

JK flip flop to T flip flop

T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

$$J = \sum_m (2) + \sum_d (1, 3)$$

$$K = \sum_m (3) + \sum_d (0, 2)$$

T	Q_n	0	1
0	\boxed{x}	0	1
1	$\boxed{1}$	X	2

$$G_2 = (2, 3)$$

$$\begin{array}{r} T \quad Q_n \\ 0 \quad 0 \\ 1 \quad 0 \\ \hline T \end{array}$$

$$J = T$$

T	Q_n	0	1
0	\boxed{x}	0	1
1	$\boxed{1}$	3	X

$$G_1 = (2, 3)$$

$$\begin{array}{r} T \quad Q_n \\ 1 \quad 0 \\ 1 \quad 1 \\ \hline T \end{array}$$

$$K = T$$

St

Registers

Register is a set of flip-flops used to store the binary data and which has a common clock to each one and capable of storing 1 bit of information.

⇒ An 'n' bit register consists of a group of n flip-flops and capable of storing n bits of binary data.

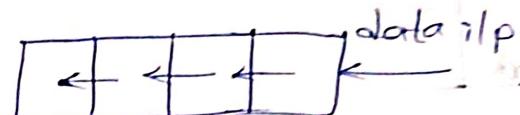
Shift Register:-

⇒ A register capable of shifting the binary information in each cell to its next cell in a selected direction is called shift registers.

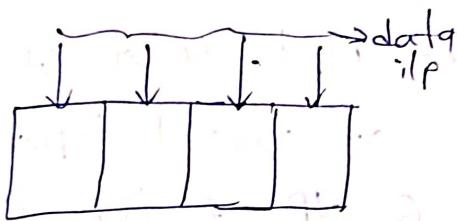
Data transmission in shift Register:-



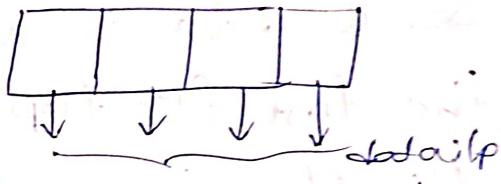
a) serial shift right



b) serial shift left.



c) parallel shift in



d) parallel shift out.

⇒ Basically, there are 4 different types of shift registers are there.

(1) serial in serial out register (SISO)

(2) serial in, like out register (SIPO)

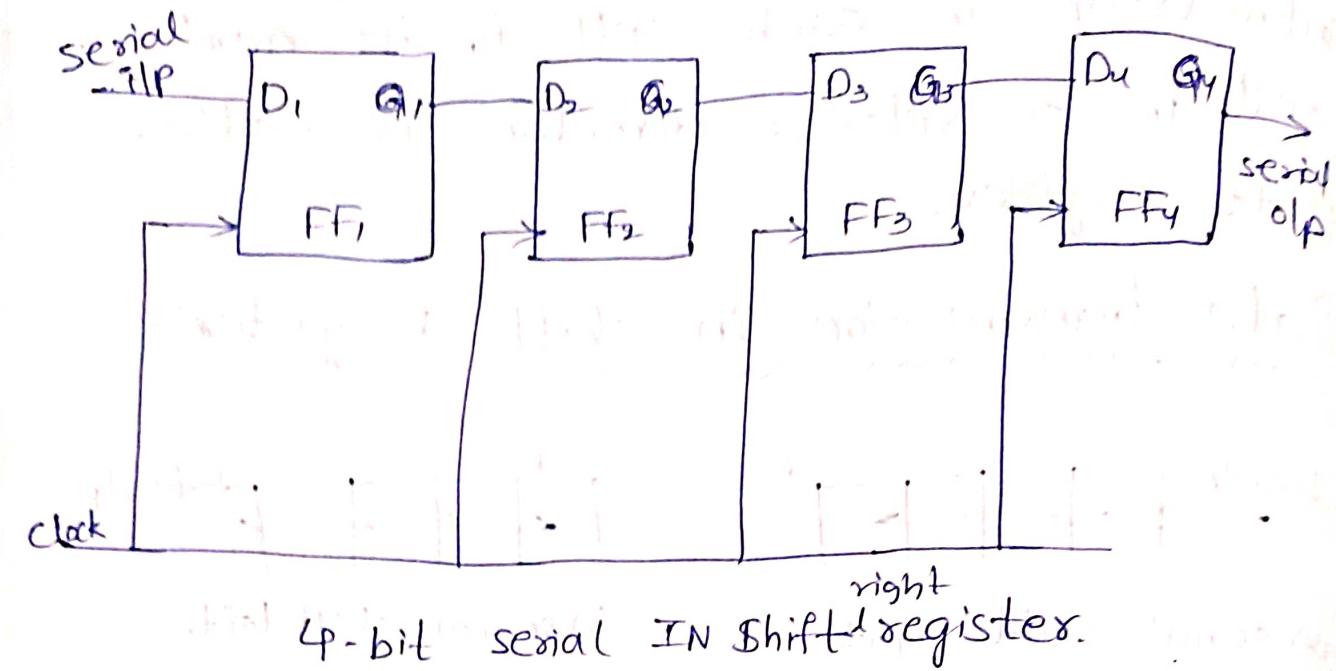
(3) Parallel in serial out register (PISO)

(4) Parallel in, like out register (PIPO)

⇒ Serial in serial out register with shift right:-

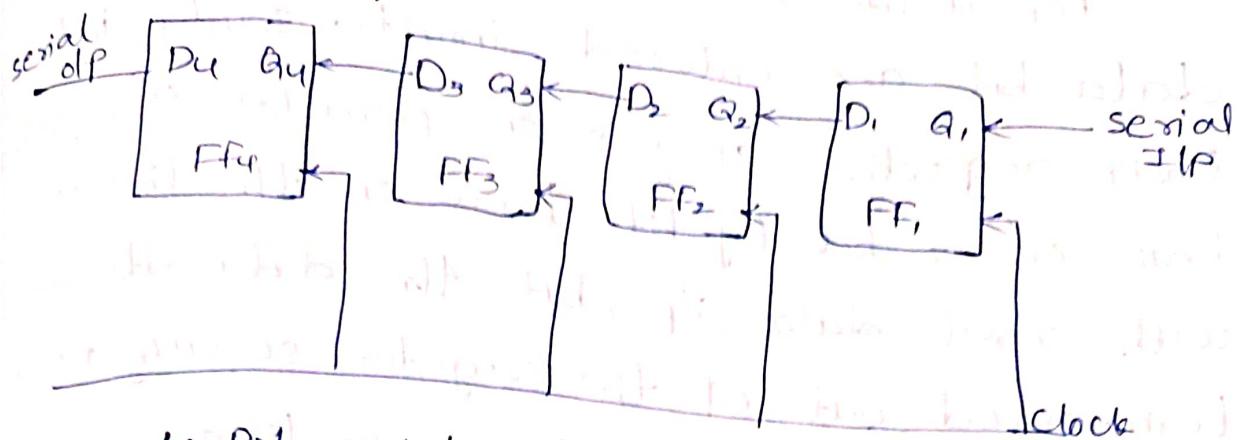
⇒ This type of shift registers accepts data serially i.e; 1 bit at a time and also outputs data serially.

Logic diagram:-



- ⇒ The register can store upto 4 bits of data.
- ⇒ Serial data is applied at the D input of the first flip-flop and Q o/p of the first flip-flop is connected to the D i/p of 2nd flip-flop.
- ⇒ The o/p of 2nd FF is connected to the D i/p of 3rd FF and Q o/p of 3rd FF is D i/p of 4th FF and the data is o/p from the Q terminal of the last flip-flop.
- ⇒ When serial data is transferred into registers each new bit clocked into the first FF at the +ve edge of each clk pulse.

Serial in serial out register with left shift

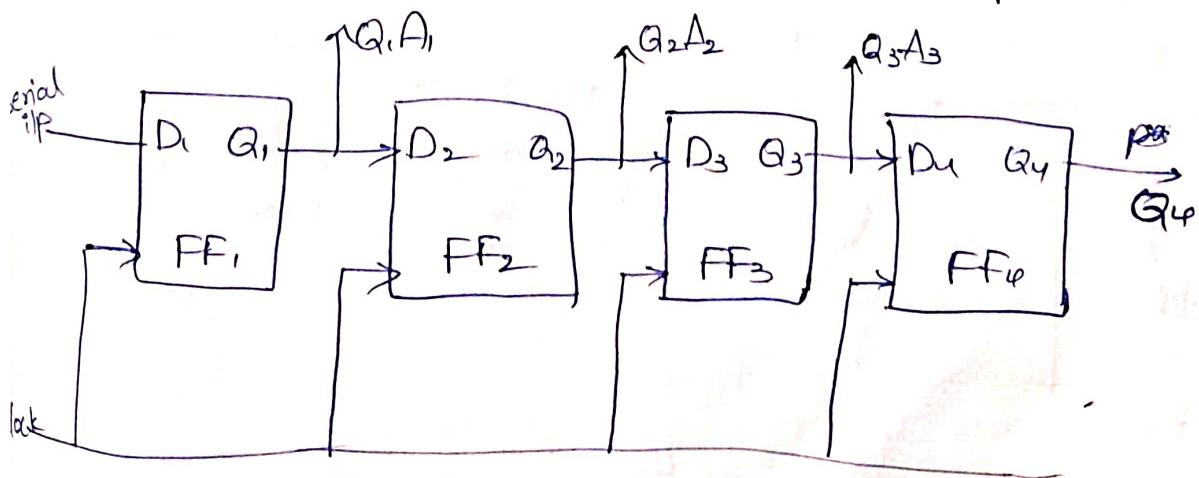


4 Bit serial out shift register.

(b) Serial in parallel out register:-

⇒ In these registers data bits are entered into the registers serially but the data stored in the register is shifted out in the form.

⇒ Once the data bits are stored each bit appears on its respective output line & all bits are available simultaneously on a bit-by-bit with the serial o/p

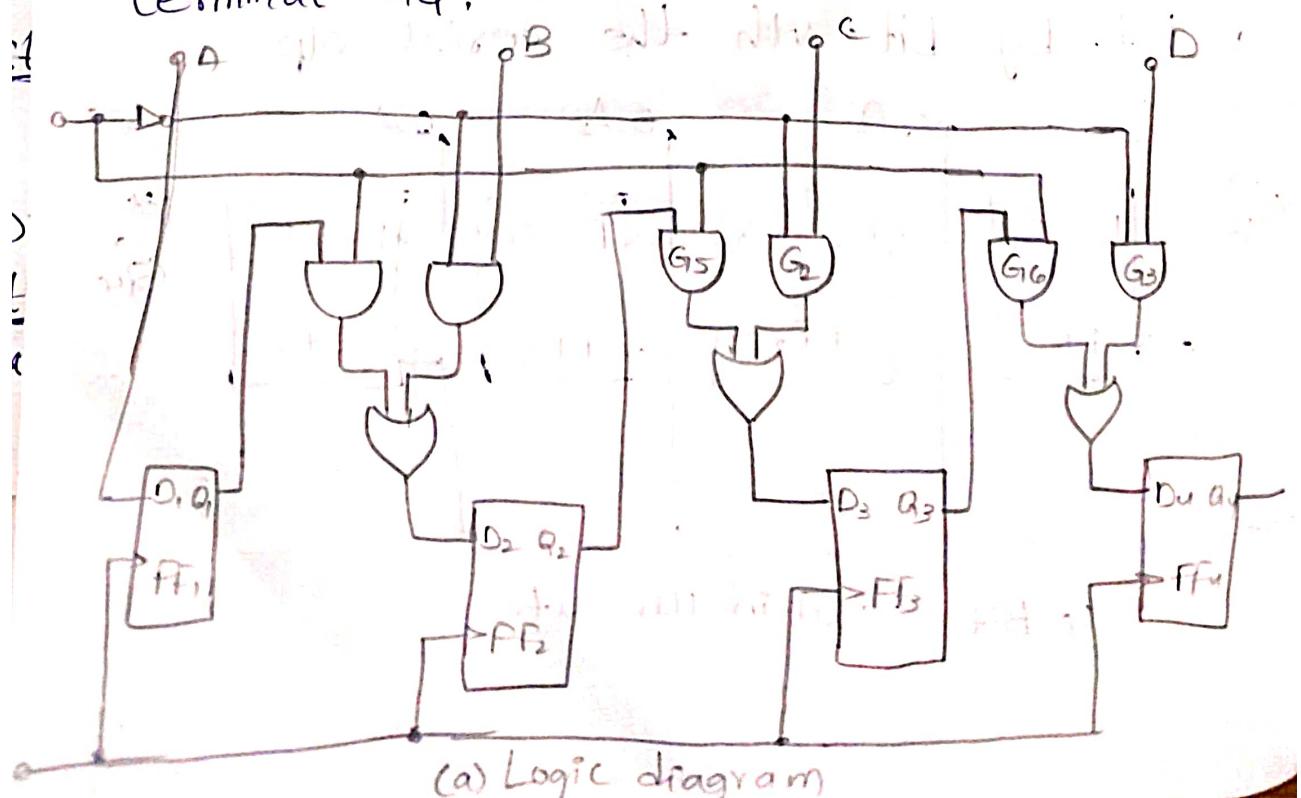


4 Bit serial in parallel out.

(3) Parallel in serial out register!

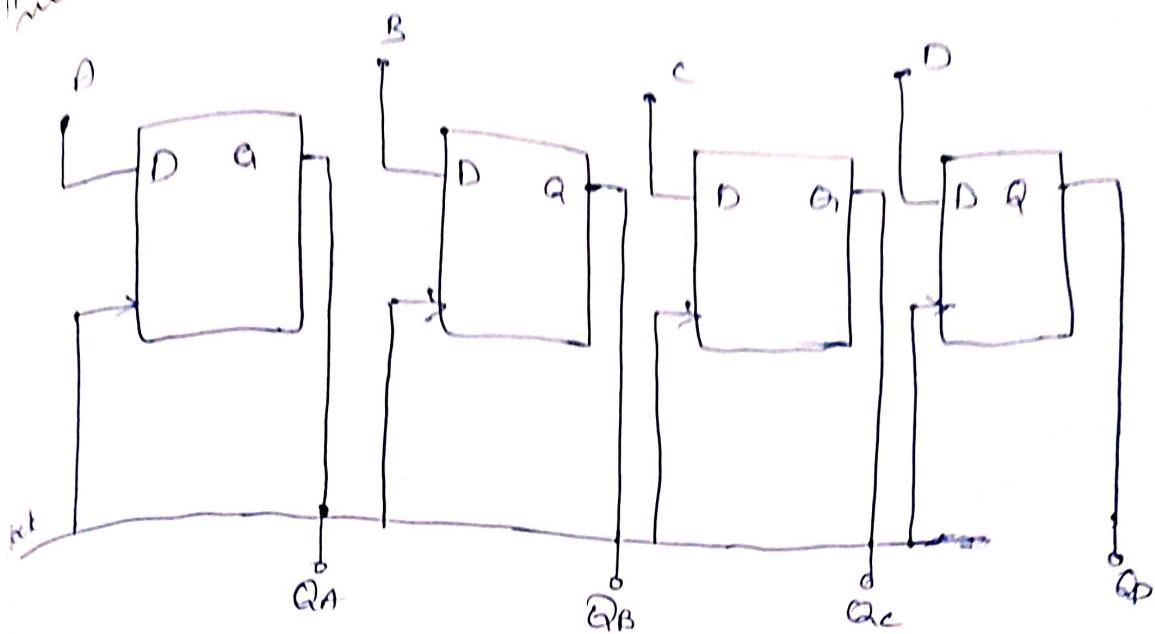
For a ~~line~~-in, serial-out, shift register, the data bits are entered simultaneously into their respective stages on parallel lines, rather than on a bit-by-bit basis on the line as with serial data ips, but the data bits are transferred out of the register serially, i.e., on a bit-by-bit basis over a single line.

Figure illustrates a 4-bit parallel-in-serial-out, shift register using DFFs. There are four data lines A, B, C & D through which the data is entered into the register in parallel form. The signal shift / LOAD allows (a) the data to be entered in parallel form into the register and (b) the data to be shifted out serially from terminal Q_4 .



(a) Logic diagram

Parallel in parallel out shift register

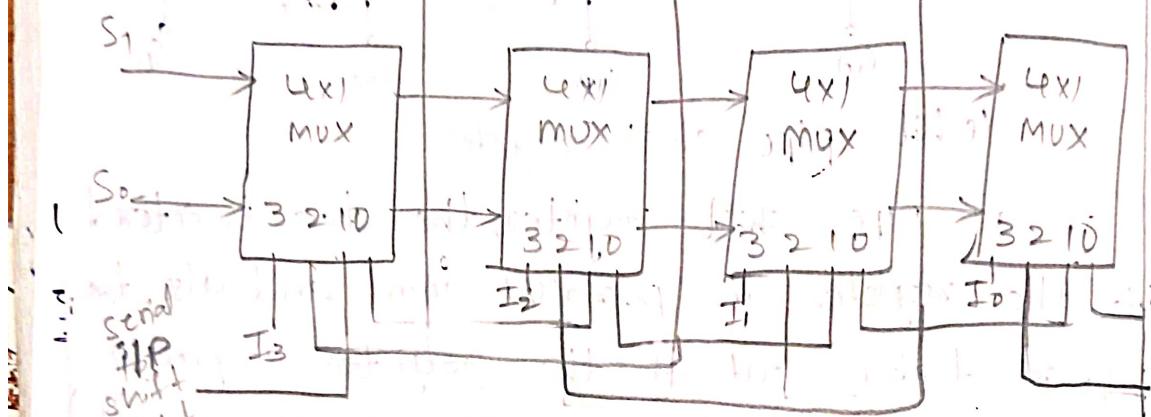
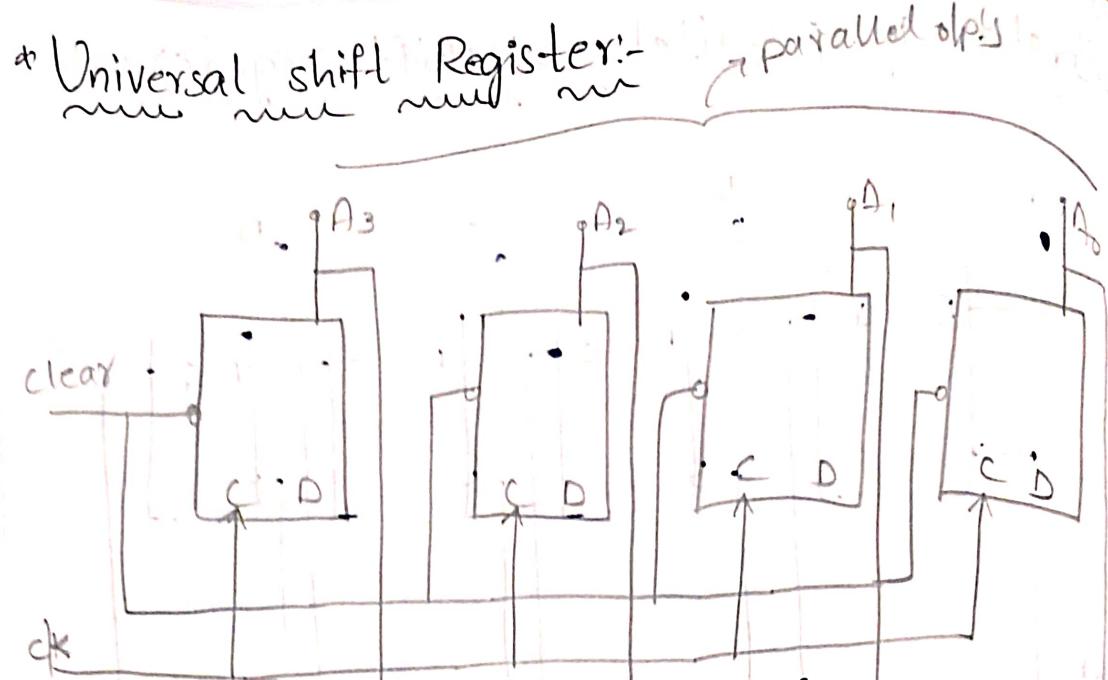


4-bit PIPD shift register.

In a PIPD shift register, the data is entered into the register in parallel form and also the data is taken out of the register in parallel form. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.

Figure shows a 4-bit PIPD shift register using D-FF's. When a data bit, D_{in} , is applied to the $D_{in/p}$ terminals of the FF's, when a clock pulse is applied at the +ve going edge of that pulse the $D_{in/p}$'s are shifted into the $Q_{out/p}$ of the FFs. The register now stores the data. The stored data is available instantaneously for shifting out in parallel form.

Input Address	1	0
Bit Address	1	0
Serial Address	1	0



S₁ ⇒ It is a bidirectional shift register whose ilp's can be in either series form or.

C parallel form and olp can be either

S₁ & S₀ serial or parallel form.

⇒ It consists of 4 D-flipflops along with 4 multiplexers having with 2 common selected lines for all the multiplexers with the operations

S ₁	S ₀	Register operation
0	0	no change
0	1	shift right
1	0	shift left
1	1	parallel loads

Operation:-

Case-1:- When $S_0 S_1 S_0 = 0,0,0$, the ilp '0' of each multiplexer is selected when $S_1 S_0 = 0,0$. Here, the present state value of the register is applied to the D-ilps of the each flip-flop.

→ This condition forms a path from the ilp of each flip flop to ilp of same FF. Hence no change takes place.

Case-2:-

when $S_1 S_0 = 0,1$. The ilps selected in each multiplexer when $S_1 S_0 = 0,1$. Here, the terminal '1' of multiplexers ilp's have a path to D-ilps of the FF, which causes shift right operation with serial ilp to the D-FF.

Case-3:-

When $S_1 S_0 = 1,0$. The ilp of a register with left shift operation which results in serial ilp of each D-FF.

Case-4:-

When $S_1 S_0 = 1,1$. The binary information on the ilp lines is transferred into the register simultaneously during the next clock edge.

Counters:-

A counter is a register capable of counting the no:of clock pulse that have arrived at the i/p of clock signal.

⇒ It is a device which stores the no:of times a particular event or process as occurred in relation to the clock signal.

⇒ A digital counter is a set of FF's whose state changes in response to clock pulses applied at the i/p of the counter.

⇒ There are two types of counters.

(1) Asynchronous counter / Ripple counter

(2) Synchronous counter

Mod-N counters:-

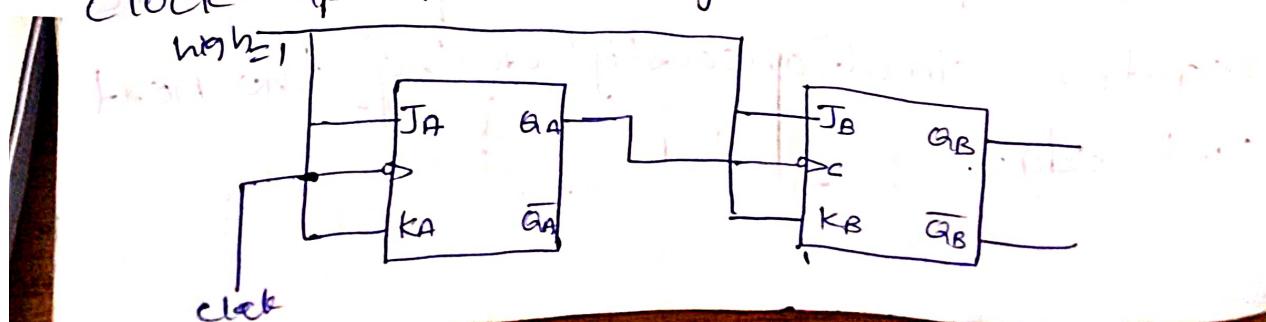
N = no:of states required to counter.

$N \leq 2^n$

where, n = no:of FF's.

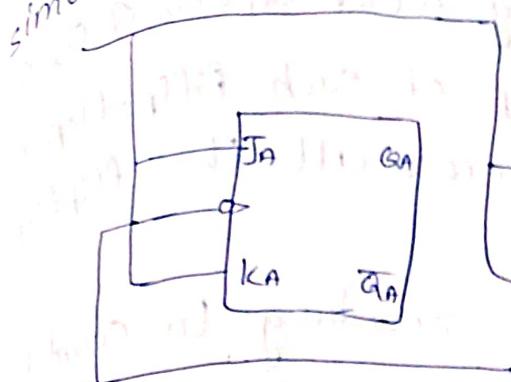
(1) Asynchronous counter:-

This counter consists of series of FF's connected with the o/p of each FF connected to the clock i/p of next higher order of FF.



Synchronous counters-

In synchronous counter, clock is given simultaneously to all the flip-flops.



Difference b/w synchronous and Asynchronous counters.

Asynchronous counter

In this counter the output of first FF drives the clock for the next FF.

All the FF's are not clocked simultaneously.

Logic circuit is very simple to design & low speed.

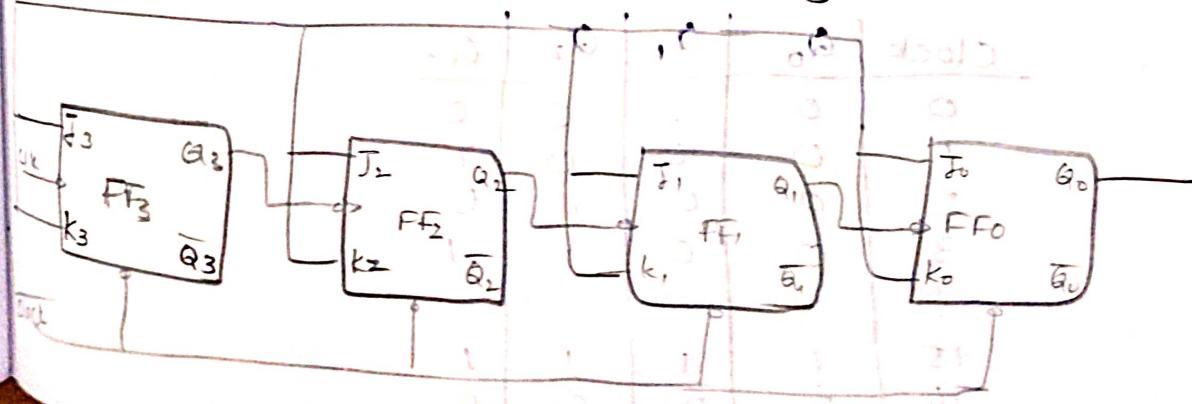
Synchronous counter

In this counter, there is no connection b/w output of first FF and clock input of the next FF.

All the FF's are clocked simultaneously.

Complex to design and high speed.

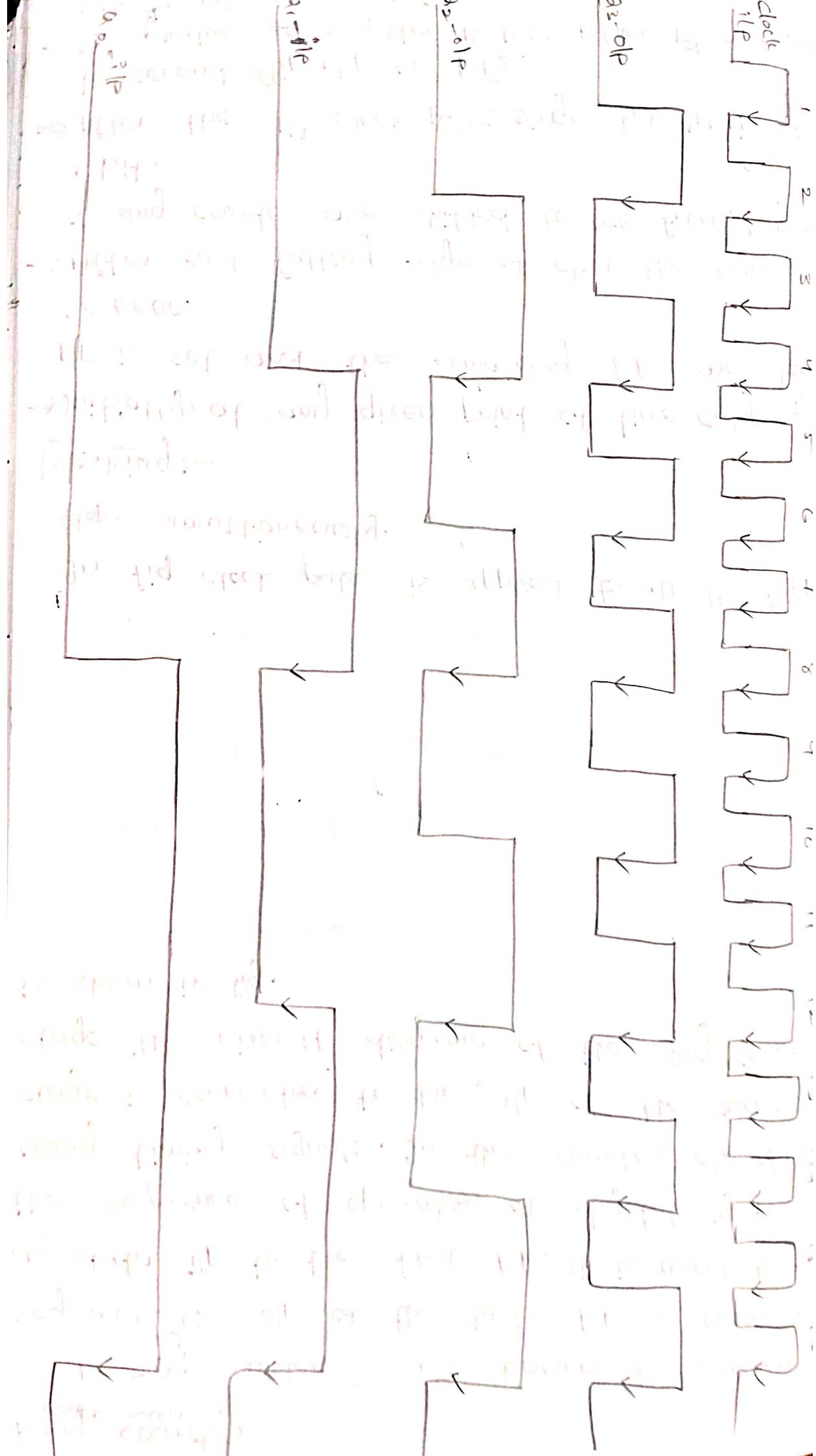
Ripple counter- [Mod 16 counter]



Operations-

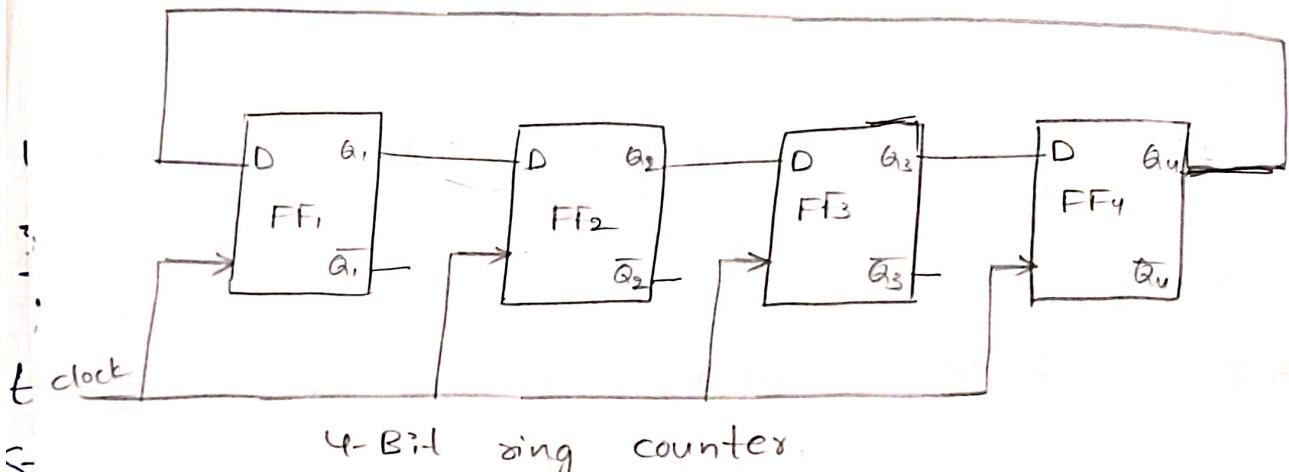
- ⇒ The clock is connected to flip flop 3 and the FF₃ is triggered by the o/p of FF₃ [Q₃] and so on. Hence the o/p as a binary word Q₁=Q₀ Q₂ Q₃.
- ⇒ When clear=0 then the dp of each flip-flop in digital word is Q₁=0000 becoz all the flipflops are in reset condition.
- ⇒ When clear=1 the counter reading to count the clock pulse since flip flop 3 receives each clock pulse. So Q₃ toggles on per for every -ve large edge.
- 1 ⇒ When 1st clock pulse is applied.
- 2 ⇒ When clockpulse is Applied Q₃=1 this o/p is applied to clock of the flip flop Q.
- t ⇒ Hence the o/p's of remaining flipflop are unchanged i.e Q₂, Q₁, Q₀=0.
- c: 3 ⇒ When 2nd clock pulse, is applied the FF₃ is toggle from high to low i.e; Q₃=0 which is applied to second flip flop that.
- S1 ⇒ Makes 2 flipflop to toggle and Q₁ Q₀ are unchanged.
- D ⇒ This process repeats till 15th clockpulse and at 16th clockpulse the o/p of flipflops are 0000.

Clock	Q ₀	Q ₁	Q ₂	Q ₃
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	1	1	1	1
5	1	1	1	1
15	1	1	1	1
16	0	0	0	0



Ring counter:-

A ring counter is also known as circuit shift register. The output of the last FF is connected as data input to the first FF. It is used to control the sequence of operation of digital system by using timing signals. In this counter, output of each stage is connected to the input of the successive stage. The circuit diagram of the ring counter is shown in fig.



4-Bit ring counter.

In fig. clock pulse is applied to all the flip-flops simultaneously.

Working:-

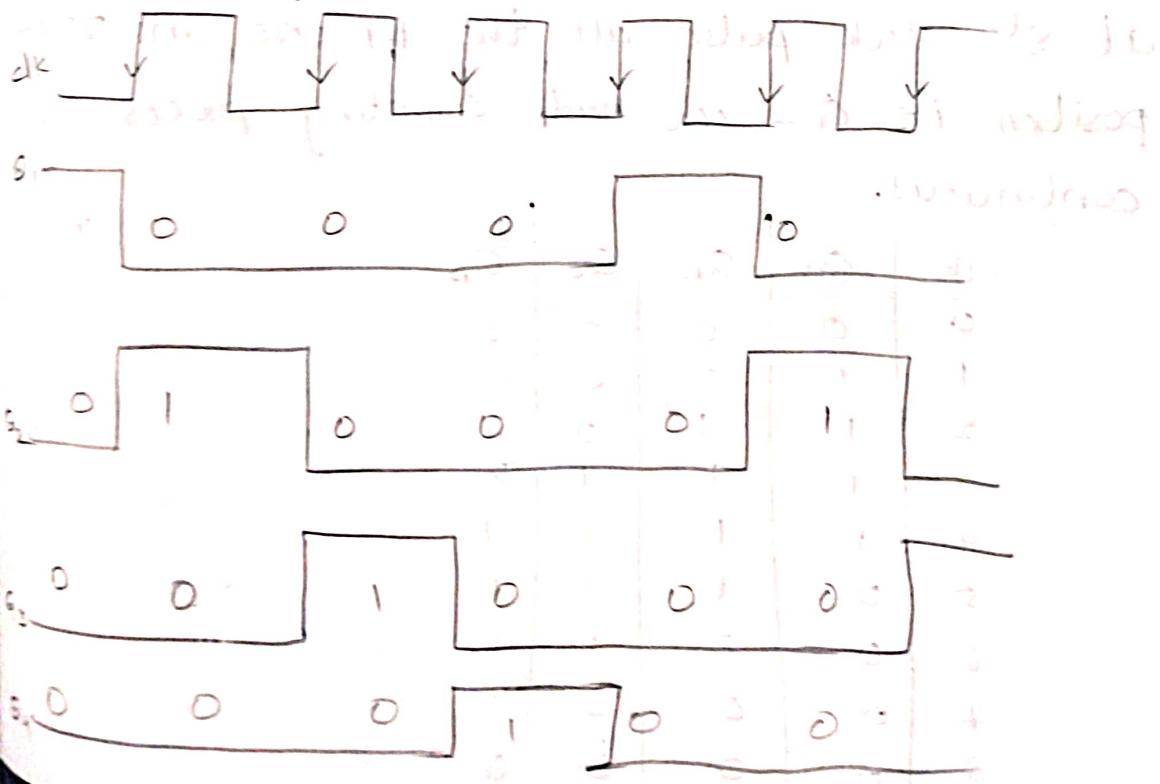
- ⇒ Initially, at any given point of time, only one FF is set and the remaining FF's are cleared i.e. 0000.
- ⇒ After each falling edge of clock, the contents of ring counter are shifted to MSB from LSB by 1 bit.
- ⇒ After the 1st clock pulse, single bit '1' is shifted to second flip-flop i.e. FF₂.

⇒ The value of register is 1000. After 1st clock pulse, it is initially shifted to Q₃.

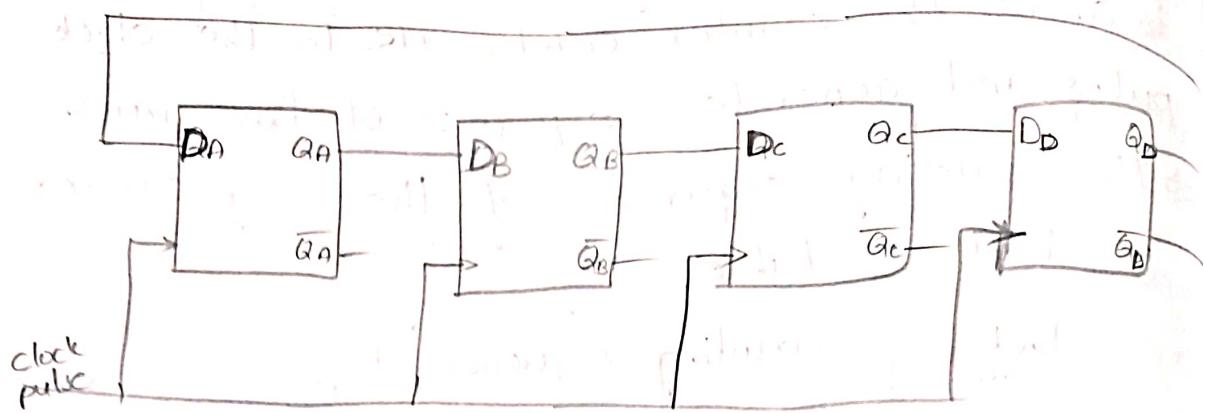
- After the 2nd clockpulse, Q1 is shifted to Q2 and at the end of 4th clock pulse Q1 is again shifted to Q3 i.e. the counter counts according to the clock pulses and generates sequence of four states.
- The counting sequence of the ring counter is shown in table.

clock	counting sequence			
	Q1	Q2	Q3	Q4
0	1	0	0	0
1	0	1	0	0
2	1	0	1	0
3	0	0	1	0
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1

The timing diagram of a ring counter is as shown in fig.



Johnson's counter / Twisted ring counter:-



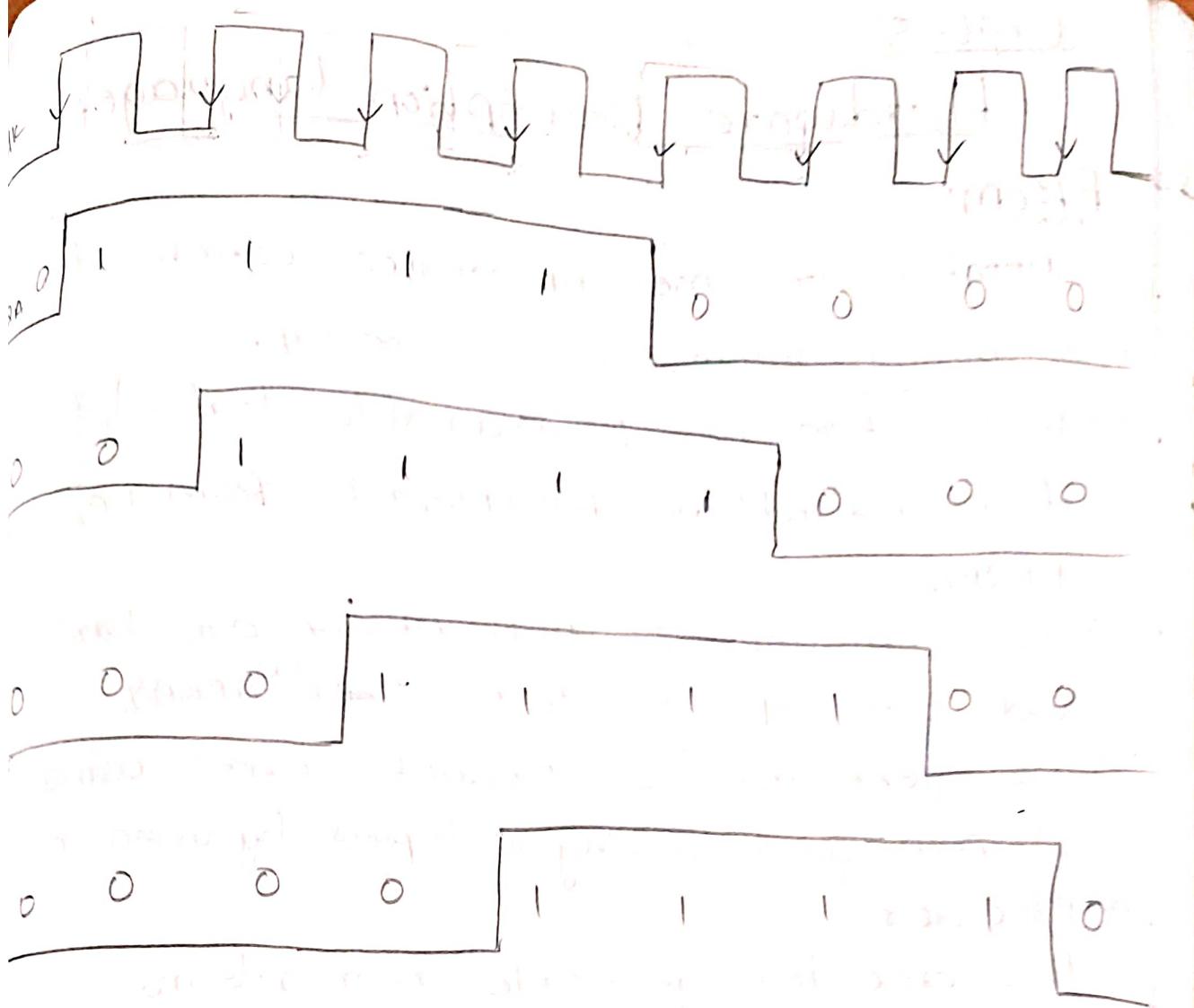
⇒ In Johnson's counter, the o/p Q of each FF is connected to i/p of the next FF except the complimented o/p of the last FF \bar{Q}_D is connected to the i/p of the 1st FF.

⇒ When clock is low all the FFs are in reset position i.e; $Q = 0000$.

⇒ When 1st clock pulse is applied the complimented o/p of last FF is applied to the o/p of 1st FF.
Then $Q = 1000$.

⇒ The process repeats till 7th clock pulse and at 8th clock pulse all the FF are in reset position i.e; $Q = 0000$ and counting process is continuous.

clk	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0



Assignment - 3 :-

- 1) Explain the working of a master-slave JK FF.
- 2) Convert T-FF to D-FF with relevant truth tables and expressions.
- 3) Explain the working of a universal shift register.
- 4) Explain the working of a Johnson counter.
- 5) Explain positive edge triggering triggered S-R Flip-flop.