Code: 20A04505

R20

B.Tech III Year I Semester (R20) Supplementary Examinations August 2023

DIGITAL ELECTRONICS

(Common to CE, ME and FT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a)	Draw the NOR gate using NAND Gate.	2M
(b)	Perform $(932)_{10} - (725)_{10}$ using 10's complement method.	2M
(c)	Distinguish between the binary parallel adder and carry look ahead adder.	2M
(d)	Draw Full Adder and Full Subtractor.	2M
(e)	Distinguish between latch and flip-flop.	2M
(f)	Denote a 2-bit down counter with a state diagram.	2M
(g)	What are the different types of ROM's?	2M
(h)	What is Programmable Logic Array?	2M
(i)	Write any two advantages of TTL.	2M
(j)	Draw the diagram of CMOS logic family.	2M

PART – B

(Answer all the questions: 05 X 10 = 50 Marks)

2 Obtain minimal SOP expression for the Boolean function; 10M
F = ∑m (0, 5, 7, 8, 9, 10, 11, 14, 15) using K-map, and realize using NAND and NOR gates.

OR

3 Perform the following operations: 10M
(i) $(231)_{10} - (159)_{10}$ using 9's complement method.
(ii) $(111001)_2 - (100111)_2$ using 2's complement method.
(iii) Reduce the Boolean expression into three literals.
$F = \overline{\left(\overline{\overline{X}\,\overline{Y} + Z}\right)} + Z + XY + WZ$

4 Realize F (A, B, C, D) = ∑m (1, 3, 4, 11, 12, 13, 14, 15) using 8x1 MUX. 10M

OR

5 Design and implement a full adder circuit using 3:8 decoder. 10M

6 Find the characteristic equations for SR flip-flop, T flip-flop, D flip-flop and JK flip-flop. 10M

OR

7 Design a 4-bit universal shift register using multiplexers and flip flops. 10M

8 Realize the given functions using PLA; 10M
(i) F_1 (P, Q, R) = ∑m (2, 3, 4, 6, 7) (ii) F_2 (P, Q, R) = ∑m (1, 3, 5, 7).

OR

9 Write short notes on: 10M
(i) PAL (ii) FPGA (iii) EAPROM (iv) Static and Dynamic RAM.

10 Discuss Emitter coupled logic circuit working, features, and applications with a suitable diagram. 10M

OR

11 Compare different logic families using the following parameters. 10M
(i) Fan-in (ii) Fan-out (iii) noise margin (iv) power dissipation (v) propagation delay.

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