1. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is

a) AND

b) NAND

c) NOR

d) OR

2. In 2's complement form, 10010011 represents

a) -109

b) +109

c) -91

d) +91

3. Which one of the following expressions does not represent exclusive NOR of x and y

a) xy+x'y'

b) $x \oplus y'$

c) $x' \oplus y$

d) $x' \oplus y'$

4. Define the connective * for the Boolean variables X and Y as: X * Y = XY + X' Y'. Let Z = X * Y. Consider the following expressions P, Q and R.

P: X = Y⋆Z

Q: Y = X⋆Z

R: X⋆Y⋆Z=1

Which of the following is TRUE?

a) Only P and Q are valid

b) Only Q and R are valid.

c) Only Q and R are valid.

d) All P, Q, R are valid.

5. Which digital system translates coded characters into a more useful form?

a) Encoder

b) Decoder

c) Counter

d) Display

6. An AND gate has two inputs A and B and one inhibit input S, Output is 1 if

a) A = 1, B = 1, S = 1

b) A = 1, B = 1, S = 0

c) A = 1, B = 0, S = 1

d) A = 1, B = 0, S = 0

7. In a BCD to 7 segment decoder the minimum and maximum number of outputs active at any time is ….

a) 2 and 7

b) 3 and 7

c) 1 and 6

d) 3 and 6

8. In a BCD-to-seven-segment converter, why must a code converter be utilized?

a) To convert the 4-bit BCD into 7-bit code

b) To convert the 4-bit BCD into 10-bit code

c) To convert the 4-bit BCD into gray code

d) No conversion is necessary

9. Max term designation for A + B + C is

a) M0

b) M1

c) M3

d) M4

10. How many gates would be required to implement the following Boolean expression after simplification? XY + X(X + Z) + Y(X + Z)

a) 1

b) 2

c) 4

d) 5

11. Which of the examples below expresses the distributive law of Boolean algebra?

a) (A + B) + C = A + (B + C)

b) A(B + C) = AB + AC

c) A + (B + C) = AB + AC

d) A(BC) = (AB) + C

12. CMOS logic dissipates _____ power than NMOS logic circuits

a) More

b) Less

c) Equal

d) None of the Mentioned

13. TTL stands for

a) Transistor Transistor logic

b) Tristate Transistor logic

c) Transistor Tristate logic

d) Tristate Tristate logic

14. Which of the following combinations of logic gates can decode binary 1101?

a) One 4-input AND gate.

b) One 4-input AND gate, one OR gate.

c) One 4-input NAND gate, one inverter.

d) One 4-input AND gate, one inverter

15. Which of the following expressions is in the product-of-sums form?

a) (A + B)(C + D)

b) (AB)(CD)

c) AB(CD)

d) AB + CD

16. The complex programmable logic device (CPLD) features _____ type of memory.

a) Volatile

b) Nonvolatile

c) EPROM

d) Volatile EPROM

17. Most look-up tables in field-programmable gate arrays (FGPAs) use _____ inputs, resulting in _____ possible outputs.

a) 4,16

b) 8,16

c) 4,12

d) 6,12

18. To implement the expression AB+BC+CA, how many gates are needed

a) Three AND gates and two OR gates

b) Three AND gates and four inverters

c) Three AND gates

d) One AND gate

19. A binary code that progresses such that only one bit changes between two successive codes is

a) Nine's-complement code

b) 8421 code

c) Excess-3 code

d) Gray code

20. In an aircraft there are three lavatories, each lavatory has a sensor outputting 1 if the lavatory door is locked, 0 otherwise.Obtain the Boolean expression for the Aircraft lavatory sign circuit that outputs lavatory available sign by setting the circuits output to 1

a) A + B

b) B+C

c) A’+ B+ C

d) A’+B’+C’

21. The main stairway in a block of flats has two switches for controlling the lights. Switch A is located at the top of the stairs, and switch B is positioned at the bottom of the stairs. The light is ON when both switches are in the same position, the light is OFF otherwise. Obtain the Boolean expression to control the light on the staircase.

a) A + B

b) AB + A’B’

c) A’+ B+ C

d) A’+B’+C’

22. The Universal gates are

a) AND,OR

b) NAND, NOR

c) XOR, XNOR

d) NOR, OR

23. A typical TTL gate has a fan-out of

a) 2

b) 4

c) 10

d) 3

24. Assume a 4 X 1 Multiplexer's four inputs presently have the following values i0 = 1, i1 = 1, i2 = 0, and i3 = 0 . What would be the output of MUX for the select input 11?

a) 11

b) 0

c) 1

d) 10

25. How many select lines are there in a 16 X 1 MUX?

a) 1

b) 2

c) 3

d) 4

26. Convert binary 111111110010 to hexadecimal.

a) EE2

b) FF2

c) 2FE

d) FD2

27. Convert the binary number 1001.0010 to decimal

a) 90.125

b) 9.125

c) 125

d) 12.5

28. Which of the following is the most widely used alphanumeric code for computer input and output?

a) Gray

b) ASCII

c) Parity

d) EBCDIC

29. If a typical PC uses a 20-bit address code, how much memory can the CPU address?

a) 20 MB

b) 10 MB

c) 1 MB

d) 580 MB

30. Assign the proper odd parity bit to the code 111001.

a) 1111011

b) 1111001

c) 0111111

d) 0011111

31. A binary number's value changes most drastically when the _____ is changed.

a) MSB

b) frequency

c) LSB

d) duty cycle

32. The sum of the two BCD numbers, 0111 + 0011, is _____.

a) 1001

b) 0111

c) 0011

d) 1100

33. Convert 1100101000110101 to hexadecimal.

a) 121035

b) CA35

c) 53AC1

d) 530121

34. Two's complement of decimal 111 is _____.

a) 0001011

b) 0001100

c) 0010001

d) 0010010

35. Convert the binary number 1100 to Gray code.

a) 0011

b) 1010

c) 1100

d) 1001

36. Which of the following is an invalid BCD code?

a) 0011

b) 1101

c) 0101

d) 1001

37. Determine the decimal equivalent of the signed binary number 11110100 in 1's complement.

a) 116

b) –12

c) 11

d) 128

38. In Boolean algebra, the word "literal" means _____.

a) a product term

b) all the variables in a Boolean expression

c) the inverse function

d) a variable or its complement

39. An AND gate with schematic "bubbles" on its inputs performs the same function as a(n)_____ gate.

a) NOT

b) OR

c) NOR

d) NAND

40. How many two input gates would be required to implement the following Boolean expression before simplification? XY + X(X + Z) + Y(X + Z)

a) 1

b) 2

c) 4

d) 5

41. What is the primary motivation for using Boolean algebra to simplify logic expressions?

a) It may make it easier to understand the overall function of the circuit.

b) It may reduce the number of gates.

c) It may reduce the number of inputs required.

d) all of the three options

42. AC + ABC in reduced form is equal to

a) 1

b) 0

c) ABC

d) AC

43. When A' B ' are the inputs to a NAND gate, according to De Morgan's theorem, the output expression could be:

a) X = A + B

b) X=(AB)'

c) X = (A)(B)

d) X=AB'

44. Applying DeMorgan's theorem to the expression ((X+Y)'+Z ') ' , we get _____

a) (X+Y)Z

b) (X '+Y')Z

c) (X+Y)Z '

d) (X '+Y')Z'

45. According to Boolean law, A+AB represents

a) A

b) B

c) 1

d) 0

46. Use Boolean algebra to find the most simplified SOP expression for F = ABD + CD + ACD + ABC + ABCD.

a) F = ABD + ABC + CD

b) F = CD + AD

c) F = BC + AB

d) F = AC + AD

47. Which of the examples below expresses the distributive law of Boolean algebra?

a) (A + B) + C = A + (B + C)

b) A(B + C) = AB + AC

c) A + (B + C) = AB + AC

d) A(BC) = (AB) + C

48. An OR gate with schematic "bubbles" on its inputs performs the same functions as a(n)_____ gate.

a) NOR

b) OR

c) NOT

d) NAND

49. Which of the following combinations cannot be combined into K-map groups?

a) corners in the same row

b) corners in the same column

c) diagonal

d) overlapping combinations

50. AND operation can be produced with

a) 2 NAND gates

b) 3 NAND gates

c) 1 NOR gate

d) 3 NOR gates

51. When four 1s are taken as a group on a Karnaugh map, the number of variables eliminated from the output expression is _____.

a) 1

b) 2

c) 3

d) 4

52. A certain digital-to-analog converter has a step size of 0.25V and a full-scale output of 7.75V. Determine the percent of resolution and the number of input binary bits.

a) 3.23% 5 bits

b) 3.23% 4 bits

c) 31% 4 bits

d) 31% 5 bits

53. An actuator is usually a device that:

a) converts analog data to meaningful digital data.

b) stores digital data and then processes that data according to a set of specified instructions.

c) controls a physical variable.

d) is a microprocessor

54. When comparing the conversions from digital-to-analog and analog-to-digital, the A/D conversion is generally:

a) more complicated and more time consuming than the D/A conversion.

b) less complicated but more time consuming than the D/A conversion.

c) more complicated but less time consuming than the D/A conversion.

d) less complicated and less time consuming than the D/A conversion.

55. The quantization error in an analog-to-digital converter can be reduced by:

a) decreasing the number of bits in the counter and increasing the number of bits in the DAC.

b) decreasing the number of bits in the counter and DAC.

c) increasing the number of bits in the counter and decreasing the number of bits in the DAC.

d) increasing the number of bits in the counter and DAC.

56. Two principal advantages of the Dual-Slope ADC are its:

a) high speed and low cost

b) high sensitivity to noise and low cost.

c) low sensitivity to noise and low cost.

d) low sensitivity to noise and high speed.

57. An analog quantity varies from 0-7V and is input to a 6-bit A/D converter. What analog value is represented by each step on the digital output?

a) 1.17V

b) 0.857V

c) 0.111V

d) 0.109V

58. What is the major advantage of the R/2R ladder DAC as compared to a binary-weighted-input DAC?

a) The virtual ground is eliminated and the circuit is therefore easier to understand and troubleshoot.

b) It has fewer parts for the same number of inputs.

c) It uses only two different resistor values.

d) Its operation is much more easily analyzed.

59. What is the percentage resolution of a D/A converter?

a) It is the deviation between the ideal straight-line output and the actual output of the converter expressed as a percentage.

b) It is the reciprocal of the number of discrete steps in the D/A output expressed as a percentage.

c) It is the comparison between the actual output of the converter and its expected output expressed as a percentage.

d) It is the ability to resolve between forward and reverse steps when sequenced over its entire range of inputs.

60. What is the resolution, in percent, of a 12-bit DAC?

a) 8.33

b) 0.000488

c) 0.0244

d) 0.083

61. A 4-bit digital-ramp A/D converter has a clock frequency of 100kHz and maximum input voltage of 10V.

a) The maximum number of samples per second will be 6250.

b) The minimum sample rate will be 6250 samples/second.

c) The minimum sample rate will be 100,000 samples/second.

d) The maximum sample rate will be 100,000 samples/second.

62. What is the main disadvantage of the digital-ramp A/D converter?

a) It requires a precision clock in order for the conversion to be reliable.

b) It requires an enable signal together with precision clock

c) The counter must count up from zero at the beginning of each conversion sequence, and the conversion time will vary depending on the input voltage.

d) It requires a counter.

63. Which of the following describes the basic operation of a single-slope A/D converter.

a) Any of the above could be correct, depending on the specific type of A/D converter involved.

b) A ramp voltage and analog input voltage are applied to a comparator. As the input voltage causes the integrating capacitor to charge, it will at some point equal the ramp voltage. The ramp voltage is measured and displayed on the digital panel meter.

c) A ramp generator is used to enable a counter through a comparator. When the ramp voltage equals the input voltage the counter is latched and then reset. The counter reading is proportional to the input voltage since the ramp is changing at a constant V/second rate.

d) The input voltage is used to set the frequency of a voltage-controlled oscillator (VCO). The VCO quits changing frequency when the input voltage stabilizes. The frequency of the VCO, which is proportional to the analog input voltage, is measured and is displayed on the digital display as a voltage reading.

64. One disadvantage of the tracking A/D converter is:

a) that it requires two counters-one for up and one for down.

b) the need for a latch and its associated control circuit.

c) that the binary output will oscillate between two binary states when the analog input is constant.

d) the need for an accurate clock reference for the counter.

65. The basic approach to testing D/A converters is to:

a) single-step the device through its full input range while checking the output with a DMM.

b) apply the correct input to the analog terminal and then check to see if the proper binary code exists on the digital inputs.

c) apply a sequence of binary codes covering the full range of the input to the input while observing the output on an oscilloscope. The output should consist of a linear stairstep ramp.

d) check the output with zero input and then full input. The output of the converter should extend from zero to its maximum value. If so, then everything in between can be assumed to be operating properly.

66. How may the operation of a DAC may be checked?

a) Using a static accuracy test and a staircase test

b) Using a static accuracy test and sampling

c) Using sampling and a staircase test

d) Using data acquisition and sampling

67. Which of the statements below best describes the basic operation of a dual-slope A/D converter?

a) A ramp voltage and analog input voltage are applied to a comparator. As the input voltage causes the integrating capacitor to charge, it will at some point equal the ramp voltage. The ramp voltage is measured and displayed on the digital panel meter.

b) The input voltage is used to set the frequency of a voltage-controlled oscillator (VCO). The VCO quits changing frequency when the input voltage stabilizes. The frequency of the VCO, which is proportional to the analog input voltage, is measured and is displayed on the digital display as a voltage reading.

c) Two ramps are generated: one by the input voltage and the other by a reference voltage. The input voltage ramp charges the integrating capacitor, while the reference voltage discharges the capacitor and

enables the counter until the capacitor is discharged, at which time the counter value is loaded into the output latches.

d) A ramp generator is used to enable a counter through a comparator. When the ramp voltage equals the input voltage, the counter is latched and then reset. The counter reading is proportional to the input voltage since the ramp is changing at a constant V/second rate.

68.

What is the linearity error of a D/A converter?

a) It is the comparison between the actual output of the converter and its expected output.

b) It is the maximum deviation in step size from the ideal step size.

c) It is the reciprocal of the number of discrete steps in the D/A output.

d) The ability to resolve between forward and reverse steps when sequenced over its entire range of inputs.

69. What is full-scale error of a D/A converter?

a) It is the deviation between the ideal straight-line output and the actual output of the converter.

b) It is the reciprocal of the number of discrete steps in the D/A output.

c) The ability to resolve between forward and reverse steps when sequenced over its entire range of inputs.

d) It is the maximum deviation of the output of the converter from its expected output.

70. Which of the equations below expresses the voltage gain relationship for an operational amplifier?

a) Vin/Vout = Rout/Rin

b) Vout/Vin = -Rf/Rin

c) Vout/Vin = -Rin/Rf

d) Vout/Vin = Rout/Rin

71. Which of the following characterizes an analog quantity?

a) Discrete levels represent changes in a quantity.

b) Has a continuous set of values over a given range.

c) Its values follow a logarithmic response curve.

d) Can be described with a finite number of steps.

72. An analog-to-digital converter has a four-bit output. How many analog values can it represent?

a) 0.0625

b) 0.25

c) 4

d) 16

73. What is the purpose of a sample-and-hold circuit?

a) To hold data after a multiplexer has selected an output

b) To hold a voltage constant so an ADC has time to produce an output

c) To hold a voltage constant so a DAC has time to produce an output

d) To keep temporary memory

74. The difference between analog voltage represented by two adjacent digital codes, or the analog step size, is the:

a) Resolution

b) Quantization

c) Accuracy

d) Monotonicity

75. A binary-weighted digital-to-analog converter has an input resistor of 100 k . If the resistor is connected to a 5 V source, the current through the resistor is:

a) 50 µA

b) 50 mA

c) 5 mA

d) 500 µA

76. A binary input 000 is fed to a 3bit DAC/ADC. The resultant output is 101. Find the type of error?

a) Settling error

b) Gain error

c) Offset error

d) Linearity error

77. 8051 Microcontroller has how many 16 bit registers?

a) 2

b) 3

c) 1

d) 0

78. How are the bits of the register PSW affected if we select Bank2 of 8051?

a) PSW.5=0 and PSW.4=1

b) PSW.2=0 and PSW.3=1

c) PSW.3=1 and PSW.4=1

d) PSW.3=0 and PSW.4=1

79. On power up, the 8051 uses which RAM locations for register R0- R7?

a) 00-2F

b) 00-07

c) 00-7F

d) 00-0F

80. The 8051 can handle _____ interrupt sources.

a) 3

b) 4

c) 5

d) 6

81. In 8051, I/O ports that are used as address and data for external memory are

a) port 1 and 2

b) port 1 and 3

c) port 0 and 2

d) port 0 and 3

82. How is the status of the carry, auxiliary carry and parity flag affected in 8051 PSW register, if following instruction get executed,

MOV A,#9C

ADD A,#64H

a) CY=0,AC=0,P=0

b) CY=1,AC=1,P=0

c) CY=0,AC=1,P=0

d) CY=1,AC=1,P=1

83. The contents of the accumulator after this operation,

MOV A,#0BH

ANL A,#2CH

a) 11010111

b) 11011010

c) 00001000

d) 00101000

84. Which commands are used for addressing the off-chip data and associated codes respectively by data pointer in 8051 instructions?

a) MOVX & MOVC

b) MOVY & MOVB

c) MOVZ & MOVA

d) MOVC & MOVY

85. What is the correct order of priority that is set after a controller gets reset?

a) TI/RI > T1 > T0 >EX1 > EX0

b) TI/RI < T1 < T0<EX1 < EX0

c) EX0 > T0 > EX1 >T1> TI/RI

d) EX0 < T0 < EX1 < T1 < TI/RI

86. Find the number of times the following loop will be executed by the 8051 microcontroller?

MOV R6,#200

BACK:MOV R5,#100

HERE:DJNZ R5, HERE

DJNZ R6,BACK

END

a) 100

b) 200

c) 20000

d) 50000

87. What should be done if we want to double the baud rate in 8051 serial communication?

a) change a bit of the TMOD register

b) change a bit of the PCON register

c) change a bit of the SCON register

d) change a bit of the SBUF register

88. What steps are followed when we need to turn on any timer in 8051 microcontroller?

a) load the count, start the timer, keep monitoring it, stop the timer

b) load the TMOD register, load the count, start the timer, keep monitoring it, stop the timer

c) load the TMOD register, start the timer,load the count, keep monitoring it, stop the timer

d) load the TCON register and SCON register

89. Does the two instructions mean the same in 8051 microcontroller?

1)BACK: DEC R0

JZ BACK

2) BACK: DJNZ RO, BACK

a) yes

b) no

c) can’t be determined

d) yes and second one is preferred

90. How many bytes of bit addressable memory is present in 8051 based micro controllers?

a) 8 bytes

b) 32 bytes

c) 16 bytes

d) 128 bytes

91. The total external data memory that can be interfaced to the 8051 is,

a) 32K

b) 64K

c) 128K

d) 256K

92. How many registers can be utilized to write the programs by an effective selection of register bank in program status word (PSW)?

a) 8

b) 16

c) 32

d) 64

93. in 8051, Auto reload mode is allowed in which mode of the timer?

a) Mode 0

b) Mode 1

c) Mode 2

d) Mode 3

94. Which among the below mentioned reasons is/are responsible for the generation of 8051 Serial Port Interrupt?

A. Overflow of timer/counter 1

B. High to low transition on pin INT1

C. High to low transition on pin INT0

D. Setting of either TI or RI flag

a) A & B

b) Only B

c) C & D

d) Only D

95. In 8051 which interrupt has highest priority?

a) INT1

b) TF0

c) INT0

d) TF1

96. Which of the following supprots bit-level operations?

i.SP

ii.P2

iii.TMOD

iv.SBUF

v.IP

a) ii, v only

b) ii, iv, v only

c) i, v only

d) iii, ii only

97. In 8051, a valid division instruction always makes,

a) CY=0,AC=1

b) CY=1,AC=1

c) CY=0,AC=0

d) no relation with AC and CY

98. Which one of the following is valid for MOV SCON, #88H?

a) 8-bit, 1-start bit, 1-stop bit, Receive enabled

b) 9-bit, 1-start bit, 1-stop bit, Receive disabled

c) 9-bit, 1-start bit, 1-stop bit, Receive enabled

d) 8-bit, 1-start bit, 1-stop bit, Receive disabled

99. In 8051, I/O port that does not have a dual-purpose role is?

a) Port-0

b) Port-1

c) Port-2

d) Port-3

100. In 8051, MOV A, @ R1 will perform the operation of

a) copy R1 to the accumulator

b) copy the accumulator to R1

c) copy the contents of memory whose address is in R1 to the accumulator

d) copy the accumulator to the contents of memory whose address is in R1

101. Find out the roll over value for the 8051 timer in Mode 0, Mode 1 and Mode 2?

a) 00FFH,0FFFH,FFFFH

b) 1FFFH,0FFFH,FFFFH

c) 1FFFH,FFFFH,00FFH

d) 1FFFH,00FFH,FFFFH

102. MOV A,0FFh

XRL A,#15h yields

a) A=77h

b) A=FFh

c) A=15h

d) A=00h

103. Since, ROM has the capability to read the information only then also it has been designed, why?

a) For controlling purpose

b) For loading purpose

c) For booting purpose

d) For erasing purpose

104. The ROM is a

a) Sequential circuit

b) Combinational circuit

c) Magnetic circuit

d) Static circuit

105. ROM is made up of

a) NAND and OR gates

b) NAND and AND gates

c) Decoder and OR gates

d) NAND and decoder

106. Why are ROMs called non-volatile memory?

a) They lose memory when power is removed

b) They do not lose memory when power is removed

c) They lose memory when power is supplied

d) They do not lose memory when power is supplied

107. In ROM, each bit is a combination of the address variables is called

a) Memory unit

b) Storage class

c) Data word

d) Address

108. The MOS technology based semiconductor ROMs are classified into _____ categories.

a) 2

b) 3

c) 4

d) 5

109. MOS ROM is constructed using

a) FETs

b) Transistors

c) MOSFETs

d) BJTs

110. Which ROM can be erased by an electrical signal?

a) ROM

b) Mask ROM

c) EPROM

d) EEPROM

111. What is the major difference between DRAM and SRAM?

a) Dynamic RAMs are always active; static RAMs must reset between data read/write cycles

b) SRAMs can hold data via a static charge, even with power off

c) The only difference is the terminal from which the data is removed—from the FET Drain or Source

d) DRAMs must be periodically refreshed

112. On execcuting

MOV A, #0A5h

RRC A

yields

a) A=25h

b) A=52h

c) A=22h

d) A=55h

113. By which technology, semiconductor memories are constructed?

a) PLD

b) LSI

c) VLSI

d) Both LSI and VLSI

114. The chip by which both the operation of read and write is performed

a) RAM

b) ROM

c) PROM

d) EPROM

115. RAM is also known as

a) RWM

b) MBR

c) MAR

d) None of the Mentioned

116. Computers invariably use RAM for

a) High complexity

b) High resolution

c) High speed main memory

d) High flexibility

117. Static RAM employs

a) BJT or MOSFET

b) FET or JFET

c) Capacitor or BJT

d) BJT or MOS

118. The magnetic core memories have been replaced by semiconductor RAMs, why?

a) Semiconductor RAMs are highly flexible

b) Semiconductor RAMs has highest storing capacity

c) Semiconductor RAMs are smaller in size

d) All of the Mentioned

119. The memory capacity of a static RAM varies from

a) 32 bit to 64 bit

b) 64 bit to 1024 bit

c) 64 bit to 1 Mega bit

d) 512 bit to 1 Mega bit

120. Which of the following RAM is volatile in nature?

a) SRAM

b) DRAM

c) EEPROM

d) Both SRAM and DRAM

121. Which of the following IC implements the static MOS RAM?

a) TMS 4015

b) TMS 4014

c) TMS 4016

d) TMS 2114

122. Dynamic RAM is more preferable than static RAM, why?

a) DRAM is of the lowest cost, lowest density

b) DRAM is of the highest cost, reduced size

c) DRAM is of the lowest cost, highest density

d) DRAM is more flexible and lowest storage capacity

123. The DRAM stores its binary information on

a) MOSFET

b) Transistor

c) Capacitor

d) BJT

124. Dynamic RAM is used as main memory in a computer system as

a) It has lower cell density

b) It needs refreshing circuitry

c) Consumes less power

d) Has higher speed

125. Which characteristic of RAM memory makes it not suitable for permanent storage?

a) Unreliable

b) Too slow

c) Too bulky

d) It is volatile

126. A ripple counter's speed is limited by the propagation delay of:

a) each flip-flop

b) all flip-flops and gates

c) the flip-flops only with gates

d) only circuit gates

127. What type of register would shift a complete binary number in one bit at a time and shift all the stored bits out one bit at a time?

a) PIPO

b) SISO

c) SIPO

d) PISO

128. Synchronous counters eliminate the delay problems encountered with asynchronous (ripple) counters because the:

a) input clock pulses are applied only to the first and last stages

b) input clock pulses are applied only to the last stage

c) input clock pulses are not used to activate any of the counter stages

d) input clock pulses are applied simultaneously to each stage

129. One of the major drawbacks to the use of asynchronous counters is that:

a) Low-frequency applications are limited because of internal propagation delays

b) High-frequency applications are limited because of internal propagation delays

c) Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications.

d) Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications.

130. Mod-6 and mod-12 counters are most commonly used in:

a) Frequency counters

b) Multiplexed displays

c) Digital clocks

d) Power consumption meters

131. What is/are the crucial function/s of memory elements used in the sequential circuits?

a) Storage of binary information

b) Specify the state of sequential

c) Both A & B

d) None of the Mentioned

132. Which memory elements are utilized in asynchronous & clocked sequential circuits respectively?

a) Time- delay devices & registers

b) Time- delay devices & flip-flops

c) Time- delay devices & counters

d) Time-delay devices & latches

133. The characteristic equation of D-flip-flop implies that _____.

a) The next state is dependent on previous state

b) The next state is dependent on present state

c) The next state is independent of previous state

d) The next state is independent of present state

134. What is the bit storage binary information capacity of any flip-flop?

a) 1 bit

b) 2 bits

c) 16 bits

d) infinite bits

135. What is/are the directional mode/s of shifting the binary information in a shift register?

a) Up-Down

b) Left - Right

c) Front - Back

d) All of the Mentioned

136. A counter is fundamentally a _____ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it.

a) Register

b) Memory unit

c) Flip-flop

d) Arithmetic logic unit

137. Match the following sequential Circuits with associated functions

1. Counter -------- A. Storage of Program & data in a digital computer

2. Register -------- B. Generation of timing variables to sequence the digital system operations

3. Memory --------- C. Design of Sequential Circuits

a) 1-A , 2-B , 3-C

b) 1-C , 2-B , 3-A

c) 1-C , 2-A , 3-B

d) 1-B , 2-C , 3-A

138. What contributes to the triggering of clock pulse inputs for all the flip-flops excluding the first flip-flop in a ripple counter?

a) Incoming Pulses

b) Output Transition

c) Double Clock Pulses

d) All of the Mentioned

139. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?

a) Low input voltages

b) Synchronous operation

c) Gate impedance

d) Cross coupling

140. The truth table for an S-R flip-flop has how many VALID entries?

a) 1

b) 2

c) 3

d) 4

141. Which of the following is correct for a gated D-type flip-flop?

a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW

b) The output complement follows the input when enabled

c) Only one of the inputs can be HIGH at a time

d) The output toggles if one of the inputs is held HIGH

142. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?

a) AND or OR gates

b) XOR or XNOR gates

c) NOR or NAND gates

d) AND or NOR gates

143. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called

a) Combinational circuits

b) Sequential circuits

c) Latches

d) Flip-flops

144. Whose operations are more faster among the following?

a) Combinational circuits

b) Sequential circuits

c) Latches

d) Flip-flops

145. When an 8 bit SISO register is used for time delay of 25micro seconds, the clock frequency must be

a) 41.67 KHz

b) 333 KHz

c) 125 KHz

d) 8 MHz

146. The basic latch consists of

a) Two inverters

b) Two comparators

c) Two amplifiers

d) None of the Mentioned

147. What is a trigger pulse?

a) A pulse that starts a cycle of operation

b) A pulse that reverses the cycle of operation

c) A pulse that prevents a cycle of operation

d) None of the Mentioned

148. In Mealy models output are functions of both

a) Present state

b) Input state

c) Next state

d) Reset state

149. Time sequence for flip-flop can be enumerated by

a) State table

b) Map

c) Truth table

d) Graph

150. With a 100KHz frequency supply, 8 bits can be entered in a shift register in

a) 80 microseconds

b) 8 microseconds

c) 80 ms

d) 8 ms

----------Key----------

1. (b)

2. (a) (b)

3. (d)

4. (d)

5. (b)

6. (b)

7. (a)

8. (a)

9. (a)

10. (b)

11. (b)

12. (b)

13. (a)

14. (d)

15. (a)

16. (b)

17. (a)

18. (a)

19. (d)

20. (d)

21. (b)

22. (b)

23. (c)

24. (b)

25. (d)

26. (b)

27. (b)

28. (b)

29. (c)

30. (b)

31. (a)

32. (a)

33. (b)

34. (c)

35. (b)

36. (b)

37. (c)

38. (d)

39. (c)

40. (d)

41. (d)

42. (d)

43. (a)

44. (a)

45. (a)

46. (a)

47. (b)

48. (d)

49. (c)

50. (a)

51. (b)

52. (a)

53. (c)

54. (a)

55. (d)

56. (c)

57. (c)

58. (c)

59. (b)

60. (c)

61. (b)

62. (c)

63. (c)

64. (c)

65. (c)

66. (b)

67. (c)

68. (b)

69. (d)

70. (b)

71. (b)

72. (d)

73. (c)

74. (a)

75. (a)

76. (c)

77. (a)

78. (d)

79. (b)

80. (c)

81. (c)

82. (b)

83. (c)

84. (a)

85. (c)

86. (c)

87. (b)

88. (b)

89. (b)

90. (c)

91. (b)

92. (c)

93. (c)

94. (d)

95. (c)

96. (a)

97. (c)

98. (b)

99. (b)

100. (c)

101. (c)

102. (a)

103. (c)

104. (b)

105. (c)

106. (b)

107. (d)

108. (b)

109. (c)

110. (d)

111. (d)

112. (b)

113. (d)

114. (a)

115. (a)

116. (c)

117. (d)

118. (d)

119. (c)

120. (d)

121. (c)

122. (c)

123. (c)

124. (d)

125. (d)

126. (a)

127. (b)

128. (d)

129. (b)

130. (c)

131. (c)

132. (b)

133. (d)

134. (a)

135. (b)

136. (a)

137. (d)

138. (b)

139. (d)

140. (c)

141. (a)

142. (c)

143. (b)

144. (a)

145. (b)

146. (a)

147. (a)

148. (d)

149. (a)

150. (a)