1. The propagation delays of the XOR gate, AND gate and multiplexer (MUX) in the circut shown in the figure are $4ns$, $2ns$ and $1ns$, respectively. If all the inputs P, Q, R, S and T are applied simultaneously and held constant, the maximum propagation delay of the circuit is (GATE-EC2021,31)

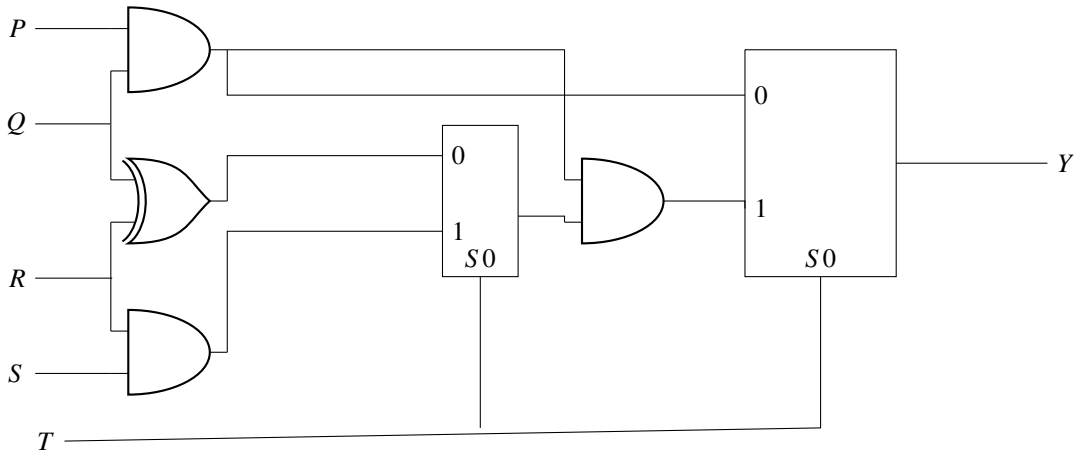

Figure 1: circuit daigram

1. $3ns$
2. $5ns$
3. $6ns$
4. $7ns$