

THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™

Producing the Perfect Data Package



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Prototron Circuits

Peer Reviewers



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Retired Engineer, Ph.D

Douglas Brooks has a BSEE and an MSEE from Stanford and a Ph.D. from the University of Washington. For the last 27 years, he has owned a small engineering service firm, written numerous technical articles on PCB design and signal integrity issues, and published two books on these topics. He published *PCB Trace and Via Temperatures: The Complete Analysis, 2nd Edition* in 2017 and *PCB Trace Current/Temperature Curves, 1/4 Oz. to 5.0 Oz., The Complete Set* in 2018, both with Johannes Adam.

Brooks has given seminars several times a year all over the U.S., Moscow, China, Taiwan, Japan, Israel, Melbourne, and Canada. His primary focus has been making complex technical issues easily understood by those without advanced degrees. Brooks is now retired and lives with his wife of over 50 years in Issaquah, Washington.



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Kelly Dack understands that PCB design involves much more than getting electrons to flow through a circuit on a PCB. He has dedicated his career to demonstrating that PCB design also includes how well a designer can get a PCB layout to flow efficiently through the manufacturing process floors of fabrication and assembly. Kelly's holistic experience in the printed circuits industry is underlined by employment serving companies in aerospace, medical, telecommunications, gaming, PCB fabrication, and EMS assembly.

Currently, Kelly provides PCB design and manufacturing engineering services for a dynamic EMS provider in the Pacific Northwest. Additionally, he serves on the executive staff of IPC Designer Council and is employed by EPTAC Corporation as a CID instructor. Kelly is an author and contributes on-camera talent for the I-Connect007 *RealTime with...* video program. He can be reached at kelly@eptac.com.

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Mark Thompson

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With more than 38 years of experience, Mark Thompson has reviewed thousands of data packages and worked with customers' designers and engineers to help them hand off better data. Over his career, he has become one of the most trusted names in the industry when it comes to advising customers on how to productively work with PCB vendors.

Mark believes that the PCB will only be as good as the data it takes to build it, and he has dedicated his career to fulfilling this philosophy. His popular column "The Bare Board Truth," one of I-Connect007's most widely read columns, covers design, layout, and engineering practices as they relate to PCB fabrication. Mark also manages Prototron's "[PCB Bare Board Truth](#)" LinkedIn group—a conversational forum devoted to networking solutions to today's PCB fabrication issues. Mark's other passions include flying aerobatics, art, history, and music. He can be reached at markt@prototron.com

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Producing the Perfect Data Package

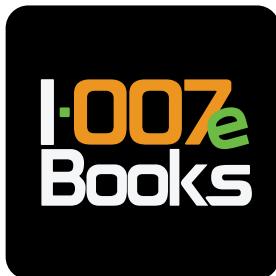
Mark Thompson

PROTOTRON CIRCUITS

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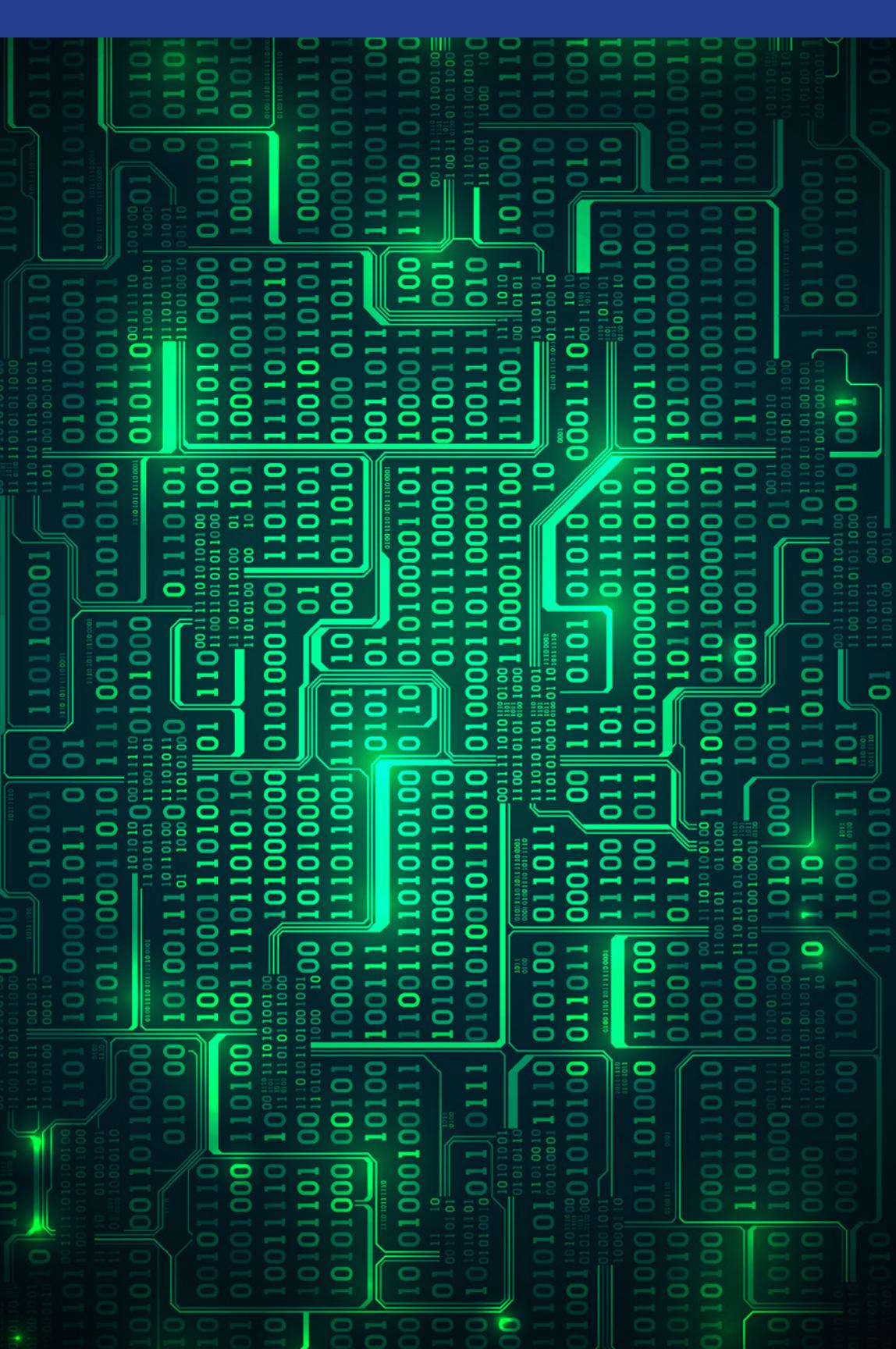
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CONTENTS

- 1 Introduction**
- 3 Identifying Product Board Class and Pre-Quote Software**
- 9 Contents of the PCB Output Package**
- 26 Conclusion**
- 27 References & Acknowledgements**
- 29 Appendix: Fab Output File Checklist**
- 30 Glossary**
- 33 About Prototron**



Introduction

My expertise comes from almost four decades of rolling up my sleeves and working closely with engineers to develop printed circuit solutions that will work best for their specific applications. In this book, I leverage this knowledge to help educate PCB designers about the impact their design output package has on the bare board engineering process.

Fabricators are constantly asked to turn a concept into a tangible, functional piece of hardware. The most effective way to assure success is early engagement between the designer and the fabricator, because decisions made on either side will certainly impact the other. One of the biggest complaints we hear as fabricators relates to quote response time. Many of the fabrication packages we are asked to quote are incomplete and require additional clarifications, technical discussions, and data files. The best-case scenario is these back-and-forth interactions take time and become the largest contributing factor in delayed quotes. The worst-case scenario is that a customer receives product that does not meet the design intent due to an incomplete, missing, or incorrect design output package.

It cannot be overstated that any discrepancies between drawings, README files, and data and quote request information should be eliminated *before* sending an output package to a fabricator for a quote. Care should be taken to update the drawings so they properly reflect what is needed.

A case-in-point example: One board once started its life as an eight-layer PCB, but it was redesigned into a six-layer. However, the impedance requirements listed in the output package we received had not been updated. Had we not discovered this discrepancy, our material stackup and final PCB would not have worked per the intended design requirements.

It is my hope that this book will provide designers a desk reference for exactly what a PCB fabricator requires in a design output package, while helping them understand the consequences of not providing the most complete and accurate package possible. At the end of this book, I include a file checklist for output to ensure you have everything that your fabricator needs to provide you with a fast and accurate quote. I hope you find this effort valuable.



Identifying Product Board Class and Pre-Quote Software

Deciding upon the class of the final product will determine what files are needed for fabrication and assembly. It is critical to note that for a product to be built to any class level, it must be designed to that class level from its inception.

STANDARDS AND SPECIFICATIONS

Let's review the various PCB classes as defined by IPC—Association Connecting Electronics Industries. IPC is the trade association for the electronics industry that provides standards, training and certification, market research, education, and public policy advocacy to support all facets of the industry, including design, PCB manufacturing, and electronics assembly.

First, understand that IPC has different specifications depending on the PCB type. This book will address rigid and rigid-flex PCBs. The industry standards for these PCB types are:

- IPC-6012: Qualification and Performance Specification for Rigid Printed Boards
- IPC-6013: Qualification and Performance Specification for Flexible Printed Boards
- IPC-6018: Qualification & Performance Specification for High Frequency (Microwave) Printed Boards
- IPC-6012DS: Space and Military Avionics Applications Addendum to IPC-6012D: Qualification and Performance Specification for Rigid Printed Boards

There are three different board classes as defined by IPC-6012 and IPC-6013. The appropriate class will be defined by the criticality of the product the PCB will be integrated with.

CLASSES

- **Class 1** is for “general electronic products” and is the lowest reliability class. Therefore, it requires the least amount of additional information in a fabrication package to meet product reliability. For instance, a Class 1 or Class 2 PCB does not require a netlist compare, whereas Class 3 and Class 3A do require it. Thus, for a Class 1 or Class 2 part, if IPC netlists and any instructions expressing the need for a net compare are not provided, a separate netlist file is not required in the output package.
- **Class 2** is for “dedicated service products” and requires a little more information to be provided, as continued performance and extended life cycle are required. Uninterrupted service is not mandatory for Class 2 PCBs. It is important to note that while a Class 2 PCB does not require an IPC netlist be provided to do a design versus exported image data comparison, it is highly recommended as part of the output package.
- **Class 3** is specified for the highest reliability and continued high performance in segments where equipment failure simply cannot be tolerated, such as the medical or aerospace industries. For IPC 6012 Class 3 an IPC netlist comparison is required. Netlists typically follow IPC-D-356, IPC-D-356A, or a Mentor neutral file. Other older forms of IPC netlists can be used if a fabricator has the ability to use raw computer-aided design (CAD) data, but by far the most common formats for fabrication are the three previously mentioned.

As a fabricator, we constantly see PCBs called out as IPC-6012 Class 3 that have not been designed to meet Class 3 requirements, such as minimum annular ring or clearance (Figure 1.1). If the PCB was not designed to meet Class 3 requirements, the fabricator does not have a chance to provide the customer a Class 3 PCB. Designers should use the IPC-2220 series of docu-

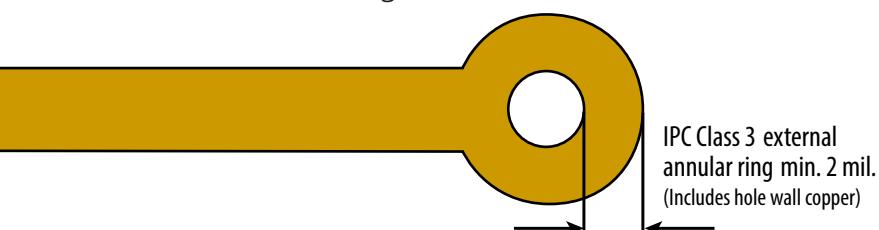


Figure 1.1.



Fun fact: The term "annular ring" comes from the reliable indicator of yearly tree growth.

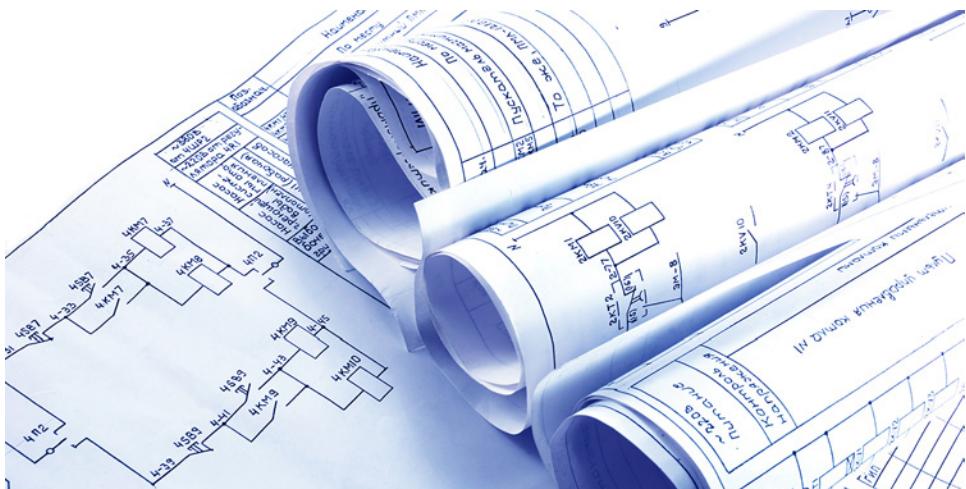
ments concerning board design and fabrication to ensure a design-to-fabrication match.

Part sizes are shrinking and part densities are growing, which reduces space and makes it increasingly difficult to have enough supporting annular ring or clearance. One way to minimize delays in the fabrication quote or manufacturing process is to qualify this by saying the product is to be built to IPC-6012 Class 3 with an allowance for annular ring and clearance to Class 2. This may preclude a phone call from your fabricator to tell you the quote is on hold because the design does not meet Class 3 minimum annular ring requirements (Figure 1.1).

PRE-QUOTE SOFTWARE

Many PCB fabricators have some type of pre-quote analysis software that can quickly tell them if the PCB meets certain design rules, such as whether spaces on a given design do not support the copper callout specified on the drawing or stackup detail, or if the annular ring is insufficient for the specified hole sizes. As a cautionary note, these are quoting tools the fabricator uses to catch obvious concerns. They are not intended to take the place of a full-blown computer-aided manufacturing (CAM) design rule check (DRC) tool.

Pre-quote software is typically a quoting tool for managing and assessing the customer's incoming PCB data files. Depending on the system in place,



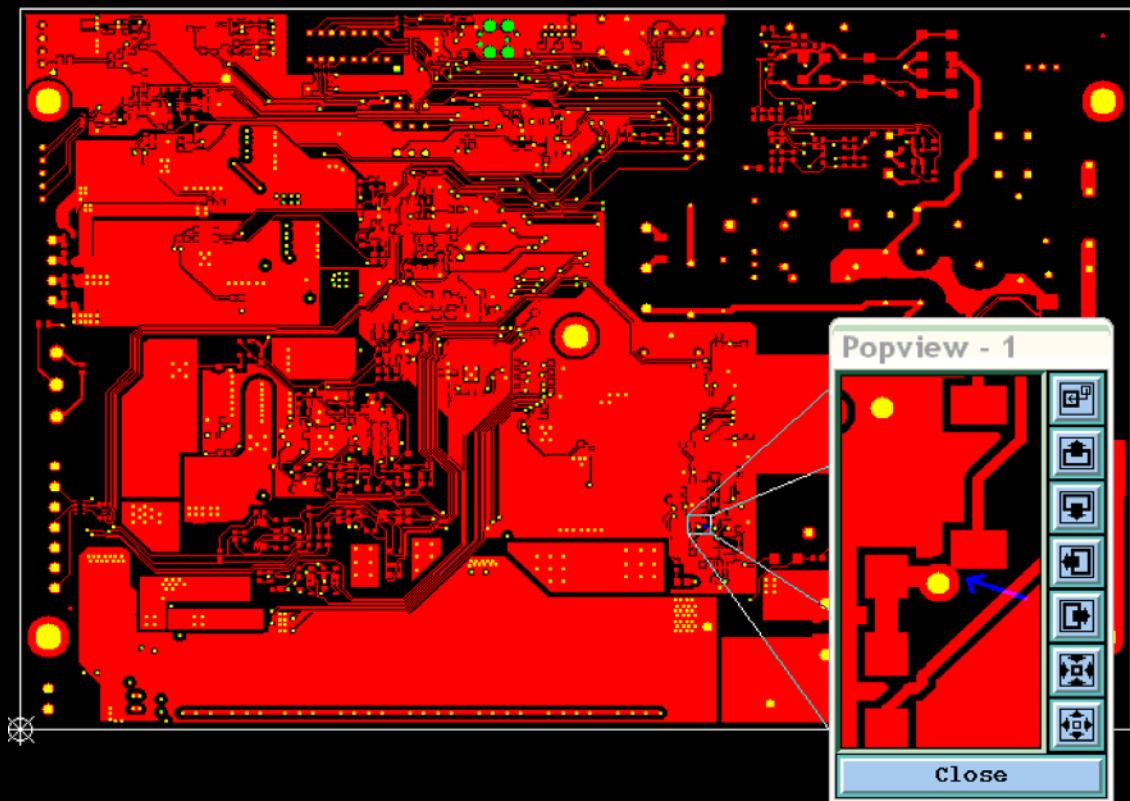
Fun fact: The process of printing blueprints is now obsolete, however, the term continues to be used informally to refer to various digital images known as "prints" or "drawings".

this can include automatically retrieving design information and generating precise summary reports that identify potential risks and challenging design features. These tools allow sales and quoting personnel, who typically do not have a technical engineering background, to work more independently from engineering and provide a highly accurate quote.

Many of the fabricators using these software packages offer them as an online check prior to submitting a quote. However, they typically have a support person run the files through the software for the customer. If you are utilizing any of these services, you can do yourself a favor and minimize quote response times by standardizing your file names to avoid sending any conflicting information. These quote software packages do not have the ability to read and interpret drawings. If your file names are not readily recognized to prepare the layer stack, the system may pause to allow the user to enter this missing or misinterpreted information and continue to process the job.

Incoming files are placed into a "hopper" with some type of naming convention that establishes which files go to which quoting person (presuming your fabricator has more than one). The files are then loaded into the system and the software runs an analysis of your data; in some cases, it will even run your provided IPC design netlist against the provided customer image data. The benefit of using a pre-quote software solution is identifying potential manufacturing problems early during the quote stage without tying up engineering resources.

EVERY
ACCOMPLISHMENT
STARTS WITH
THE DECISION
TO TRY



Chapter 2

Contents of the PCB Output Package

This chapter will cover the five “must-haves” for an output package—drawings and README files, image data, NC Drill files, IPC netlists, and assembly array drawings—and conclude with a brief note on manufacturability data edits.

A. DRAWINGS AND README FILES

Since one of the first things a salesperson will do to create a quote is review your drawings and README files, let's start with what should be included on a fabrication drawing. README files are typically simple text documents (Word or Notepad) that describe the files and provide information to be conveyed to the fabricator that may not be on the drawing, such as known netlist shorts or opens, specifics about controlled impedances, etc. Drawings are typically exported as a PDF, DXF, or Gerber image file.

Note: Any discrepancies or conflicts between drawings or files will require clarification between the salesperson and designer, which will delay the quote process. A frequent issue is inaccurate, confusing, or conflicting notes on drawings. A quick cursory look at all your output documents is advised to make sure you have no troublesome notes.

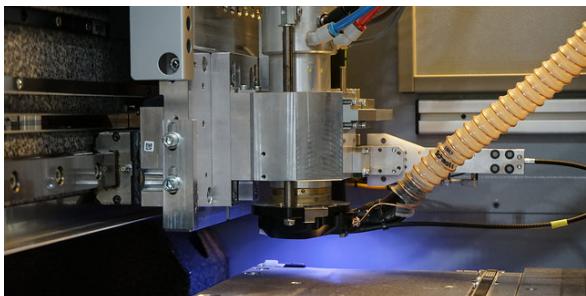
Drawings should include the following nine fabrication specifications at a minimum:

A1. Board outline with dimensions and tolerances

Many output packages come in with files that use different origins (i.e., not all files are aligned as they should be). This creates issues with layer-to-layer alignment, as well as X and Y board dimensional requirements and tolerances associated with those dimensions. It is always good practice to have a dimensioned hole as the X0Y0 origin. This allows the fabricator to align the NC Drill

file with the image data. Ideally, the board outline should also exist on the image data. If an assembly array drawing is being provided for specific panelization needs, make sure there are no conflicts between the board outline in the image data and the array image data , such as showing chamfered corners on the image data but radii on the array drawing.

A2. Tool chart showing symbols for each different tool size used and plating status (plated or non-plated, as well as a tolerance)



A modern high-speed CNC drill. (Source: I-Connect007)

Again, care needs to be taken to make sure the tool list on the drawing matches the NC Drill file provided. You may have to make a change depending on when the files are generated, such as the NC Drill file that is not reflective of what is shown on the tool list. This type of discrepancy will result in a phone call or email, again delaying the quote or fabrication process.

Some common examples might include:

- Tolerances for press-fit plated holes, typically $\pm 0.002"$
- Tolerances for plated component holes, typically $\pm 0.003"$
- Tolerances for non-plated holes, typically $\pm 0.002"$
- Via holes, typically expressed as $\pm 0.003"/-$ the entire hole size (this tells a fabricator that you do not care what size the particular via finishes at as long as you have continuity)
- Unique tolerances sometimes exist where the nominal hole size shown on the drawing is actually the *absolute minimum*, typically expressed as $+0.004" -0.000"$

All of these tolerance scenarios tell the fabricator how they need to set up the tool sizes before plating so they will attain the desired finished hole size after plating. You should specify hole size tolerances based on actual design intent and functionality rather than a boilerplate tolerance from a design guideline. This will save both time and money because the fabricator will not have to implement special processing to achieve a tight tolerance that is unnecessary.

A3. Material type and copper weights desired

Specify the material type and whether material deviations or substitutions are allowed. The industry standard for materials is IPC-4101: Specification for Base Materials for Rigid and Multilayer Printed Boards.

Drawings often specify the performance requirements needed from a given material set, including glass transition temperature (T_g) or high-speed application frequencies, such as those over 10 GHz (the higher the frequency, the lower the dielectric constant, or D_k , of the chosen material). This is critical information for properly calculating impedances.

Unless required by design, avoid specifying a single material type if multiple materials are suitable for the design. List them to avoid a phone call from your chosen fabricator. When specifying copper weights, define whether they are prior to (base) or after (final) plating. This difference can represent a swing in the copper thickness of several thousandths of an inch for standard technology and exponentially more if the design has sequential lamination.

Material stackups typically depict base copper weights prior to plate upon surface layers. However, some drawings will show all layers, but have no note about whether or not this is the base or finished copper weight. In cases like this, since most inner layers are processed on the cladding, they will finish with a "print and etch." The fabricator may contact you to clarify the intent of the surface layer copper if the intent on the drawing is unclear.

An example of a typical material specification note might read: *Material: Laminate and prepreg shall be in accordance with IPC-4101/26, 170°C Tg.*

A4. Overall PCB thickness (including tolerance)

Note any specific measurement methods, such as those that include or exclude plating and surface finishes. For example: *Thickness: Finished board shall be $0.062 \pm 10\%$ measured over final finish and mask.*

This is sometimes shown as a Z-axis depiction on the drawing as well. If a chassis fit is tight, the designer may want to call out the overall thickness as a maximum, including all plating, surface finishes, and masks.

A5. Surface finish type and thickness (including tolerance)

Examples of common surface finish include bare copper, electroless nickel immersion gold (ENIG), hot air solder leveling (HASL), lead-free HASL, electroless nickel/electroless palladium immersion gold (ENEPIG), etc.

A typical note may read something like this: *Finish: ENIG plated according to IPC-4552. Thickness shall be a minimum of 0.05 µm gold over 3-6 µm nickel.* This is where your chosen surface finish needs to be supported by your design.

An extreme example would be a customer who submits a design containing a 0.4-mm pitch BGA pattern void of any solder mask webs between lands, while specifying an HASL finish. The problem is the deposition of HASL is much thicker than ENIG, ENIPIG, or immersion (IMM) silver. Without webs of mask between surface mounts, the surface finish tends to wick between them, which creates electrical shorts. In a case like this, you should get a phone call or email asking for another thinner surface finish to prevent a disaster from happening.

A6. Solder mask and ID type/color (plus any information regarding process type and minimum or maximum thickness)

With regard to today's materials, liquid photoimageable (LPI) solder mask is a polymer plastic that will outgas in the vacuum of space if sent up uncannistered (i.e., not in an enclosure). NASA has provided Class 3A flight/aerospace parts with a specification on how much off-gassing one may expect. Of course, the best way to make sure you have no electrical anomalies is to make sure the product will be in an enclosure.



Additionally, since there are so many different mask colors, some of the colors may have to be hand flood-screened prior to image by a human. This being the case, humans cannot match an automated flood coater for mask that lays down a uniform and predictable dielectric thickness over glass and metal. The increased thickness of the mask due to the color chosen may affect impedances. Twenty years ago, when traces and spaces were 0.008"/0.008", this additional dielectric did not have much impact on the impedances. However, with trace and spaces routinely around 0.1 mm (0.00393") today, this additional dielectric thickness of mask will affect the impedances and needs to be taken into account by your chosen fabricator.

A typical solder mask drawing note may read: *Liquid photoimageable solder mask per IPC-840, color: blue.*

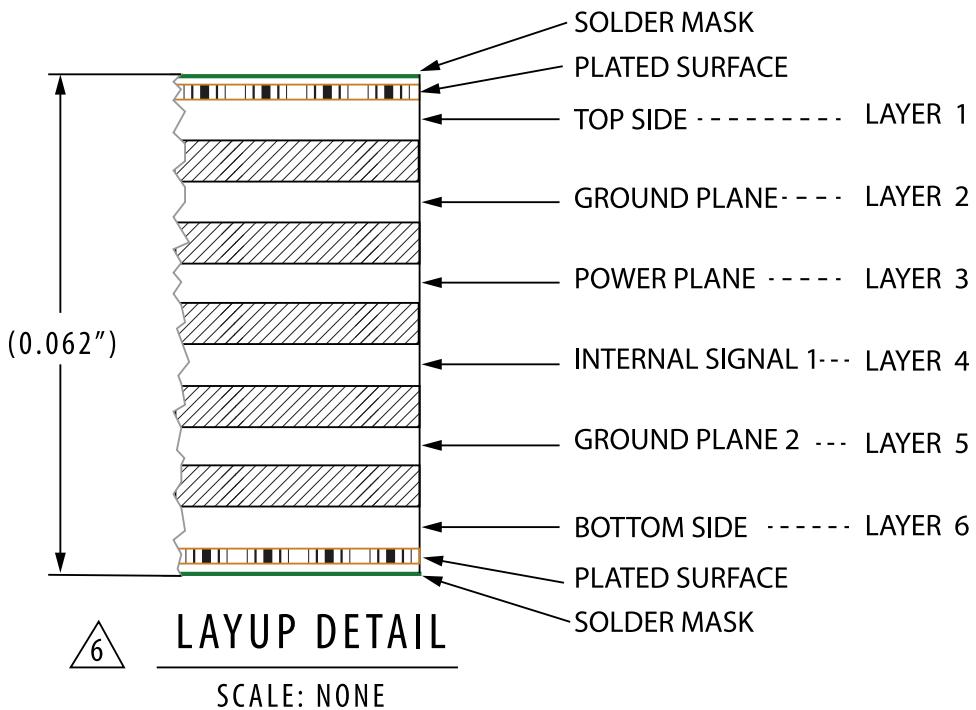
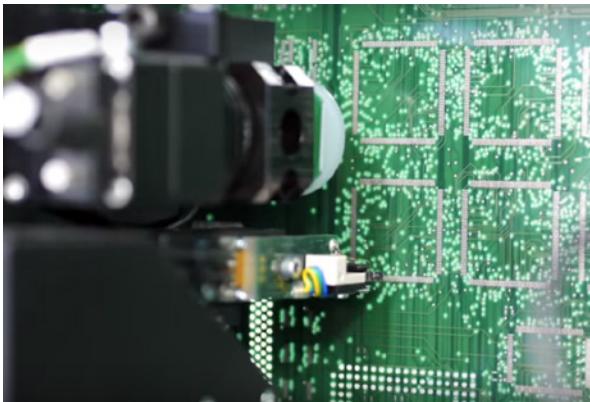


Figure 2.1: Stackup drawing.

A7. Board stackup

In PCB parlance, a stackup is the Z-axis description of the layer sequence, dielectric thickness, and copper weights of the finished part. This is a critical part of any drawing that the fabricator will use to quote the PCB, order the raw laminate, and physically construct the board. It is also an input to impedance modeling. Ideally, the layer names should be identical to the image data file layer names to avoid any errors or interpretation issues. The stackup should include any specific dielectrics that may be required, copper weights, thickness tolerances, and identification of which layers are signals and which are planes (Figure 2.1).

Make sure that any other documentation referring to a stackup, such as a README file or an additional notes page, has no conflicting information that would require clarification by the fabricator. Also, if you provide an EXTREP file showing the file extension names, make sure this also does not conflict with any stackup represented on the physical drawing. A disconnect between the image file labeling and the drawing or other ancillary instructional files is one of the most frequent reasons for confusion with the fabricator.



High-speed, accurate, flying-probe tester.
(Source: MicroCraft)

A8. Fabrication testing requirements

Some common PCB test requirements include standard electrical testing, IPC netlist compare, high-potential (hipot) testing, and highly accelerated stress testing (HAST). Also, any special requirements outside of industry standards for continuity and isolation thresholds need to be specified.

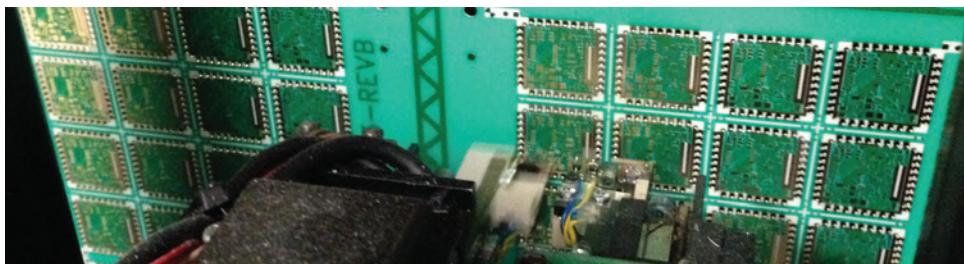
A typical electrical test drawing note may read: *100% bare board electrical test to be done with reference to supplied IPC-D356 netlist.*

A9. Impedance requirements

The fabricator will need to know which trace widths are controlled, on what layers they reside and specific thresholds and tolerances. The fabricator will base their impedance modeling on these requirements, which will impact material selection, the CAD output image files and process controls.

A sample impedance drawing note may read: *0.005" trace widths on layers 1, 3, 4, 7, 8, and 10 to be 50 ohms ±10%.*

It is important to ensure there are no discrepancies between the drawing callout for impedances and the actual provided data. Let me give you a couple of examples. If a drawing states, "All 0.005" traces on layers 1 and 12 need to meet 50 ohms ±10%," but the provided image data files contains no 0.005" trace widths, this can be due to any number of reasons, such as:



Another angle of fixtureless flying-probe tester. (Source: Prototron Circuits)

- Going from a 10-layer to a 12-layer board and the impedances change but are not reflected on the drawing
- Rounding errors when going from the metric to the imperial system and vice versa (e.g., the note says all 0.005" traces but they may actually be 0.00492 on the image data due to rounding from inches to metric units)
- Reference planes (e.g., a new revision with a different layer count or a brand-new design often do not have the proper reference planes for the impedances called out on the drawing)

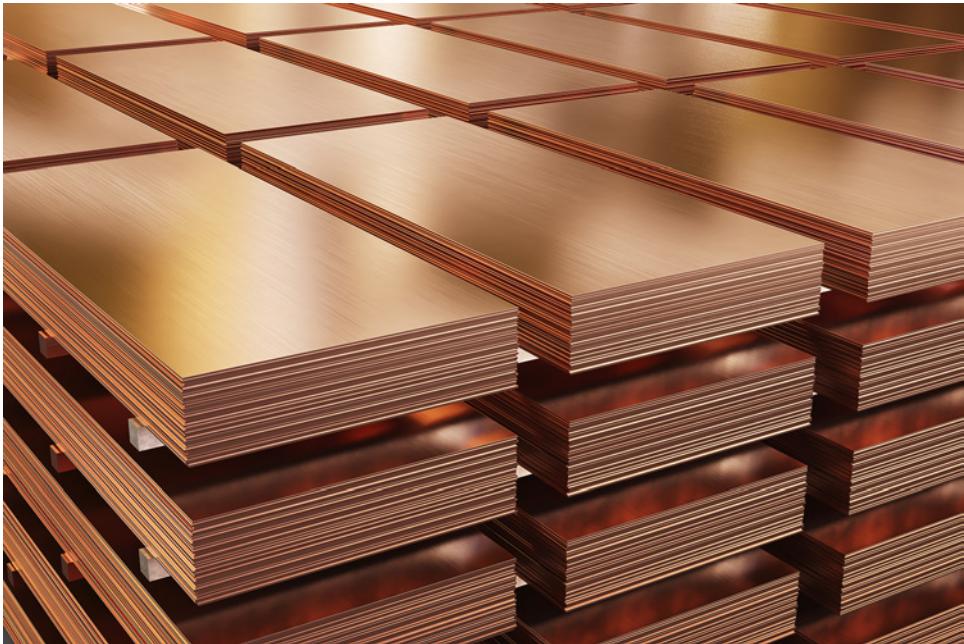
An example we frequently see is a board being changed from a 0.062" six-layer design to a 0.062" twelve-layer design. The impedance trace widths and dielectrics decreased for a twelve-layer PCB of the same thickness as the six-layer PCB, so you can count on the split planes acting as part of a reference plane with these reduced dielectrics.

An engineer might want layer 3 impedances to reference only layer 2, but not the layer 4 plane on the other side of layer 3. This can be done in a 6-layer configuration by increasing the dielectric distance between layers 3 and 4 to 3X that of the dielectric between layers 2 and 3. This mitigates any coupling effect that layer 4 might have on layer 3. But once we reach 12 layers, the necessary dielectrics required to keep 12 layers within an 0.062" package are thinner, and we can't count on this 3X rule. This may mean that a signal layer or split plane (layer 4) now needs to act as a reference plane for layer 3.

From a fabrication standpoint, any metal on either side of an impedance-controlled trace that is not separated by a factor of three times the dielectric distance, as in the stripline example, will be considered a reference plane.

Additionally, it is helpful to note any unusual reference plane scenarios that exist on the drawing. For example, when layer 1 uses layer 3 as a reference plane and not layer 2 in an effort to increase the dielectric to make the trace width for the desired impedance more reasonable.

"...it is helpful to note any unusual reference plane scenarios that exist on the drawing."



Two examples where this may be utilized include:

1. Types of serial advanced technology attachment (SATA) connectors: Traces for SATA can be fairly wide, which may mean they will require an increased dielectric to the reference plane so a “pass through layer,” as previously described, would be a good solution.
2. A need for both 50- and 75-ohm structures to be the same width on the surface layer: By making the reference plane for the 50-ohm scenario layer 2, and for the 75-ohm structures cutting a “pass through” in the plane of layer 2, the trace widths on layer 3 can be the same by adding an additional metal to the layer.

Moreover, with raw laminate material costs continuing to increase, we see customers managing product costs by asking for very specific dielectrics and material properties, but not mentioning any impedance requirements they may need. This is a huge risk. For example, if a project coordinator or engineer researches electrical properties of materials for the purpose of establishing line sizes and dielectrics for impedance values, such as FR-4/FR-406, a material's electrical properties may indicate a Dk value between 4.2 and 4.9 at 1

GHz. This is a cured core value generally based on a thicker material core, such as 0.008".

Most fabricators build what is commonly called a "foil cap" construction to save material costs. Therefore, depending upon the dielectric thickness, the prepreg interface may have a Dk value as low as 3.3. This mismatch reflects the reality of the material in effective DK and what was predicted by the designer or engineer, which many times results in either dielectric or line size adjustments to meet the desired impedances—sometimes to the point where the part is no longer producible when line and space geometries are already at process minimums and do not allow for line resizing. That's why it's key to engage a fabricator as early as possible in the design evolution.

Lastly, use common sense when creating your drawings. Generic drawing templates and boilerplates are great, but if any of the information does not apply to a specific part number, it should be removed. One example would be an electrically nonfunctional part being used for a chassis test fit or part placement check. If the final drawing for the part is provided for such an unclad test vehicle, much of the information is not applicable, such as stackups, surface finishes, copper weights, etc. Remove any notes not relevant to the particular build or communicate them directly to your chosen fabricator.

B. IMAGE DATA

Today, fabricators have two main ways to image: film, where a phototool is created to be used in conjunction with a core or part coated with a photosensitive resist, and LED/laser direct imaging (LDI), with the latter becoming the most common. LDI eliminates the need for a film phototool that uses laser or LED to "draw" the image directly onto the photosensitized panel. Every time you have to reproduce an image onto another media, you take the chance of losing trace width or edge acuity. The benefit of this method is there is no loss of line width or edge acuity due to the phototool reproduction. Unless you have your boards built by a fabricator that does both CAD and CAM, sending the raw CAD data is not useful for most fabricators. This means you will need to export some files in formats readily used by fabricators.

Many design software packages have multiple output types for image data. The four most common and accepted export image file types include:

B1. ODB++

ODB++ is a proprietary data exchange format used to design and manufacturer PCBs. ODB++ is a common format in the industry that provides intelligence via additional attributes to create a single data platform. This provides a transition from your design software (CAD) to a usable PCB manufacturing output (CAM) data. Created by Valor Computerized Systems and released as ODB in 1995, the “++” was added in 1997 with more embedded attributes for component names. ODB++ became part of Mentor when that company acquired Valor in 2010.

Some of the benefits of outputting ODB++ are:

- The IPC netlist is embedded in the data and does not need to be sent as a separate file
- Fabricators using Genesis manufacturing software are looking at a true comparison because no conversion or interpretation issues exist (e.g., odd-shaped pads rotated at unusual angles are not always interpreted correctly with some of the older CAM systems, but this is not an issue with ODB++ data)
- NC Drill files are contained

B2. Gerber X2

This is the newest form of Gerber output, but not all fabricators have the ability to use this type of data. Much like the 274 format, this data has the apertures embedded and the X2 Gerber files have additional attributes added.

B3. Gerber 274X

Gerber 274X includes data with apertures embedded. It was by far the most common output format used until ODB++ was released. 274X image data is a more sophisticated version of previous Gerber 274 formats that required a separate aperture list or wheel to be interpreted by a fabricator’s CAM system.

B4. Gerber 274D

One of the older types of Gerber output, Gerber 274D requires a separate aperture list or wheel be sent and is a little more cumbersome than the “X” Gerber data. Providing this type of Gerber data requires that the aperture list be complete, or again, you will get a phone call from the fabricator for potential unassigned D-codes in the wheel or list.

C. NC DRILL FILES

NC Drill files are files that contain the physical X- and Y-hole coordinates on the PCB. Features such as hole sizes, tolerances, and plating status (plated or not) are usually represented on either the drawing or a .DRR report file that comes with the NC Drill file. NC Rout files contain the X and Y paths to cut out, or singulate, the PCB from the fabrication panel, including any internal cutouts, slots, etc.

Usable file types for the NC Drill file are as follows:

1. Excellon 1
2. Excellon 2
3. American Standard Code for Information Interchange (ASCII) text drill file

Typical extensions for NC Drill files can include .DRL, .NCD, or .EXL—all of which depend greatly on the system outputting the NC Drill files.

Tips on NC Drill Files:

- Do not mix output formats on the NC Drill and NC Rout files—stick with a single convention (e.g., 2:4 trailing zero suppression and inch units). Do not mix inches and metric units on the same file (e.g., inch tool sizes, but metric increments for position or vice versa).
- Do not mix formats (e.g., one file output as 2:4 trailing zero, but another in the same output package as 1:5 leading zero).
- If the job has epoxy-filled vias that are not all one tool size or easily identified by the fabricator via a note like, *All 0.008" vias under 'U1' and 'U2' to be epoxy-filled and planarized*, output a separate file denoting just those to be filled. A note simply stating that all vias-in-pad to be epoxy-filled means the board fabricator would have to identify all via-in-pad locations on both the top and bottom, pull them out, and create a separate NC Drill file to be done after lamination and before the standard through-hole drill. Again, to eliminate the opportunity for error, provide a separate NC Drill file for epoxy-filled vias in pad whenever possible.

- Provide separate NC Drill files for each blind or buried drill scenario. As with filled vias, all blind or buried vias need a separate NC Drill file with only those blind or buried holes on them.

For example, if you have an eight-layer PCB with blind vias 1–2, buried vias 3–6, and another set of blinds from 7–8, there should be at least four drill files output in this scenario:

1. Blind via holes for layers 1–2
2. Buried via holes for layers 3–6
3. Blind via holes for layers 7–8
4. All through holes for layers 1–8

A discrepancy between drawing drill tables and the NC Drill file are one of the most common issues in this area. Another frequent issue requiring contact and resolution is disconnects in hole counts, sizes, and plating status depicted on the drill drawing. Be sure to double-check these before releasing the files. Avoid “double hit” holes—two holes of the same size, or even two holes of a different size, placed in precisely the same X and Y coordinate. This will also require a phone call or email from your fabricator, or worse, excessive scrap or defective product.

It is important to understand during the design process that both plated and non-plated holes require a drill size compensation. This means that the hole size for plated holes needs to be drilled a larger size so that the finished hole size will be correct after plating. Typical drill compensation for a fabricator is around 0.004”–0.005” larger than the nominal finished hole size. Non-plated holes will need a slight increase to offset material shrinkage during fabrication.

D. IPC NETLISTS

As discussed in Chapter 1, an IPC netlist is used for a comparison between the design criteria and the output Gerber data from the customer. The most common forms of IPC netlists provided by customers are IPC-D356, IPC-D356A, or Mentor neutral files, and fabricators advocate providing these. If the part specification requires IPC-6012 Class 3, Class 3A, or an AS9102 FAI, the fabricator is required to run an IPC netlist compare. This means that parts for any other board class should have netlists provided. The best way to ensure electrical design integrity is to provide an IPC netlist. You will be glad you did.

Netlist comparisons are not to be confused with a one-up comparison done at the CAM stage by fabricators to eliminate the possibility they changed anything electrically via etch or drill manufacturing compensations. The intent of a netlist compare is to compare the electrical design criteria against the exported Gerber files.

Here is one very important point: Customers frequently ask fabricators to “just make an IPC netlist for us.” It is absolutely critical to understand that this would defeat the entire purpose of the netlist compare in the first place. Netlists are a direct reflection of the customer’s electrical design. By definition, creating one from the customer’s exported Gerber data would never find an actual electrical mismatch. If netlist mismatches are found at the fabrication level, it is necessary for the fabricator to contact the customer and share the net-compare results with them. These results may include legitimate netlist issues such as unconnected features (opens), missing relief pads on planes (shorts), bridged isolation barriers (shorts), or netlist issues caused by the netlist definition.

Common Causes of Netlist Mismatch

Netlist mismatch can be caused when:

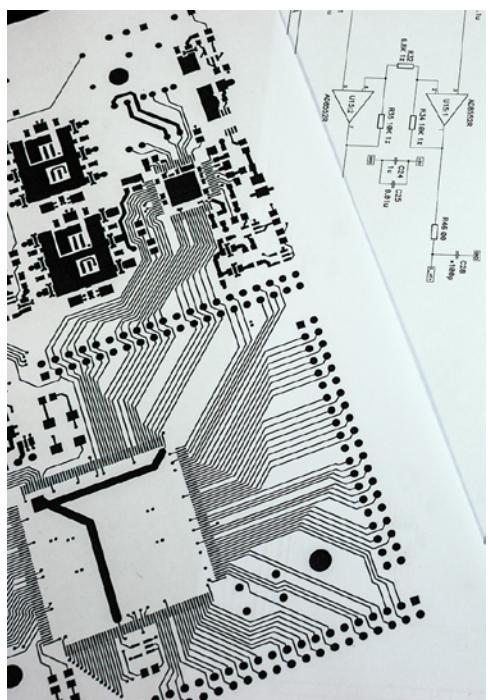
- An analog ground (AGND) to digital ground (DGND) short is intentional by the customer but not identified on a README drawing note or in the header of the IPC file. This is helpful when a board is time-critical and the customer cannot afford delays.
- Mounting-hole electrical connections are made during assembly by the mounting screws themselves. The IPC netlist may show these as connected, but the Gerber files and drawings call these holes non-plated. Therefore, they are designated as “non-electrical,” which causes the broken or open net.
- Layers and netlists are not properly registered. Symmetrical boards are particularly susceptible to this. Also, if metal features extend past the outside fabrication profile on a part and the profile line is not removed before running netlist compare, the netlist compare will come up as erroneous shorts where the fabrication line connected to the overhanging feature.

- Castellations are edge-plated features that the netlist defines as connected during assembly, but they may show up as broken or open nets at the fabrication level. This will require a phone call to the customer to clarify. Again, this confusion can be avoided by calling out any intentional shorts or opens on a README file or other fabrication note. Some customers have entities on a Gerber file, such as a metal-land area, split into two separate nets that show up as shorted nets after etch compensation—a compensation to all metal features to account for the known loss during the etching process. Other times, depending on the netlist definition, non-plated through-holes might be flagged as “missing” in a netlist compare.

Whereas these anomalies are not “real” netlist issues, they still must be communicated to the customer for disposition and will cause delays. A good fabrication shop can usually tell the customer what is creating the short or open and can generally provide an answer fairly quickly.

You may be asking yourself, “Do I even need to supply an IPC netlist?” Your next question might be, “Is this a Class 3 or aerospace PCB?” If the first answer is yes, then the second answer is non-negotiable. Again, if the PCB is being called

out on the drawing, specification, PO, or README file as a Class 3, Class 3A 6012, or AS9102 part, the fabricator is obligated to run a netlist compare. If not, you should ask, “Is electrical integrity important?” From a fabrication standpoint, we would always like to see IPC netlists provided, regardless of their respective board class. Many times, we have received incomplete data on densely packed multilayers that were saved by a provided netlist.



E. ASSEMBLY ARRAY DRAWINGS

If you have already chosen your assembler for a given part, they may ask that you panelize the part in an

array—a multiple-up subpanel where scoring is utilized for the outside profile, or tabs that remain after the fabricator routs out the profile. The assembler will then singulate the PCBs after assembly. This is accomplished by creating a subpanel drawing.

For most fabricators, if subpanelization is required but no drawing exists, your fabricator can create the subpanel for you. However, there are certain things the fabricator would need to know, basically, the same things a designer would need to know if a subpanel drawing is requested by your chosen assembler. Many autoinsertion devices for loading components at an assembly level require specific sizes for board fiducials and tooling, and there may be specific areas where fiducials or tooling must be located for programming the pick-and-place machines.

There are nine main things fabricators need to know to create a subpanel array drawing:

E1. Breakaway Rails

Breakaway rails around the array can be anywhere from 0.2" to 1", but most are approximately 0.5".

E2. Fiducials

Targets used for location and orientation at the assembly level are usually specific to the assembler and between 0.04" and 0.1" in size. It is most common for pick-and-place machines to have a 0.040" fiducial with either a 0.080" or 0.1" mask clearance associated with them. Assemblers usually require a minimum of three fiducials to triangulate and orient for assembly programming. Some assemblers even require "local" fiducials, or fiducials designated for individual parts. These should be negotiated with the assembler beforehand for proximity to the part and should ideally be done at the layout stage because board manufacturers may not know the assembler's preferences.

E3. Tooling Holes

Usually measuring 0.1" or 0.125", tooling holes typically have a specific location on the rails based on the assembler's preference, but are often located in each corner of the array.

E4. Nomenclature

Additional text for serialization or part information is occasionally needed. Sometimes the end-user wants additional text on the rails of the subassembly panel. Be sure to include a preferred text size and specific information about what should be in the text on the periphery, part number, revision, silkscreen

blocks for serialization after assembly, etc.

E5. Keep-Out Areas

Define any areas of the part where you would not like tabs to exist or where you want a cutout in the rail frame. If you have specific areas on your part where you cannot have any tabs or perforation holes for depaneling, or areas where proximity of features to the board edge is too tight for tabs or score lines, you will want to denote that on a sub-drawing.

E6. Tabs

Define both the minimum number of tab locations and the width of the tabs. Depending on the assembler's equipment sets and processes, some may want a smaller quantity of wider tabs for more stability through assembly. Others may want a higher number of thinner tabs. When defining the placement of tabs in the array, consider tip five on keep-out areas. The location of tabs is important because it directly impacts the stability of the array during assembly.

E7. Perforation Holes

Perforation holes are typically drilled at the tab/PCB edge interface to facilitate breakaway but may also be assembler-specific depending on their singulation method. Again, either the designer or chosen assembler may have something to say on this topic and all information must be conveyed to the board fabricator.

If left unspecified, a fabricator will usually locate the perforation holes on the tabs centered on the PCB part edge. It is important to define this because many designers and assemblers prefer the fabricator to back the perforation holes on the tab away from the fabrication line if there is a feature proximity issue. This deals with the issue of traces/pads lifting when depaneling due to close proximity to the PCB edge. The downside to this is it results in a protruding "nub" of material left on the PCB edge that will need to be removed by sanding to be flush with the part edge.

If there is room to the edge in the design, it may be preferable to go the opposite direction and ask that the perforation holes be located inside the PCB edge so when the parts get broken out of the array, the parts are flush and do not require any additional sanding operations.

E8. Scoring

The alternative to an array with tabs holding the parts in place is to score the part edges for breakaway. In scoring, a "V" cut is made from both sides of the

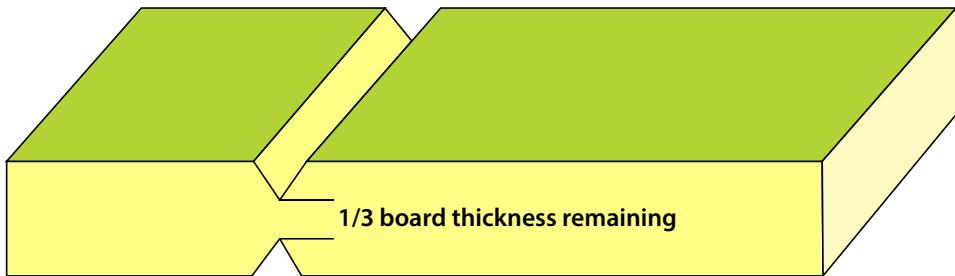


Figure 2.2: Ideal scoring "V" cut.

PCB, which leaves a “web” of material that is easily singulated after assembly (Figure 2.2). This requires some communication with the fabricator regarding his score blade width to help prevent any metal features from being too close to the part edge such that they could be clipped or exposed by the score blade itself.

You may want to avoid scoring small parts with a thin overall dielectric thickness because it may not provide the structural strength to hold up during the assembly processes. Further, a part with corner radii or chamfer requirements will have to be routed prior to scoring.

E9. Nesting

Nesting PCBs within the array can be done to increase material utilization if the shape of the PCB allows for this, such as with an “L” or triangle shape. In these cases, the PCBs can be rotated 180° to one another, which allows you to put more parts on a given array. Again, this should be discussed with both the fabricator and assembler because tab locations may not be repeatable, meaning that the space between parts may have to increase, which defeats the purpose of the nesting in the first place.

F. MANUFACTURABILITY DATA EDITS

Lastly, if you are requesting stepped array data from your fabricator to provide to your assembler, please note that subpanel data should not be transferred from one fabricator to another because the subpanel data will have manufacturability and compensation edits specific to a PCB fabricator that may not fit with another fabricator’s processes. The same applies for subpanel arrays with impedance coupons—they too are fabricator-specific. They may be based on a different allowable material type and have different Dk values with different trace widths and spaces to meet the designed impedance requirements.

Conclusion

In today's electronic environment, designers are challenged more than ever with the task of designing PCBs to meet the ever-changing needs of the technology driving our world today. The importance of a close working relationship between the PCB designer and fabricator cannot be overstated. The quality of the designer's output package has a direct correlation to accurate quoting, fabrication, and product functioning. This will certainly vary from one fabricator to another, but the guidelines defined in this book should be common to any experienced fabricator. The hope is this book has helped you to understand what critical files and information are needed for PCB fabrication, and what pitfalls to avoid in exporting data files from CAD systems. Remember, the key to success for any new PCB design project is early engagement and expert consultation with your PCB fabricator.

REFERENCES

IPC-2220-FAM: Family of Design Standards for Printed Boards

IPC-4101: Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4552: Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

IPC-6012: Qualification and Performance Specification for Rigid Printed Boards

IPC-6012DS: Space and Military Avionics Applications Addendum to IPC-6012D: Qualification and Performance Specification for Rigid Printed Boards

IPC-6013: Qualification and Performance Specification for Flexible Printed Boards

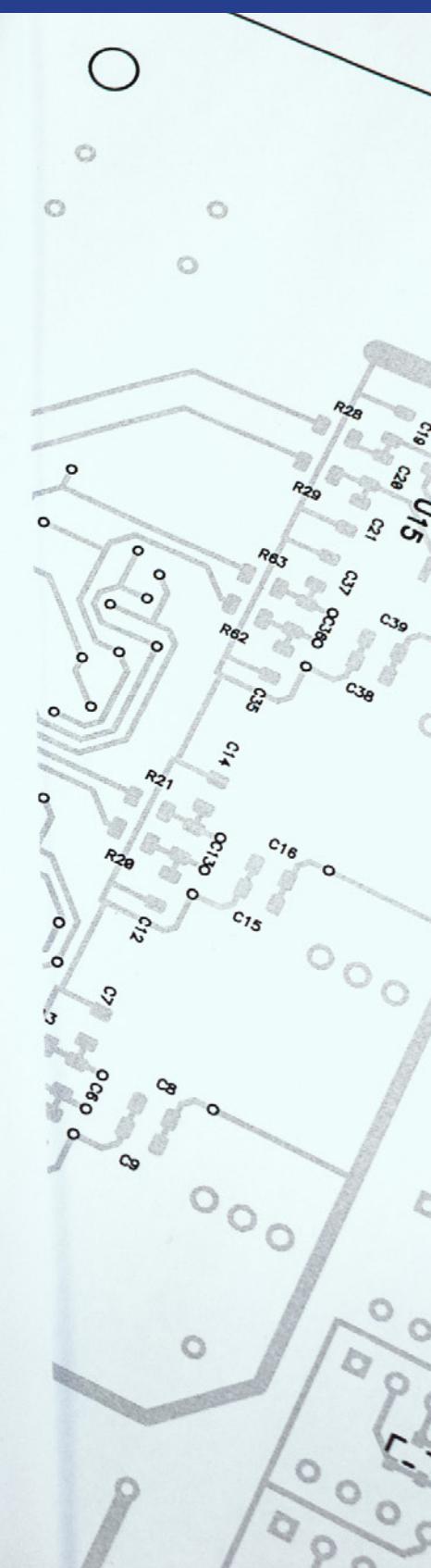
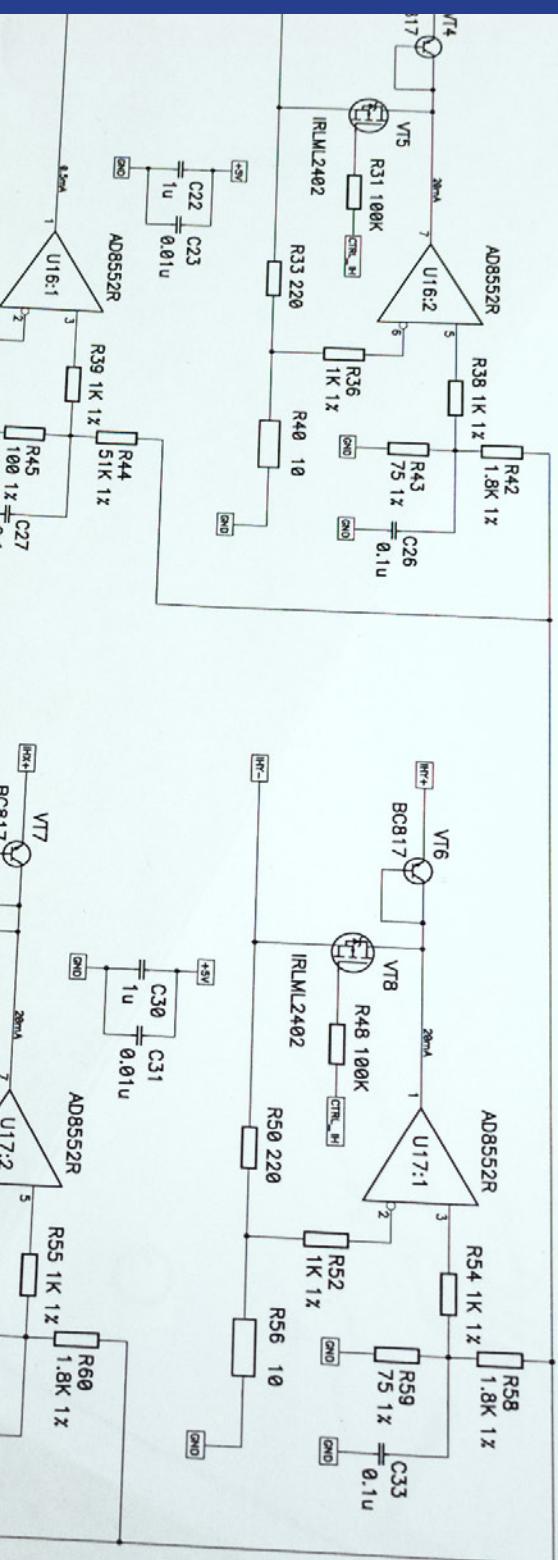
IPC-6018: Qualification & Performance Specification for High Frequency (Microwave) Printed Boards

IPC-D-356B: Bare Substrate Electrical Test Format

IPC-SM-840: Qualification and Performance Specification of Permanent Solder Mask

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Fab Output File Checklist

IMAGE DATA

- ODB++
- Gerber 274D (with separate aperture file)
- Gerber 274X (with apertures embedded)
- Gerber 2

Images

(Not all may apply to your given job)

- Inner layers
- Outer layers
- Solder mask top
- Solder mask bottom
- Silkscreen top
- Silkscreen bottom

NC Drill file included?

YES NO

File Type

- Excellon 1
- Excellon 2
- ASCII text

Please send a **separate** NC file for each blind or buried via scenario:

- Blind vias
- Buried vias

Numerical Format

- Tool unit: inch
- Tool unit: metric

Zero Suppression

- Leading
- Trailing
- None

DRAWINGS / NETLIST

Drawing provided?

YES NO

File Type

- PDF

- Gerber

- DXF

- IPC netlist

IPC netlist provided?

YES NO

File Type

- IPC-D-356

- IPC-D-356A

- Mentor neutral file

README file provided?

YES NO

Controlled impedance?

YES NO

Epoxy fill?

YES NO

If epoxy fill is not regional such as "all .008 vias at UI," please provide a separate file denoting the epoxy fill as either an image file or a separate NC Drill file.)

Include any special information relevant to unique tolerance requirements:

GLOSSARY

Analog Circuit: An electrical circuit that provides a continuous quantitative output as a response from its input.

Array: Combining multiple individual PCBs into a subpanel to facilitate the assembly process.

ASCII: American Standard Code for Information Interchange. ASCII is the basis of character sets used in almost all present-day computers.

Assembly: The process of positioning and soldering components to a PCB. The act or process of fitting together parts to make a whole.

Assembly Drawing: A drawing depicting the locations of components with their reference designators on a printed circuit. Also called "component locator drawing."

Automated Test Equipment (ATE): Equipment that automatically tests and analyzes functional parameters to evaluate performance of the tested electronic devices.

Blind Vias: Used in multilayer boards where a drilled hole requires connections from an outer layer to an inner layer, when the hole must not go through the entire PCB.

Buried Vias: Used in multilayer boards where inner layers require connections between a subassembly of layers, but the via does not extend to the outer layers.

Copper Weight: The thickness of copper on the surface of a PCB layer. It is measured in oz./sq. ft. For example, 1 oz. = a nominal thickness of 0.00014".

Design for Manufacturing (DFM): Ensures that the design fits the fabrication process requirements. DFM includes assessments for minimal trace width, minimal trace-to-trace distance, minimal hole size, and minimal hole clearance in context with industry established guidelines for limits of producibility.

Dielectric: An insulating medium between conductors or conductive layers.

Etch Compensation: Small adjustments to nominal customer-provided Gerber data that compensate for the amount of copper that will be etched from the traces and pads. This will vary depending on the copper weight but will be transparent to the final PCB.

Gerber File: Data file used to control a laser-imaging machine, such as a photoplotter.

Ground Plane: A conductive plane as a common ground reference in a multi-layer board for current returns of the circuit elements and shielding.

Impedance: The measure of the opposition (resistance) that a circuit presents to the passage of a current when a voltage is applied in an alternating current circuit. Controlled impedance is the process of manufacturing a PCB to meet a specific impedance requirement.

Land: Metallized area of the board for connection and attachment of electronic components.

Legend (Silk Screen): A layer designated to place legend elements on the top or bottom side of the board. Two corresponding layers are available—the top and bottom silk.

Minimum Conductor Width: The smallest width of any conductors, such as traces, on a board.

Minimum Conductor Space: The smallest distance between any two adjacent conductors, such as traces, on a board.

Net: A set of connection points that are to be connected electrically on the board.

Netlist: A list of parts and their connection points that are connected in each net of a circuit.

Pick-and-Place (Automatic Component Placement): Machines used to automate component placement. High-speed component placement machines, known as chip shooters, place the smaller, lower pin count components. More complex components with higher pin counts are placed by fine pitch machines that have greater precision.

Plated Through-Hole (PTH): A plated hole used as a conducting interconnection between different layers or sides of a board. Serves as a connection for through-hole components or vias.

Signal Layer: Layer of a board in which traces can be placed. For a two-sided board, two signal layers are available—the top and the bottom layers.

Test Point: A specific point on a PCB used for specific testing of functional adjustment or quality in the circuit-based device.

Through-Hole: A drilled hole in the board, usually used for mounting purposes.

Via: A plated through-hole used for the interconnection of conductors on different sides or inner layers of a circuit board.

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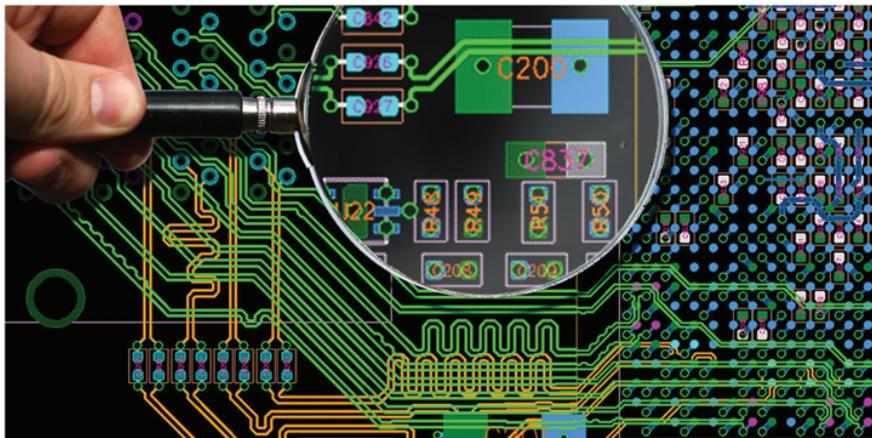


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With over 30 years in business, Prototron Circuits is one of the industry leaders when it comes to high-technology, quick-turnaround (QTA) PCBs. Their continued outstanding performance (98%+ quality and delivery) has made them a true preferred source of all companies needing reliable QTA PCBs. With their new global sourcing solution, Prototron Circuits is truly America's board source.

Prototron Circuits has facilities in Redmond, Washington, and Tucson, Arizona. Due to their focus on the high-mix, low-volume market, they see thousands of new part numbers and data packages, making them especially qualified to write *The Printed Circuit Board Designer's Guide to... Producing the Perfect Data Package*.

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Great Data Produces Great PCBs

For over 30 years Prototron Circuits has been committed to providing the best printed circuit boards in the world. During that time we have helped thousands of engineers, designers and their companies create the best data packages possible.

As a further service to our customers as well as PCB users globally, we have compiled our many years of experience into this one valuable and informative book to help everyone produce great data packages.

Read, enjoy and don't hesitate to contact us with any questions or comments. We'd love to talk to you.

CALL: **888-847-7686** EMAIL: **info@prototron.com**



Author and PCB front-end expert Mark Thompson is available to present a seminar on creating great data packages. Contact us today to set yours up.

CERTIFICATIONS

ISO 9001:2015
AS 9100D
MIL-PRF-55110
MIL-PRF-31032

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