VERIFICATION OF LOGIC GATES

EXP NO. : 1

DATE :

AIM

To verify the logic gates operation with its truth tables.

APPARATUS REQUIRED

SL NO.	COMPONENT	SPECIFICATION	QTY
1.	AND GATE	IC 7408	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	NAND GATE 2 I/P	IC 7400	1
5.	NOR GATE	IC 7402	1
6.	EX-OR GATE	IC 7486	1
7.	NAND GATE 3 I/P	IC 7410	1
8.	IC TRAINER KIT	-	1
9.	PATCH CORD	-	As per Requirement

THEORY

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND & NOT are basic gates. NAND, NOR are known as universal gates. Basic gates can be formed from these gates. XOR & XNOR are derived gates.

AND GATE

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND GATE

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the inputs is low.The output is low level when both inputs are high.

NOR GATE

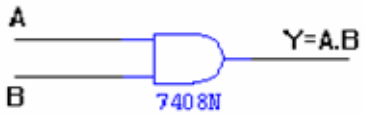
The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

X-OR GATE

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

AND GATE

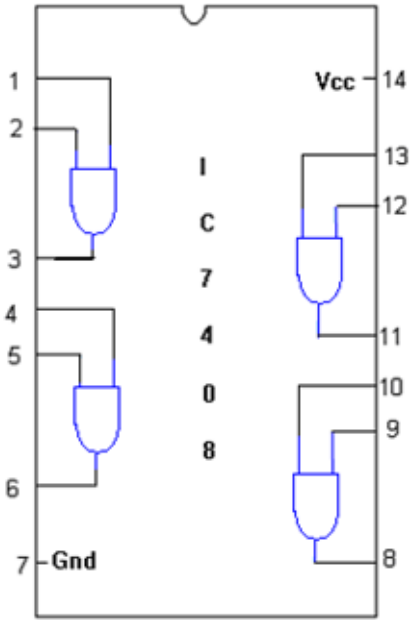
SYMBOL



TRUTH TABLE

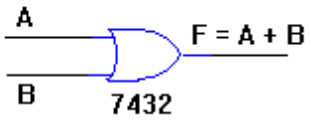
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

PIN DIAGRAM

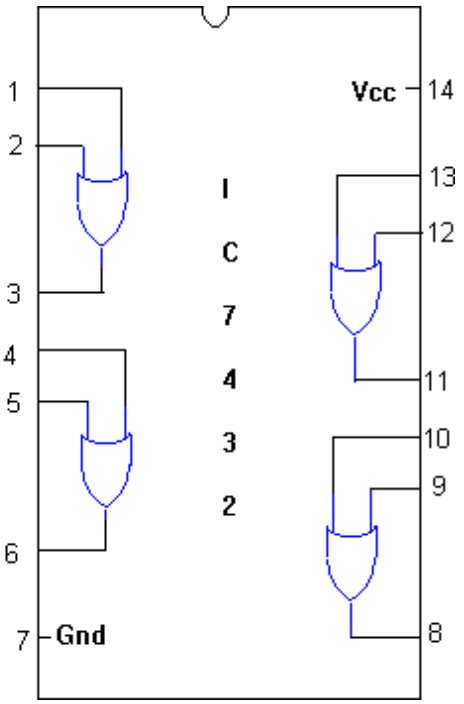


OR GATE

SYMBOL



PIN DIAGRAM

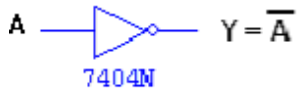


TRUTH TABLE

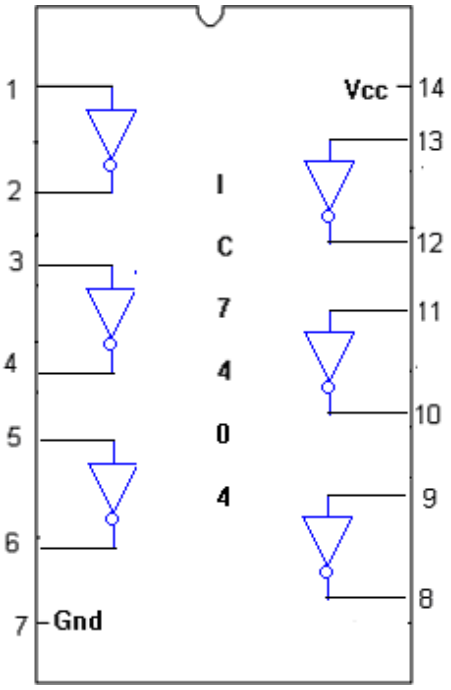
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE

SYMBOL



PIN DIAGRAM

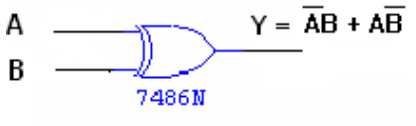


TRUTH TABLE

A	$\overline{A}$
0	1
1	0

EX-OR GATE

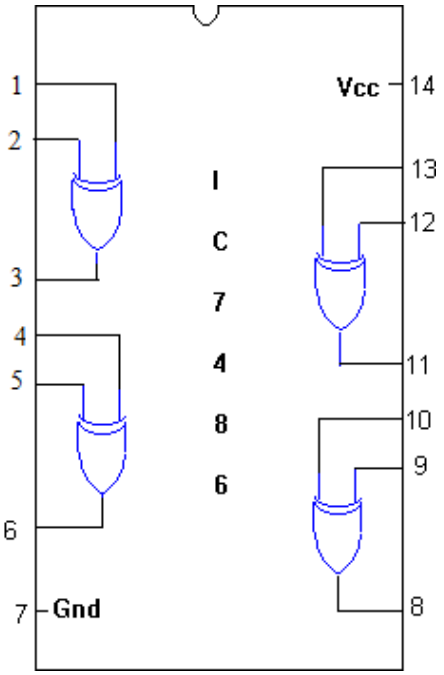
SYMBOL



TRUTH TABLE

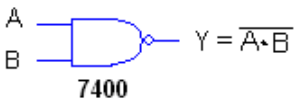
A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM



2- INPUT NAND GATE

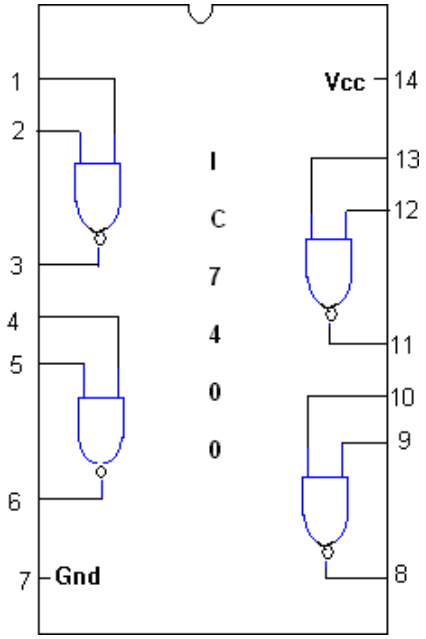
SYMBOL



TRUTH TABLE

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIAGRAM



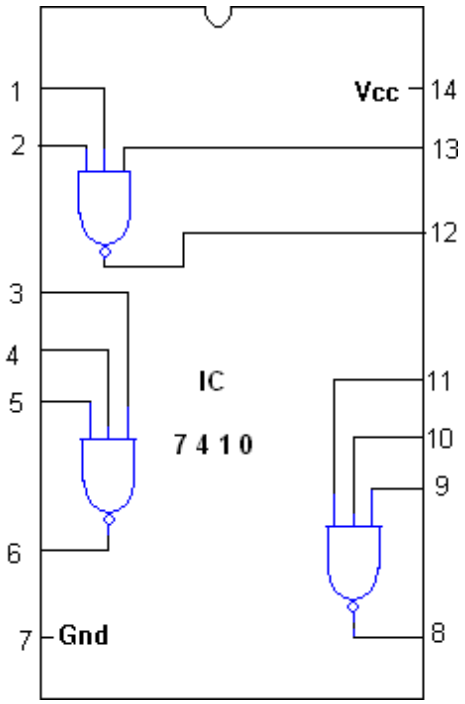
3-INPUT NAND GATE

SYMBOL

TRUTH TABLE

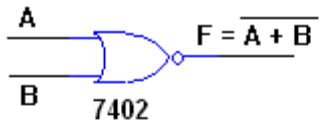
A	B	C	$\overline{A.B.C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

PIN DIAGRAM

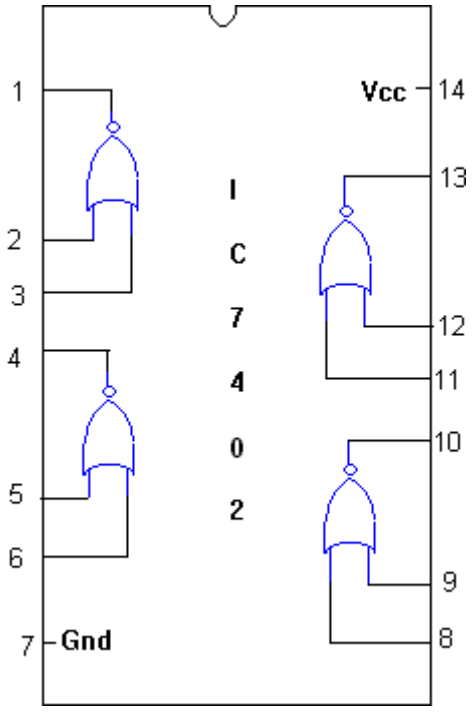


NOR GATE

SYMBOL



PIN DIAGRAM



TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

PROCEDURE

Connections are given as per circuit diagram. Logical inputs are given as per circuit diagram. Observe the output and verify the truth table.

RESULT :

Thus the working of the logic gates was studied and their truth tables were verified.