	Course title		L T P J C
CSE5006	MULTICORE ARCHITECTURES		2 0 2 0 3
			Syllabus version
			V. 1.
Course Ob	jectives:		
1. To provide	knowledge on basics of Multicore architect	ures and paral	lel programming
models	-	-	
2. To design	and develop parallel programs using parallel	el computing p	latforms such as
OpenMP, C		7 6 7	
•	program optimizations on parallel programs	and evaluate	the performance
using profil		and cyanance	the performance
using prom	ing tools		
Ermantad Course	Outcomo		
Expected Course	completing the course the student should be at	lo to	
	line the developments in the evolution of mul		tures and parallel
	gramming paradigms	ir-core architect	tures and paramer
CO2. Cor	nprehend the various programming languages	and libraries fo	or parallel computin
	forms		or paramer companie
	of profiling tools to analyse the performance	of applications	by interpreting the
	en data	11	, 1
CO4. Cor	npare and contrast the features of parallel prog	gramming langu	ages such as
Ope	enMP and CUDA		
	te parallel programs using OpenMP and CUD		
CO6. Eva	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative p		ing architectures for
CO6. Eva an e	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design	parallel comput	_
CO6. Eva an e CO7. Ana	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design alyse performance parameters such as speed-u	parallel comput	_
CO6. Eva an e CO7. Ana	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design	parallel comput	_
CO6. Eva an e CO7. Ana	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design alyse performance parameters such as speed-u	parallel comput	_
CO6. Eva an e CO7. Ana	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design alyse performance parameters such as speed-u	parallel comput	_
CO6. Eva an e CO7. Ana aga	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design alyse performance parameters such as speed-u	parallel comput	_
CO6. Eva an e CO7. Ana aga Student Learning	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17	p, efficiency for	r parallel programs
CO6. Eva an e CO7. Ana aga Student Learning	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures	parallel computer p, efficiency for 2 hours	r parallel programs
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intra	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of signs.	parallel computer p, efficiency for 2 hours	r parallel programs
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intra	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of signs.	parallel computer p, efficiency for 2 hours	r parallel programs
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intro Evolution of mult processing and hy	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of signer threading	p, efficiency for the state of	sLO:
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intra Evolution of mult processing and hy Module:2 Para	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of signer threading allel Computers and programming	p, efficiency for the state of	sLO: 2
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intro Evolution of mult processing and hy Module:2 Para Threading Conce	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of sign per threading allel Computers and programming pts, Communication Architectures and Computers and Co	p, efficiency for 2 hours ngle core, multi- 5 hours munication Co	SLO: 2 i-core, multi- SLO: 2 osts, Thread Level
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intre Evolution of mult processing and hy Module:2 Para Threading Conce Parallelism(TLP),	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of signer threading ple Computers and programming pts, Communication Architectures and Confustruction Level Parallelism(ILP), Confusions of Signer and Confusions and Conf	2 hours ngle core, multi 5 hours nmunication Conparisons, Cac	SLO: 2 i-core, multi- SLO: 2 osts, Thread Level the Hierarchy and
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intra Evolution of mult processing and hy Module:2 Para Threading Conce Parallelism(TLP), Memory-level Pa	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of sign per threading tallel Computers and programming pts, Communication Architectures and Confirmation Instruction Level Parallelism(ILP), Confirmallelism, Cache Coherence, Parallel program	2 hours ngle core, multi 5 hours nmunication Conparisons, Cac	SLO: 2 i-core, multi- SLO: 2 osts, Thread Level the Hierarchy and
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intre Evolution of mult processing and hy Module:2 Para Threading Conce Parallelism(TLP),	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of sign per threading tallel Computers and programming pts, Communication Architectures and Confirmation Instruction Level Parallelism(ILP), Confirmallelism, Cache Coherence, Parallel program	2 hours ngle core, multi 5 hours nmunication Conparisons, Cac	SLO: 2 i-core, multi- SLO: 2 osts, Thread Level the Hierarchy and
CO6. Eva an 6 CO7. Ana aga Student Learning Module:1 Intre Evolution of mult processing and hy Module:2 Para Threading Conce Parallelism(TLP), Memory-level Pa Message Passing,	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of signer threading ollel Computers and programming pts, Communication Architectures and Confirmation Instruction Level Parallelism(ILP), Confirmallelism, Cache Coherence, Parallel program Vectorization	2 hours ngle core, multi 5 hours nmunication Conparisons, Caciming models, S	SLO: 2 i-core, multi- SLO: 2 osts, Thread Level the Hierarchy and Shared Memory and
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intre Evolution of mult processing and hy Module:2 Para Threading Conce Parallelism(TLP), Memory-level Pa Message Passing, Module:3 Ope	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative pefficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of signer threading pts, Communication Architectures and Confinity Communication Architectures and Confinity Confin	2 hours ngle core, multi 5 hours nmunication Conparisons, Cac	SLO: 2 i-core, multi- SLO: 2 osts, Thread Level the Hierarchy and
CO6. Eva an e CO7. Ana aga Student Learning Module:1 Intro Evolution of mult processing and hy Module:2 Para Threading Conce Parallelism(TLP), Memory-level Pa Message Passing, Module:3 Operation of the Concept of	te parallel programs using OpenMP and CUD luate efficiency trade-offs among alternative perficient parallel Application design alyse performance parameters such as speed-usinst serial programs g Outcomes (SLO): 2,11,14,17 oduction to Multi-Core Architectures icores through Moor's Law, Comparisons of signer threading ollel Computers and programming pts, Communication Architectures and Confirmation Instruction Level Parallelism(ILP), Confirmallelism, Cache Coherence, Parallel program Vectorization	2 hours ngle core, multi 5 hours munication Comparisons, Cacaming models, S 5 hours	SLO: 2

Module:4 | CUDA Programming(Compute Unified | 6 hours | Device Architecture) | 6 hours | 6 hours

SLO: 2

		to GPU Computing, CUDA Programming Mod			
		on in CUDA, CUDA Memory Model, Shared CUDA API Features	Memory Matri	ix Multiplication,	
Addit	ionai C	LUDA AFI realules			
Modu		Performance Analysers	4 hours	SLO: 14	
		yzer and collector (ITAC), VTune Amplifier XE, En	ergy Efficient Pe	rformance,	
Integ	gratea .	Performance Primitives (IPP)			
Modu	ıle:6	Contemporary tools	3 hours	SLO: 14	
MKI	L (Mat	h Kernel Library), Threading Building Blocks, CUD	OA Tools		
N / . 1	1.7	HTC I MTC	21	ST O. 14	
Modu		HTC and MTC Throughput Computing), MTC (Many Task Compu	ting) Top 500 S	SLO: 14	
		op 10 Super Computer architectural details, Explori	0,	uper computers in	
		r r r r r r r r r r r r r r r r r r r	8 1		
Modu	ıle:8	Contemporary issues:	2 hours	SLO: 11	
		Total Lecture hours:	30 hours		
		Total Dectare nours.	30 110413		
Text 1	Book(s)	<u> </u>		
&	•				
	ence I				
	Rob Fa 2013	rber, "CUDA Application Design and Developmen	t", Morgan Kau	fmann Publishers,	
	Shameem Akhter and Jason Roberts, "Multi-Core Programming", 1st edition, Intel Press, 2012				
	Robert Oshana, "Multicore Software Development Techniques: Applications, Tips, and Tricks", Newnes,1 edition, 2015				
	David B. Kirk, Wen-mei W. Hwu, "Programming Massively Parallel Processors: A Hands-				
	on Approach (Applications of GPU Computing Series)", 1st edition, Morgan Kaufmann,				
2	2010.				
List o	f Cha	llenging Experiments (Indicative)	SLC	D: 14,17	
		e with Open MP		2 hours	
		Ip Sample Programs		2 hours	
		ion Time estimation ing sample programs			
		pment of documentation for observations			
		p a sample program using Execution Environmen	nt Routines	2 hours	
		ite interesting observations by comparing variou			
		p a program using following construct and descri	be scenario for	8 hours	
		ed of construct			
		parallel Construct Determining the Number of Threads for a parallel R	egion		
		Work-sharing Constructs	2051011		
		5		1	

	a. loop construct						
	b. sections construct						
	c. single construct						
	4. schedule clause						
	a. static						
	b. Dynamic						
	c. guided						
	5. Data Environment Constructs						
	a. Shared Clause						
	b. Critical Construct						
	c. Reduction Clause						
	6. Master Construct						
	7. Nowait clause						
	8. Barrier Construct						
	9. Atomic Construct						
5.		6 hours					
	1 Experimental setup						
	2 Parallelizing given serial program into parallel						
	3 Analysing parallel programs						
6	1 · 8 · · · · · · · · · · · · · · · · ·	8 hours					
	1 Write a CUDA C/C++ program that add two array of elements and						
	store the result in third array						
	2 How to Reverse Single Block in an Array using CUDA C/C++						
	3 CUDA C program for Matrix addition and Multiplication using						
	Shared memory						
	4 Write CUDA C/C++ program for Vector Addition. Modify your						
	program so, that it can add two vector of arbitrary size						
	28 hours						
	Recommended by Board of Studies DD-MM-YYYY Approved by Academic Council No. 46 Date 24.08.2017						
Apr							