IMPLEMENTATION OF ZIGBEE TRANSMITTER AND RECEIVER USING VERILOG HDL

A Report submitted

in partial fulfillment for the Degree of

Bachelor of Technology

in

Electronics and Communication Engineering

By

HENA NAAZ (13 – BEC – 0023)

Under guidance of

Dr. Dinesh Prasad

Department of Electronics & Communication Engineering

F/O Engineering & Technology, Jamia Millia Islamia

New Delhi – 110025

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CERTIFICATE

This is to certify that the project report entitled **IMPLEMENTATION OF ZIGBEE TRANSMITTER AND RECEIVER USING VERILOG HDL** submitted by **Hena Naaz** to the Department of Electronics & Communication Engineering, F/O Engineering & Technology, Jamia Millia Islamia New Delhi – 110025 in partial fulfillment for the award of the degree of B. Tech in (Electronics & Communication Engineering) is a *bonafide* record of project work carried out by them under my supervision. The contents of this report, in full or in parts, have not been submitted to any other Institution or University for the award of any degree to the best of our knowledge.

Dr. Dinesh Prasad

(Supervisor)

Associate Professor

Department of Electronics & Communication Engineering

DECLARATION

I declare that this project report titled **IMPLEMENTATION OF ZIGBEE TRANSMITTER AND RECEIVER USING VERILOG HDL** submitted in partial fulfillment of the degree of B. Tech in (Electronics & Communication Engineering) is a record of original work carried out by me under the supervision of **Dr. Dinesh Prasad** and has not formed the basis for the award of any other degree, in this or any other Institution or University. In keeping with the ethical practice in reporting scientific information, due acknowledgements have been made wherever the findings of others have been cited.

HENA NAAZ (13-BEC-0023)

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I would like to express sincere gratitude to my project guide **“Dr. Dinesh Prasad”** for giving me the opportunity to work on this topic. It would never be possible for me to take this project to this level without his innovative ideas and his relentless support and encouragement.

HENA NAAZ (13-BEC-0023)

ABSTRACT

ZigBee technology was developed for a wireless personal area network (PAN), aimed at control and military applications with low data rate and low power consumption. This thesis is mainly focusing on development of Verilog model for ZigBee transceiver at physical layer using IEEE 802.15.4. ZigBee is a low-cost, low-power, wireless mesh networking standard. First, the low cost allows the technology to be widely deployed in wireless control and monitoring applications. Second, the low power-usage allows longer life with smaller batteries. Third, the mesh networking provides high reliability and more extensive range. The work presented here is to show how we can implement ZigBee transceiver with its specifications by using Verilog, without using complex mathematical blocks.

A ZigBee chip can be tested and prepared by shifting the whole work from Verilog environment to cadence environment. This can be done by HDL languages like Verilog HDL. Here, Minimum Shift Keying (MSK) modulation technique is described, an analysis of which shows that the theoretical maximum bandwidth efficiency of MSK is 2 bits/s/Hz which is same as for Quadrature Phase Shift Keying (QPSK) and Offset Quadrature Phase Shift Keying (Offset QPSK). The implementation clearly confirms the viability of theoretical approach. Results show that OQPSK modulation with half sine pulse shaping is perfectly employed ZigBee technology.

TABLE OF CONTENTS

DESCRIPTION		PAGE NUMBER
CERTIFICATE		1
DECLARATION		2
ACKNOWLEDGEMENTS		3
ABSTRACT		4
LIST OF FIGURES		6
LIST OF TABLES		7
ABBREVIATIONS		8
1.Introduction		13
1.1	What is ZigBee	13
1.2	World's Most Common Frequency Bands	14
1.3	Why ZigBee is needed	15
1.4	Features of ZigBee	15
1.5	ZigBee General Characteristics	16
1.6	Applications of ZigBee	18

2.Architecture 20

2.1 Introduction 21

2.2 ZigBee Layers 21

2.3 ZigBee Topologies 25

2.4 ZigBee Architecture Overview 29

3.Transmitter 30

3.1 Introduction 30

3.2 Cyclic Redundancy Check 32

3.3 Bit-To-Symbol 32

3.4 Symbol-To-Chip 32

3.5 OQPSK 33

3.5.1 PSD of OQPSK Signal 36

4.Receiver 37

4.1 Introduction 37

4.2 Literature Review 39

4.3 OQPSK Demodulation 41

4.4 Chip Synchronization 42

4.5 De-Spreader 44

5.Result 46

5.1 Transmitter Simulation 46

5.2 Receiver Simulation 48

6.Conclusion 49

6.1 Project Conclusion 50

6.2 Comparison with other 51

6.3 Future Scope 52

REFERENCES

LIST OF FIGURES

FIGURE	TITLE	PAGE NUMBER
1.1.	Common Frequency Bands	14
1.2.	Star Network Topology	16
1.3.	ZigBee Applications	18
1.4.	Application Sectors of ZigBee Technology	19
2.1.	ZigBee Network Configurations	20
2.2.	ZigBee wireless Networking Protocols	21
2.3.	Acknowledgement Frame Format	24
2.4.	ZigBee Topologies	25
2.5.	ZigBee Star Topology	26
2.6.	ZigBee Tree Topology	27
2.7.	Cluster Tree Topology	28
2.8.	ZigBee Transceiver Architecture	29
3.1.	Phase Transition between QPSK and OQPSK	33
3.2.	Output after adding delay in quadrature of modulator	34

4.1.	ZigBee Receiver	38
4.2.	Demodulator block	42
4.3.	Chip synchronization block	43
4.4.	De-Spreading block	44
5.1.	Top module for Transmitter	46
5.2.	Output waveform of Symbol-to-Chip	46
5.3.	Top module for Receiver	47
5.4.	Output waveform of Demodulator	47
5.5.	Output waveform of Chip Synchronization	48
5.6.	Output waveform of De-spreader	48

LIST OF TABLES

TABLE	TITLE	PAGE NUMBER
2.1.	Frequency Range and Data rates supported by ZigBee Protocol	12
3.1.	Symbol to chip mapping using DSSS method	33
6.1.	Comparison of ZigBee with other Protocols	50

1. INTRODUCTION

1.1. What is ZigBee ?

ZigBee is an ad-hoc networking technology for LR-WPAN (low rate - wireless personal area networks). It is based on the IEEE 802.15.4 standard that defines the PHY and Mac Layers for ZigBee. It is low in cost, complexity & power consumption as compared to competing technologies such as Bluetooth or Wi-Fi. Data rates touch 250Kbps for 2.45GHz ,40 Kbps 915MHz band and 20Kbps for 868MHz band.

A wireless ad hoc network used by ZigBee is a decentralized type of wireless network. ZigBee network is ad hoc because it does not rely on a preexisting infrastructure, such as routers in wired networks or access points in managed wireless networks. Instead, each node participates in sending and receiving data to-and-fro to other nodes, so the determination of which nodes forward data is made dynamically on the basis of network connectivity.

ZigBee's applications include wireless light switches, electrical meters with in-home-displays, traffic management systems, and other consumer and industrial equipment that requires short-range low-rate wireless data transfer.

Its low power consumption limits transmission distances to 10–100 meter line-of-sight, depending on power output and environmental characteristics.

ZigBee was conceived in 1998, standardized in 2003, and revised in 2006. The name of ZigBee refers to the waggle dance of honeybees after their return to the beehive.

1.2. World's Most Common Frequency Bands

This standard specifies operation in the unlicensed 2.4 GHz (worldwide), 915 MHz (Americas and Australia) and 868 MHz (Europe) ISM bands. Sixteen channels are allocated in the 2.4 GHz band, with each channel spaced 5 MHz apart, though using only 2 MHz of bandwidth.

1.3. Why ZigBee is needed?

There are a multitude of standards that address mid to high data rates for voice, PC LANs, video, etc. However, up till now there hasn't been a wireless network standard that meets the unique needs of sensors and control devices.

Sensors and controls don't need high bandwidth, but they do need low latency, low cost and very low energy consumption for long battery lives and for large device arrays. Proprietary systems are creating significant interoperability problems with each other and with newer technologies.

Traditional point to point control system is no longer suitable to meet the new requirements, such as wireless, modularity, decentralization of control, integrated diagnostic, quick and easy maintenance, and low cost. The implementation of ZigBee architecture can improve the efficiency, flexibility, and reliability. ZigBee also reduces the installation, reconfiguration and maintenance time and cost of the network. At the same time an Infrastructure based network architecture (centralized) may introduce time delay uncertainty between sensor, actuator, and controller. This time delay is due to sharing of common medium and computational time required for signal processing.

1.4. Features of ZigBee

1. Low power consumption

The main design consideration for LR-WPANs is low power consumption, and therefore long battery life. Some of the techniques that help achieve low average power consumption are:

- Reduction of the amount of data transmitted
- Reduction of the transceiver duty cycle and the frequency of data transmissions
- Reduction of frame overhead
- Implementation of strict power management mechanisms, such as power-down and sleep modes

2. Simple protocol, global implementation

3. Network Flexibility

   Its design is flexible in nature since several parameters may be adjusted according to the application at hand.

4. Small size – less than 9mm * 9mm

   Although designing antennas is an art in of itself, keeping everything else the same, the rule is: lower frequencies require larger antennas, and where a ZigBee 2.4 GHz product can work well with a 6 cm/2.5-inch antenna

5. Hundreds of devices per network

1.5. ZigBee General Characteristics

1. Data rates of 20 kbps and up to 250 kbps:

ZigBee devices can transmit data over long distances by passing data through a mesh network of intermediate devices to reach more distant ones. ZigBee is typically used in low data rate applications that require long battery life and secure networking (ZigBee networks are secured by 128-bit symmetric encryption keys.) ZigBee has a defined rate of 250 Kbit/s, best suited for intermittent data transmissions from a sensor or input device

2. Star or Peer-to-Peer network topologies:

The star topology consists of a coordinator and several end devices (nodes). The end device communicates only with the coordinator. Any packet exchange between end devices must go through the coordinator. The disadvantage of this topology is the operation of the network depends on the coordinator of the network, and because all packets between devices must go through coordinator, the coordinator may become bottlenecked. Also, there is no alternative path from the source to the destination. The advantage of star topology is that it is simple, and packets go through at most two hops to

Fig: A star network

3. Support for Low Latency Devices: -
   In case of low latency devices, we have a centralized and a distributed slot assignment schemes for ZigBee tree networks. We observe that when assigning slots, the latency can be further reduced by reconnecting some tree links. More specifically, by the designed rules, a node is allowed to locally modify some of its neighbors′ parents, and then the node can be assigned to a better slot that can have the benefit of reducing the node's report latency.

4. Handshaking: -
   It is an automated process of negotiation that dynamically sets parameters of a communications channel established between two entities before normal communication over the channel begins. It follows the physical establishment of the channel and precedes normal information transfer.

5. Low Power Usage consumption: -

ZigBee is a low-power wireless specification based on the Institute of Electrical and Electronics Engineers (IEEE) Standard 802.15.4-2003 and was established in 2002 by a group of 16 companies. It introduces mesh networking to the low-power wireless space and is targeted towards applications such as smart meters, home automation, and remote-control units

6. 3 Frequencies bands with 27 channels: -

ZigBee operates in three different industrial, scientific, and medical radio

bands: Band 1:868-870 MHz (only one channel)

Band 2:902-928 MHz (channels 1 to 10)

Band 3:2.4-2.4835 GHz (channels 11 to 26)

In every radio band we have a number of available channels. For example, in the 2.4 GHz band there are 16 different channels, and each channel is 5MHz long. The center frequency these channels can be calculated.

7. Extremely low duty-cycle (<0.1%)

The principle behind a low duty cycle device is very simple: by restricting the duration and rate of repetition of any other user's transmission, it becomes statistically unlikely that they'll collide with those of others.

1.6 Applications of ZigBee Technology

Industrial Automation: In manufacturing and production industries, a communication link continually monitors various parameters and critical equipments. Hence ZigBee considerably reduce this communication cost as well as optimizes the control process for greater reliability.

Home Automation: ZigBee is perfectly suited for controlling home appliances remotely as a lighting system control, appliance control, heating and cooling system control, safety equipment operations and control, surveillance, and so on.

Smart Metering: ZigBee remote operations in smart metering include energy consumption response, pricing support, security over power theft, etc.

Smart Grid monitoring: ZigBee operations in this smart grid involve remote temperature monitoring, fault locating, reactive power management, and so on.

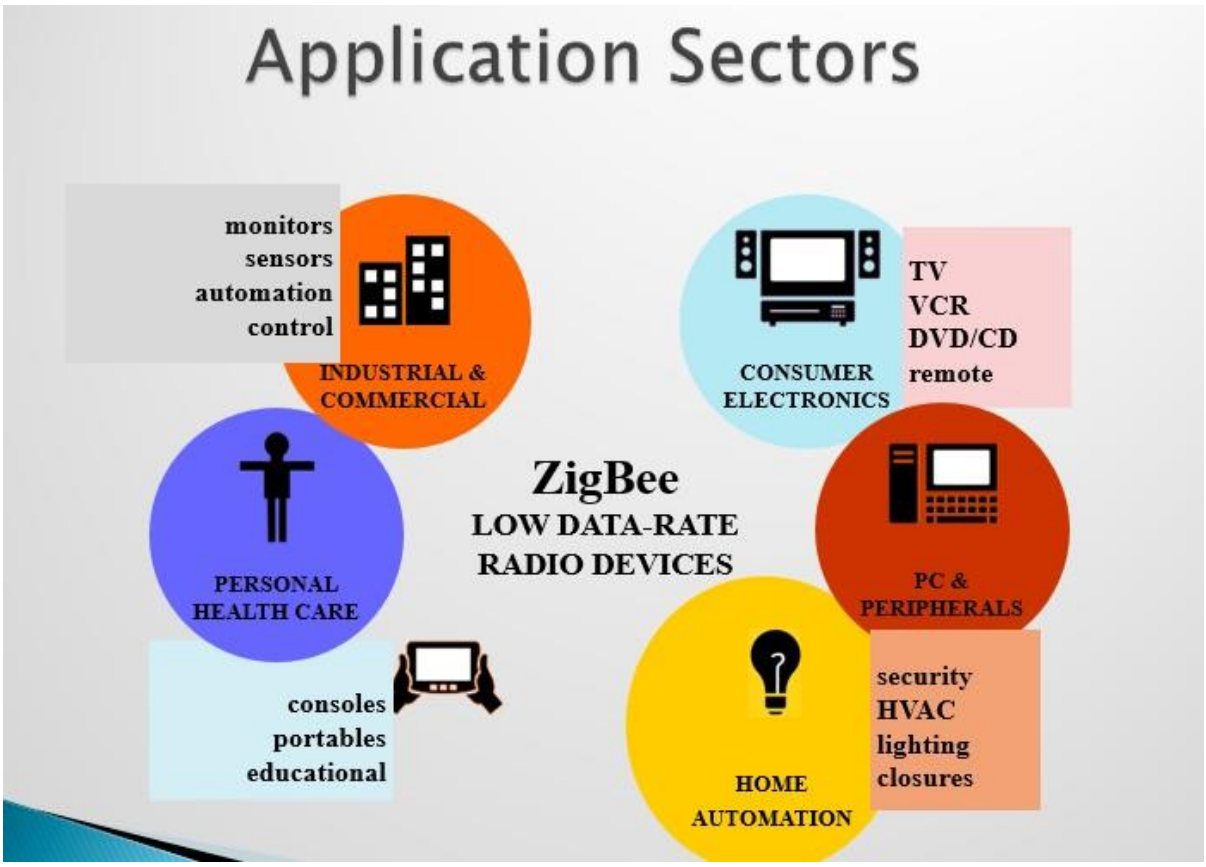


Fig: Various application sectors of ZigBee Technology

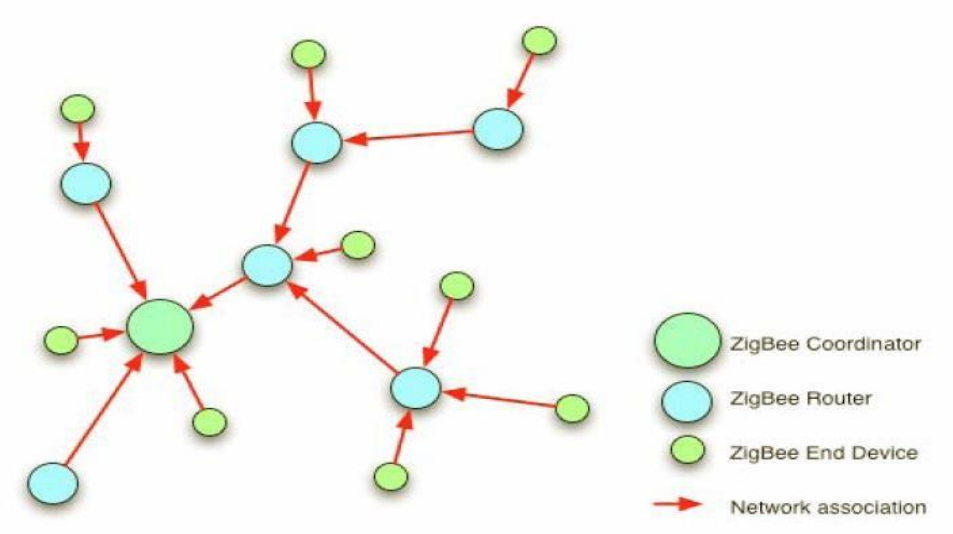
CHAPTER 2

ARCHITECTURE

2.1. Introduction

Zigbee is a low data-rate, low-power, and low-cost wireless networking protocol based on the IEEE 802.15.4 standard for wireless personal area networks (WPANs). The Zigbee protocol stack is built on top of IEEE 802.15.4, which defines the media access control (MAC) and physical (PHY) layers. It supports the frequency bands 868 MHz for European countries, 915 MHz for the United States, and 2.4 GHz for worldwide. A Zigbee end device can operate for months or even years without battery replacement. The maximum data rate is 250 kbps, and up to 65,000 nodes can be connected in a network. The transmission range is 10–100 m, based on the environment.

ZigBee supports different network configurations for master to master or master to slave communications. And also, it can be operated in different modes as a result the battery power is conserved. ZigBee networks are extendable with the use of routers and allow many nodes to interconnect with each other for building a wider area network.

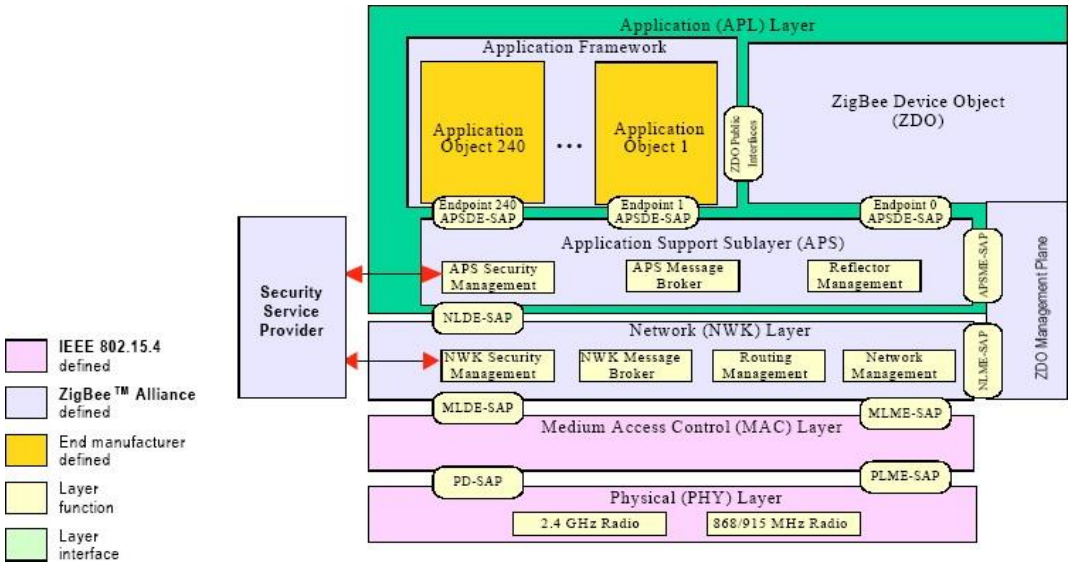


ZigBee system structure consists of three different types of devices such as ZigBee coordinator, Router and End device. Every ZigBee network must consist of at least one coordinator which acts as a root and bridge of the network. The coordinator is responsible for handling and storing the

information while performing receiving and transmitting data operations. ZigBee routers act as intermediary devices that permit data to pass to-and-fro through them to other devices. End devices have limited functionality to communicate with the parent nodes such that the battery power is saved as shown in the figure. The number of routers, coordinators and end devices depends on the type of network such as star, tree and mesh networks.

2.2. Zigbee Layers

Figure shows Zigbee wireless networking protocol layers. The protocol layers are based on the open system interconnect (OSI) basic reference model. These layers allow a layer affected by change to be replaced or modified rather than change the entire protocol [5]. Figure 1 shows that the MAC and PHY layers are defined by IEEE 802.15.4 standard [6]. Meanwhile, the networking, application, and the security layers of the protocol are defined by Zigbee standard. The Zigbee wireless networking protocol combines Zigbee and IEEE 802.15.4 standards. Therefore, any Zigbee-compliant device conforms to the IEEE 802.15.4 as well.



ZigBee protocol architecture consists of a stack of various layers where IEEE 802.15.4 is defined by physical and MAC layers while this protocol is completed by accumulating ZigBee's own network and application layers.

Physical Layer: This layer does modulation and demodulation operations up on transmitting and receiving signals respectively. This layer's frequency, date rate and number of channels are given below.

MAC Layer: This layer is responsible for reliable transmission of data by accessing different networks with the carrier sense multiple access collision avoidance (CSMA). This also transmits the beacon frames for synchronizing communication.

Network Layer: This layer takes care of all networks related operations such as network setup, end device connection and disconnection to network, routing, device configurations, etc.

Application Support Sub-Layer: This layer enables the services necessary for ZigBee device object and application objects to interface with the network layers for data managing services. This layer is responsible for matching two devices according to their services and needs.

- **Application object (endpoint):** An application object defines input and output to the APS. For example, a switch that controls a light is the input from the application object, and the output is the light bulb condition. Each node can have 240 separate application objects. An application object may also be referred to as an endpoint (EP).
- **ZigBee device object (ZDO):** A ZigBee device object performs control and management of application objects. The ZDO performs the overall device management tasks:

  Determines the type of device in a network (for example, end device, router, or

  coordinator) Initializes the APS, network layer, and security service provider

  Performs device and service discovery

  Initializes coordinator for establishing a

  network Security management

  Network management

  Binding management

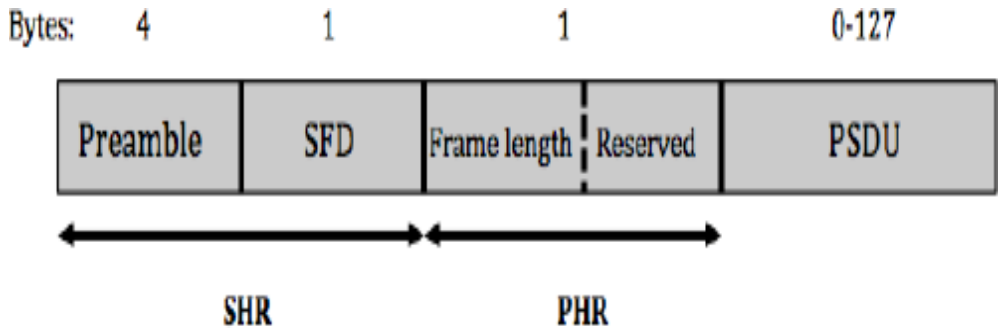
- **End node:** Each end node or end device can have multiple EPs. Each EP contains an application profile, such as home automation, and can be used to control multiple devices or a single device. More to the point, each EP defines the communication functions within a device. As shown in Figure 2.7, the bedroom switch controls the bedroom light, and the remote control is used to control three lights: bedroom, hallway1, and hallway2.
- **ZigBee addressing mode:** ZigBee uses direct, group, and broadcast addressing for transmission of information. In direct addressing, two devices communicate directly with each other. This requires that the source device has both the address and endpoint of the destination device. Group addressing requires that the application assign a group membership to one or more devices. A packet is then transmitted to the group address in which the destination device lies. The broadcast address is used to send a packet to all devices in the network.

Application Framework: It provides two types of data services as key value pair and generic message services. Generic message is a developer defined structure, whereas the key value pair is used for getting attributes within the application objects. ZDO provides an interface between application objects and APS layer in ZigBee devices. It is responsible for detecting, initiating, and binding other devices to the network.

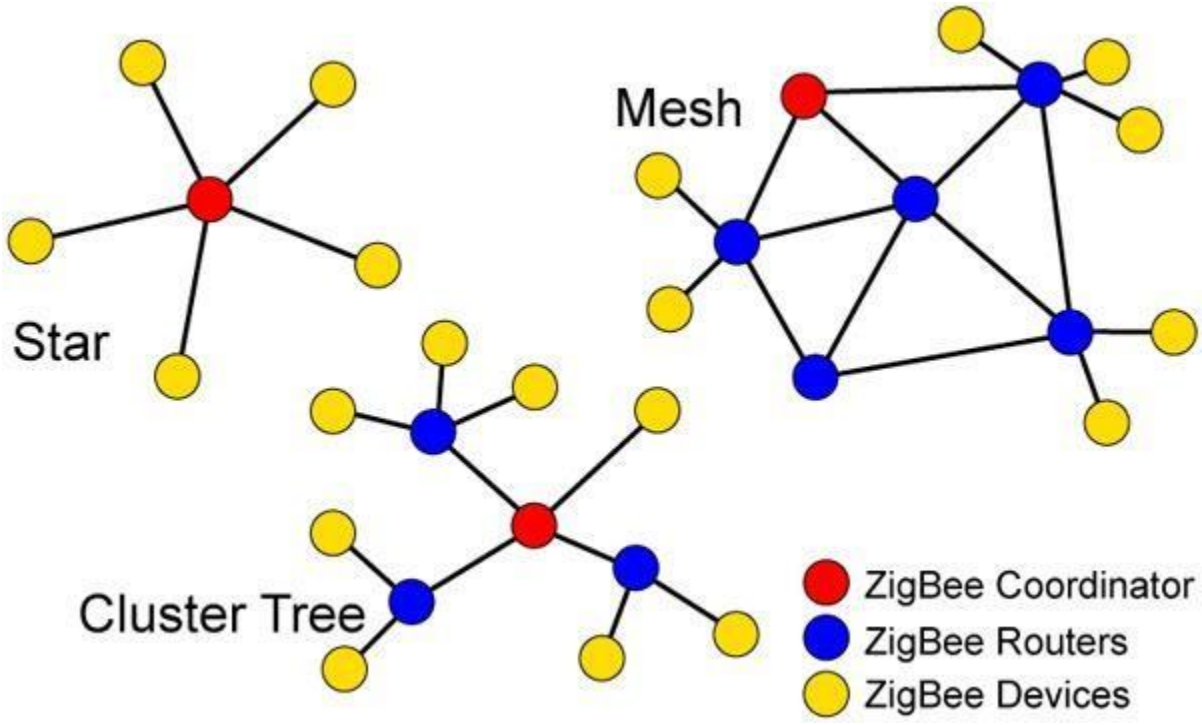
Devices in Zigbee wireless network perform three roles: (1) coordinator – principal controller of the personal area network (PAN), (2) router – relayer of messages, and (3) end device – does not act as a coordinator. Zigbee has the least memory size, cheapest product, and least processing capabilities and features.
Zigbee also possesses three network topologies: star, mesh, and tree topologies. In the star topology, every device in the network can communicate only with the coordinator. In the mesh topology, any device is allowed to communicate with another device directly or by taking advantage of the routing-capable device.
Therefore, the reliability of wireless connections could be increased because the mesh network can create and modify routes dynamically. In the tree topology, a Zigbee coordinator acts as the root of the tree, where a coordinator or router can act as a parent device and accept association from other devices in the network. An end device can act as a child only because it is not capable of routing.

The IEEE 802.15.4 developed the MAC and PHY layer frame formats, as shown in Fig. 2. The preamble field is used by the transceiver to obtain chip and
symbol synchronization with an incoming message [6]. The length of the preamble is 4 bytes (32 bits). The start of the frame delimiter (SFD) field indicates the end of the synchronization header (SHR) and the start of the PHY header (PHR).

The length of SFD is 1 byte (8 bits). The frame length field is 7 bits in length and specifies the total number of octets contained in the PHY service data unit (PSDU). The PSDU field carries the data of the PHY packet. The maximum size of this field is 127 bytes (1,016 bits). Together, the SHR, PHR, and PSDU form the PHY protocol data unit (PPDU). The IEEE 802.15.4 standard defines four frame structures, including beacon, data, acknowledgment, and MAC command frames. A coordinator uses the beacon frame to transmit beacons. The data frame transfers data, and the acknowledgment frame confirms successful frame reception. Finally, the MAC command frame handles all MAC peer entity control transfers.



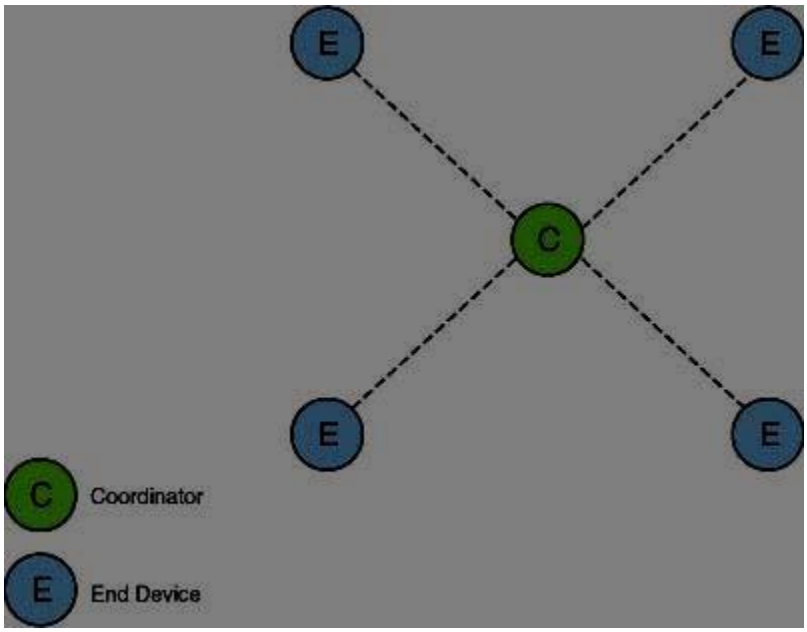
2.3. ZigBee Topologies



ZigBee supports several network topologies; however, the most commonly used configurations are star, mesh and cluster tree topologies. Any topology consists of one or more coordinator. In a star topology, the network consists of one coordinator which is responsible for initiating and managing the devices over the network. All other devices are called end devices that directly communicate with coordinator. This is used in industries where all the end point devices are needed to communicate with the central controller, and this topology is simple and easy to deploy.

It uses an association hierarchy; a device joining the network can either be a router or an end device, and routers can accept more devices.

- **Star topology:** The star topology consists of a coordinator and several end devices (nodes), as shown in Figure 2.2. In this topology, the end device communicates only with the coordinator. Any packet exchange between end devices must go through the coordinator. The disadvantage of this topology is the operation of the network depends on the coordinator of the network, and because all packets between devices must go through coordinator, the coordinator may become bottlenecked. Also, there is no alternative path from the source to the destination. The advantage of star topology is that it is simple, and packets go through at most two hops to reach their destination.



- **Tree topology:** In this topology, the network consists of a central node (root tree), which is a coordinator, several routers, and end devices, as shown in Figure 2.3. The function of the router is to extend the network coverage. The end nodes that are connected to the coordinator or the routers are called children. Only routers and the coordinator can have children. Each end device is only able to communicate with its parent (router or coordinator). The coordinator and routers can have children and, therefore, are the only devices that can be parents. An end device cannot have children and, therefore, may not be a parent. A special case of tree topology is called a cluster tree topology.

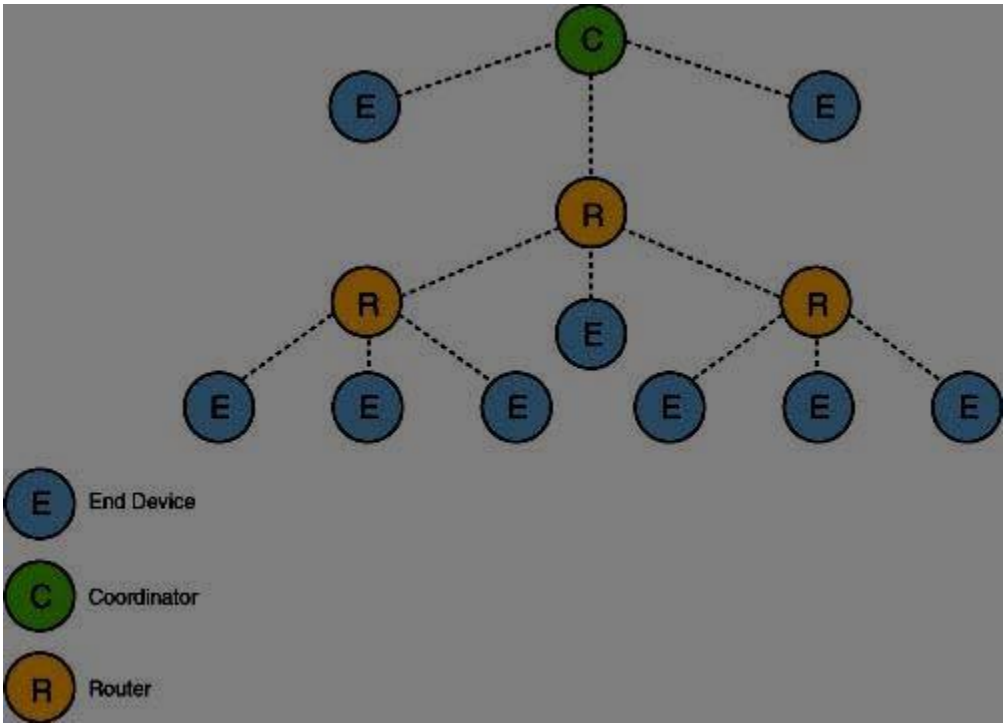


Figure 2.3 Tree topology

The disadvantages of tree topology are

a. If one of the parents becomes disabled, the children of the disable parent cannot communicate with other devices in the network.
b. Even if two nodes are geographically close to each other, they cannot communicate directly.

- **Cluster tree topology:** A cluster tree topology is a special case of tree topology in which a parent with its children is called a cluster, as shown in Figure 2.4. Each cluster is identified by a cluster ID. ZigBee does not support cluster tree topology, but IEEE 802.15.4 does support it.

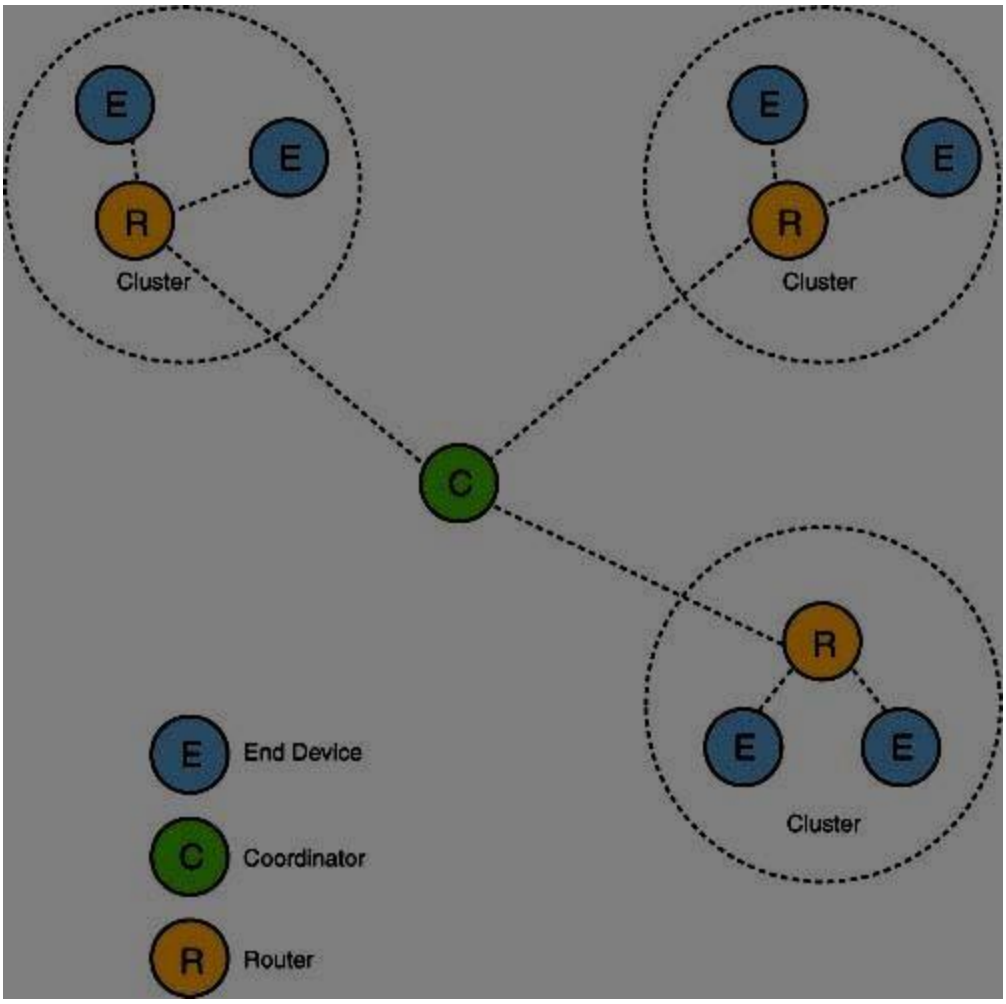


Figure Cluster tree topology

- **Mesh topology:** Mesh topology, also referred to as a peer-to-peer network, consists of one coordinator, several routers, and end devices, as shown in Figure 2.5. The following are the characteristics of a mesh topology:

A mesh topology is a multihop network; packets pass through multiple hops to reach their destination.

The range of a network can be increased by adding more devices to the network.

It can eliminate dead zones.

A mesh topology is self-healing, meaning during transmission, if a path fails, the node will find an alternate path to the destination.

Devices can be close to each other so that they use less power.

Adding or removing a device is easy.

Any source device can communicate with any destination device in the network.

Compared with star topology, mesh topology requires greater overhead.

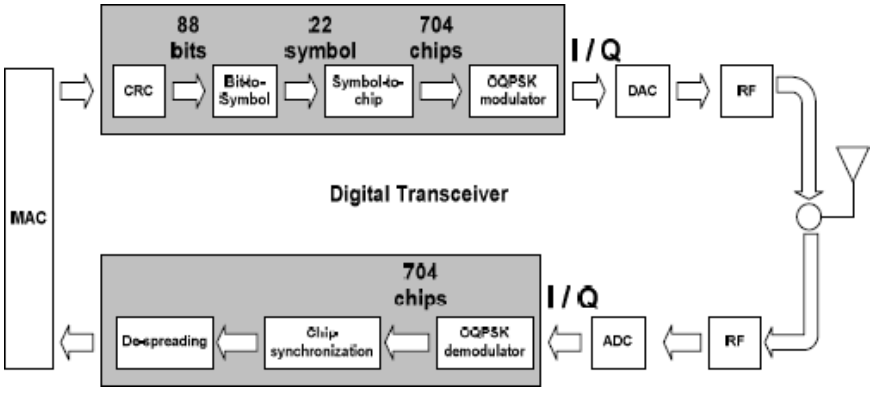
Mesh routing uses a more complex routing protocol than a star topology.

2.4. ZigBee Architecture Overview

There are mainly three types of radio transceivers. These are Direct Conversion or zero IF receiver, heterodyne receiver, and Low intermediate frequency receiver.

We choose direct conversion scheme because of low power consumption, low cost and high integrate able chip.

The overall network architecture hardware includes basically a transmitter that contains sub modules like CRC, bit-to-symbol, symbol-to-chip and OQPSK modulator; and a receiver that has sub modules like OQPSK demodulator, chip synchronization block and despreading block. The block diagram for the digital transceiver has been shown below in Figure.



A detailed study of all the blocks and sub blocks are provided in chapters to follow.

3. TRANSMITTER

3.1 Introduction

ZigBee Transmitter can be designed with analog components. Designing an analog transmitter is easier than digital. But in analog design, data transmission will be poor and the components also bigger and more. This will not allow accurate data transmission. In designing with digital, accurate data transmission will be obtained and power supply voltage range will be smaller.

One way of designing digital ZigBee transmitter is with the help of Verilog HDL through Xilinx ISE. The objective is to design the ZigBee transmitter using Verilog which will result in lesser numbers of slices and Look-up-Tables (LUTs) utilized and lossless data transmission. With lesser number of components, the power utilized shall be reduced.

ZigBee digital transmitter in 2.4GHz band is designed using Verilog for acknowledgement frame. The PHY layer supports three frequency bands: a 2.45 GHz band with 16 channels, a 915 MHz band with 10 channels and an 868 MHz band with 1 channel. This paper focuses only on 2.45 GHz band which is used worldwide, with the data rate of 250 Kbps. The MAC layer defines two types of nodes: Reduced Function Devices (RFDs) and Full Function Devices (FFDs). RFDs can only act as end-devices and are equipped with sensors or actuators like transducers, light switches, and lamps. They may only interact with a single FFD. FFDs are equipped with a full set of MAC layer functions, which enables them to act as a network coordinator or a network end-device.

3.2 Cyclic Redundancy Check

Error detection is the process of monitoring data transmission and determining when errors have occurred. Error-detection techniques neither correct errors nor identify which bits are in error – they indicate only when an error has occurred. The purpose of error detection is not to prevent errors from occurring but to prevent undetected errors from occurring. The most common error-detection techniques are redundancy checking, which includes vertical redundancy checking, checksum, longitudinal redundancy checking, and cyclic redundancy checking.

The most reliable redundancy checking technique for error detection is a convolutional coding scheme called cyclic redundancy checking (CRC). With CRC, approximately 99.999% of all transmission errors are detected. In CRC-16, 16 bits are used for the block check sequence.
Here, the entire data stream is treated as a long continuous binary number. Because the Block Check Sequence (BCS) is separate from the message but transported within the same transmission, CRC is considered a systematic code. Cyclic block codes are often written as (n, k) cyclic codes where n = bit length of transmission and k = bit length of message. Therefore, the length of the Block Check Character (BCC) in bits is

$BCC = n - k \quad (1)$

A CRC-16 BCC is the remainder of a binary division process. A data message polynomial G(x) is divided by a unique generator polynomial function P(x), the quotient is discarded, and the remainder is truncated to 16 bits and appended to the message as a BCS. The generator polynomial must be a prime number. With CRC generation, the division is not accomplished with standard arithmetic division. Instead, modulo-2 division is used, where the remainder is derived from an exclusive OR (XOR) operation. In the receiver, the data stream, including the CRC code, is divided by the same generating function P(x). If no transmission errors have occurred, the remainder will be zero.

Mathematically, CRC can be expressed as

$G(x)/ P(x) = Q(x) + R(x) \quad (2)$

Where G(x) = message polynomial P(x) = generator polynomial Q(x) = quotient R(x) = remainder

The generator polynomial for CRC-16 is

$P(x) = x16 + x15 + x2 + x0 \quad (3)$

A CRC generating circuit requires one shift register for each bit in the BCC. A review of CRC creation process is as follows:

- Get the raw frame
- Left shift the raw frame by n bits and then divide it by P.
- The remainder of the last action is the FCS.
- Append the FCS to the raw frame.
- The result is the frame to transmit CRC-16 detects.
- Any single-bit errors.

- All double-bit errors.
- All odd number of bit errors.
- All error bursts of 16 bits or less.
- 99.9% of error bursts greater than 16 bits long.

3.3 Bit-To-Symbol

All the 88 bits from the CRC block is inserted into the bit- to-symbol block. This binary information is mapped into the data symbol. The 4 LSBs (b0, b1, b2, b3) of each octet is mapped into one data symbol and the 4 MSBs (b4, b5, b6, b7) of each octet is mapped into the next data symbol. Each octet of PPDU is processed through the bit-to-symbol block sequentially, beginning with the Preamble field and ending with the last octet of the PSDU. For the result, 22 symbols will be the output of the bit-to-symbol block.

3.4 Symbol-To-Chip

Symbol-to-chip block uses DSSS (Direct Sequence Spread Spectrum) technique and maps each symbol from the bit-to- symbol block to a unique PN sequence of 32-bits length. The IEEE 802.15.4 uses this method to improve the receiver sensitivity level and increase the jamming resistance. The DSSS method is also necessary in improving receiver performance in a multipath environment because in most practical scenarios, the transmitted signal may find several different paths to the receiver due to reflections, diffractions, and scatterings. These signals have different delays and phase shifts; therefore, the summation will be a distorted signal.

Table shows the symbol-to-chip mapping using DSSS method.

Data symbol (decimal)	Data symbol (binary) ($b_0\ b_1\ b_2\ b_3$)	Chip values ($c_0\ c_1$ ..... $c_{30}\ c_{31}$)
0	0000	11011001110000110101001000101110
1	1000	11101101100111000011010100100010
2	0100	00101110110110011100001101010010
3	1100	00100010111011011001110000110101
4	0010	01010010001011101101100111000011
5	1010	00110101001000101110110110011100
6	0110	11000011010100100010111011011001
7	1110	10011100001101010010001011101101
8	0001	10001100100101100000011101111011
9	1001	10111000110010010110000001110111
10	0101	01111011100011001001011000000111
11	1101	01110111101110001100100101100000
12	0011	00000111011110111000110010010110
13	1011	01100000011101111011100011001001
14	0111	10010110000001110111101110001100
15	1111	11001001011000000111011110111000

Symbol-to-chip block in the transmitter section uses the mappings in Table 1 to generate output chips. For each data symbol, there is a corresponding 32 bits chip. Each chip is unique. Implemented this table for obtain the functionality of symbol-to-chip block.

3.5 Offset Quadrature Phase Shift Key Modulation

This is a variant of Quadrature Phase Shift keying method and can be implemented by shifting the Quadrature bit stream by a half bit period. The following constellation plot describes the need for doing so.

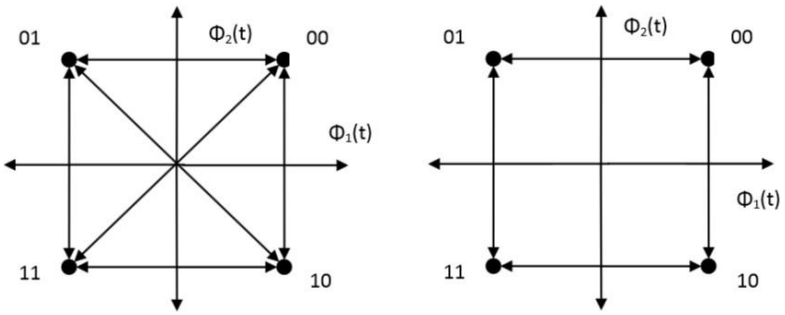


Fig. Phase transition between QPSK and OQPSK

The constellation plot shown in Figure 3.11 above includes all possible phase transitions that can arise in the generation of a QPSK signal. From the QPSK waveform, we observe the following.

- The carrier phase changes by ± 180 degrees whenever both the inphase and Quadrature components of QPSK signal changes the sign. This situation occured when the input binary sequence switches from dibit 01 to dibit 10.

- The carrier phase changes by ± 900 whenever the inphase or Quadrature components changes sign. This situation occurs when the input bit sequence switches from di-bit 10 to di-bit 00, during which the inphase component changes sign, whereas the Quadrature component is unchanged.
- The carrier phase is unchanged when neither the inphase component nor the Quadrature component changes sign. This situation occurs when di-bit 10 is transmitted in two successive symbol intervals.

Situation 1 and, to a much lesser extent, situation 2 can be of a particular concern when the QPSK signal is filtered during transmission, prior to detection. Specifically, the 1800 and 900 phase shifts in the carrier phase can result in changes in the carrier amplitude (i.e., envelope of the QPSK signal), thereby causing additional symbol errors on detection.

The extent of amplitude fluctuations exhibited by QPSK signals may be reduced by using offset QPSK. In this variant of QPSK, the bit stream responsible for generating the Quadrature component is delayed (i.e., offset) by half a symbol interval with respect to the bit stream responsible for generating inphase component as shown in Figure 3.12. Specifically, the two-basis function of offset QPSK are defined by-

$$\phi_1(t) = \sqrt{\frac{2}{T}}\cos 2\pi f_c t \quad 0 \leq t \geq T$$

$$\phi_2(t) = \sqrt{\frac{2}{T}}\sin 2\pi f_c t \quad \frac{T}{2} \leq t \leq \frac{3T}{2}$$

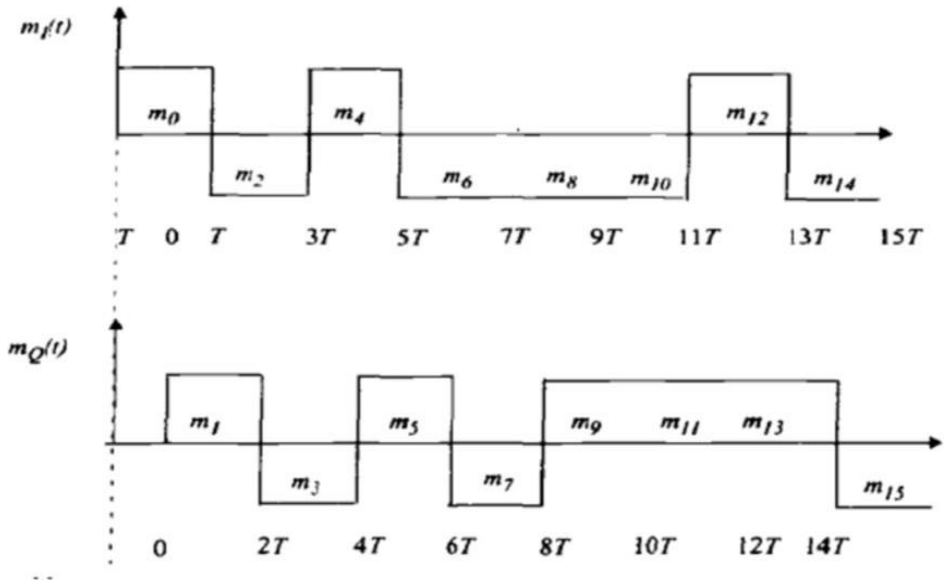


Fig. Output after adding delay in the quadrature arm of OQPSK modulator.

Unlike QPSK, the phase transitions likely to occur in offset QPSK are confined to ±900, as indicated in the signal space diagram. However, ±900 phase transitions in offset QPSK occur twice as frequently but with the half intensity encountered in QPSK. Since, in addition to ±900 phase transitions, ±1800 phase transitions also occur in QPSK, we find that amplitude fluctuations in offset QPSK due to filtering have a smaller amplitude than in the case of QPSK. The equation for OQPSK modulated signal is given by

$$V_{OQPSK}(t) = \sqrt{P_s}\, b_e(t) \cos \omega_0 t + \sqrt{P_s} b_0(t) \sin \omega_0 t$$

Despite the delay T/2 applied to the basis function $\phi 2(t)$ in equation 3.18, compared to the equation in QPSK, the offset QPSK has exactly same probability of symbol error in an AWGN channel as QPSK. The equivalence in noise performance between these phase shift keying schemes assumes the use of coherent detection. The reason for the equivalence is that statistical independence of the inphase and Quadrature components applies to both QPSK and OQPSK. We may therefore say that error probability in the inphase and Quadrature components applies to both QPSK and offset QPSK. We may therefore say that the error probability in the inphase or Quadrature channel of a coherent offset QPSK receiver is still equal to $erfc/2\sqrt{\frac{E}{N_0}}$. Hence this formula applies equally well to the offset QPSK.

3.5.1 PSD of OQPSK signal

The spectrum of an OQPSK signal is identical to that of a QPSK signal, hence both signals occupy the same bandwidth. The total power spectral density is twice the density generated by either of the Quadrature carriers and is given by

$$G_{OQPSK}(f) = E_b \left\{ \left[\frac{\sin \frac{2\pi(f - f_o)}{f_b}}{\frac{2\pi(f - f_o)}{f_b}} \right]^2 + \left[\frac{\sin \frac{2\pi(f + f_o)}{f_b}}{\frac{2\pi(f + f_o)}{f_b}} \right]^2 \right\}$$

The main lobe contains 90 percent of signal energy. Still, the not inconsiderable power outside the mainlobe is a source of trouble QPSK is to be used for multichannel communication on adjacent carriers. If we say, we establish additional channels at carrier frequencies f0' = f0 + fb then the sidelobe associated with first channel, having a peak value at frequency f0 + 3fb/4, will be a source of serious interchannel interference. These sidebands are smaller than the main lobe by 14dB.

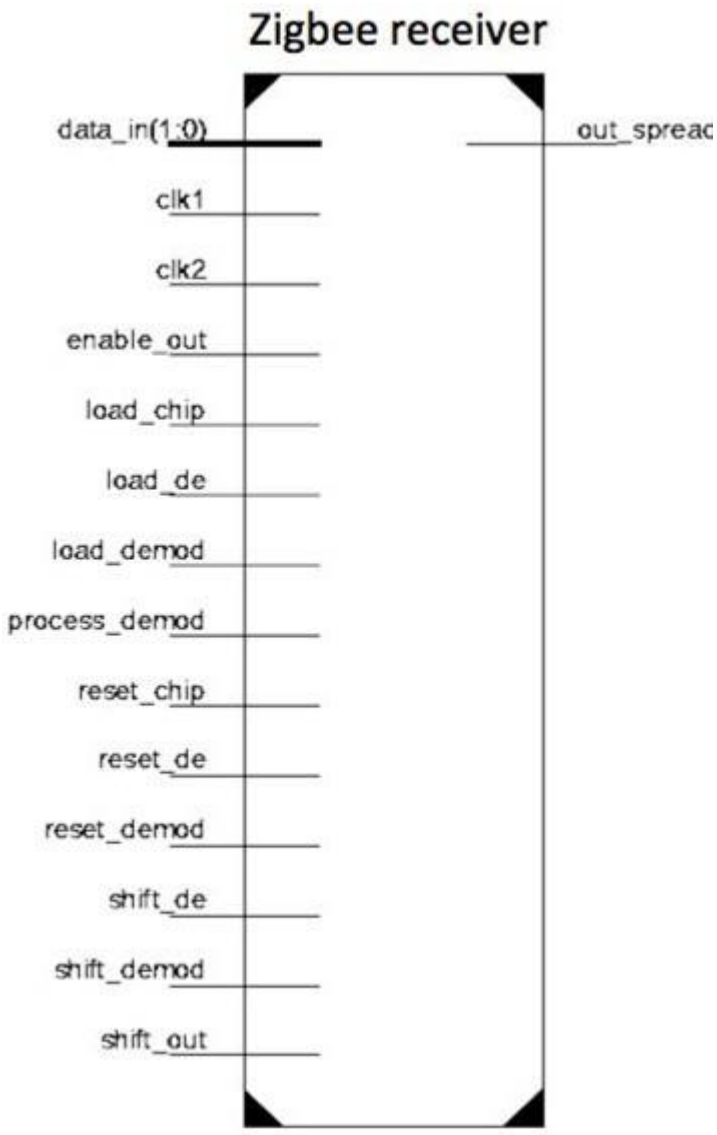
The staggered alignment of the even and odd bit streams does not change the nature of the spectrum. OQPSK retains its handlimited nature even after nonlinear amplification, and therefore it is very attractive for mobile communication systems where bandwidth efficiency and efficient nonlinear amplifiers are critical for 1ow power drain.

CHAPTER-4

RECEIVER

4.1. Introduction

The functions to be implementing in receiver are RF to base band conversion, sampling and thresholding, parallel to serial conversion and despreading. The received signal from the channel is coherently correlated in one arm of the receiver with the result of the multiplication between the in-phase carrier and the shaping function $cos\left(\frac{\pi t}{2T_b}\right)$. In the other arm, the received signal is correlated with the result of the multiplication between the Quadrature carrier and the shaping function $\sin\left(\frac{\pi t}{2T_b}\right)$. These correlations are made in a 2Tb interval, reflecting the duration of the half-cycle cosine and sine shaping pulses and are time-aligned with these pulses. The estimated sequences at both inphase and Quadrature arms are parallel to serial converted to form serial data of the transmitted sequence. After that signal is despreaded. This signal must be same as the signal that we have sent at the transmitter side.



Sixteen channels based on IEEE 802.15.4 standard are available with an ample channel spacing of 5 MHz for 2.4 GHz-band applications. A direct sequence spread spectrum (DSSS) with a digital spreading function representing pseudorandom noise (PN) chip sequences is employed. The

DSSS is used to improve the performance of the receivers in a multipath environment. The transmitted signal in most practical scenarios may find several different paths to the receiver because of reflections, diffractions, and scatterings. In DSSS, every 4 bits of octet of a PPDU are grouped together to form a symbol. This symbol is mapped to a 32-bit chip represented by *c0c1c2c3…c31*, which is also known as the PN sequence. A total of 16 different symbols and 32-bit chips are found.

4.2. Literature Review

Various studies design digital receivers using different methodologies, such as MATLAB, VHDL, and schematic. However, MATLAB can only be used for modeling and simulation. Schematic is not practical when the circuit is complex because the method needs a long design timeframe. Behavioral modeling of digital design goes through HDL, which is more time-efficient than other methods. Most important the HDL code can be simulated and implemented directly on FPGA as a prototyping device, or on an ASIC.

Di Stefano et al. designed a simple receiver architecture. The architecture involves only four blocks, and the design was implemented on Spartan3-200 FPGA. A 1 MHz low-pass filter reduces signal noise and co-channel interferences. The noncoherent OQPSK demodulator functions as a phase detector. The correlator and bit-timing block retains the original code, and it acquires timing and phase reference during the reception of each frame preamble. The frame-processing block then decodes the data field before sending it to the MAC or the host. Zigbee configuration requires less than 200 slices at 22 MHz sampling frequency.

Meng et al. proposed a digital receiver architecture for Zigbee applications. The architecture comprises six blocks: carrier synchronizer, IF downconverter, filter, quadrature demodulator, chip synchronizer, and despreading. The IF downconverter changes IF signals from the ADC to the Iphase, earlier I-phase, later I-phase, and Q-phase signals. The filter blocks determine the phase offset between the carrier and the local oscillator. The quadrature demodulator then removes the phase offset. The chip synchronizer synchronizes the I-Q signals. The despreading block recovers the bits after the correct chip synchronization is obtained. This receiver was designed with VHDL and implemented on Xilinx Virtex-4 LX60 FPGA. The configuration obtained 3,047 slices out of 26,624; 3,659 FFs out of 53,248; 4,125 four-input LUTs out of 53,248; and 24 multipliers out of 64.

Kim et al. successfully designed and fabricated a low-complexity demodulation scheme for a Zigbee receiver with 0.18 μm CMOS standard cell library. Multiple active correlators for demodulation are replaced with a matched filter-based cross-correlator. The demodulator shares correlators with a synchronization unit, which requires only a few additional control units. This correlator sharing reduces the total complexity. The proposed receiver reduced 36 nontrivial multipliers to 6; 338 adders to 259; and 59 k to 27 k logic gates over the existing hardware architecture from IEEE Std.802.15.4.

Chen and Ma designed and fabricated a different architecture of Zigbee receivers using TSMC 0.18 μm technology. The receiver works in three steps: packet detection, synchronization, and data recovery. At the packet-detection stage, other blocks are turned off until the packet is detected. At synchronization, the carrier frequency synchronization block is turned on to estimate the frequency error by preamble, and the phase compensation block works for phase rotation.

The despreading block collects the packet information. Finally, at the data recovery stage, the symbol-to-bit block recovers the data bit stream for media access control (MAC). The phase-tracking block begins to track the phase error. In the present paper, the packet error rate (PER) can achieve 0.01 at an SNR lower than 5 dB. This design has a chip area of 1.63

mm2 x 1.63 mm2 (including the transmitter and the receiver) with a gate count of 78 k.

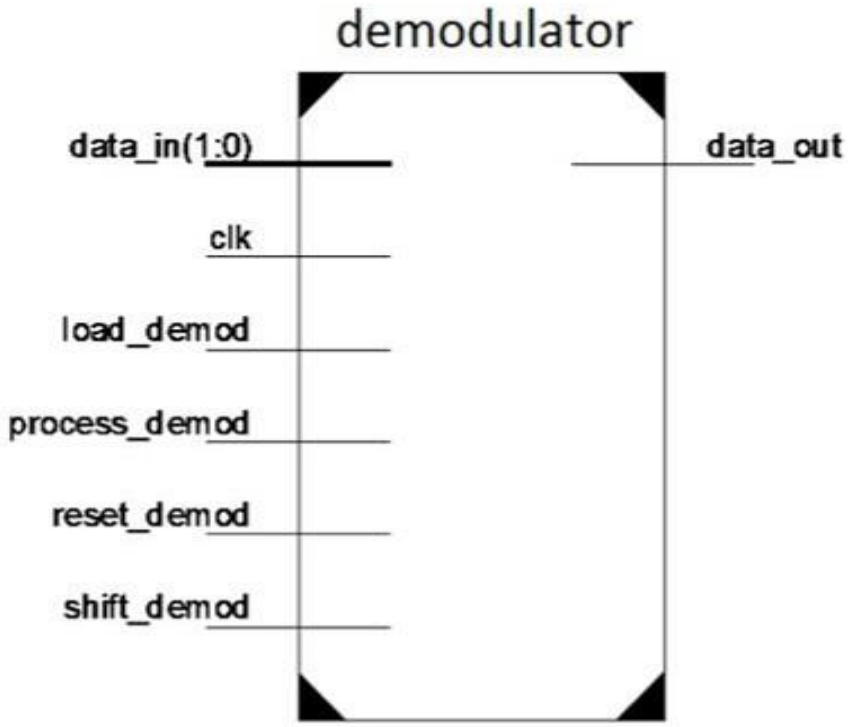
Bernier et al. designed an ultra-low-power Zigbee digital receiver using 130 nm CMOS technology. The 4 MSps 3-bit I/Q streams are half-sine-filtered before they are fed to the synchronization block and the decoding module. The synchronization block recovers the symbol clock using a code-matched filter and a recursive channel filter. The code-matched filter is implemented by eight partial correlation banks. The recursive channel filter increases the SNR by averaging the samples over symbol periods. The SFD then locks the symbol clock, and the required symbol correlations are performed for each symbol period. The sample stream is decimated by a factor of 2, which means that a single complex sample per chip is retained. At 1.2 V, the design drains 5.4 mW in receiver active modes and achieves 1% PER for a -81 dBm input power.

Using six blocks with Matlab and CoWare's signal processing designer, Zhang et al. designed a digital receiver. The chip recoverer in the proposed architecture regains the two chip streams from the I-Q input signals. The chip recoverer is controlled by a chip synchronizer to align the chips. A received signal strength indicator (RSSI) detects the presence of a valid input signal. The IQ channel detector identifies the Q-channel chip stream between the two chip streams and locates the bit stream head. I-channel chip data are ignored to simplify the receiver implementation. Only Q-channel chip data are used to extract the bit data with a bit-synchronizer module. Finally, the bit data are processed into symbol data by a symbol recoverer. The receiver was implemented on an element computing array (CXI ECA-64) platform, which delivers faster reconfiguration time and higher-computational-density FPGAs with similar computational power. The results show that 84% logical operations used, with 18% of the memory units implementing delay functions and shift registers. Wang et al. designed another Zigbee digital receiver for 2.4 GHz band.

The authors implemented the receiver on FPGA and fabricated it using 0.18 μm CMOS technology. The architecture, which involves eight blocks, is quite complicated. The packet detector discriminates whether the incoming signal is data or noise. The phase difference detector determines the phase difference of each sample data. The downsampling block finds the maximum phase difference and performs the downsampling. Meanwhile, the frequency-offset compensation computes and compensates the frequency offset. The noncoherent demodulator uses minimum shiftkeying (MSK) scheme to perform demodulation. MSK is assumed to be like OQPSK. The preamble removal block acquires and removes the preamble from the PPDU packet. The despreading block despreads each chip PN sequence to the symbol data. The confirmed SFD block acquires the PSDU length and notifies the MAC layer of the PSDU obtained from the receiver. All process corners (0 0C, +100 0C) and (SS, TT, FF) models were simulated to verify the design. The fabrication results shows that the PER is less than 1% at 8 MHz system clock.

4.3. OQPSK Demodulation

There are two type detection schemes available for the detection of original baseband data. They are coherent detection and non-coherent detection. In coherent detection, the phase of carrier that we used in the transmitter and phase of recovered carrier must be same. So proper carrier synchronization is necessary in the coherent demodulation. In case of non-coherent demodulation, there is no need of carrier synchronization. Coherent detection is costlier to implement, that is, the receiver must be equipped with a carrier recovery circuitry, which inturn increases system complexity, and can increase size and power consumption. Additionally, there is no ideal carrier recovery circuit. So, no practical digital communication system works under perfect phase coherence. While non coherent detection uses previous bit information for extracting the original data and there is no need of using the carrier recovery circuit. Non-coherent detection is simpler, but it suffers from performance degradation as compared to coherent detection, but this difference can be small in practice modulation schemes due to the specifics of the modulation and also due to the penalty caused by imperfections in the carrier recovering process.



The proposed design methodology of the chip synchronization block is described as follows:

• The input data comprise 704 chips per acknowledgment frame, with 352 chips each for the I-phase (even chips) and the Q-phase (odd chips). The number of data chips is calculated based on (2) [17]. The input frequency is very low at 2 MHz.

[88 bits ÷ 4 symbols] × 32 chips = 704 chips (2)

• With the same frequency, each chip of input data is processed based on

output_data [2*k* - 1] = I_phase [2*k* - 2]

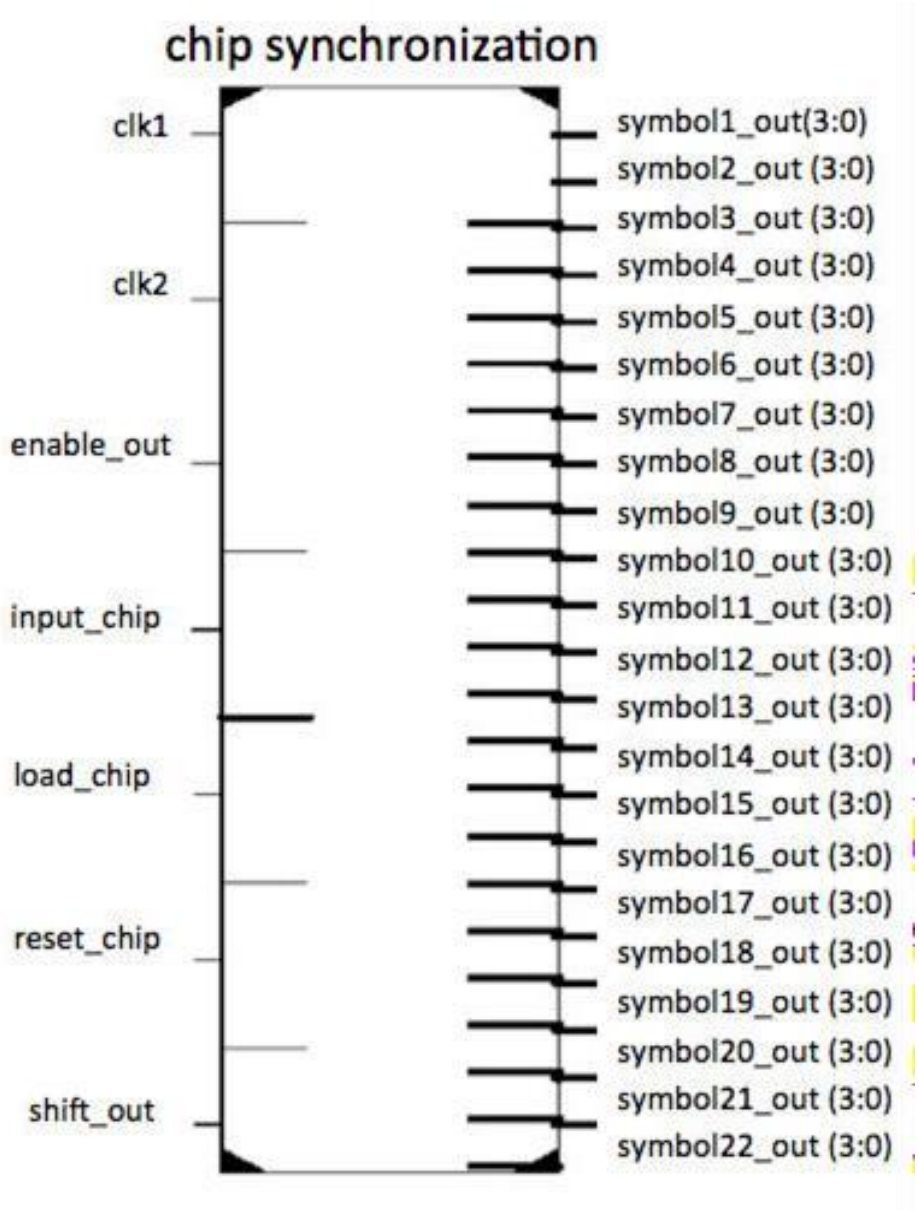
output_data [2*k*] = Q_phase [2*k* - 1] (3)

where $1 \leq k \leq 352$.

Based on this equation, each even chip of output data is registered as *C0*, *C2*, … *C704*, and each odd chip is registered as *C1, C3 …C703*, with a total 352 chips each for the I-phase and the Q-phase. These data chips will be the input for the next block in the Zigbee receiver.

Figure 6(a) shows the OQPSK demodulator structure. The *data_in[0]* and *data_in[1]* represent the even and odd input signals, respectively. The *load_demod*, *reset_demod*, *shift_demod*, and *process_demod* are the pins of the input signals. Meanwhile, *clk* is the clock frequency of 2 MHz. The *data_out* represents the output signal.

4.4. Chip Synchronization



The proposed design methodology of the chip synchronization block is described as follows:

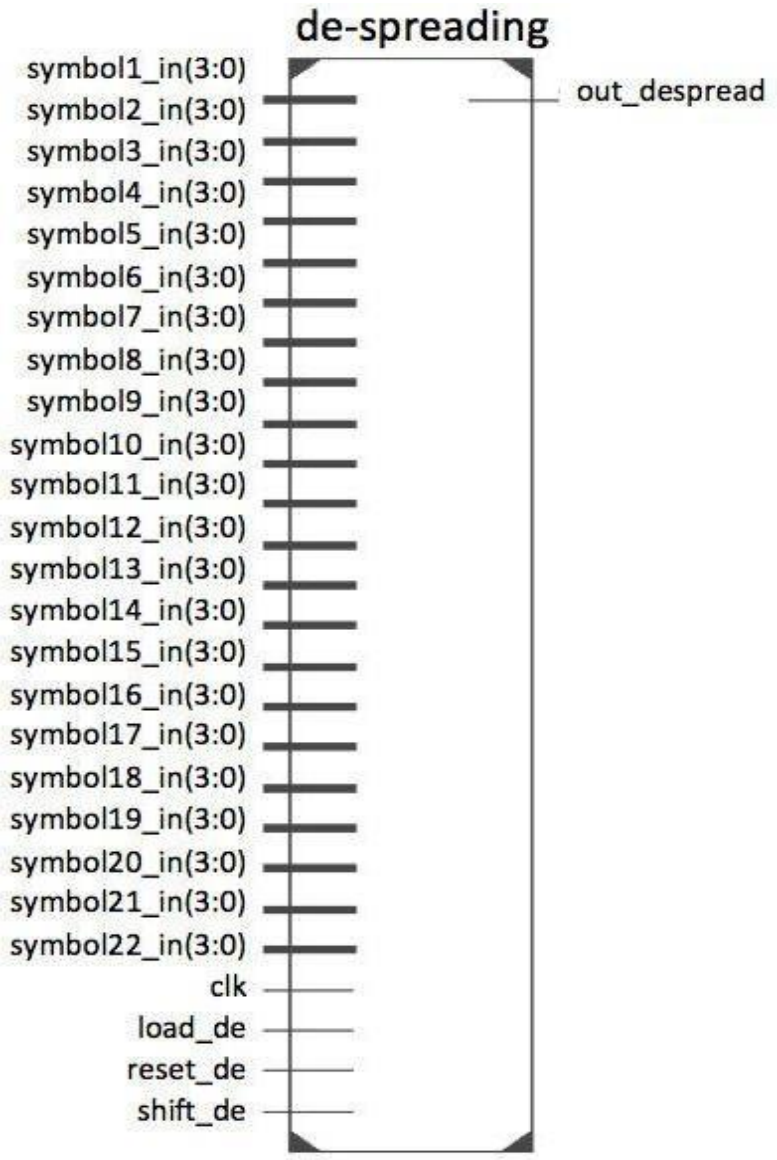
• The input data for this block comprise 704 chips. Every 32 chips of the input data are mapped into 1 symbol data with the DSSS, as shown in Table 1. At a frequency of 250 kHZ and 2 MHz, the numbers of the symbols produced as output data are calculated as follows:

704 chips / 32 = 22 symbols (4)

• The basic process of this block is described briefly in Eq. (5), where the last 32 input chips are the most significant bits (MSBs) of the output data as symbol 22th. These output symbol data will be the input data for the despreading block.

chip [{704 – 32m} : {673-32m}] => symbol [22-m] (5)
where $0 \leq m \leq 21$.
Figure 6(b) shows the schematic block of chip synchronization. *clk1* and *clk2* are the clock frequencies of 2 MHz and 250 kHz, respectively. The other input ports are *enable_out*, *input_chip*, *load_chip*, *reset_chip*, and *shift_out*. The *symbol1_out(3:0)* until *symbol22_out(3:0)* are the output ports for this block.

4.5. De-spreading



The proposed design mehodology for the de-spreading block is described as follows:

• The input data comprise 22 symbols. For each symbol, the input data are mapped into 4-bit data. The logic value of these bits is based on Table 1.

• With a frequency of 250 kHz, the total number of output bits produced is obtained from the following equation. These output data form the PPDU packet for the acknowledgment frame.

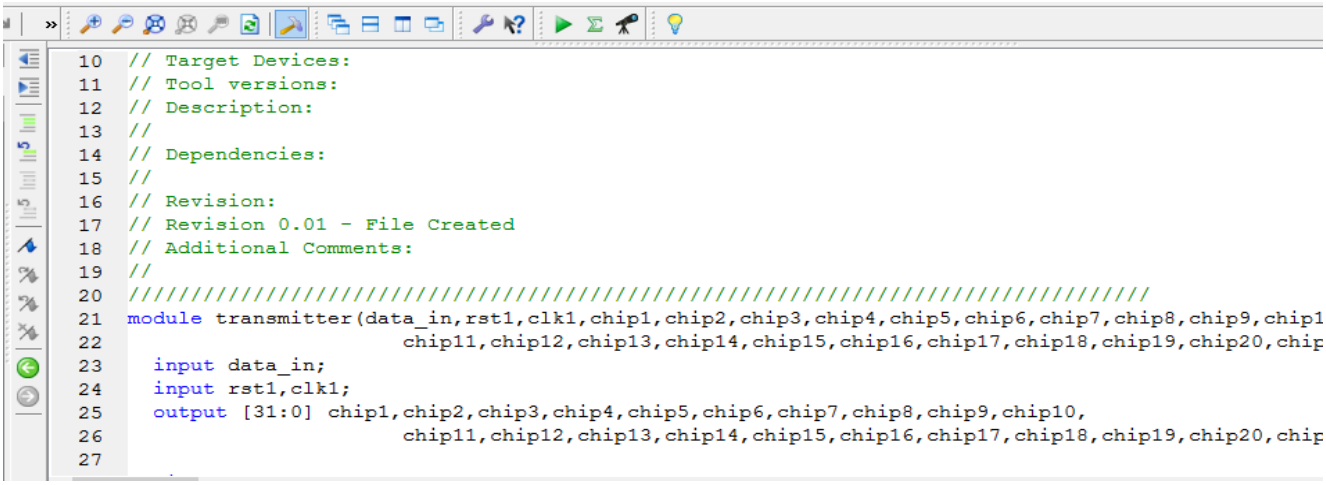
22 symbols x 4 = 88 bits (6)

Figure 6(c) shows the schematic of the de-spreading block. The frequency clock represented by *clk* is 250 kHz. The output data in bits are sent to *out_despread* port serially within 352,000 ns. The input ports comprise *clk*, *load_de*, *reset_de*, *shift_de*, and 22 ports of *symbol_in(3:0)*.

5. RESULT

5.1 Transmitter Module

The top-level module for the Transmitter is shown below:

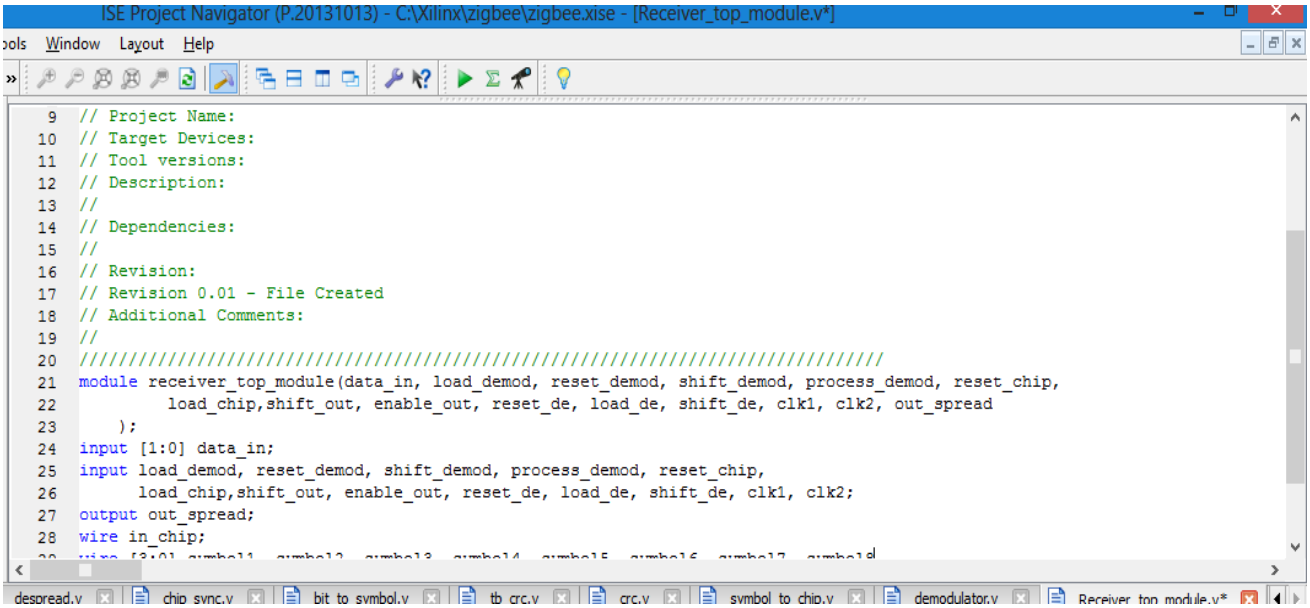


```
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module transmitter(data_in,rst1,clk1,chip1,chip2,chip3,chip4,chip5,chip6,chip7,chip8,chip9,chip1
                   chip11,chip12,chip13,chip14,chip15,chip16,chip17,chip18,chip19,chip20,chip
  input data_in;
  input rst1,clk1;
  output [31:0] chip1,chip2,chip3,chip4,chip5,chip6,chip7,chip8,chip9,chip10,
                chip11,chip12,chip13,chip14,chip15,chip16,chip17,chip18,chip19,chip20,chip

```

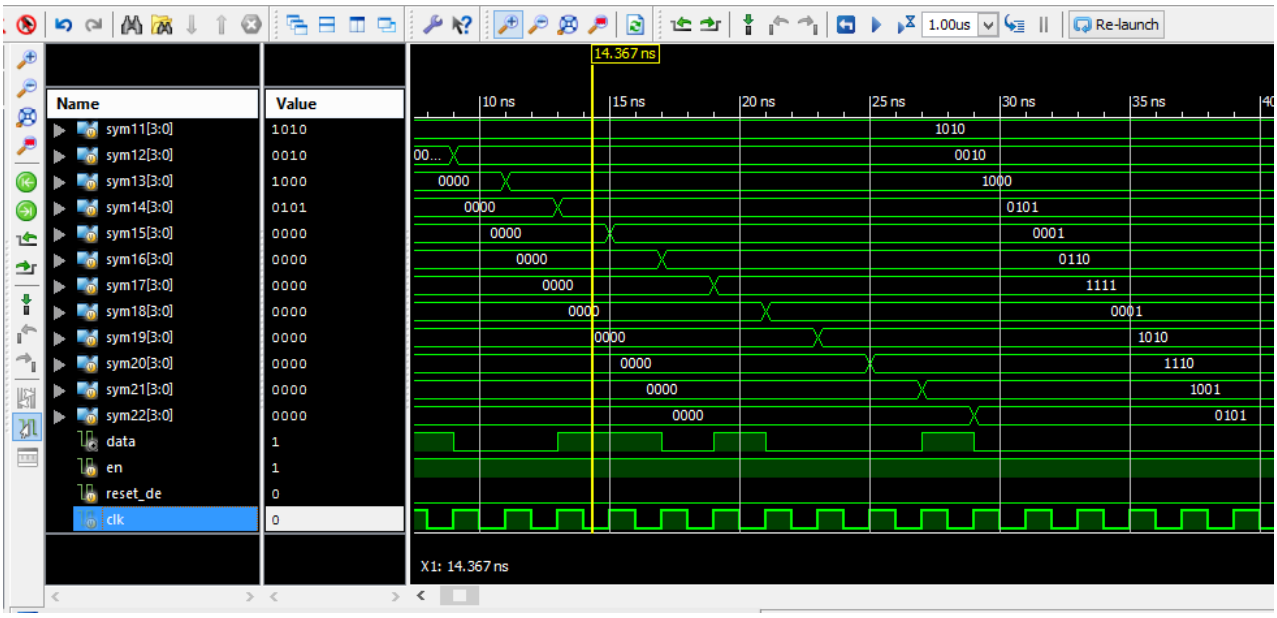
Fig. Top level Module for Transmitter

Top-level module for Receiver is shown below:



```
ISE Project Navigator (P.20131013) - C:\Xilinx\zigbee\zigbee.xise - [Receiver_top_module.v*]
ools Window Layout Help
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module receiver_top_module(data_in, load_demod, reset_demod, shift_demod, process_demod, reset_chip,
        load_chip,shift_out, enable_out, reset_de, load_de, shift_de, clk1, clk2, out_spread
    );
input [1:0] data_in;
input load_demod, reset_demod, shift_demod, process_demod, reset_chip,
     load_chip,shift_out, enable_out, reset_de, load_de, shift_de, clk1, clk2;
output out_spread;
wire in_chip;
despread.v | chip_sync.v | bit_to_symbol.v | tb_crc.v | crc.v | symbol_to_chip.v | demodulator.v | Receiver_top_module.v*
```

Fig. Top level Module for Receiver



The output waveforms for various blocks used in Receiver:

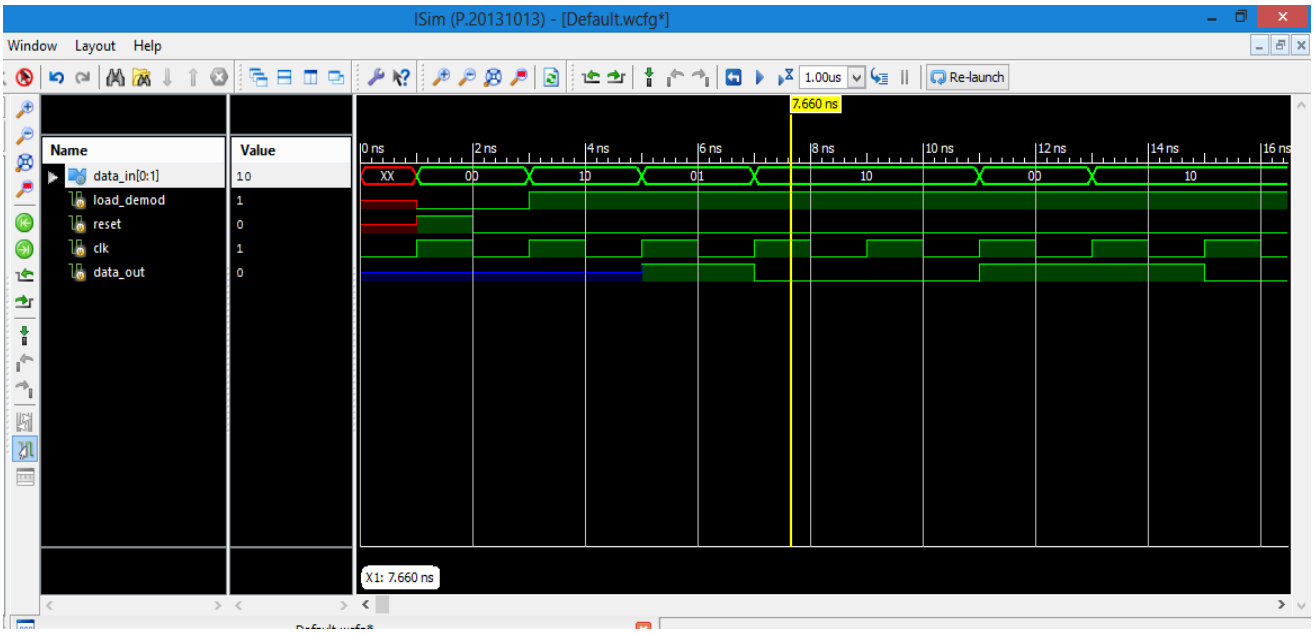


Fig. Output Waveform of Demodulator Block used in Receiver

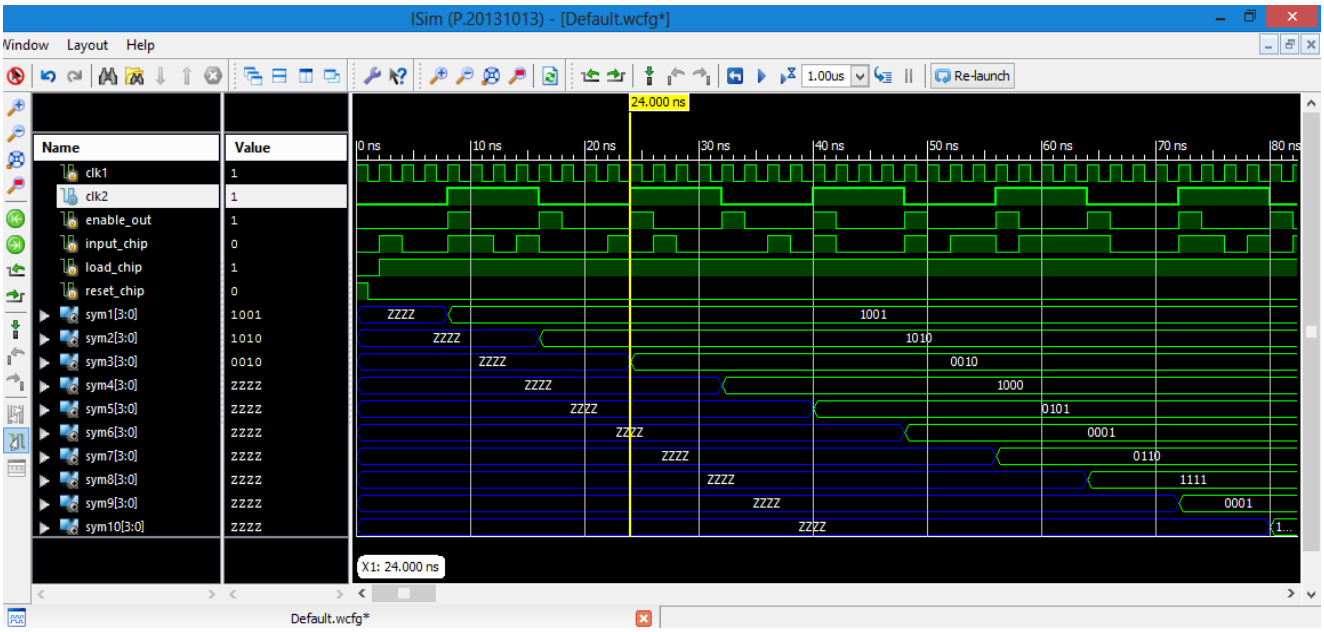


Fig. Output Waveform of Chip Synchronization Block used in Receiver

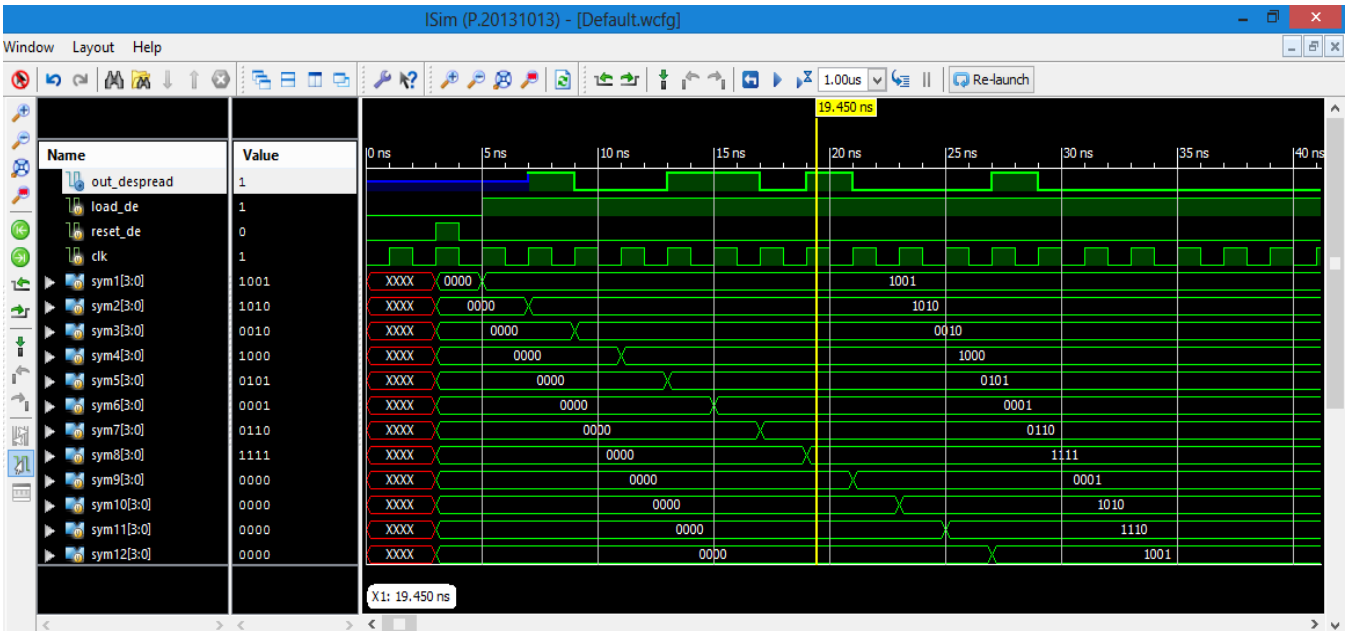


Fig. Output Waveform of Despreader Block used in Receiver (Final Output of Receiver)

CHAPTER 6

CONCLUSION

6.1. PROJECT CONCLUSION

Various digital receiver designs in the last six years were analyzed in terms of performance. The study concludes that the proposed Verilog-based design reduces the design area, shortens the simulation time, compared with VHDL-based designs. Verilog also speeds up the design process and produces output quickly.

Hence, we can say that ZigBee Transmitter and Receiver specifications were implemented in the project using Verilog HDL.

The work presented here helps to implement a transceiver for ZigBee wireless communication system using Verilog. Without using mathematically complex blocks, we designed and tested a ZigBee wireless transceiver in Verilog. In this thesis previous work of seminar and minor are used as reference to implement ZigBee transceiver.

A comparative model for MSK has been presented, the theoretical maximum bandwidth efficiency of MSK is 2 bits/s/Hz, the same as for QPSK and Offset QPSK. Here, we are indirectly implementing Minimum Shift Keying modulation and demodulation (OQPSK with half sine pulse shaping). Half sine pulse shaping avoids the abrupt phase shifts in the transmitted signal so that it reduced lot of burden and the modulated signal is amplifier friendly in real time scenario. Use of direct spread spectrum technique, reduces the interference effects. Out of the three commonly used radio transceivers (super heterodyne, Low IF and direct conversion transceiver), the use of direct conversion receiver fulfils the requirement of ZigBee i.e., low cost and low power consumption.

6.2. COMPARISON OF ZIGBEE WITH OTHER

A comparison of the ZigBee with other wireless networks has been provided based on features like modulation scheme, frequency ranges supported, as given below:

	Bluetooth	UWB	ZigBee	802.11a/b/g	802.11n	Proprietary	802.16a	2G/2.5G/3G
Typical Range	< 10m	10-30m	70-300m	100m	100m	10km	50km	Cellular Network
Modulation	Adaptive FHSS	OFDM or DS-UWB	DSSS	DSSS	DSSS	FHSS	QAM	CDMA/GSM/ AMPS
Freq. Range	2.4GHz	3.1-10.6GHz	868/915MHz 2.4GHz	2.4GHz -b/g 5.8GHz - a	2.4GHz	915MHz & 2.4GHz	2-11GHz	869-894MHz
Network	P2P	P2P	Mesh	IP & P2P	IP & P2P	P2P	IP	IP
IT Network Connectivity	No	No	No	Yes	Yes	No	Yes	Yes
Cost of Data	Free	Free	Free	Free	Free	Free	Free	Monthly Charge
Application	Cable replacement	Sync and Transmission of video/ audio data	Sensor networks	LAN, Internet	LAN, Internet	Point to point connectivity	Metro area broadband Internet connectivity	Celular telephones and telemetry

6.3. Future Scope for Zigbee Techniques

This project discusses the implementation of digital receiver for 2.4 GHz-band Zigbee applications on Spartan3E FPGA. Various digital receiver designs in the last six years were analyzed in terms of performance. The study concludes that the proposed Verilog-based design reduces the design area, shortens the simulation time, and decreases the clock frequency compared with VHDL-based designs.

Verilog also speeds up the design process and produces output quickly. These advantages are particularly important to engineers or designers who are on a tight deadline. Future work will implement the transmitter and the receiver parts integrated together as a top module by instantiating the modules using the Verilog code on FPGA. Thus, the receiver and the transmitter will be integrated to obtain a digital transceiver that can be tested over a 2.4 GHz Zigbee communication standard in a different transmission range.

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