Hena Naaz

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Education

MS Electrical & Computer Engr, Georgia Institute of Technology, USA (GPA-3.8) **Aug 2022 - May 2024**

Scholarship: Received 5000$ Women in Technology (academia) Scholarship from Cadence Design System
Coursework: Advanced Computer Architecture, GPU, Machine Learning, Secure & Reliable Computer Architecture

B.Tech Electronics & Communication Engr, Jamia Millia Islamia, India (GPA-3.9) **Jul 2013 - Jun 2017**

Experience

CPU Intern, AMD, USA | *Computer Architecture, C++, Assembly, Verilog, Scan debug* **May 2023 - Present**
- Owned microcode patches and design WAs no-harm/stress testing efforts for server/client CPU cores using C++ tests.
- Debugged CPU core micro-architecture pre-Si issues and post-Si hangs for modules like branch predictor, LSU, and caches.
- Working on CPU DataFabric RTL-HWA automation and specification documentation for each DF(NoC) subcomponent.

Graduate Research Assistant, Georgia Tech, USA | *Computer Architecture, C++* **Jan 2023 - May 2023**
- Supported RISC-V rev cores standard memory operations on Sandia SST simulator for data-centric architecture.

Senior ASIC Engineer, NVIDIA, India | *GPU Microarchitecture, C++, Verilog, FSDB debug* **Apr 2020 - Aug 2022**
- Delivered GPU core Context Switching units microarchitectural optimization for autonomous vehicles (ISO 26262).
- Debugged Verilog/design failures and created new C++ unit tests for the GPU core architecture coverage enhancement.
- Updated the VA/PA mappings during bind for 32 to 64 bits transition and verified features like Multi-instance GPU.
- Reviewed functional descriptions, analyzed performance and formulated architecture specifications with the team.

Application Engineer, Synopsys, India | *Verilog, System Verilog, FSDB debug* **Oct 2018 - Mar 2020**
- Worked on Test Plan Development, and FPGA-based Emulator hardware-software co-design using Verilog, SVA.
- Validated ZeBu Servers frontend and Verdi debug features on complex Soc/CPU/GPU Customer designs.

Product Validation Engineer, Cadence Design Systems, India | *Verilog, System Verilog* **Sep 2017 - Sep 2018**
- Validated design and improved performance of Xcelium Multi-core Simulator for Designs on multi-core/socket systems.
- Created assertions test banks (SVA) that identified significant gaps in new releases for designs on different architectures.

Projects

Vortex - Matrix Multiplication for Tensor Cores | *C++, Verilog, SimX* **Feb 2024 - Present**
- Extending the Vortex RISC-V GPU architecture with Matrix Multiplication Unit as Tensor core and an open-source interface on GPU + ML Accelerator for plug-and-play architecture.

Row-Hammer mitigation on memory system for low thresholds | *C++, Linux* **Mar 2023 - May 2023**
- Implemented C++ architectural simulator based on research works Graphene, CRA, Hydra for tracking, and RRS, Aqua for row hammer mitigation to prevent security threats due to bit flips in memory hierarchy for extremely low thresholds.

Multicore architecture with distributed memory | *C++, Makefiles, Linux* **Oct 2022 - Nov 2022**
- Designed a distributed memory system with multi level cache for multicore architecture. Also added static and dynamic cache partitioning schemes and presented performance analysis on benchmarks to compare.

5 stage and 7 stage pipelined MIPS processor | *C++, Verilog, Makefiles, Linux* **Aug 2022 - Oct 2022**
- Designed multi-cycle-per-instruction MIPS processor, with forwarding logic, stall detection, branch hazard logic and gshare branch predictor for superscalar machines. Extended the architecture for Tomasulo's algorithm with out-of-order execution.

Image Edge Detector on FPGA using VGA display | *Verilog, Xilinx ISE, MATLAB* **Dec 2016 - Mar 2017**
- Developed a laplacian-based pixel-preserver image edge detector and analyzed the hardware resources on FPGA.

Technical Skills

Software/Hardware Languages: C++, C, Verilog, System Verilog, HLS, Python, Linux Shell Scripting
Tools: Synopsys VCS and Verdi, Cadence Xcelium, Mentor Questasim, Xillinx ISE and Vivado, Sandia SST, gem5
MISC Technology Exposure: OpenCL, CUDA, OpenMPI, PyTorch

Paper Publication

Conference Paper on ML Accelerators | *IEEE WinTechCon* **Jun 2022**
- "Secure and Reliable Configurable and Reconfigurable Computing for Artificial Intelligence Applications".

Leadership

NVIDIA, International Toastmasters | *Served as Vice President, Education. Won annual best club award* **2021 - 2022**
NVIDIA, LeanIn Circle | *Founded WIT Bangalore group and served as the Circle Leader for a team of 12* **2021 - 2022**