# A Demonstration of Sampling Frequency Switching in the LTC2145 ADC

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*official name still to be determined

# Overview

- This is an update on the development of the SloDAQ*. My previous presentation was about two months ago and can be found here.

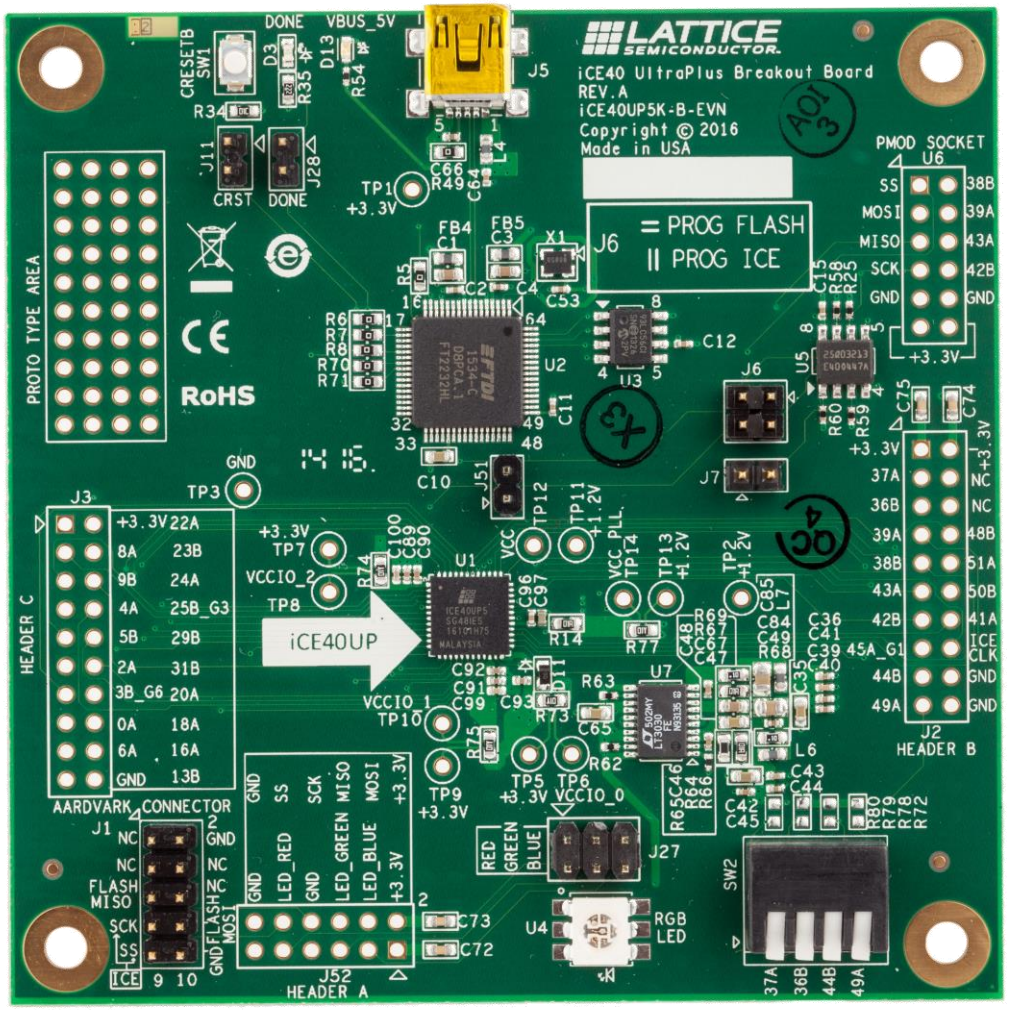
- The main result here is the demonstration of sampling frequency switching in the LTC2145 ADC, between idle (10 MHz) and triggered state (120 MHz), which can save us significant power.

*official name still to be determined

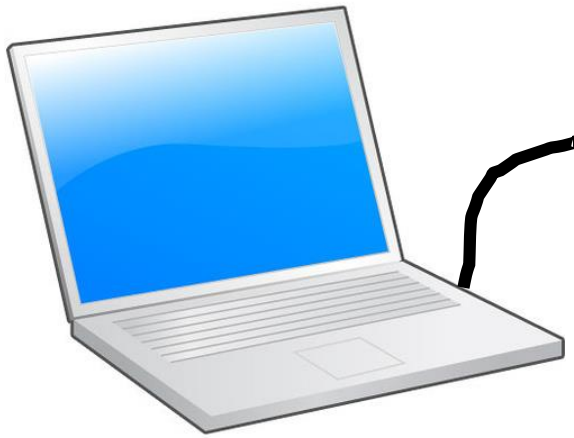
# From Last Time…

- Tested the iCE40 FPGA on a dev board. Demonstrated digital waveform capture and transfer (via UART) to my laptop.

ICE40UP5K-B-EVN



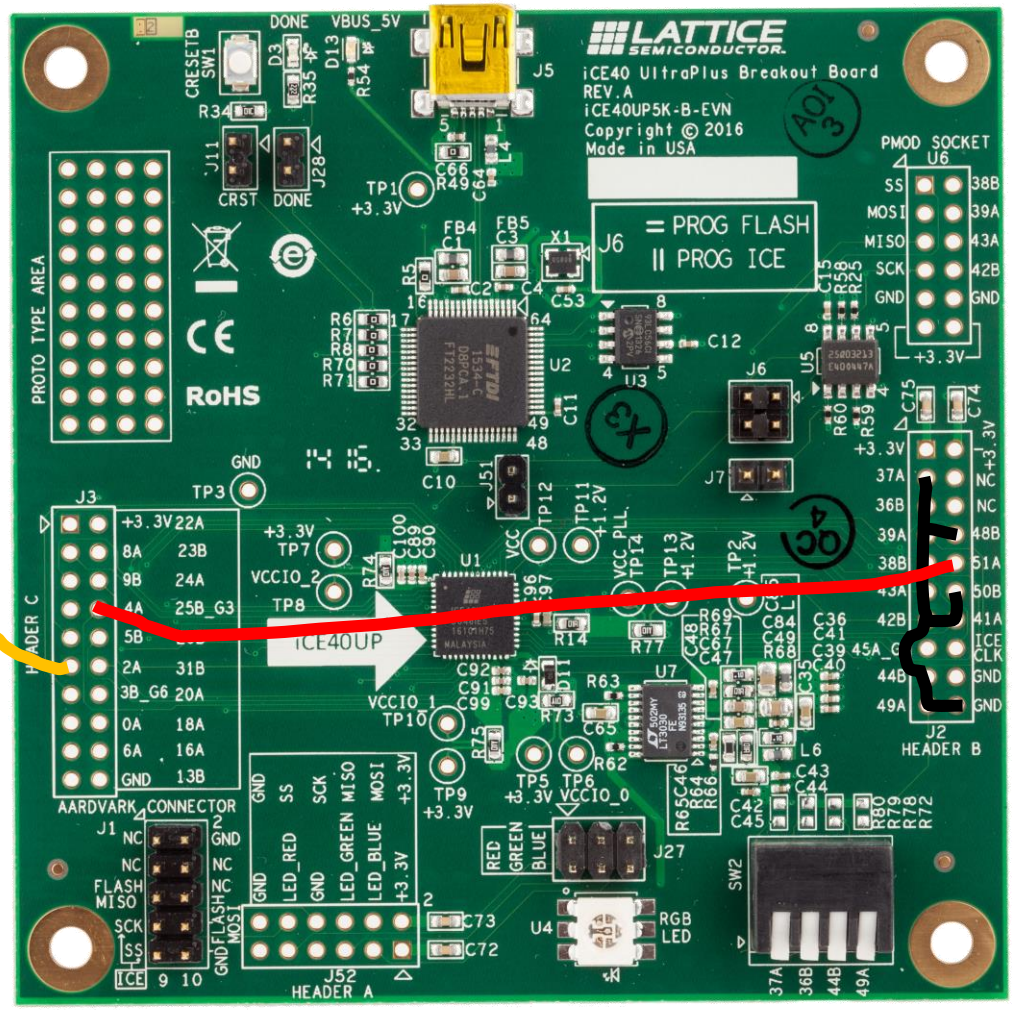
# From Last Time…



FTDI TTL-232R-3V3

Tx (2Mbaud)

ICE40UP5K-B-EVN



# From Last Time…

Command Prompt

```
C:\Users\Bunheng\Desktop\ice40UP>python pyserial_read_new.py
00000000
11111111


00010000
10000100
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000100
01000000
00000000
00000100
01000000
00000000
00000100
01000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000


00010000
00001100
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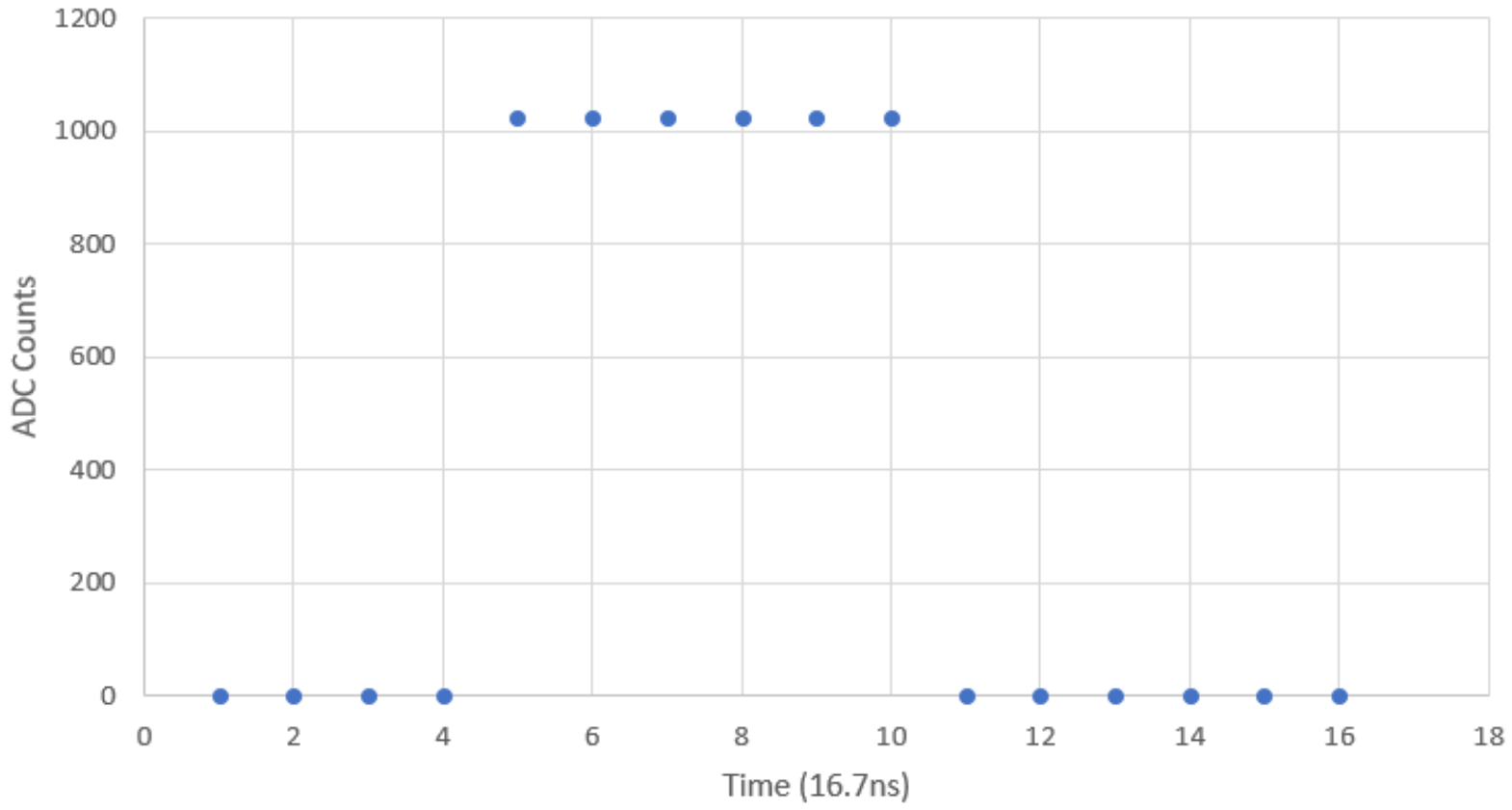
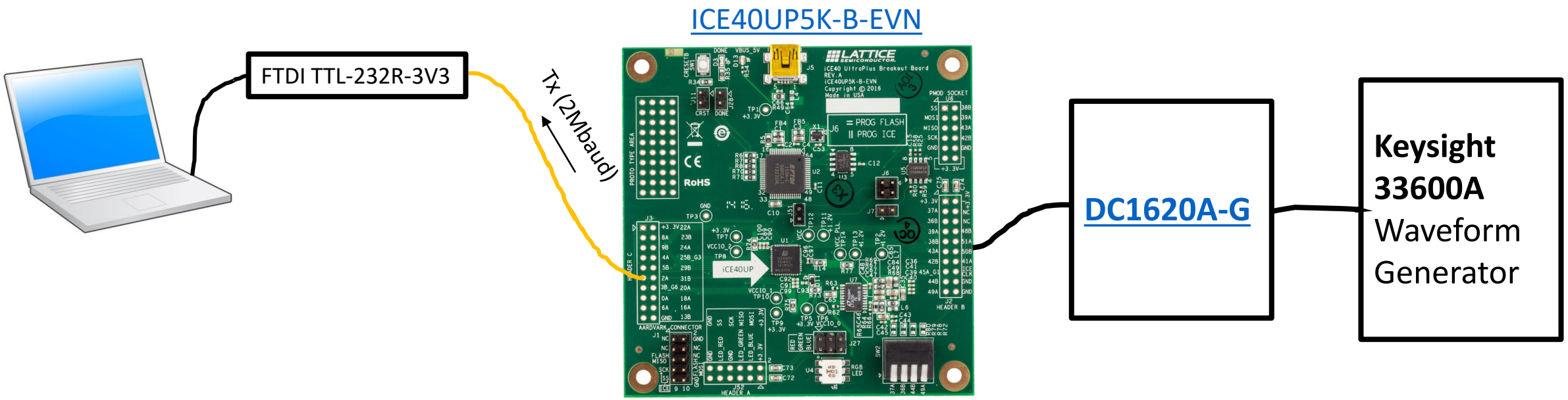


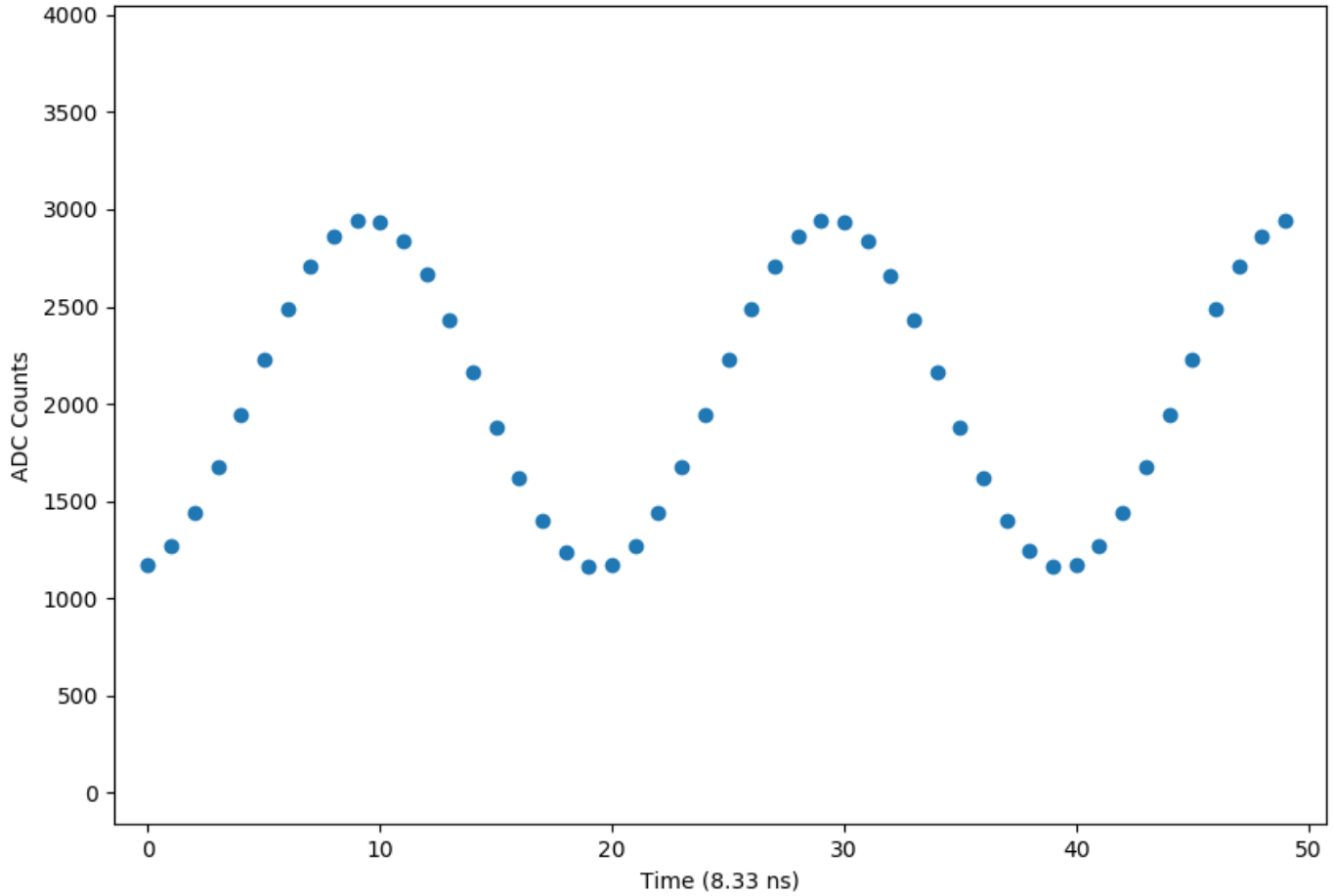
# This time


ICE40UP5K-B-EVN
FTDI TTL-232R-3V3
Tx (2Mbaud)
DC1620A-G
Keysight
33600A
Waveform
Generator

# This time

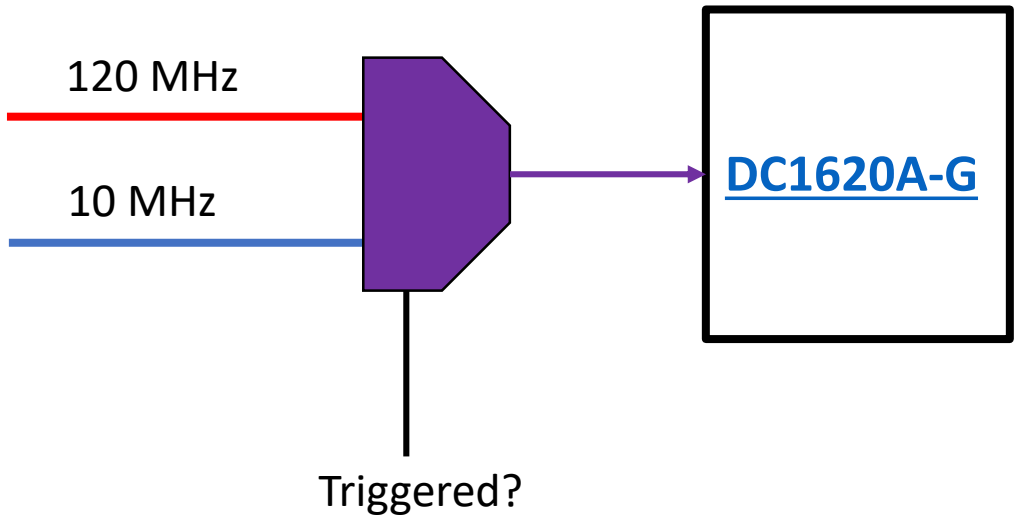
- 1Vpp at 6 MHz Sine wave from the waveform generator, digitized at 120MHz by the DC1620A dev board, buffered and sent to my computer by the ICE40UP5K dev board.

- Note: this is twice the sampling frequency from last time.

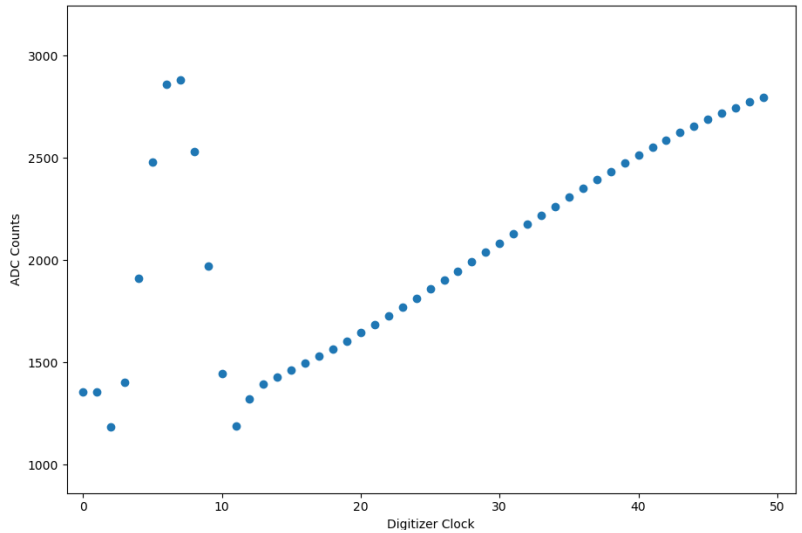


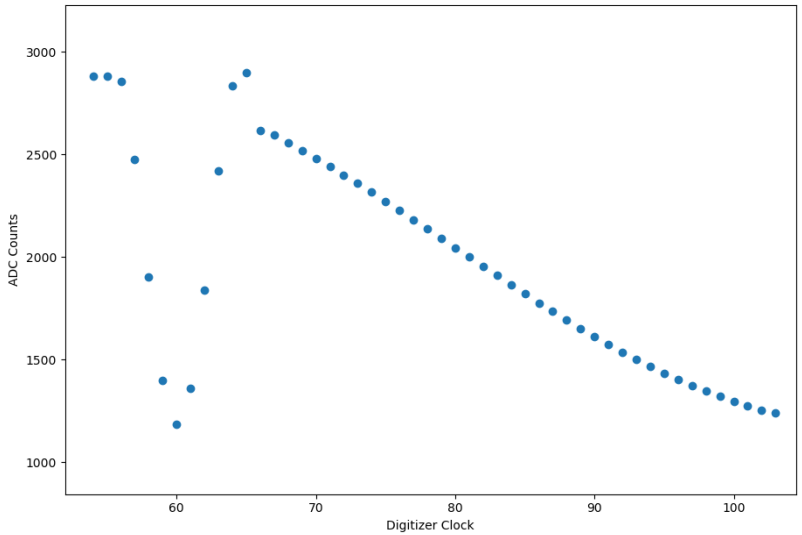
# The Main Test

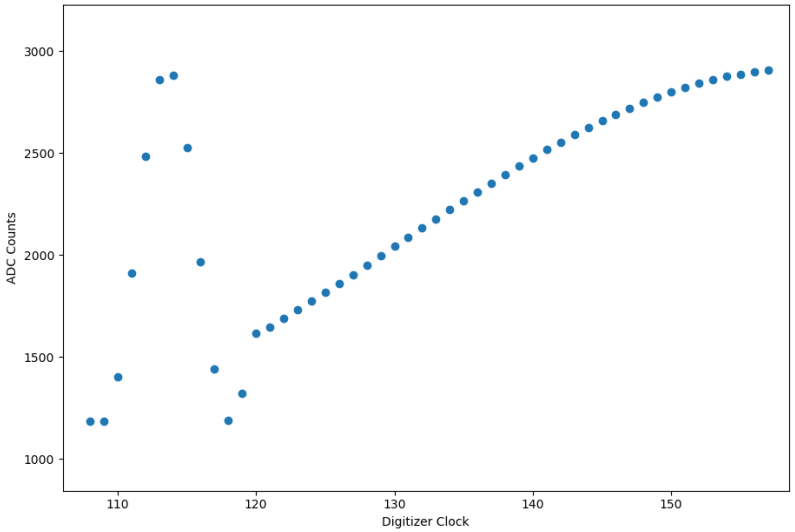
- It is wasteful to digitize at full clock speed during idle periods (no signal). Can the ADC be slowed down and only digitize at full speed during a trigger?

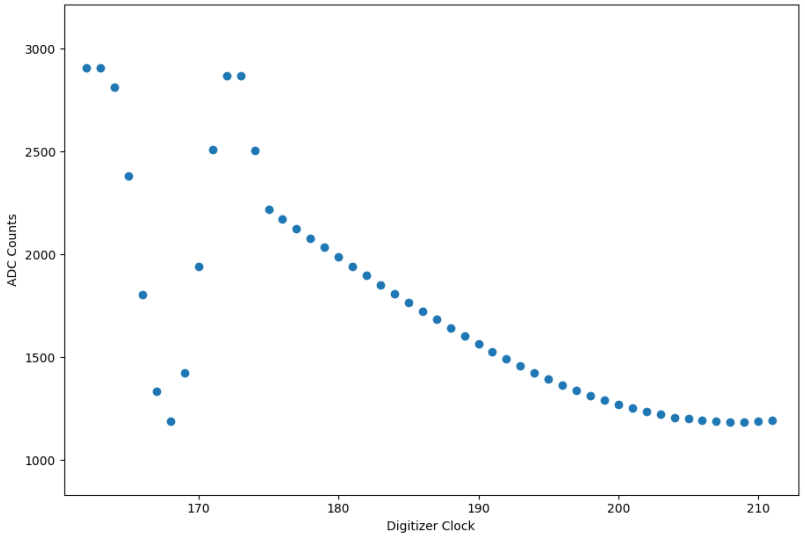


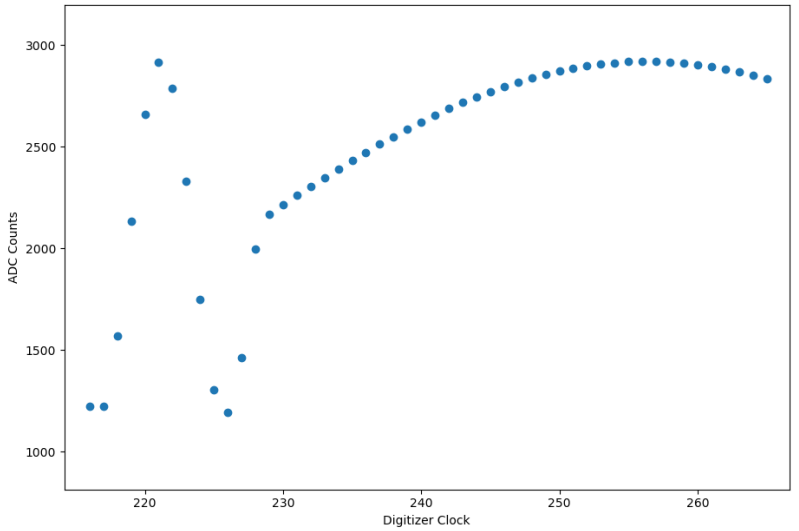
# The Main Test



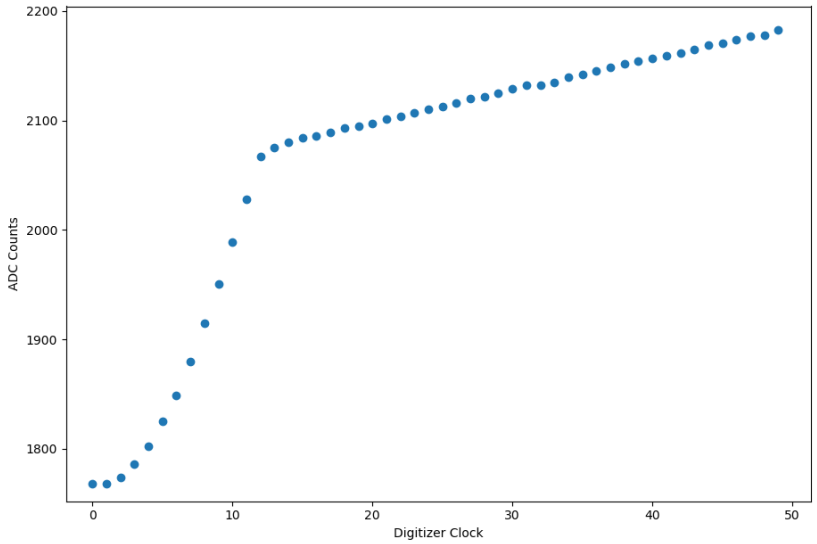



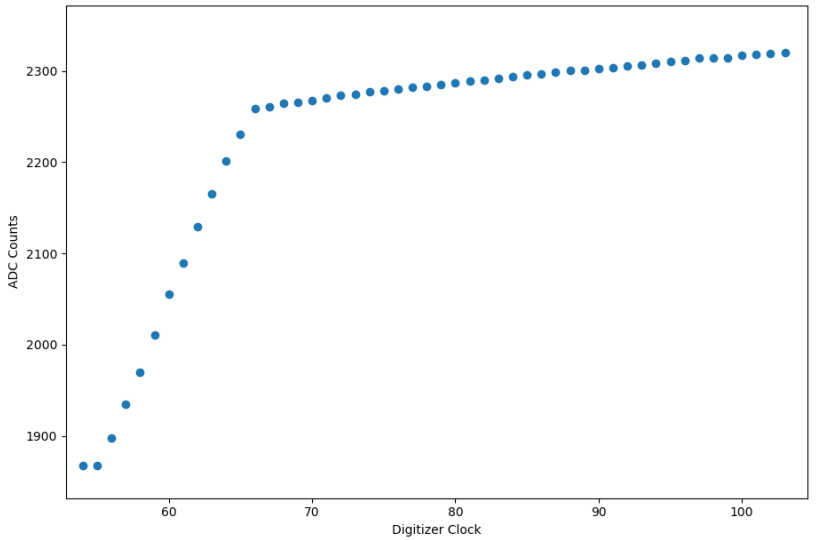



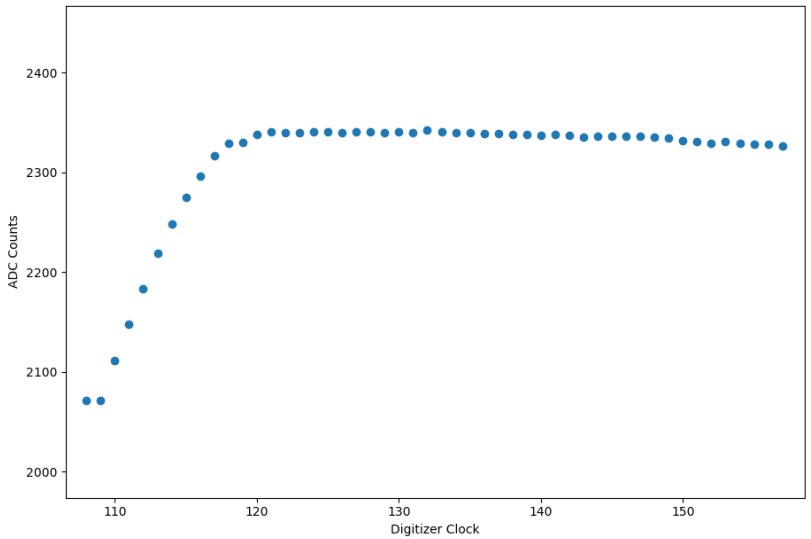



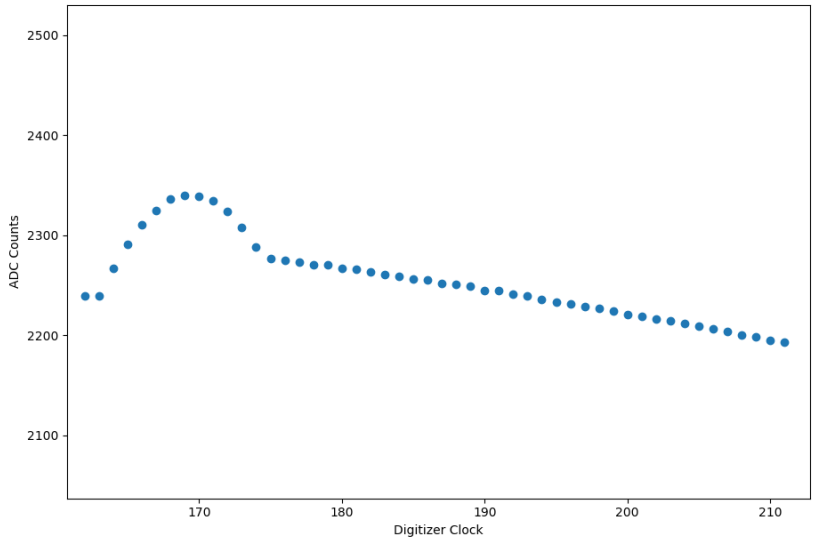

1 Vpp at 1MHz
Sine wave

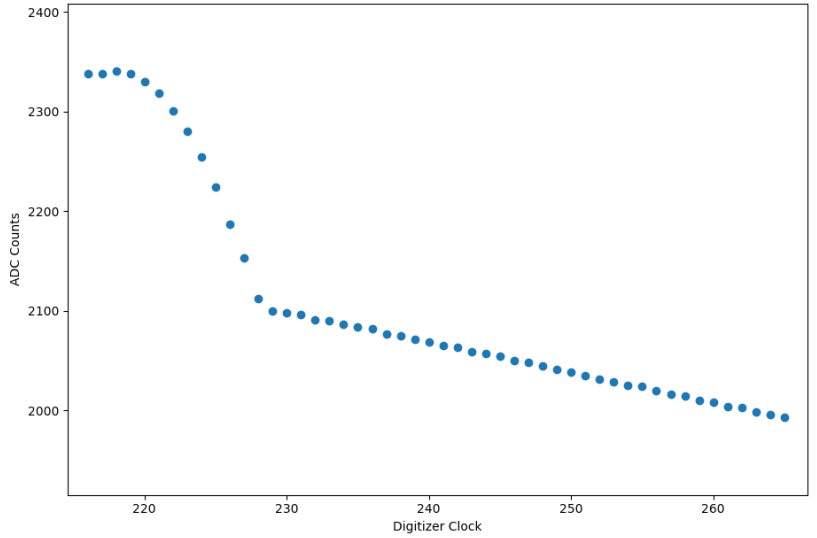
# The Main Test




1 Vpp at 200KHz
Sine wave

Raw data in the
SloDAQ folder

# Conclusions

- No quantitative statement to make at this point.
- But from the look at these waveforms, it seems like the ADC is able to handle the sudden frequency change from 10MHz to 120MHz fine.
- Mystery irregularities seen in waveforms might be due to noise in the setup, and bugs in my firmware.
- A quantitative test can be done after we route our own board. Also power measurements.
- iCE40 running at 120MHz, (What about 240?)

# Backup Slide