Parallelized sequential composition, pipelines, and hardware weak memory models

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Abstract

Since the introduction of the CDC 6600 in 1965 and its "scoreboarding" technique processors have not (necessarily) executed instructions in program order. Programmers of highlevel code may sequence independent instructions in arbitrary order, and it is a matter of significant programming abstraction and computational efficiency that the processor can be relied upon to make sensible parallelizations/reorderings of low-level instructions to take advantage of, for instance, multiple arithmetic units. At the architectural level such reordering is typically implemented via a per-processor pipeline, into which instructions are fetched in order, but possibly committed out of order depending on local considerations, provided any reordering preserves sequential semantics from that processor's perspective. However, multiprocessing and multicore architectures, where several pipelines run in parallel, can expose these processor-level reorderings as unexpected, or "weak", behaviours. Such weak behaviours are hard to reason about, and (via speculative execution) underlie at least one class of widespread security vulnerability.

In this paper we introduce a novel program operator, parallelized sequential composition, which can be instantiated with a function M that controls the reordering of atomic instructions. The operator generalises both standard sequential composition and parallel composition, and when appropriately instantiated exhibits many of the weak behaviours of the well-known hardware weak memory models TSO, Release Consistency, ARM, and RISC-V. We show that the use of this program-level operator is equivalent to sequential execution with reordering via a pipeline. Encoding reordering as a programming language operator admits the application of established compositional techniques (such as Owicki-Gries) for reasoning about weak behaviours, and is convenient for abstractly expressing properties from the literature such as sequential consistency. The semantics and theory is encoded and verified in the Isabelle/HOL theorem prover, and we give an implementation of the pipeline semantics in the Maude rewriting engine and use it empirically to show conformance of the semantics against established models of ARM and RISC-V, and elucidate some stereotypical weak behaviours from the literature.

Keywords: Semantics, pipelines, weak memory models

1 Introduction

The 1960s saw significant improvements in processor efficiency, including allowing out-of-order instruction execution in cases where program semantics would not be lost (e.g., the "scoreboarding" technique of the CDC 6600 [92]) and maximising use of multiple computation units (e.g., Tomasulo's algorithm [93], implemented in the IBM System360/91 [17]). These advances meant that instructions could be distributed in parallel among several subunits and their results combined, provided the computation of one did not depend on an incomplete result of another. Furthermore, interactions with main memory can be relatively slow in comparison to local computation, and so allowing independent loads and stores to proceed in parallel also improved throughput. Even more complex is speculative execution, in the sense of guessing the result of a branch condition evaluation and transiently executing down that path. These features had the effect of greatly increasing the speed of processors, and without any visible intrusion on programmers: the conditions under which parallelization could take place ensured the sequential semantics of any computation was maintained.

When concurrency is used, either explicitly as threads sharing a single processor or via multicore architectures, the effect of out-of-order execution may be exposed, as the reordering of accesses of shared memory can dramatically change concurrent behaviour. This has provided a challenge for developing efficient, correct and secure concurrent software for modern processors that communicate via shared memory [8, 24, 44]. Order can be restored by injecting artificial dependencies between instructions (usually called fences or barriers), but the performance cost is significant; for instance, performance concerns hamper the widespread mitigation of the Spectre class of security vulnerabilities, despite their seriousness [56, 94].

To reason about the impact of reorderings on program behaviour we introduce *parallelized sequential composition* as a primitive operator of an imperative language. The program ' c_1 ," c_2 ', for some function on instructions M, may execute c_1 and c_2 in order, or it may interleave actions of c_2 with those of c_1 provided M allows it. We give the weakest M such that c_1 , c_2 preserves the intended sequential semantics of a single process despite executing some instructions out of

order, and show how modern memory models are strengthenings of this concept, with the possible addition of further instruction types to restore order. Based on restrictions built into processors as early as the 1960s, we show that this concept of thread-local reorderings explains many of the behaviours observed on today's multicore architectures, such as TSO [49] and ARM [18], and conforms to RISC-V [84]. We derive language-level properties of parallelized sequential composition, and use these to explain possibly unexpected behaviours algebraically. In particular, under some circumstances the possible reorderings can be reduced to a nondeterministic choice between sequential behaviours, and then existing techniques for reasoning about concurrency, such as the Owicki-Gries method [78], can be employed directly. The language, its semantics, and the properties in the paper are encoded and machine-checked in the Isabelle/HOL theorem prover [76, 79] (see supplementary material).

In Sect. 2 we provide a foundation for instruction reordering, and provide a range of theoretical memory models. In Sect. 3 we give a straightforward abstract semantics for a hardware pipeline with reordering. In Sect. 4 we fully define the syntax and semantics of an imperative language, IMP+pseq, that includes conditionals, loops, and parallelized sequential composition. In Sect. 5 we show how standard Hoare logic and weakest preconditions can be used to reason about IMP+pseq. We then define TSO (Sect. 6), Release Consistency (Sect. 7), ARM (Sect. 8) and RISC-V (Sect. 9) as instances of parallelized sequential composition, showing conformance via both general properties and empirically (ARM and RISC-V). We discuss related work in Sect. 10.

2 Foundations of instruction reordering

In this section we describe instruction reordering in a simple language containing a minimal set of instruction types and the novel operator parallelized sequential composition (we give a richer language in Sect. 4). Instances of this operator are parameterized by a function on instructions, which for convenience we call a *memory model.*¹ We use this foundation to explore theoretically significant memory models that underlie modern processors.

We start with a basic imperative language containing just assignments and guards as actions (type *Instr*) with parallelized sequential composition as combinator.

$$\alpha ::= x := e \mid (e)$$
 $c ::= \mathbf{nil} \mid \alpha \mid c_1 \stackrel{\text{\tiny M}}{;} c_2$

An assignment x := e is the typical notion of an update, encompassing stores and loads, while a guard action (e) represents a test on the state (does expression e evaluate to True) which can be used to model conditionals/branches. A command is either the terminated command nil (corresponding

to a no-op), an action α , or the composition of two commands according to some memory model M.

The intention is that a simple command $\alpha^{\text{M}}_{:}\beta$ is free to execute instruction β before instruction α (possibly with modifications due to forwarding, described below) provided the constraints of M are obeyed. Clearly this potential reordering of instructions may destroy the programmer's intention if unconstrained; however the reordering (or parallelization) of independent instructions can potentially be more efficient than the possibly arbitrary order specified by the programmer. For example, consider a load followed by an update $r := x \stackrel{\text{M}}{;} y := 1$. If x is a shared variable then retrieving its value from main memory may take many processor cycles. Rather than idle the independent instruction y=1 can be immediately issued without compromising the programmer's intention assuming a single-threaded context. In general, two assignments can be reordered if they preserve the sequential semantics on a single thread.

A memory model M is of type $Instr \to \mathbb{P}(Instr \times Instr)$. However we will typically express a memory model as a binary relation on instructions, the reordering relation, with the implicit application of a forwarding function, which is either a straightforward variable substitution or the identity function. We first consider the reordering relation and then forwarding, which significantly complicates matters.

Reorderings. First consider the base of a memory model, the "reordering relation", which is a binary relation on instructions. We write $\alpha \stackrel{\text{\tiny M}}{\Leftarrow} \beta$ if β may be reordered before instruction α according to the reordering relation of memory model M, and $\alpha \stackrel{\text{\tiny M}}{\Leftarrow} \beta$ otherwise. We define the special case of the *sequentially consistent* memory model as that where no reordering is possible.

Model 1 (sc). For all
$$\alpha, \beta \in Instr$$
, $\alpha \stackrel{sc}{\Leftarrow} \beta$.

We may now explicitly state the notion of a *sequential* model [62], which is the minimal property that any practical memory model M should establish. Letting the 'effect' function eff return the relation between pre- and post-states for a program (see Sect. 5) we can state this property as follows

Definition 2.1. M is sequential if
$$eff(c_1 \overset{\text{M}}{;} c_2) \subseteq eff(c_1 \overset{\text{sc}}{;} c_2)$$
.

That is, M is sequential if its reorderings give the same results (on a single thread) as when executed in program order. The weakest sequential memory model is one that allows reordering exactly when sequential semantics is maintained.

Model 2 (EFF).
$$\alpha \stackrel{\text{EFF}}{\longleftarrow} \beta$$
 iff $\text{eff}(\beta \stackrel{\text{sc}}{;} \alpha) \subseteq \text{eff}(\alpha \stackrel{\text{sc}}{;} \beta)$

Theorem 2.2. EFF *is* sequential.

Proof. The property
$$\alpha \stackrel{\text{EFF}}{\longleftarrow} \beta$$
 lifts to commands. \Box

EFF is impractical since processors cannot make semantic judgements about the overall effect of two instructions

¹Memory models may embrace global features in addition to weak behaviours due to pipelining; since many behaviours of weak memory models are explained by pipeline reordering we use this more general term.

dynamically; however there are some simple syntactic constraints which guarantee sequential semantics. As such we propose the following memory model as the weakest possible that is of practical use.

Model 3(G₀).
$$\alpha \stackrel{G_0}{\longleftarrow} \beta$$
 iff $wv(\alpha) \not \cap fv(\beta)$ and $wv(\beta) \not \cap fv(\alpha)$

Model 3 (abbreviated **M3**) allows instructions to be reordered based on a simple *syntactic* test, namely, is any variable that β references (fv(β)) modified by α , and vice versa, using naming conventions below.

$$fv(e)$$
, $fv(\alpha)$ Free variables in expr. e or action α (1)

$$wv(\alpha)$$
, $rv(\alpha)$ Write, read variables (2)

$$s_1 \not \cap s_2 = s_1 \cap s_2 = \emptyset$$
 (mutual exclusion) (3)

Reorderings eliminated by **M3** include $(x := 1 \stackrel{G_0}{\longleftarrow} x := 2)$, $(x := 1 \stackrel{G_0}{\longleftarrow} r := x)$ and $(r := x \stackrel{G_0}{\longleftarrow} x := 1)$. In general, if $\text{wv}(\alpha) \subseteq \text{rv}(\beta)$, for $\alpha, \beta \in Instr$, then there is a *data dependency* between α and β , that is, the value of a variable that β depends on is being computed by α . It is straightforward that $(\alpha \stackrel{G_0}{\longleftarrow} \beta) \Rightarrow (\alpha \stackrel{\text{EFF}}{\longleftarrow} \beta)$ i.e., G_0 is stronger than EFF. We can therefore infer that G_0 is *sequential*.

Theorem 2.3. *If* M *is stronger than* EFF *then* M *is* sequential.

Proof. A stronger model admits fewer behaviours (24). \Box

The memory model G_0 is lacking in the age of multicore processors because it does not require two consecutive loads of the same *shared* variable to be performed in order. For instance, consider the following concurrent processes.

$$r_1 := x \stackrel{c_0}{;} r_2 := x \quad || \quad x := 1 \stackrel{c_0}{;} x := 2$$
 (4)

The two loads should read values of x in a globally "coherent" manner, that is, the value for x loaded into r_1 must occur no later than that loaded by r_2 . Hence program (4) should not reach the final state $r_1 = 2 \land r_2 = 1$. However, although $x := 1 \stackrel{G_0}{\longleftarrow} x := 2$, we have $r_1 := x \stackrel{G_0}{\longleftarrow} r_2 := x$ in the first thread.

To cope with shared variables and coherence we divide the set of variables, Var, into mutually exclusive and exhaustive sets Shared and Local, with specialised definitions below

$$sv(\alpha)$$
, $rsv(\alpha)$, $wsv(\alpha)$ As (1), (2), restricted to Shared (5)

$$isStore(\alpha) = wsv(\alpha) \neq \emptyset \land rsv(\alpha) = \emptyset$$
 (6)

$$isLoad(\alpha) \stackrel{\frown}{=} wsv(\alpha) = \emptyset \wedge rsv(\alpha) \neq \emptyset$$
 (7)

$$isReg(\alpha)$$
 iff α is an assign. or guard and $sv(\alpha) = \emptyset$ (8)

To maintain "coherence per location" we extend G_0 to G by adding a constraint on the loaded shared variables. Additionally, since we are now explicitly concerned with concurrent behaviour, we add a fence instruction type to restore order, i.e., $\alpha := \dots \mid$ **fence**. We call this an "artificial" constraint, since it is not based on "natural" constraints arising from the preservation of sequential semantics.

Model 4 (G). $\alpha \stackrel{G}{\rightleftharpoons} \beta$ iff $\alpha \stackrel{G_0}{\rightleftharpoons} \beta \wedge rsv(\alpha) \not \cap rsv(\beta)$, except $\alpha \stackrel{G}{\rightleftharpoons} \mathbf{fence} \stackrel{G}{\rightleftharpoons} \alpha$.

When specifying a memory model we typically give the base relation first, and then list the "exceptions", which take precedence. **M4** strengthens the condition of **M3** to require loads from main memory to be kept in program order per shared variable. In addition fences block reordering, reinstating program-order execution explicitly if desired by the programmer (at the potential cost of efficiency). We let $\alpha \stackrel{\text{M}}{\leftarrow} \beta \stackrel{\text{M}}{\leftarrow} \gamma$ abbreviate $\alpha \stackrel{\text{M}}{\leftarrow} \beta \wedge \beta \stackrel{\text{M}}{\leftarrow} \gamma$, and similarly for $\stackrel{\text{M}}{\leftarrow}$.

We consider G to be the weakest memory model of practical consideration in a concurrent system as it maintains both coherence-per-location and sequential semantics.

Definition 2.4. Model M is *coherent* if it is stronger than G.

Most modern processors are coherent. A memory model that is not coherent, and is the obvious weakest dual of **M1**, is one that allows any instructions to be reordered under any circumstances. If we disallow forwarding in this model (discussed in the next section), this weakest memory model corresponds to parallel composition.

Model 5 (PAR). For all
$$\alpha, \beta \in Instr$$
, $\alpha \stackrel{\text{PAR}}{\longleftarrow} \beta$

We may now define $c \parallel d = c^{\text{\tiny PAR}}$; d, lifting instruction-level parallelism to thread-level parallelism.

The key point about the sc memory model (M1) is that reasoning is "straightforward", or classical, in that all the accepted techniques work. This is the property of *sequential consistency* [62], formalised below.

Definition 2.5. Command $c_{(M)}$ is structurally identical to c but every parallelized sequential composition, except for instances of PAR, is parameterized by M.

Definition 2.6 (Sequentially consistent). A memory model M is sequentially consistent if, for any programs c and d, ignoring local variables, $c_{\langle M \rangle} \parallel d_{\langle M \rangle} = c_{\langle SC \rangle} \parallel d_{\langle SC \rangle}$.

By definition sc is sequentially consistent, however even sequentially consistent uniprocessors are not as strong as M1, for instance, some speculate loads and reissue them if a change is detected (relatively quickly via the cache [100]). Note the difference between *sequential* and *sequentially consistent*: a sequentially consistent memory model is sequential, but not vice versa. None of TSO, ARM or RISC-V are sequentially consistent in general, but are for programs in a particular form, e.g., where shared variables are accessed according to a lock-based programming discipline.

Forwarding. We now complicate matters significantly by considering *forwarding*, where the effect of an earlier operation can be taken into account when deciding if instructions can be reordered.² For instance, given a program x:=1; r:=x,

²We use the term "forwarding" from ARM and POWER [16], sometimes referred to as "bypassing" in TSO [87].

we have $x:=1 \stackrel{G}{\leftarrow} r:=x$ because $wv(x:=1) = \{x\} \subseteq fv(r:=x)$, violating **M3**. In practice however it is possible to *forward* the new value of x to the later instruction – it is clear that the value assigned to r will be 1 if x is local, and in any case is a valid possible assignment to r even if x is shared. We define $\beta_{\ll \alpha}$, representing the effect of forwarding the (assignment) instruction α to β , where the expression $f_{[x \setminus e]}$ is f with references to x replaced by e.

Definition 2.7 (Forwarding). $\beta_{\alpha} = \beta$, except

$$(y := f)_{\langle x \rangle := e} = y := (f_{[x \setminus e]})$$
 $(f)_{\langle x \rangle := e} = (f_{[x \setminus e]})$

Forwarding and reordering are combined to form a memory model as follows, where the effect of forwarding is taken into account *before* calculating reordering.

$$\mathbf{M} \ \widehat{=} \ \lambda \alpha . \{ (\beta_{\alpha \alpha}, \beta) \mid \alpha \stackrel{\mathbf{M}}{\Leftarrow} \beta_{\alpha \alpha} \}$$
 (9)

$$\beta' \ll \alpha \stackrel{\mathrm{M}}{\ll} \beta \quad \widehat{=} \quad (\beta', \beta) \in \mathrm{M}(\alpha) \tag{10}$$

Thus a memory model M for a given action α returns a set of pairs (β', β) where β reorders with α , after the effect of forwarding α to β (β') is taken into account. For convenience we sometimes use the notation $\beta' \ll \alpha \ll \beta$ which notationally conveys the bringing forward of β with respect α . For example, since $(r := x)_{\ll x := 1} = (r := (x_{\lceil x \setminus 1 \rceil})) = r := 1$, the load r := x "reorders" with x := 1, becoming r := 1.

$$r := 1 \, {}^{\mathsf{G}} x := 1 \, {}^{\mathsf{G}_0} r := x \tag{11}$$

Forwarding is significant because it can change the orderings allowed in a non-standard way, since a later instruction that was blocked by r := x may no longer be blocked, and potentially can now also be reordered before x := 1. Of course, this is potentially a significant efficiency gain, because local computation can proceed using the value 1 for x without waiting for the update to propagate to the rest of the system.

Memory models with out-of-order execution typically use forwarding. (As noted above, one exception is PAR for interleaving parallel). In G and G_0 reordering is symmetric, however when calculated after the effect of forwarding is applied there are instructions that may be reordered in one direction but not the other. In general a reordering relation is neither reflexive nor transitive.

Memory model refinement. We define model refinement as a strengthening per action.

Definition 2.8.
$$M_1 \sqsubseteq M_2 = \forall \alpha \bullet M_2(\alpha) \subseteq M_1(\alpha)$$

As we explore in the rest of the paper, the Total Store Order memory model (TsO) strengthens G considerably (or alternatively, weakens sc for the particular case of stores and loads), while ARM strengthens G to prevent stores from coming before branches. ARM, RISC-V, and the release consistency models RC_{pc} and RC_{sc} are related as below, focusing on their common instruction types; since each introduces

unique instruction types a direct comparison is not possible.

Theorem 2.9 (Hierarchy of models).

$$\mathsf{EFF} \sqsubseteq \mathsf{G}_0 \sqsubseteq \mathsf{G} \sqsubseteq \mathsf{RC}_{pc} \sqsubseteq \mathsf{RISC}\text{-}\mathsf{V} \sqsubseteq \mathsf{RC}_{sc} \sqsubseteq \mathsf{ARM} \sqsubseteq \mathsf{TSO} \sqsubseteq \mathsf{SC}.$$

Proof. Straightforward from definitions. □

This result is similar to other classifications [11, 41, 43]. Note that PAR does not fit into the hierarchy because it does not allow forwarding.

Well-behaved models. A memory model could theoretically allow arbitrary reorderings and effects of forwarding; however from a reasoning perspective we make the following definition of well-behaved memory models.

Definition 2.10. A memory model M is well-behaved if it is sc or if: i) the result of reordering is deterministic; ii) any resulting action β' must arise from the application of the forwarding function (Definition 2.7), or have no change at all, i.e., we do not allow arbitrary effects of forwarding; and iii) if an action allows any reordering then it must allow reordering with *internal* ("silent") steps.

Conditions i) and ii) ensure determinacy and sequential semantics, while condition iii) simplifies reasoning (silent steps are defined in Sect. 4). All the memory models we consider are well-behaved, with the exception of PAR.

3 Pipeline semantics

Before defining a full language we consider how a reordering relation can be used to define the semantics of a processor pipeline where instructions can be reordered. The command ($\mathbf{pline}_{\mathbf{m}}$ t: c) represents the execution of c with t a sequence of instructions that are currently (in) the pipeline; instructions in t can be issued to the wider system in order, or out-of-order according to \mathbf{m} . Assume that c is executed sequentially, (i.e., is of the form $c_{\langle \mathbf{sc} \rangle}$), then the behaviour of the pipeline is as follows.

$$\frac{c \xrightarrow{\alpha} c'}{(\mathbf{pline}_{\mathsf{M}} \ \mathsf{t} : c) \xrightarrow{\tau} (\mathbf{pline}_{\mathsf{M}} \ \mathsf{t} \cap \alpha : c')} \tag{12}$$

$$\frac{\alpha' \otimes \mathsf{t}_1 \overset{\text{\tiny M}}{\otimes} \alpha}{(\mathbf{pline}_{\text{\tiny M}} \ \mathsf{t}_1 \cap \alpha \cap \mathsf{t}_2: \ c) \xrightarrow{\alpha'} (\mathbf{pline}_{\text{\tiny M}} \ \mathsf{t}_1 \cap \mathsf{t}_2: \ c)} \ (13)$$

Rule (12) states that the next instruction in c in sequential order can be "fetched" and placed at the end of the pipeline; c is effectively the "code base". We use ' ' for appending lists, and for convenience allow it to apply to individual elements as well. The promoted step τ represents an internal action of the processor, which is ignored by the rest of the system. Rule (13) states that an instruction α somewhere in the pipeline can be "committed" out of order, provided it can be reordered with all prior instructions currently in the pipeline. The notation α' « $t \stackrel{\text{\tiny M}}{=} \alpha$ (cf. (10)) is a shorthand

for $(\alpha', \alpha) \in M(t)$, i.e., lifting M from a function on instructions to sequences of instructions, that is, M([]) = id and $M(\alpha \cap t) = M(\alpha) \circ M(t)$, where '[]' is the empty list, 'id' is the identity relation, and '9' is relational composition.

Consider executing the program $r_1 := x :; r_2 := y :; c$ in a pipeline. Both loads can be fetched (in order) into the pipeline by (12), but then, assuming $r_1 := x \stackrel{\text{M}}{\leftarrow} r_2 := y$, $r_2 := y$ may be committed before $r_1 := x$ by (13) (or further instructions from c could be fetched and potentially committed). The fetch/commit rules abstract from other stages in a typical pipeline (see, e.g., [67]), for instance, the two loads above would be issued to the system in order, with the out-of-order commit corresponding to the second load being serviced earlier by the memory system.

We encoded this semantics straightforwardly in the Maude rewriting engine [29, 97] as a model checker (see supplementary material). We find this processor-level view to be convenient for showing equivalence with other models of reordering, for instance, the store buffer model of TSO (Sect. 6.1) and an axiomatic specification of ARM (Sect. 8.1). However it is not directly amenable to established techniques for reasoning about programs such as Hoare Logic [45], Owicki-Gries (OG) [78] or rely/guarantee [51], which are over the structure of a program. As such we now consider embedding reordering into a typical imperative language, where the following theorem holds (recall Definition 2.5).

Theorem 3.1. For well-behaved M, $c_{\langle M \rangle} = (\mathbf{pline}_{M} []: c_{\langle SC \rangle})$ *Proof.* By induction on traces. \Box

An imperative language with parallelized sequential composition

In this section we give the syntax and semantics for an imperative programming language, "IMP+pseq", which uses parallelized sequential composition (extending that of Sect. 2).

Syntax. The syntax of IMP+pseq is given below.

$$\alpha ::= x := e \mid (e) \mid \mathbf{barrier}(f)$$

$$c ::= \mathbf{nil} \mid \alpha \mid c_1 \stackrel{\mathsf{sc}}{}_{1} c_2 \mid c_1 \sqcap c_2 \mid c_{\mathsf{m}}^{\omega}$$

$$c_1 :: c_2 = c_1 \stackrel{\mathsf{sc}}{}_{1} c_2 \qquad c_1 \parallel c_2 = c_1 \stackrel{\mathsf{par}}{}_{1} c_2 \qquad (14)$$

$$c_{\mathsf{m}}^{0} = \mathbf{nil} \qquad c_{\mathsf{m}}^{n+1} = c \stackrel{\mathsf{sc}}{}_{1} c_{\mathsf{m}}^{n} \qquad (15)$$

(if b then
$$c_1$$
 else c_2)_M $\stackrel{\frown}{=}$ (b) $\stackrel{\text{\tiny M}}{;}$ c_1 \sqcap ($\neg b$) $\stackrel{\text{\tiny M}}{;}$ c_2 (16)

(while
$$b \operatorname{do} c)_{M} = ((b))^{M} (c)^{M} (c)^{M} (c)^{M} (c)^{M}$$
 (17)

The basic actions of a weak memory model are an update x := e, a guard (e), and a barrier. (We give an atomic expression evaluation semantics for assignments and guards, which is typically reasonable for assembler-level instructions.) The barrier instruction type can be instantiated for some data type which we leave unspecified at this point; particular memory models typically introduce their own barrier/fence types and we define them in later sections. We assume that every model has at least a "full" fence, and define fence = **barrier**(full). The special instruction $\tau = ||True||$ is a silent step (defined later), having no effect on the state, possibly corresponding to some internal actions of a microprocessor.

A command c may be the terminated command **nil**, a single instruction, the parallelized sequential composition of two commands (parameterised by a memory model), a binary choice, or an iteration. Iterations are parameterised by a memory model, as they implicitly contain sequencing.

In (14) we use parallelized sequential composition to define '.;' as the usual notion of sequential composition (see M1), and '||' as the usual notion of parallel composition (see **M5**). Finite iteration of a command, c_M^n , is the *n*-fold composition of c with reordering according to M (15). Conditionals are modelled using guards and choice (where false branches are never executed) (16). By allowing instructions in c_1 or c_2 to be reordered before the guards one can model speculative execution, i.e., early execution of instructions which occur after a branch point [90]. We define a while loop using iteration (17) following [38, 59]. Both conditionals and loops are parameterised by a memory model since they include a parallelized sequential composition.

Operational semantics. The meaning of IMP+pseq is formalised using an operational semantics, given below. The operational semantics generates a sequence of syntactic instructions (as opposed to Plotkin-style pairs-of-states [80]), allowing syntactic analysis of instructions to decide on reorderings. We show how to convert straightforwardly to pairs-of-states style in Sect. 5.

$$\alpha \xrightarrow{\alpha} \mathbf{nil}$$
 (18) $c_{\mathrm{M}}^{\omega} \xrightarrow{\tau} c_{\mathrm{M}}^{n}$ (19)

$$c \sqcap d \xrightarrow{\tau} c$$
 (20) $c \sqcap d \xrightarrow{\tau} d$ (21)

$$c \sqcap d \xrightarrow{\tau} c \qquad (20) \qquad c \sqcap d \xrightarrow{\tau} d \qquad (21)$$

$$c_{1} \xrightarrow{\alpha} c'_{1} \qquad (22) \qquad \text{nil}_{;c_{2}} \xrightarrow{\tau} c_{2} \qquad (23)$$

$$\frac{c_1, c_2}{c_2 \xrightarrow{\beta} c'_2 \qquad \beta' \ll c_1 \overset{M}{\ll} \beta}{c_1 \overset{M}{;} c_2 \xrightarrow{\beta'} c_1 \overset{M}{;} c'_2} \tag{24}$$

Sequential fragment. The operational semantics of an instruction is simply a step labelled by the instruction itself (18). After executing the corresponding step an instruction α is terminated, i.e., becomes **nil**. The semantics of loops is given by unfolding a nondeterministically-chosen finite number of times (19) (recall (15)). A nondeterministic choice (the internal choice of CSP [46]) can choose either branch (20, 21). A parallelized sequential composition $c_1 \stackrel{\text{\tiny M}}{;} c_2$ can take a step if c_1 can take a step (22), and continues with c_2 when c_1 has terminated (23), as in standard sequential composition.

³We ignore infinite loops to avoid the usual complications they introduce, since they do not add anything to the discussion of instruction reordering.

Together these rules give a standard sequential semantics for imperative programs, and we refer to them as the "sequential fragment".

Parallelized sequential composition. We now consider a further rule, unique to IMP+pseq, that allows reordering of instructions. Rule (24) states that given a program $c_1 \stackrel{\text{\tiny M}}{:} c_2$, an instruction β of c_2 can happen before the instructions of c_1 , provided that $\beta' \ll c_1 \stackrel{\text{\tiny M}}{\ll} \beta$, i.e., β is not dependent on instructions in c_1 (according to the rules of model M), and the result of (accumulated) forwarding of instructions in c_1 to β results in β' . This is given by lifting a model M to commands, defined inductively below (recall (9) and (10)).

$$M(\mathbf{nil}) = id \quad M_1(c_1 \overset{M_2}{;} c_2) = M_1(c_1) \circ M_1(c_2)$$
 (25)

$$M(c_1 \sqcap c_2) = M(c_1) \cap M(c_2) \quad M(c_M^{\omega}) = \bigcap_n M(c_M^n) \quad (26)$$

Any instruction may reorder with the empty command **nil**. Reordering according to memory model M_1 over $c_1 \stackrel{M_2}{;} c_2$ is the relational composition of the orderings of c_1 and c_2 with respect to M_1 (independent of M_2) (25). Reordering over a choice is possible only if reordering can occur over both branches (26) (but choices can be resolved via (20, 21)). Reordering over an iteration is possible only if reordering is possible over all possible unrollings.

Trace semantics. Given a program c the operational semantics generates a trace, that is, a finite sequence of steps $c_0 \xrightarrow{\alpha_1} c_1 \xrightarrow{\alpha_2} \dots$ where the labels in the trace are actions. We write $c \stackrel{t}{\Rightarrow} c'$ to say that c executes the actions in trace t and evolves to c'. Traces of visible actions are accumulated into the trace, and *silent* actions (such as τ) are discarded, i.e., we have a "weak" notion of equivalence [74]. A visible action is any action with a visible effect, for instance, fences, assignments, and guards with free variables. Silent actions include any guard which is *True* in any state and contains no free variables; for instance, (0 = 0) is silent while (x = x)is not. A third category of actions, infeasible α , includes exactly those guards (b) where b evaluates to False in every state. This includes actions such as (False) and $(x \neq x)$. The meaning of a command c is its set of all terminating behaviours, written [c], with behaviours containing infeasible actions being excluded from consideration.

Refinement. We take the usual (reverse) subset inclusion definition of refinement, i.e., $c \sqsubseteq d$ if every behaviour of d is a behaviour of c; our notion of command *equivalence* is refinement in both direction. From this definition we can derive expected properties for the standard operators such as $[c \sqcap d] = [c] \cup [d]$ and $[c : d] = [c] \cap [d]$ (overloading ' \cap ' to mean pairwise concatenation of sets of lists).

Properties for parallelized sequential composition are, of course, more interesting, and we provide some below that

we make use of in the rest of the paper.

$$c_1 \stackrel{\scriptscriptstyle{\mathsf{M}}}{;} c_2 \sqsubseteq c_1 .; c_2$$
 (27)

$$c \sqcap d \sqsubseteq c$$
 (28)

$$(c_1 \overset{\text{\tiny M}}{;} c_2) \overset{\text{\tiny M}}{;} c_3 = c_1 \overset{\text{\tiny M}}{;} (c_2 \overset{\text{\tiny M}}{;} c_3)$$
 (29)

$$(\alpha :; c) \parallel d \sqsubseteq \alpha :; (c \parallel d) \tag{30}$$

$$(c_1 \sqcap c_2) \parallel d = (c_1 \parallel d) \sqcap (c_2 \parallel d)$$
 (31)

Law 27 states that sequential composition is always a refinement of parallelized sequential composition. Law 28 is the standard resolution of a choice to its left operand (a symmetric law holds for the right operand). Parallelized sequential composition is associative by Law 29, provided both instances are parameterised by the same model M. The interleaving semantics allows us to derive Law 30, a typical interleaving law, and Law 31 for distributing choice over parallel composition; these laws are important for reasoning about the effects of different instruction reorderings.

Now consider the case of two instructions in sequence.

$$\alpha \stackrel{\mathsf{M}}{\Leftarrow} \beta \Rightarrow \alpha \stackrel{\mathsf{M}}{;} \beta = \alpha :; \beta \tag{32}$$

$$\beta' \ll \alpha \stackrel{\mathrm{M}}{\ll} \beta \Longrightarrow \quad \alpha \stackrel{\mathrm{M}}{;} \beta \quad \sqsubseteq \quad \beta' .; \alpha \tag{33}$$

$$\beta' \ll \alpha \stackrel{M}{\ll} \beta \Longrightarrow \alpha \stackrel{M}{;} \beta = (\alpha .; \beta) \sqcap (\beta' .; \alpha)$$
 (34)

$$c_1 \stackrel{\text{\tiny M}}{;} \mathbf{fence} \stackrel{\text{\tiny M}}{;} c_2 = c_1 .; \mathbf{fence} .; c_2$$
 (35)

Law 32 states that if β cannot be reordered according to M then they are executed sequentially. Law 33 states that if reordering is allowed then that is one possible behaviour. Law 34 composes these two rules to reduce parallelized sequential composition to a choice over sequential compositions, eliminating the memory model. Similarly, a full fence restores order and hence sequential reasoning as in Law 35.

Monotonicity. Monotonicity (congruence) holds for the standard operators of IMP+pseq, but monotonicity of parallelized sequential composition contains a subtlety in that the allowed traces of $c_1 \stackrel{\text{\tiny M}}{;} c_2$ are dependent on the reorderings allowed by c_1 with respect to M (Rule (24)). To handle this we need a stronger notion of refinement, written $c \stackrel{\text{\tiny M}}{\sqsubseteq} c'$, where traces are augmented to track the reorderings allowed,⁴ allowing strengthening only.

Theorem 4.1.
$$c \stackrel{\text{M}}{:} d \sqsubseteq c' \stackrel{\text{M}'}{:} d'$$
 if $c \stackrel{\text{M}}{\sqsubseteq} c'$, $d \sqsubseteq d'$, and $M \sqsubseteq M'$.

Proof. By induction on traces: the requirement for the left argument is a consequence of (24); and strengthening of the memory model reduces the number of possible traces. \Box

5 Reasoning about IMP+pseq

So far we have considered trace-level properties; now we turn attention to state- and predicate-based reasoning. The

⁴Similarly to refusal sets in CSP's failures/divergences model [85].

action-trace semantics can be converted into a typical pairsof-states semantics straightforwardly.

eff
$$(x := e) = \{(\sigma, \sigma_{[x := e_{\sigma}]})\}$$
 (36)

$$eff(\langle e \rangle) = \{(\sigma, \sigma) \mid \sigma \in e\}$$
 $eff(barrier(f)) = id$ (37)

$$eff([]) = id$$
 $eff(a^t) = eff(a) \circ eff(t)$ (38)

$$\operatorname{eff}(c) = \bigcup \{\operatorname{eff}(t) \mid t \in \llbracket c \rrbracket \} \tag{39}$$

$$wp(c) \stackrel{\frown}{=} \lambda q. \{ \sigma \mid \forall \sigma' \bullet (\sigma, \sigma') \in eff(c) \Rightarrow \sigma' \in q \}$$
 (40)

$$\{p\}\ c\ \{q\}\ \widehat{=}\ p \Rightarrow wp(c)q$$
 (41)

Let the type Σ be the set of total mappings from variables to values, and let the effect function eff: $Instr \to \mathbb{P}(\Sigma \times \Sigma)$ return a relation on states given an instruction. We let 'id' be the identity relation on states, and given a Boolean expression e we write $\sigma \in e$ if e is True in state σ . The effect of actions is straightforward from (36) and (37), giving the trivial case eff(τ) = id. The relationship with standard Plotkin style operational semantics [80] is straightforward.

$$c \xrightarrow{\alpha} c' \land (\sigma, \sigma') \in \text{eff}(\alpha) \implies \langle c, \sigma \rangle \longrightarrow \langle c', \sigma' \rangle \quad (42)$$

The advantage of our approach is that syntax of the action α can be used to reason about allowed reorderings using (13, 24), whereas in general one cannot reconstruct the action from a pair of states. Mapping eff onto a trace t, map(eff, t), yields the sequence of relations corresponding to the set of sequences of pairs of states in a Plotkin-style trace. We can lift eff to traces by inductively composing such a sequence of relations (38), and we define the overall effect of a command by the union of the effect of its traces (39).

The predicate transformer for weakest precondition semantics is given in (40). A predicate is a set of states, so that given a command c and predicate q, wp(c)(q) returns the set of (pre) states σ where every post-state related to σ by eff(c) satisfies q (following, e.g., [35]). Given these definitions we can show the following.

Theorem 5.1. For Sequential M,
$$wp(c_1 \stackrel{\text{M}}{;} c_2) = wp(c_1 :; c_2)$$

Proof. By Definition 2.1, Theorem 2.2 and (40). □

We define Hoare logic judgements using weakest preconditions (41) (note that we deal only with partial correctness as we consider only finite traces). From these definitions we can derive the standard rules of weakest preconditions and Hoare logic for commands such as nondeterministic choice and sequential composition, but there are no general compositional rules for parallelized sequential composition.

$$\{q_{\lceil x \setminus e \rceil}\} x := e\{q\} \quad \{q \land e\} \ |e| \ \{q\} \quad \{q\} \ \text{ fence } \{q\} \quad (43)$$

$$\{p\}\ c_1: c_2\{q\} \Leftrightarrow \{p\}\ c_1\{r\} \land \{r\}\ c_2\{q\}$$
 (44)

$$\{p\}\ c_1 \sqcap c_2 \{q\} \Leftrightarrow \{p\}\ c_1 \{q\} \land \{p\}\ c_2 \{q\}$$
 (45)

$$\{p\}\ c_1 \stackrel{\text{\tiny M}}{:} \mathbf{fence} \stackrel{\text{\tiny M}}{:} c_2 \{q\} \Leftrightarrow \{p\}\ c_1 \{r\} \land \{r\}\ c_2 \{q\}$$
 (46)

Law 43 follows from (37) and (40), while Laws 44 and 45 are straightforward by definition. Law 46 is a key rule that

shows how, for any M where **fence** acts as a full fence, inserting a fence restores sequential reasoning in that a mid-point (predicate r) can be used for compositional reasoning.

Theorem 5.2. If
$$c \sqsubseteq c'$$
 then $eff(c') \subseteq eff(c)$, $wp(c) \subseteq wp(c')$, and $\{p\} \ c \ \{q\} \Rightarrow \{p\} \ c' \ \{q\}$

Proof. Straightforward from definitions. □

We use two key theorems to establish (or deny) properties of programs executing under weak memory models.

Theorem 5.3 (Verification).

(i) If
$$c = c'_{\langle SC \rangle}$$
 then $\{p\} c \{q\} \Leftrightarrow \{p\} c'_{\langle SC \rangle} \{q\}$
(ii) If $c \sqsubseteq c'$ and $\{p\} c' \{\neg q\}$ then $\neg \{p\} c \{q\}$

Proof. Straightforward from definition and Theorem 5.2. □

Theorem 5.3(i) is simply monotonicity of a Hoare triple, but we make the reduction to a sequential form explicit; once this has happened standard compositional rules from Hoare logic can be applied to establish a property of the original program. Theorem 5.3(ii) applies when a particular reordering of instructions in c (typically c' will be a sequence of instructions) contradicts some postcondition, from which we can determine that the original program does not establish that postcondition (for a given p). Hoare logic is used as the basis for reasoning about concurrent programs in the Owicki-Gries method [78], and so Theorem 5.3(i) enables the application of standard techniques for concurrent programs.

We now encode some well-known memory models in our framework and show how properties and behaviours can be derived from the base we have provided.

6 Total store order (TSO)

The "total store order" memory model (used in Intel, AMD and SPARC processors; a history of its development is given in [87]) maintains program order on stores but is relaxed in the sense that it allows loads to come before stores.

Model 6 (TSO). $\alpha \stackrel{\mathsf{TSO}}{\longleftarrow} \beta$ except, for $x \in \mathsf{Shared}, r \in \mathsf{Local},$

$$x := e \stackrel{\text{TSO}}{\longleftarrow} r := f \quad if \ x \notin \text{sv}(f) \ and \ r \notin \text{fv}(e)$$
 (47)

TSO allows loads to come before independent stores, and, due to forwarding, for dependent loads to "bypass" (recall (1) and (5)). That is, even though by **M6** we have $x:=1 \stackrel{\text{TSO}}{\longleftarrow} r:=x$, due to forwarding we have $r:=1 \, \stackrel{\text{TSO}}{\ll} r:=x$. Note that TsO allows independent register operations to also be reordered before stores. We define $\text{mfence} \, \widehat{=} \, \text{fence}$, which is x86-TSO's primary way to restore order.

⁵x86-TSO also has store and load fences, which we discuss in the context of later memory models, but these are effectively no-ops for TSO; however TSO's lfence blocks speculative execution [49].

The classic behaviours defining TSO as opposed to SC can be summarised by the equations below.

$$x := 1 \stackrel{\text{\tiny TSO}}{;} y := 1 = x := 1 .; y := 1$$
 (48)

$$x := 1 \stackrel{\text{\tiny TSO}}{;} r := x \sqsubseteq r := 1 .; x := 1$$
 (49)

$$x := 1$$
; $r := y = (x := 1 :; r := y) $\sqcap (r := y :; x := 1)$ (50)$

Stores are kept in program order by TsO (48) (an instance of Law 32). A load of x preceded by a store can use the stored value immediately (49) (an instance of Law 33); only later will the store become visible to the rest of the system – the classic *bypassing* behaviour. A load of y preceded by a store of x, for $x \neq y$, could be executed in either order (50). Perhaps the simplest system which can observe this behaviour is the classic "store buffer" (SB) test [10].

SB
$$\widehat{=}$$
 $x := 1 :: r_1 := y \parallel y := 1 :: r_2 := x$

First note that in a sequential system at least one register must read the value 1.

Theorem 6.1.
$$\{x = y = 0\}$$
 SB $\{\neg(r_1 = r_2 = 0)\}$.

Proof. Lahav and Vafeaidis [61] provide an Owicki-Gries proof, which we replicated using Isabelle/HOL [75]. \Box

However this behaviour is not ruled out under TSO.

Theorem 6.2.
$$\neg \{x = y = 0\} SB_{(TSO)} \{ \neg (r_1 = r_2 = 0) \}.$$

Proof. Abbreviate $c_1 = r_1 := y$.; x := 1 and $c_2 = r_2 := x$.; y := 1, and hence $SB_{\langle TSO \rangle} = c_1_{\langle TSO \rangle} \parallel c_2_{\langle TSO \rangle}$. Also let $\widehat{c_i}$ represent c_i with its instructions reordered.

$$SB_{\langle TSO \rangle} = c_{1\langle TSO \rangle} \parallel c_{2\langle TSO \rangle}$$

$$= (c_1 \sqcap \widehat{c_1}) \parallel (c_2 \sqcap \widehat{c_2}) \qquad By (50)$$

$$= (c_1 \parallel c_2) \sqcap (\widehat{c_1} \parallel c_2) \sqcap (c_1 \parallel \widehat{c_2}) \sqcap (\widehat{c_1} \parallel \widehat{c_2}) \qquad Law 31$$

We have reduced SB $_{\langle TSO \rangle}$ to four concurrent, sequential programs representing each possible combination of reorderings. By Law 45 we can complete the proof by showing any one of the four violates the postcondition; we already know that the first reordering does establish the pre/post condition by Theorem 6.1, however the other three all violate it, as we demonstrate below for the fourth case.

$$c_1 \parallel c_2 = r_1 := y :; x := 1 \parallel r_2 := x :; y := 1$$
 Def.
 $\sqsubseteq r_1 := y :; r_2 := x :; x := 1 :; y := 1$ Law 30 Hoare logic (Laws 43 and 44), gives the following.

$${x = y = 0} r_1 := y :; r_2 := x :; x := 1 :; y := 1 {r_1 = r_2 = 0}$$

The proof is completed by Theorem 5.3(ii) – a possible reordering and interleaving contradicts the postcondition. \Box

To reinstate sequential behaviour under TSO, fences can be inserted in both branches.

Theorem 6.3. Let SB^{+mfence} be SB with fences inserted into each branch; then $\{x = y = 0\}$ SB^{+mfence} $\{\neg(r_1 = r_2 = 0)\}$

Proof. By **M6**, Law 46 and the reasoning of Theorem 6.1. □

Note that reasoning is relatively direct in this framework: we can use properties of the model and the structure of the program to reduce reasoning to sequential cases where established techniques can be applied (Theorem 6.3), or a partcular case that violates a desired property can be enumerated (Theorem 6.2). Other reasoning frameworks typically monitor reorderings with respect to global abstract (graph) data structures, requiring custom assertion languages and judgements.

6.1 Equivalence to an explicit store buffer model

One of the best-known formalisations of a weak memory model is the operational model of x86-TSO [77, 87]. In that model the code is executed sequentially, but interacts with a store buffer that temporarily holds stores before sending them to the storage system, allowing loads that occur in the meantime to use values found in the buffer. Below we give an extension of IMP+pseq to add an explicit store buffer s, written (**buf** s • c), following the semantics in [77].

$$c \xrightarrow{x := v} c' \Rightarrow (\mathbf{buf} \ \mathbf{s} \bullet c) \xrightarrow{\tau} (\mathbf{buf} \ \mathbf{s} ^{\frown}(x, v) \bullet c')$$
 (51)

$$(\mathbf{buf}\ (x, v) \widehat{\ } \mathbf{s} \bullet c) \xrightarrow{x := v} (\mathbf{buf}\ \mathbf{s} \bullet c) \ (52)$$

$$c \xrightarrow{\text{mfence}} c' \Rightarrow (\mathbf{buf} [] \bullet c) \xrightarrow{\text{mfence}} (\mathbf{buf} [] \bullet c')$$
 (53)

$$c \xrightarrow{\tau} c' \Rightarrow (\mathbf{buf} \ \mathbf{s} \bullet c) \xrightarrow{\tau} (\mathbf{buf} \ \mathbf{s} \bullet c')$$
 (54)

$$c \xrightarrow{r := x} c' \land \mathtt{s} = \mathtt{s}_1 \widehat{} (x, v) \widehat{} \mathtt{s}_2 \land x \notin \mathtt{s}_2 \Rightarrow$$

$$(\mathbf{buf} \ \mathbf{s} \bullet c) \xrightarrow{r := v} (\mathbf{buf} \ \mathbf{s} \bullet c') \tag{55}$$

$$c \xrightarrow{r:=x} c' \land x \notin s \Rightarrow$$

$$(\mathbf{buf} \, \mathbf{s} \bullet c) \xrightarrow{r := x} (\mathbf{buf} \, \mathbf{s} \bullet c') \tag{56}$$

A store is a variable/value pair, (x, v), and $x \notin s$ means there is no store to x in s. In all rules c is executed using the sequential fragment of the semantics only, and we assume $x \in S$ hared and $r \in L$ ocal. If c issues a store, it is placed at the end of the store buffer (the system sees only a silent (τ) step) (51). The first store in the buffer can be flushed to the system at any time (52). A fence can only proceed when the buffer is empty (53), while internal steps of c can proceed independently of the state of the buffer (54). The interesting rules are for loads: if c issues a load c is c then this can be serviced by the buffer using the most recent value for c (say c) resulting in a step c:c, and no interaction with the global system (55). If c issues a load of c that is not in the buffer then the load is promoted to the system level (56).

Theorem 6.4. For any command c, issuing only assembler-level instructions (stores, loads, fences and register-only operations), (buf $[] \bullet c) = (\mathbf{pline}_{M} [] : c_{\langle SC \rangle})$

⁶We give a per-process buffer, whereas [77] uses a single global buffer, with each write in the buffer tagged by the originating process's id.

Theorem 6.5. For any command c, issuing only assembler-level instructions, (**buf** [] \bullet c) = $c_{(TSO)}$

Proof. By Theorem 6.4 and Theorem 3.1. □

That is, the semantics of parallelized sequential composition instantiated with reordering (and forwarding) given by Tso gives precisely those behaviours obtained by sequential execution with an (initially empty) store buffer.

7 Release consistency

The release consistency memory model [43] has been highly influential, having been implemented in the Dash processor [65], guided the development of the C language memory model [25], and the concepts incorporated into ARM [81] and RISC-V [84]. The key concept revolves around release writes and acquire loads: a release write is stereotypically used to set a flag to indicate a block of computation has ended, and and an acquire load is correspondingly used to observe a release write. Code before the release should happen before, and code after the acquire should happen after; conceptually these are weaker (one-way) fences. Release consistency's motivation was finding an easy-to-implement mechanism for interprocess communication that is feasible and inexpensive computationally, and relatively straightforward for programmers.

We extend the action syntax of IMP+pseq to include *ordering constraints* (oc) as annotations to any action, though as noted above release store and acquire load are the most commonly used.

oc ::= rel | acq
$$\alpha$$
 ::= ... | α oc (57)

$$(\beta^{\text{oc}})_{\alpha\alpha} = (\beta_{\alpha\alpha})^{\text{oc}} \qquad \beta_{\alpha(\alpha^{\text{oc}})} = \beta_{\alpha\alpha}$$
 (58)

Forwarding for the new annotated actions is defined inductively so that the base actions take effect and ignore the annotations (58); and we define $eff(\alpha^{oc}) = eff(\alpha)$.

Following [43] we distinguish two models, RC_{pc} (where pc stands for "processor consistency") and RC_{sc} (where sc stands for "sequential consistency"), the latter of which is a strengthening of the former; an alternative would be to distinguish pc/sc in the annotations themselves, allowing

mixing of the two types in one model (cf. ARM's ldar/ldapr instructions). For simplicity we assume that G (M4) controls reordering outside of annotation considerations, although in the theory of [43] stronger constraints are possible.

Model 7 (RC_{pc}). $\alpha \stackrel{\text{RC}_{pc}}{\longleftarrow} \beta$ iff $\alpha \stackrel{\text{G}}{\longleftarrow} \beta$ except

$$\alpha \stackrel{\text{RC}_{pc}}{\longleftarrow} \beta^{\text{REL}} \stackrel{\text{RC}_{pc}}{\longleftarrow} \gamma \quad iff \beta \stackrel{\text{RC}_{pc}}{\longleftarrow} \gamma$$
 (59)

$$\alpha \stackrel{\text{RC}_{pc}}{\longleftarrow} \beta^{\text{ACQ}} \stackrel{\text{RC}_{pc}}{\longleftarrow} \gamma \quad iff \alpha \stackrel{\text{RC}_{pc}}{\longleftarrow} \beta$$
 (60)

Model 8 (RC_{sc}).
$$\alpha \stackrel{\text{RC}_{sc}}{\rightleftharpoons} \beta$$
 iff $\alpha \stackrel{\text{RC}_{pc}}{\rightleftharpoons} \beta$ except $\alpha^{\text{REL}} \stackrel{\text{RC}_{sc}}{\rightleftharpoons} \beta^{\text{ACQ}}$.

 RC_{pc} straightforwardly follows the intuition of [43], where a release action β^{REL} is always blocked from reordering and hence all earlier instructions must be complete before it can execute, but it does not block later instructions from happening early (59) (provided β does not on its own block later instructions, calculated by recursively applying the reordering relation). An acquire action is the converse (60). RC_{sc} strengthens RC_{pc} by additionally requiring order between release and acquire actions in the one thread (the reverse direction is already implied). Consider the behaviour of the classic "message passing" pattern (MP).

$$MP = x := 1 :; y := 1 \quad || \quad r_1 := y :; r_2 := x$$
 (61)

Theorem 7.1.
$$\{x = y = 0\} \text{ MP } \{r_1 = 1 \Rightarrow r_2 = 1\}$$

Proof. Straightforward by Owicki-Gries reasoning: the stores are executed in the order x, y, and read in reverse order, hence if the latter is observed the former must have taken effect. \square

Consider using the weaker RC_{pc} model with annotations.

$$\mathsf{MP}^+ \ \widehat{=} \ x := 1 \stackrel{\mathsf{RC}_{pc}}{;} (y := 1)^{\mathsf{REL}} \ \| \ (r_1 := y)^{\mathsf{ACQ}} \stackrel{\mathsf{RC}_{pc}}{;} r_2 := x$$

Here the release annotation on the write to y means that y acts as a flag that x has been written, and so if the other process sees the modification to y via an acquire it must also see the write to x.

Theorem 7.2.
$$\{x = y = 0\} \text{ MP}^+ \{r_1 = 1 \Rightarrow r_2 = 1\}$$

Proof. Using the definition of MP+,

$$x := 1$$
; $(y := 1)^{\text{REL}}$ || $(r_1 := y)^{\text{ACQ}}$; $r_2 := x$
 $x := 1$; $(y := 1)^{\text{REL}}$ || $(r_1 := y)^{\text{ACQ}}$; $r_2 := x$

The equality holds by applying Law 32 in each process from (59) and (60). Now the proof follows using the same reasoning as Theorem 7.1 (annotations have no effect on sequential semantics, only reorderings). \Box

Note that without the annotations the instructions in each process could be reordered according to **M**4, under which conditions it is straightforward to find a behaviour that contradicts $r_1 = 1 \Rightarrow r_2 = 1$.

ARM version 8

In this section we consider the latest version of ARM v8, which is simpler than earlier versions due to it being "multicopy atomic" [81]. ARM's instruction set has artificial barriers including a "control fence" isb $\hat{=}$ barrier(ctrl), a write barrier dsb.st $\hat{=}$ barrier(ww), and a full fence dsb $\hat{=}$ fence.

$$|b| \stackrel{\text{ARM}}{\longleftarrow} \text{isb} \stackrel{\text{ARM}}{\longleftarrow} \alpha \qquad if \text{ isLoad}(\alpha) \qquad (63)$$

$$|b| \stackrel{And}{\longleftarrow} \alpha \qquad if \text{ isStore}(\alpha) \qquad (64)$$

(62)

Store fences maintain order between stores (62) (recall (6)), while control fences are blocked by branches and correspondingly block loads (63) (recall (7)); when taken in conjunction a control fence enforces order between loads within and before a branch, preventing the observable effects of speculative execution. Branches block stores, including independent stores (64); this is a practical consideration to do with speculating down branches: one cannot commit stores until it is known that the branch will be taken. Other than these exceptions, ARM behaves as RCsc for release/acquire annotations,⁷ fundamentally behaving as G (M4).

As an example of the weak nature of ARM, i.e., issuing loads before the branch condition for the load is evaluated, consider the following behaviour of a variant of the reader process of MP (61), where the second load is guarded. Define $MP_w \stackrel{\frown}{=} x:=1.; y:=1 \text{ and } MP_r \stackrel{\frown}{=} r_1:=y \stackrel{\text{ARM}}{;} (\text{if } r_1=1 \text{ then } r_2:=x),$ where for brevity we leave the ARM parameter implicit on conditionals.

Theorem 8.1.
$$\neg \{x = y = 0\} \text{ MP}_w \parallel \text{MP}_r \{r_1 = 1 \Rightarrow r_2 = 1\}$$

Proof. Consider the following behaviour of MP_r .

$$\begin{array}{lll} \mathsf{MP}_{r} \, \widehat{=} & r_{1} := y \stackrel{\mathsf{ARM}}{;} \; (\mathbf{if} \; r_{1} = 1 \; \mathbf{then} \; \underline{r_{2} := x}) \\ & \sqsubseteq & r_{1} := y \stackrel{\mathsf{ARM}}{;} \; (r_{1} = 1) \stackrel{\mathsf{ARM}}{;} \; \underline{r_{2} := x} & (16), \, \mathrm{Law} \; 28 \\ & \sqsubseteq & r_{1} := y \stackrel{\mathsf{ARM}}{;} \; \underline{r_{2} := x} \; .; \; (r_{1} = 1) & \, \mathrm{Law} \; 33 \; \mathrm{by} \; \mathbf{M4} \\ & \sqsubseteq & \underline{r_{2} := x} \; .; \; r_{1} := y \; .; \; (r_{1} = 1) & \, \mathrm{Law} \; 33 \; \mathrm{by} \; \mathbf{M4} \end{array}$$

The load of *x* (underlined) may be reordered before the branch point, and subsequently before the load of y. Even with the stores to x and y being strictly ordered in MP_w we can interleave this ordering so that the postcondition is invalidated, and complete the proof by Theorem 5.3(ii). □

Hence under ARM conditionals do not guarantee sequential order. Placing an isb instruction inside the branch, before the second load, however, prevents this behaviour. Define $MP_{isb} = r_1 := y$; (if $r_1 = 1$ then isb; $r_2 := x$).

Theorem 8.2.
$$\{x = y = 0\} \text{ MP}_{w} \parallel \text{ MP}_{isb} \{r_1 = 1 \Rightarrow r_2 = 1\}$$

Proof. Consider the following behaviour of MP_{isb}.

$$r_1 := y$$
; (**if** $r_1 = 1$ **then** isb ; $r_2 := x$)
$$\sqsubseteq r_1 := y$$
; ($r_1 = 1$) $r_2 := x$; ($r_2 := x$) $r_3 := x$; ($r_1 := x$); ($r_1 := x$); ($r_2 := x$) $r_3 := x$; ($r_3 := x$) Law 32 by (63)
The loads are strictly ordered and so the proof is completed straightforwardly using OG reasoning. \square

Conformance. We validate our model using litmus tests [15, 26, 68, 69, 73, 86]. ARM has released an official axiomatic model using the herd tool [16] available online via the herdtools7 application [34] (see [18], Sect. B2.3). Using the diy7 tool and the official model [12] we generated a set of 99,881 litmus tests covering forbidden behaviours of up to 4 processes using the instruction types covered in M9. In addition we used a further 5757 litmus tests covering allowed and forbidden behaviours using the tests for an earlier version of ARM [16] and a set covering more recent features [72]. We ran these tests using the model checking tool based on the pipeline semantics in Sect. 3. In each case (approximately 105,000 tests) **M9** agreed with the published model.

8.1 An axiomatic specification

Perhaps the best known way of describing memory models is via axioms over global traces. Below we give an axiomatic model using a straightforward translation of the reordering relationship **M9**. We refer to this model as ax_{ro} .

```
let ARM = [W]; po; [dsb.st]; po; [W] | ctrl; [isb] |
            [isb];po;[R] | ctrl;[W] | po;[dsb];po
    let RC = [A]; po | po; [L] | [L]; po; [A]
let rec ob = ARM | RC | data | data;rfi |
            rfe | fre | co | ob;ob
acyclic po-loc | fr | co | rf as internal
irreflexive ob as external
```

An axiomatic specification is formed from relations over event traces, typically with acyclic or irreflexive constraints on the defined relations. Union is represented by '|' and relational composition by ';'. The ARM relation is essentially a straight translation from M9, along with the fence constraint from M4. For instance, the po relation relates instructions in textual program order, and dsb is the set of dsb instructions in the program, with the square brackets denoting the identity relation on that set. Hence the constraint "po; [dsb]; po" (the last in ARM) states a requirement that instructions before and after a fence must appear in that order in any trace. The remaining constraints in ARM are similarly translated, noting W and R are the store (write) and load (read) instructions, and ctrl relates instructions before and after a branch point. The RC relation captures release/acquire constraints ([L]/[A]) from M7/M8. The ob relation (observation) is recursively defined to include data dependencies, including forwarding (via rfi, "reads-from internal"), corresponding to M3, and the "reads-from" and "from-reads" relations, relating loads to corresponding and earlier stores, and the global

⁷As mentioned in Sect. 7, ARM's LDAPR explicitly weakens the ordering between release/acquire instructions, which can be handled by distinguishing annotations syntactically rather than within the memory model definition.

coherence order (co) on stores. Note that these relations arise directly from our small step operational semantics. The definition of ob and the acyclic and irreflexive constraints, which govern internal (local) and external (global) views of the system, are based on the pattern of [34, 81] see [16] for more details on axiomatic specifications.

The ax_{ro} model (available in the supplementary material) agrees with the official model [34] on all 100,000+ litmus tests using herd7. Following the lead of [81] we give a byhand proof that the traces of the axiomatic model in Sect. 8.1 are the same as the traces obtained by application of the operational semantics.

Theorem 8.3. The traces of a program c allowed by ax_{ro} are exactly the traces of (**pline**_M []: c).

Proof. Consider a trace t of (**pline**_M []: c). This trace must be obtained by some original sequential trace t' of c, fetched into the pipeline via (12), and then reordered by successive applications of (13). Without loss of generality consider the case where t' is fetched into the pipeline in its entirety before any commits, and is nontrivial, i.e., contains two or more actions. Then the pipeline is exactly t' and of the form $t_1 \cap \alpha \cap t_2 \cap \beta \cap t_3$, with α occurring earlier than β in program order in c. If α and β are related by ARM or RC then they must appear in order in any axiomatic trace of ax_{ro} ; and also they cannot be reordered using (13) (commit), which follows from the straightforward relationship between ARM & RC and M9 & M8, respectively. Forwarding is covered by the internal /external division in axiomatic models: the internal (local) constraints are more strict, meaning locally sequential semantics is maintained, but externally (globally) actions may appear to occur out of order. The fundamental constraints of M3 and M4 are captured by data and po-loc, with full fences captured by po; [dsb]; po. The acyclic and irreflexive constraints are implicit in an operational semantics - a trace is always strictly ordered, and in particular loads can only access previous stores, it is not possible to access "future" stores. Hence the rf, fr and co constraints are implicitly enforced – these govern the interaction between loads and stores in a trace. In summary, the pointwise description of ARM translates straightforwardly to axioms over traces, where the program order (po) relation captures the intervening actions. □

RISC-V

The RISC-V memory model [19, 84] is influenced by ARM's weak ordering on loads and stores (corresponding to G), but has release consistency annotations using the weaker RCpc (M7) rather than the stronger RC_{sc} (M8). It also defines six different types of artificial barriers (more are technically possible but their use is not recommended [19]): a full fence given by fence rw, rw = fence; a store fence given by fence w, w = proach [70, 91, 98], perhaps best exemplified by Alglave et al. **barrier**(ww) (identical to ARM's dsb.st); a corresponding

described below; and a barrier used to mimic TSO's in-built weakening where loads can come before stores, which we define as fence.tso $\widehat{=}$ fence r, rw $\stackrel{\text{\tiny RISC-V}}{;}$ fence rw, w. Additionally RISC-V has a barrier fence.i which has a technical specification beyond what is considered here, and so it is defined as a no-op (τ) .

Model 10 (RISC-V).
$$\alpha \stackrel{\text{RISC-V}}{\longleftarrow} \beta$$
 iff $\alpha \stackrel{\text{RC}_{pc}}{\longleftarrow} \beta$ except
$$\alpha \stackrel{\text{ARM}}{\longleftarrow} \text{fence r, r} \stackrel{\text{ARM}}{\longleftarrow} \alpha \qquad \text{iff isLoad}(\alpha) \quad (65)$$

$$\alpha \stackrel{\text{RISC-V}}{\longleftarrow} \text{fence rw, w} \stackrel{\text{RISC-V}}{\longleftarrow} \beta \quad \text{iff isLoad}(\beta) \quad (66)$$

$$\alpha \stackrel{\text{RISC-V}}{\longleftarrow} \text{fence r, rw} \stackrel{\text{RISC-V}}{\longleftarrow} \beta \quad \text{iff isStore}(\alpha) \quad (67)$$

$$(b) \stackrel{\text{RISC-V}}{\longleftarrow} \alpha \qquad \text{iff isStore}(\alpha) \quad (68)$$

RISC-V's load fence, fence r, r, restricts ordering with loads (65), and is is the straightforward dual of ARM's store fence (dsb.st, (62)). RISC-V's fence rw, w barrier is intended to maintain order between loads and stores and later stores only, allowing later loads to potentially come earlier; it therefore allows reordering of loads, but blocks everything else (66). Similarly the fence r, rw barrier ensures order between loads and later loads and stores, and hence can 'jump' over stores but is blocked by loads (67), which therefore are strictly ordered with later loads and stores. Like ARM, RISC-V prevents stores from taking effect before branches are resolved (68) (see [84] [Rule 11, A.3.8]).

Conformance. We tested our model against the litmus tests outlined in the RISC-V manual [84] and made available online with expected results [40]. Restricting attention to those tests involving instructions we consider in M10 (and M7) our tests agree with the official model in all 3937 cases, covering the RCpc behaviours and the six barrier types defined above, with M4 controlling interactions between stores and loads.

Related work 10

There has been significant work in defining the semantics of processor-level instruction reordering since the 1980s [37, 62, 88] and more recently under the umbrella of weak memory models [6, 22, 24, 27, 28, 32, 36, 48, 50, 55, 60, 83]. To the best of our knowledge we are the first to encode the basis for instruction reordering as a parameter to the language, rather than as a parameter to the semantics. This has allowed us to describe relevant properties and relationships at the program level, based on per-process properties about how individual cores manage their pipeline, and supporting program-structure-based reasoning techniques. In the literature weak memory model specifications are typically described with respect to properties of the global system. The most well-used framework in this style is the axiomatic ap-[16], in which many of the behaviours of diverse processors

load fence fence r, r; two new types fence rw, w and fence r, rw such as ARM, IBM's POWER, and Intel's x86 are described,

and common properties elucidated, and whose approach we compared with in Sect. 8.1. Another common approach to formalisation is with a semantics that is closer to the behaviour of a real microarchitecture, e.g., [39, 81, 86] (we gave a direct semantic comparison to the operational model of [77, 87] in Sect. 6). In both the axiomatic and the concrete style it is more difficult to derive abstract properties and to reason about a particular system over the structure of the program, however both give rise to efficient tools for model checking [1–5, 21, 23, 57, 58].

The Promising semantics [54, 64, 82] is operational and can be instantiated with different memory models (including software memory models), and a proof framework has been developed for reasoning about programs. Weak behaviours are governed by abstract global data structures that maintain a partial order on events, and hence the semantics is defined and reasoning is performed with respect to these global data structures.

This paper supersedes [30], which defines only a simple prefixing command for actions (a special case of parallelized sequential composition). That paper does not consider a general theory for memory models (Sect. 2), nor consider pipelines, and does not address TSO, Release Consistency, or RISC-V (but does consider POWER), and showed conformance for ARM against an older version without release/acquire atomics, against a much smaller set of litmus tests (approximately 400 vs over 100,000 in this paper). That theory is not machine-checked, contains only a few simple refinement rules, and does not employ Owicki-Gries reasoning.

The "PipeCheck" framework of Lustig, Martonosi et al. [67, 71, 95, 96] is designed to validate that processors faithfully implement their intended memory model, using a detailed pipeline semantics based on an axiomatic specification. Given that our approach has an underlying link to the behaviour of pipelines it may be possible to extend our framework so that it can make use of those existing tools for processor validation.

Our operational approach based on out-of-order instruction execution follows work such as Arvind et al. [20, 99, 102], and the development of the Release Consistency and related models [7, 9, 10, 42, 43, 101]. The algebraic approach we adopt to reducing programs is similar in style to the Concurrent Kleene Algebra [47], where sequential and parallel composition contribute to the event ordering.

11 Conclusion

In this paper we have formalised instruction-level parallelism (ILP), a feature of processors since the 1960s, and a major factor in the weak behaviours associated with modern memory consistency models. We showed how modern memory models build on generic properties of instruction reordering with respect to preservation of sequential semantics, calculated pointwise on instructions. We gave a straightforward

abstract semantics of a pipeline, lifting pointwise comparison to sequences of instructions. We also lifted the comparison to the command level, and hence defined a program operator (parallelized sequential composition) which is behaviourally equivalent to using a pipeline, but supports compositional reasoning about behaviours over the structure of parallel processes. We empirically validated the models for large sets of litmus tests for ARM and RISC, showed that the reordering semantics for TSO is equivalent to the established store buffer semantics, and showed how sterotypical results emerge across a range of models, for instance, the store buffer pattern of TSO where loads can come before stores, the message passing paradigm from release consistency using release/acquire flags to control interprocess communication, and load speculation from ARM. We provide in the supplementary material a model checker based on the pipeline semantics in Maude [29, 97] and encoded and machine-checked the theory for the IMP+pseq language in Isabelle [76, 79].

The reasoning style in this framework is more direct than many in the literature, in that the nondeterminism due to ILP can be made explicit in the structure of the program, and either shown to have no effect on desired properties, or a specific trace that contradicts a desired property can be elucidated. In the literature reasoning about memory models is often with respect to orderings over global event traces, rather than per-process reorderings. Our approach, e.g., to prepare for the application of the Owicki-Gries method, appears to be simpler than techniques that incorporate memory model constraints directly [13, 33, 61]. Furthermore, we could have instead chosen to apply rely/guarantee reasoning [51, 52] once the programs were reduced to concurrent sequential processes. The reduction of commands involving parallelized sequential composition to a sequential form (e.g., Laws 34 and 35) might be infeasible for large programs with few memory barriers, but such programs are not typically where one is concerned with memory models: more commonly memory models apply to library data structures and low-level applications where shared-variable communication is tightly controlled [53, 63]. An advantage of our language-level encoding is that other program properties can be tackled in a familiar setting and at the program level, for instance, information flow logic for security or progress properties [31, 89], making use of existing frameworks di-

As future work we intend to extend the semantics to cover other features of modern processors that contribute to their memory models, for instance, POWER's cache system that lacks multicopy atomicity, TSO's global locks, and ARM's global monitor for controlling load-linked/store-conditional instructions. As these features are global they cannot be captured directly as behaviours of per-processor pipelines. A

proof technique for this extended framework will incorporate features from existing work, perhaps as a hybrid separating local reordering from global behaviours [14, 54]. Our relatively simple semantics for the pipeline contains only two stages, fetch and commit, neglecting in particular *retirement*; this could be crucial to include in security vulnerability analysis; for instance, it is the retirement of loads where invalid memory accesses are detected, and this in association with early load speculation leads to the Meltdown vulnerability [66, 94].

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