HENGYANG ZHAO

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Department of Electrical and Computer Engineering, University of California, Riverside
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EDUCATION

University of California, Riverside *September 2014 – present*
Ph.D. Candidate, in Electrical and Computer Engineering
Advisor: Dr. Sheldon X.-D. Tan

Shanghai Jiao Tong University *September 2007 – March 2014*
M.S., in Instrument and Meter Engineering
B.S., in Computer Science

PROFESSIONAL SKILLS HIGHLIGHT

Programming language Solid skills in C/C++ and Python.

Tools/Platforms Solid skills and rich project experiences in scripting/automation/batch in Bash and/or Python; experienced in GNU core utilities, GNU sed, Vim, Git and Linux server (Fedora) management and virtualization.

EXPERIENCE

Learning Based Electrical Vehicle Power Modeling February 2016 – present
Research Assistant *UC Riverside, Collaboration with KAIST*

· Electrical vehicle power modeling based on feed-forward neural network.
· Neural network input preprocessing based on simple physical knowledge.

Research on Smart Building Energy Reduction with Special Focus on Learning-Based Techniques March 2015 – present
Research Assistant *UC Riverside*

· Recurrent neural network based approximate thermal modeling in smart building applications.
· People occupancy estimation based on analysis of sensor output.
· Sensor outlier/offset/fault detection using learning and probabilistic techniques.

Research on GPU-Based Matrix LU Factorization (Direct Approach) for Circuit Simulation September 2014 – Feburary 2015
Research Assistant *UC Riverside*

· Development of a fine grained parallel approach of GPU-based matrix LU factorization algorithm.
· Design Automation Conference 2015 Poster Session (Richard Newton Young Fellowship Program).

Internship at Intel Inc. July 2013 - August 2014
Software Engineer *Shanghai*

- Developed tool for automatically testing/profiling run-time data on a mobile operating system∗. (hidden product name: "∗")
- Developed an auxiliary tool to inspect the migration of the relationship between browser∗ thread and the corresponding CPU* core's∗ status within an interested duration.

FPGA Based Capsule Endoscopy February 2012 - March 2014
FPGA/Verilog Developer *SJTU*

- Participated in the design of wireless capsule endoscopy, including an FPGA-based swallow-able electronic capsule, a wireless data receiver and PC software.
- Implemented Verilog algorithm of color image baseline JPEG on the capsule-end Xilinx FPGA.
- Worked on the digital communication between the capsule endoscopy and the data receiver.

Data Management System
at Sayes Medical Technology Co., LTD September 2012 – January 2013
Team Leader *Shiyuan Inc., Shanghai*

- Developed a data management system for managing, browsing, processing and backing up the gastrointestinal data of PH, pressure and temperature records captured by electronic capsules.
- The management system was based on the server-client model, with one centralized Microsoft SQL Server database and multiple PC clients.

Internship at Cisco Systems Inc. December 2011 – June 2012
Testing Engineer *Shanghai*

- Participated in the automatic sanity test and duration test of Cisco phone models . The actual testing work was to use Tcl script to setup test servers for automatically testing a large amount of phones.
- Maintained two Linux testing servers and resident guest virtual machines.
- Developed and maintained auxiliary scripts/tools to help debugging the testing scripts in Tcl/Tk.

Implantable Physiological Parameters Detector December 2010 – June 2011
Hardware & Software Designer *SJTU*

- The animal physiological parameters detector system consists of a miniature implantable detector for measuring and transmitting ECG and blood pressure and body temperature information, and a hand-held wireless receiver.
- Designed and implemented the wireless receiver, supporting real-time ECG plotting, SD card storage and USB communication.
- Won the 3rd prize of outstanding graduation design in Dept. of Computer Science & Engineering, SJTU.

Undergraduate Innovation Project October 2009 – September 2010
Team Leader *Shanghai*

· Designed an LED based, distributed intellectual lighting system. This system was a distributed network of independent lighting nodes with passive infrared sensors. Nodes negotiate and optimize the overall power consumption according to their different lighting demands acquired from the infrared sensors.
· Designed an 100W current-controlled, bulk-type switching power supply.
· This project was sponsored CNY 10000 by Shanghai government.

IEEE Standard Micromouse Contest October 2009
Team Leader *Shanghai*

· Designed an micromouse, equipping one ARM Cortex-M3 micro controller, five infrared sensors and two stepper motors.
· The micromouse was placed in and was supposed to solve a IEEE standard 16 by 16 sized maze. Our team won the 2nd prize in the contest of Yangtze River delta division.

PUBLICATIONS

1. **Hengyang Zhao**, Zhongdong Qi, Shujuan Wang, Kambiz Vafai, Hai Wang, Haibao Chen, and Sheldon X.-D. Tan "Learning-Based Occupancy Behavior Detection for Smart Buildings." International Symposium on Circuits and Systems ('16 Invited, Accepted)

2. Wandi Liu, Hai Wang, **Hengyang Zhao**, Shujuan Wang, Haibao Chen, Yuzhuo Fu , Jian Ma , Xin Li , Sheldon X.-D. Tan "Thermal Modeling for Energy-Efficient Smart Building With Advanced Overfitting Mitigation Technique." Asia and South Pacific Design Automation Conference, pp. 417-422.

3. **Zhao, Hengyang**, Daniel Quach, Shujuan Wang, Hai Wang, Haibao Chen, Xin Li, and Sheldon X-D. Tan. "Learning Based Compact Thermal Modeling for Energy-Efficient Smart Building Management." In Proceedings of the IEEE/ACM International Conference on Computer-Aided Design, pp. 450-456. IEEE Press, 2015

4. He, Kai, Sheldon X.-D. Tan, **Hengyang Zhao**, Xue-Xin Liu, Hai Wang, and Guoyong Shi. "Parallel GMRES solver for fast analysis of large linear dynamic systems on GPU platforms." Integration, the VLSI Journal 52 (2016): 10-22.