**Modelsim Simulation**

You can use ModelSim either on Linux.

1. Use Linux based ModelSim available on ECE machines ( e.g. ece001.ece.cmu.edu )

1) Change to bash

-bash

2) Setting up the path and the related environment for ModelSim

-source /afs/ece/class/ece667/f2013/setup.sh

3) Creating work directory

‐vlib work

4) Compiling

‐vlog \*.v

5) Simulating

‐vsim display& (display is the top‐level module name)

‐Simulate ‐> Run ‐> Run –All (runs simulation)

‐Simulate ‐> Break (stops simulation)

6) Debugging with waveforms

‐View ‐> Wave (opens up wave form window)

‐View ‐> Structure/Signals (opens signals to drag into wave form window)

For more info on Modelsim, check the below link:

<http://www.ece.cmu.edu/~jhoe/doku/doku.php?id=a_short_intro_to_modelsim_verilog_simulator>

**FPGA Synthesis/Download Procedures**

Hardware Specifications:

The main board (FPGA board): The Altera® DE2-115 Development and Education board was designed by professors, for professors. It is an ideal vehicle for learning about digital logic, computer organization, and FPGAs. Featuring an Altera Cyclone® IV 4CE115 FPGA, the DE2-115 board is designed for university and college laboratory use.

The procedures are specified in the file “Hardware Design Flow Using Verilog in Quartus II”.