Addis Ababa University
Addis Ababa Institute of Technology
Center of Information Technology and Scientific Computing
FPGA Programming
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Assignment No 01
Total Mark: 10%
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Individual Assignment -I for Extension only

1. Simplify the following expression by means of Boolean algebra

$$F = \overline{A}\,\overline{B}\,\overline{C}D + A\overline{B}\,\overline{C}\,\overline{D} + \overline{A}B\overline{C}D + AB\overline{C}D + \overline{A}BCD + ABCD + \overline{A}\,\overline{B}C\overline{D} + A\overline{B}C\overline{D}$$

2. Design a majority voting machine with three inputs A,B,C and one output F. F=1 when at least two of the inputs are equal to 1 and F=0 when the majority of the inputs are equal to 0.
   a) Drive the truth table for the voting machine.
   b) Use Boolean algebra to derive the simplified expression from the canonical SOP form
   c) Draw the logic circuit for the simplified Boolean expression using only AND, OR , and NOT gates.
   d) Draw the logic circuit for the simplified Boolean expression using only NAND gates.
3. Design a 2-bit counter controlled by an input w. when w=0, it acts as a down-counter. When w=1, it acts as an up-counter. The output shows the current value of counter.
   a) Draw the state diagram for this counter.
   b) Derive the state-assigned table for this counter. Each state and output should be encoded with binary numbers.
   c) Derive the minimal logic expressions for Y_1,Y_0,z_1, and z_0.
   d) Draw the complete circuit diagram using D flip-flops and any additional logic gates that are required

Individual Assignment -I for Section One only

1. Simplify the following Boolean function in sum-of-products and product-of sums by means of a four-variable map. Draw the logic diagram with (a) AND-OR gates; (b) NAND gates.

$$F(w,x,y,z) = \sum(2,3,4,5,6,7,11,14,15)$$

2. Design a sequential circuit with two JK flip flops A and B and two inputs E and X. If E = 0 , the circuit remains in the same state regardless of the value of x. When E =1 and X =1 the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeat. When E =1

and X =0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeat.

3. A counter has a special counting sequence: 0,5,7,1,0,5,7,1, and so on. Design this counter with minimal number of states.
    a) Draw a state diagram for the counter
    b) Construct a state-assigned table including the next state and output
    c) Draw the circuit diagram for the counter using D flip-flops
    d) Repeat (c) using T flip-flops
    e) Repeat (c) using JK flip-flops

Individual Assignment -I for Section Two only

1. Implement the following functions using only NOR gates:

    a) $F = (A + B)(\overline{A} + \overline{B})$

    b) $F = A(B + C)(\overline{D} + E)$

2. A sequential circuit has two inputs, w1 and w2, and an output, z. Its function is to compare the input sequences on the two inputs. If w1 = w2 during any four consecutive clock cycles,the circuit produces z = 1; otherwise, z = 0. For example

    w1 : 0110111000110

    w2 : 1110101000111

    z : 0000100001110

    Derive a suitable circuit.

3. Derive a minimal state table and a suitable circuit for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Overlapping sequences should be detected.

Individual Assignment -I for Section Three only

1. Plot the following function on K map and use the K map to simplify the expression

$$F = ABC + \overline{A}BC + A\overline{B}C + A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\,\overline{B}\,\overline{C}$$

2. A given FSM has an input, w, and an output, z. During four consecutive clock pulses, a sequence of four values of the w signal is applied. Derive a state table for the FSM that produces z = 1 when it detects that either the sequence w : 0010 or w : 1110 has been applied; otherwise, z = 0. After the fourth clock pulse, the machine has to be again in the reset state, ready for the next sequence. Minimize the number of states needed and design the circuit.

3. Design a counter that counts in the sequence 0, 1, 3, 6, 10, 15, using four a) D, b) SR, c) JK and d) T flip-flops.