Mikroelektronische Schaltungen und Systeme

Lect.1
Intro/CMOS Basics

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Mikroelektronische Schaltungen und Systeme

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Introduction

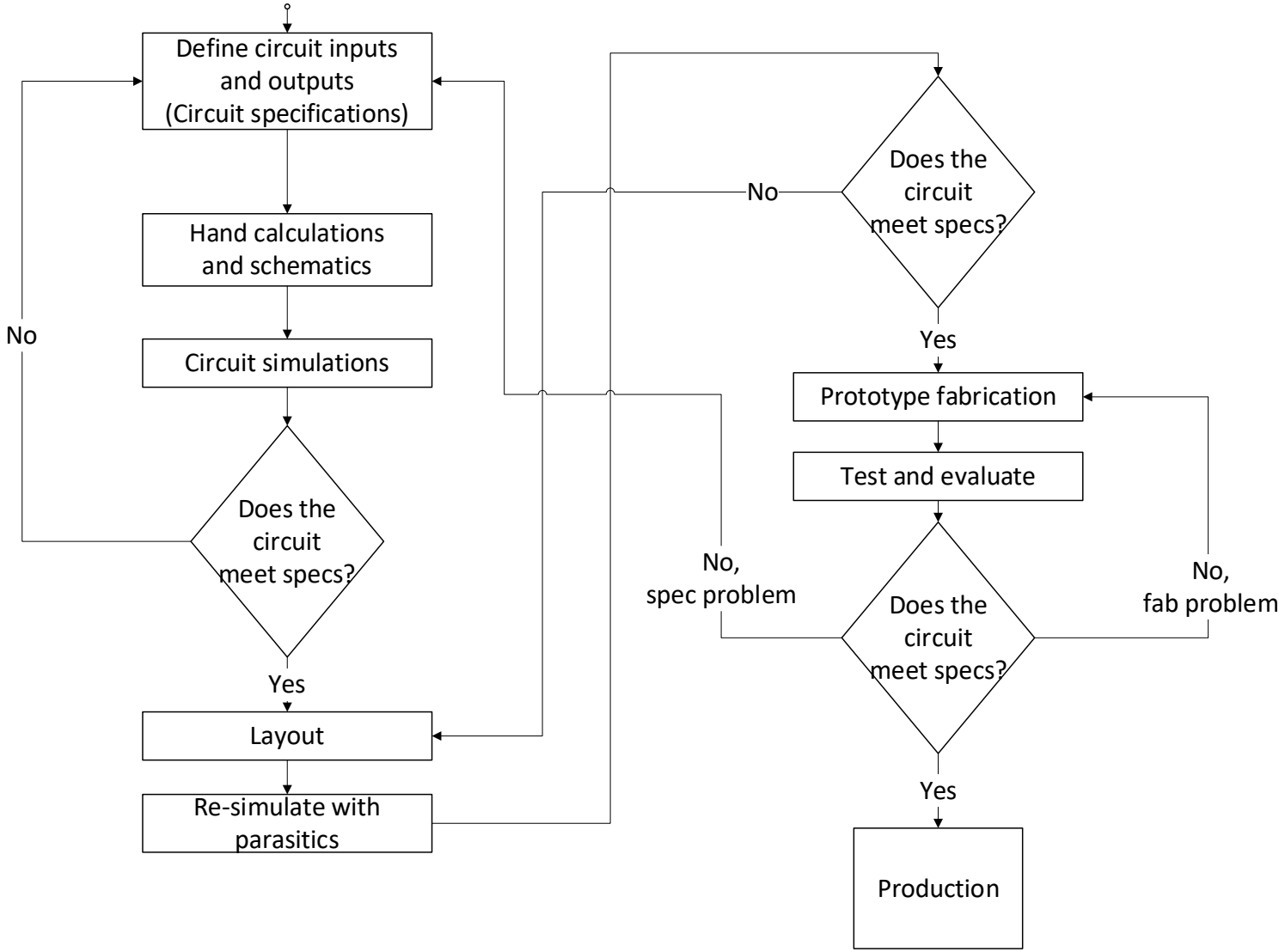
1

Parameter Definitions

- I_D: Drain Current
- V_{GS}: Gate-to-Source Voltage
- V_{DS}: Drain-to-Source Voltage
- V_{TH}: Threshold Voltage
- V_{ov}: Overdrive Voltage (= $V_{GS} - V_{TH}$)
- $V_{D,sat}$: Minimum required V_{DS} voltage for saturation
- V_{GS}: Gate-to-Source Voltage
- $\mu_{n,p}$: Mobility of Electrons, Holes
- C_{ox}: Gate-Oxide Capacitance per Unit Area
- W: MOSFET Channel Width
- L: MOSFET Channel Length
- L_{eff}: MOSFET Effective Channel Length
- λ: Channel-length modulation coefficient
- γ: Body-effect coefficient

Introduction

IC Design Process[1]



Introduction

Chip Fabrication

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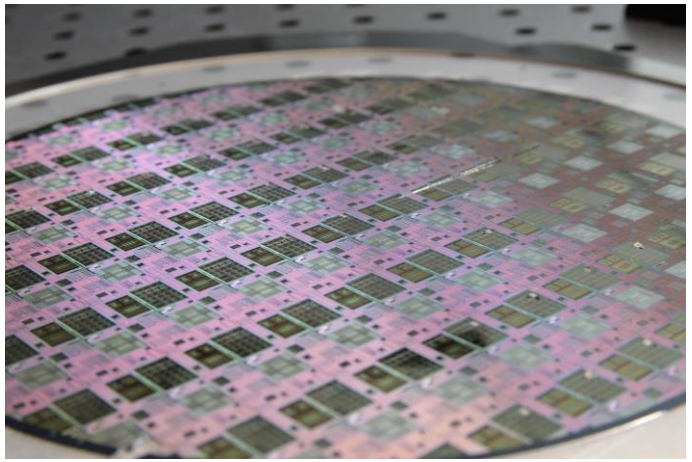
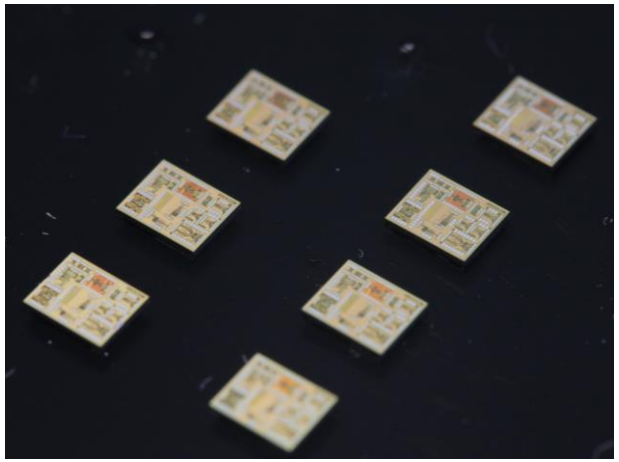
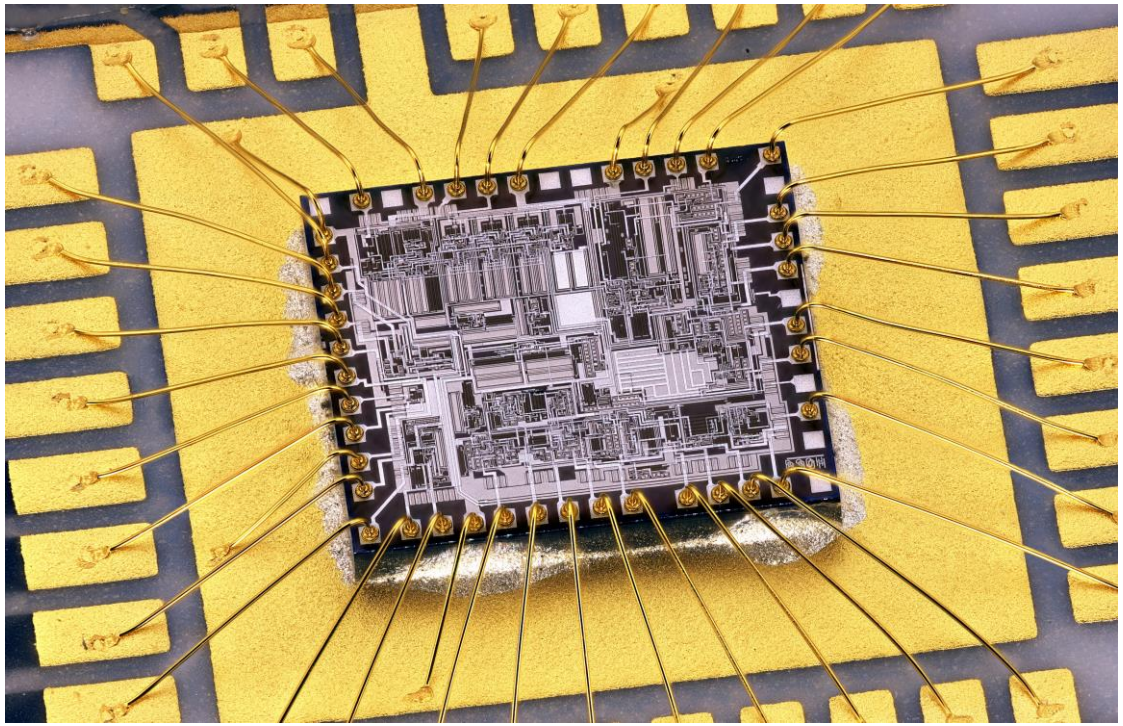




Introduction

Bondwiring & Packaging



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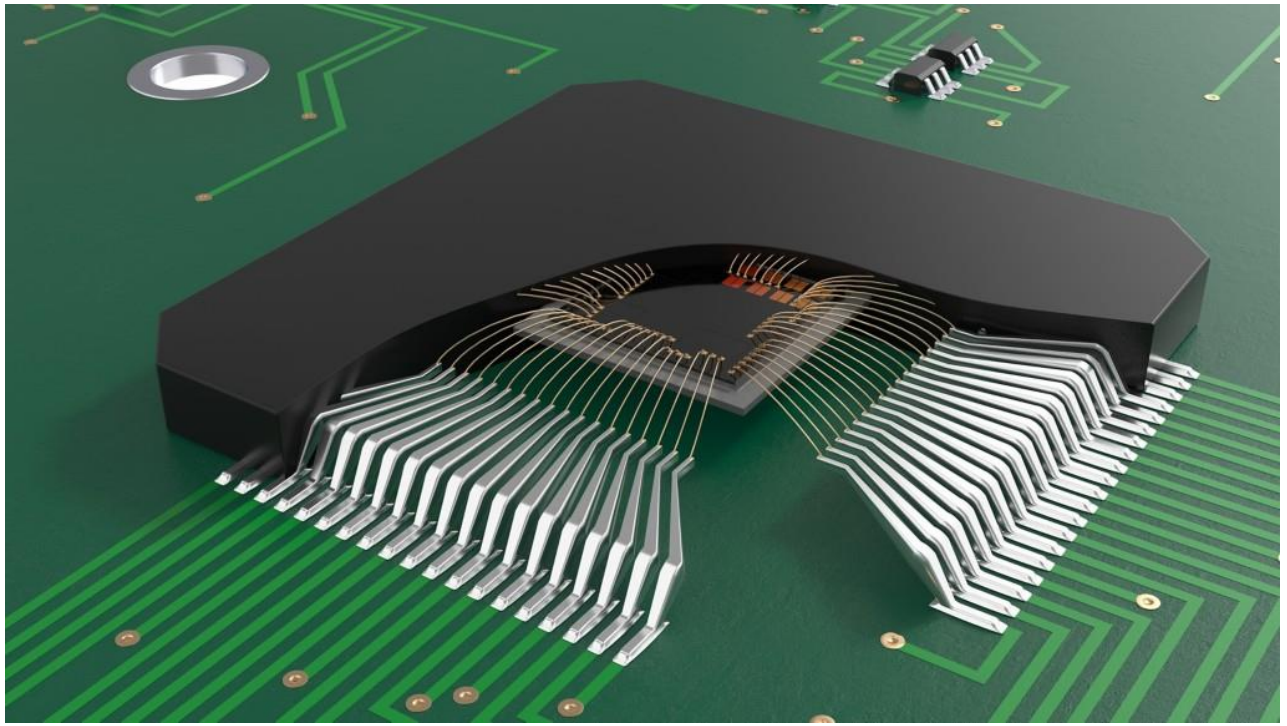

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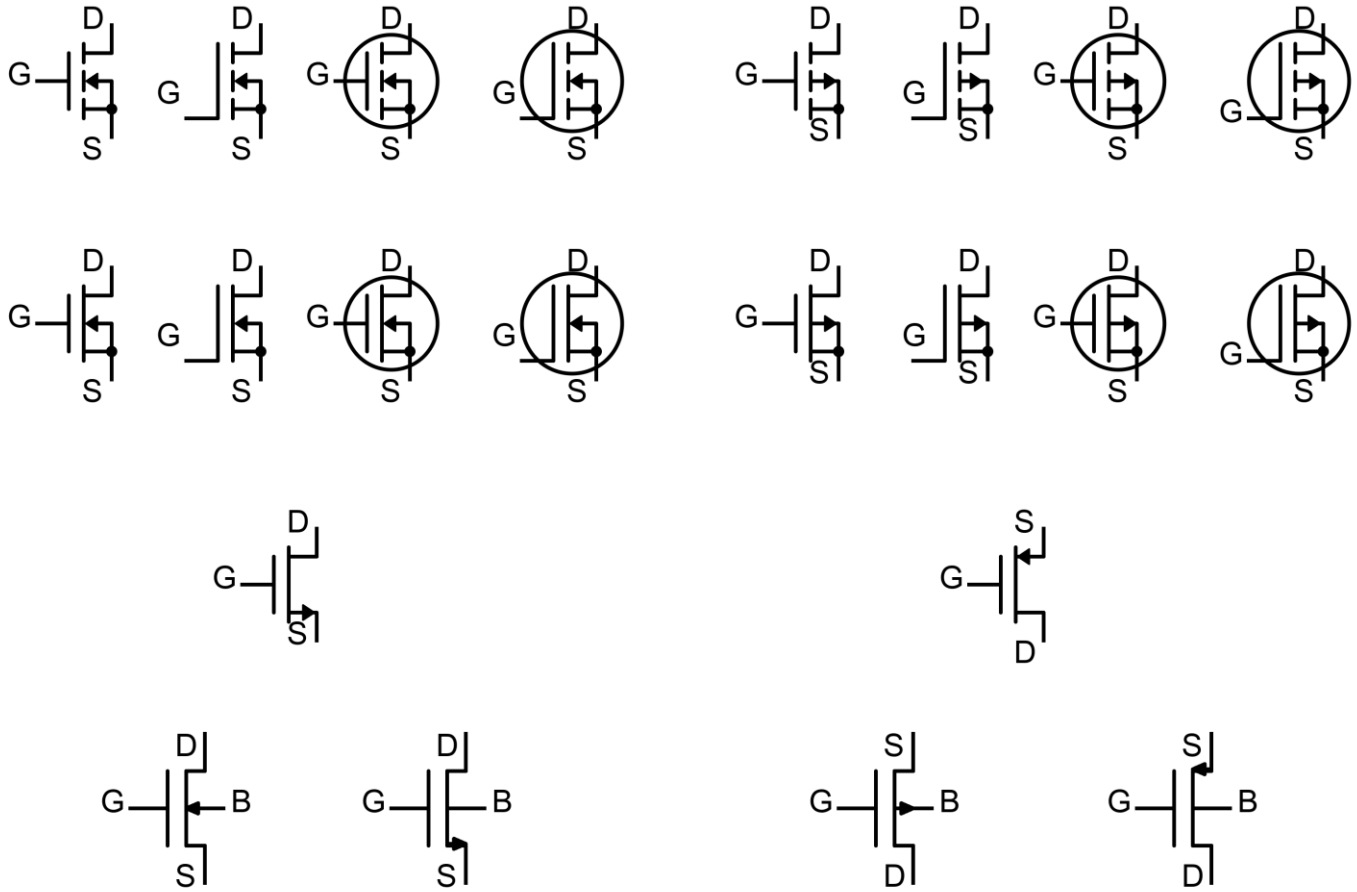
Recap

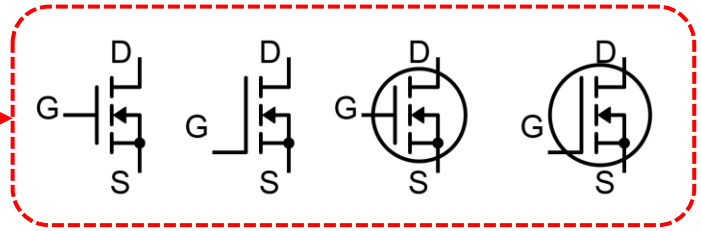
MOSFET Symbols

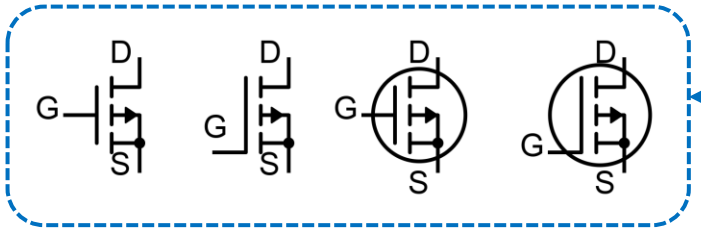


Recap

MOSFET Symbols

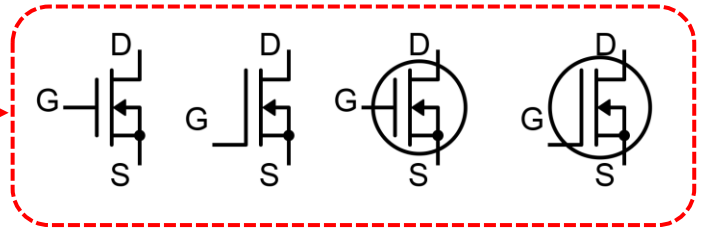
N-Channel Enhancement MOSFET

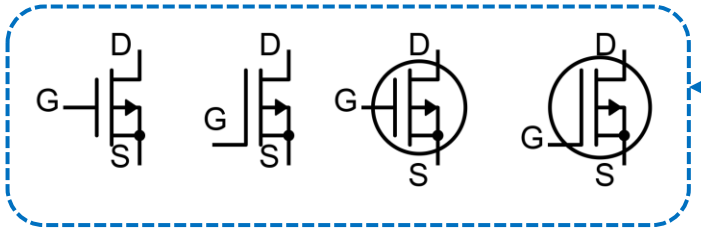




P-Channel Enhancement MOSFET

N-Channel Depletion MOSFET

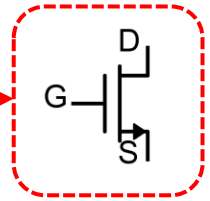


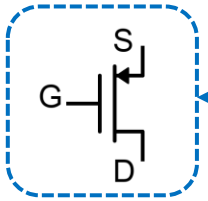


P-Channel Depletion MOSFET

N-Channel MOSFET Simplified Symbol

(Bulk connected to the ground)

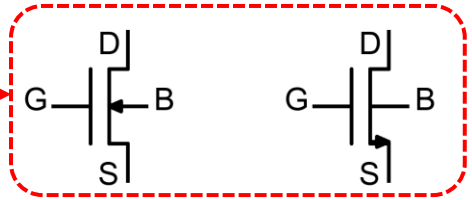


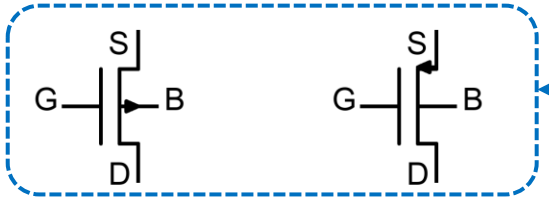


P-Channel MOSFET Simplified Symbol

(Bulk connected to V_{DD})

N-Channel MOSFET Symbol with Bulk Pin





P-Channel MOSFET Simplified Symbol with Bulk Pin

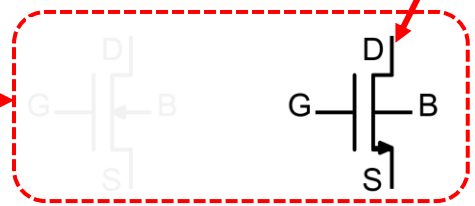
Recap

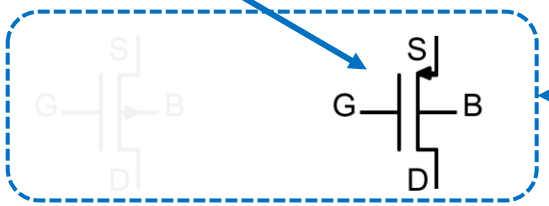
MOSFET Symbols

These symbols will be used throughout the lecture

N-Channel MOSFET

Symbol with Bulk Pin



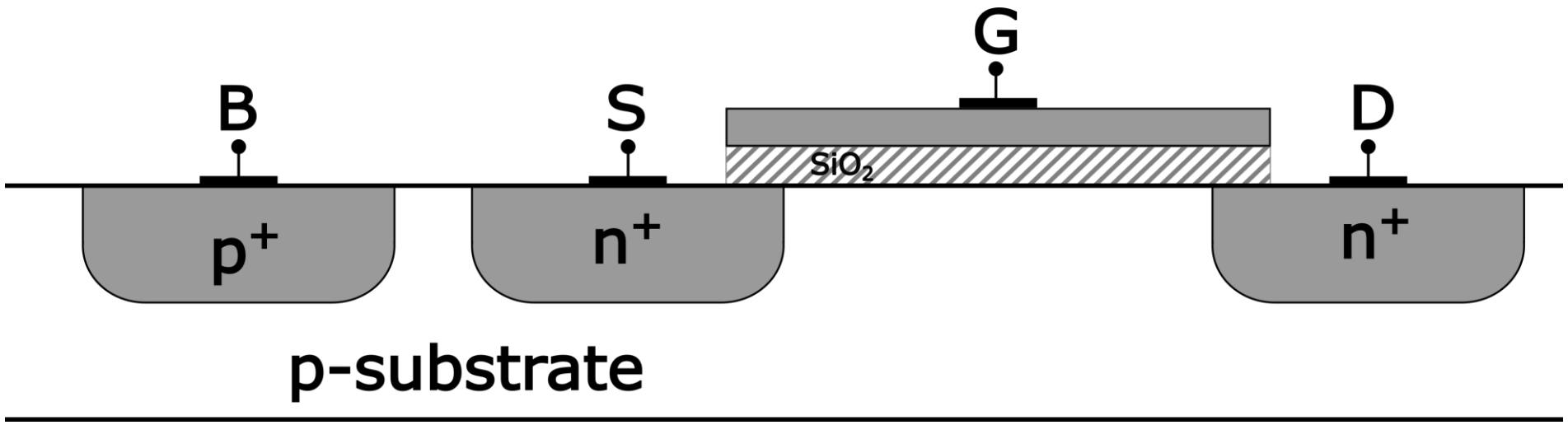


P-Channel MOSFET

Simplified Symbol with Bulk Pin

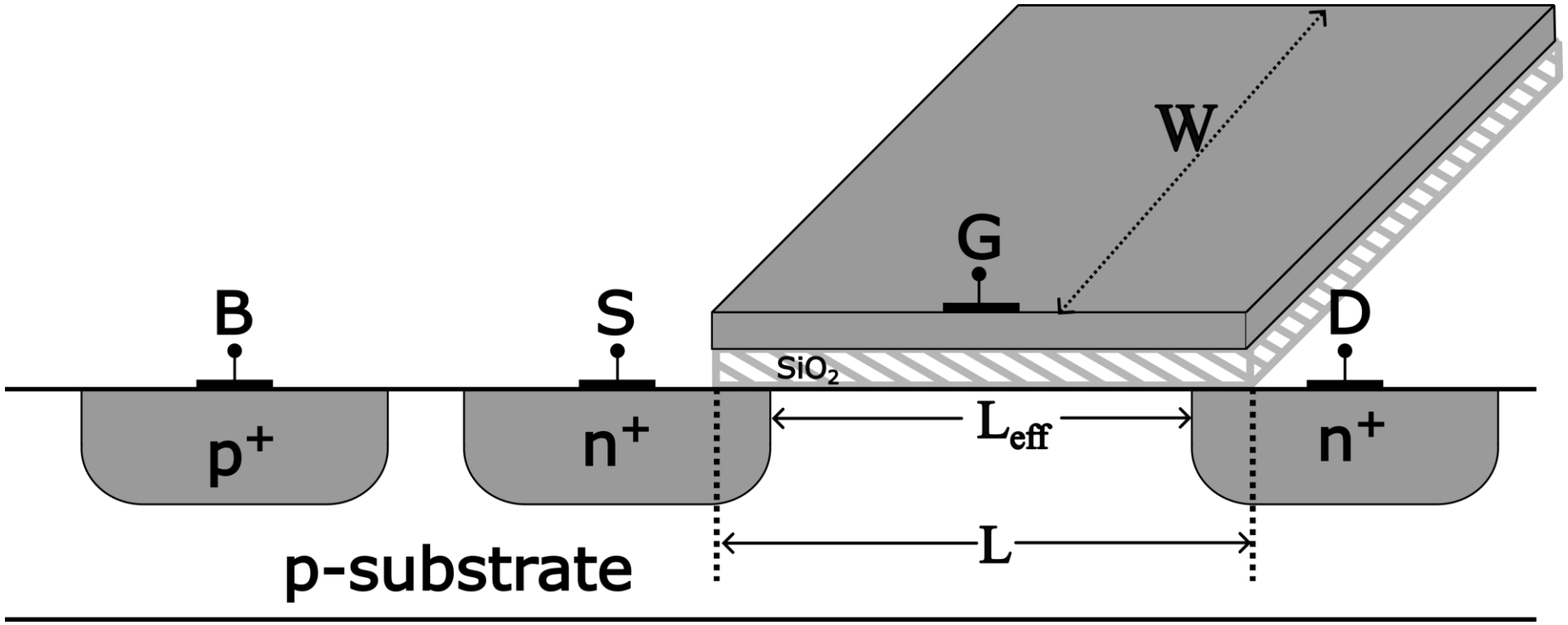
MOSFET Layout Side View

NMOS

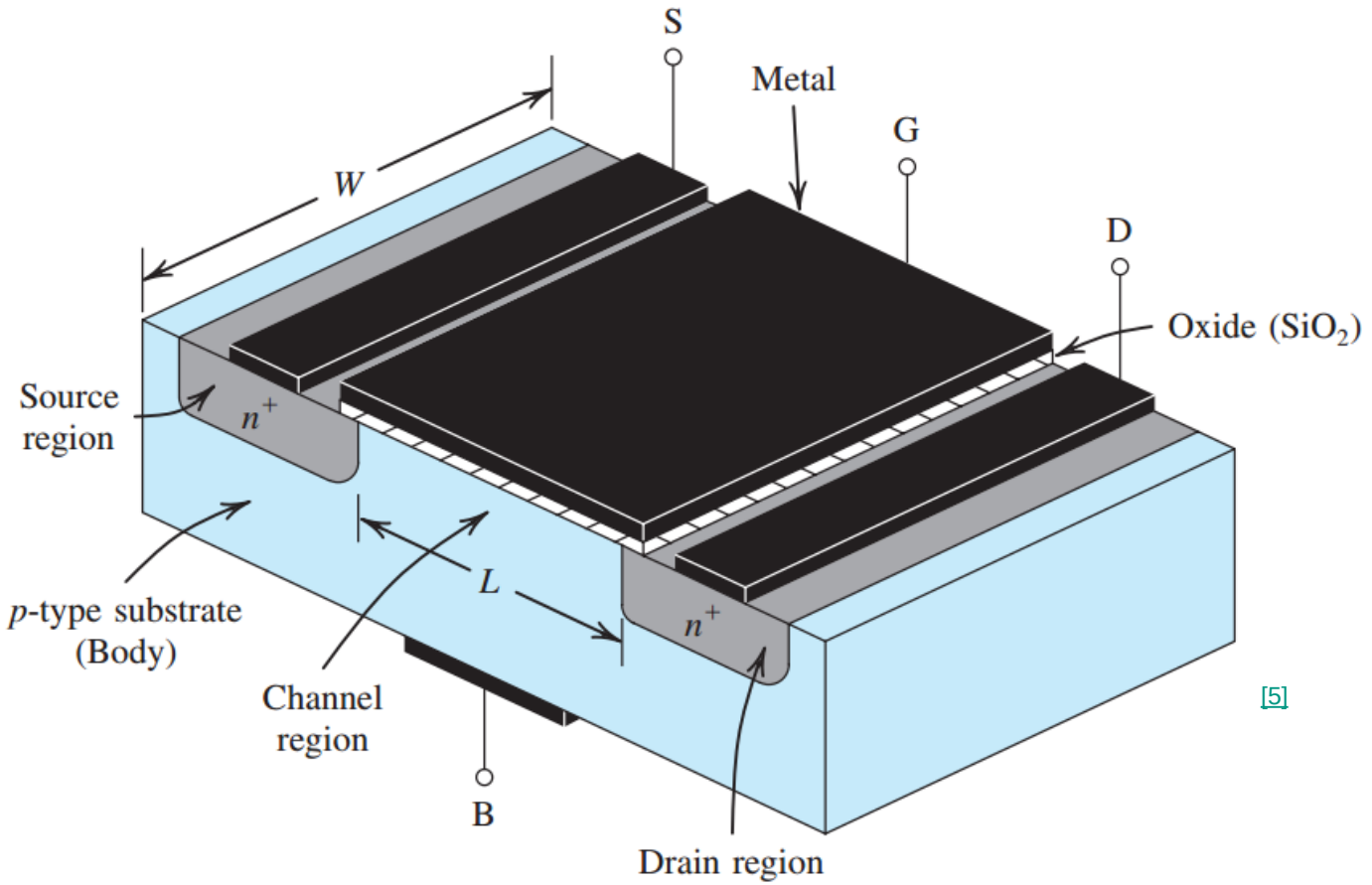


MOSFET Layout Side View

NMOS

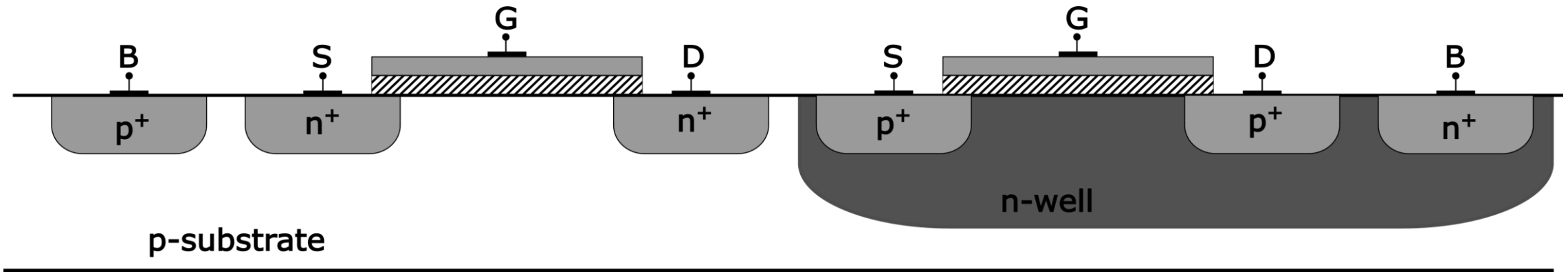


MOSFET Layout 3D View

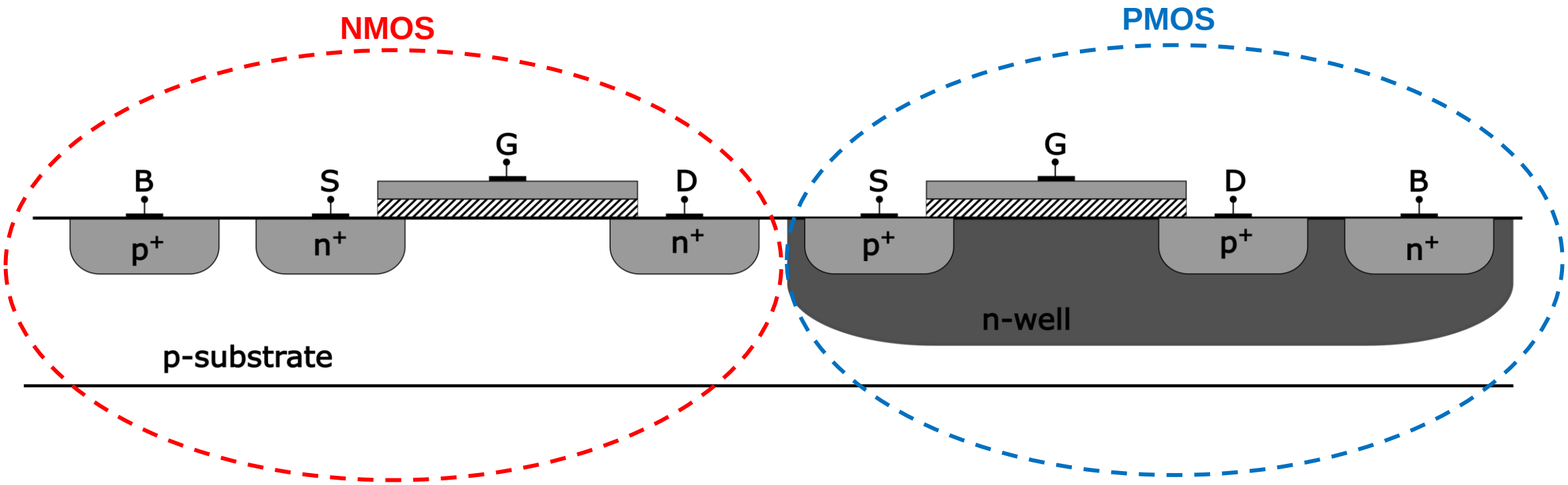


[5]

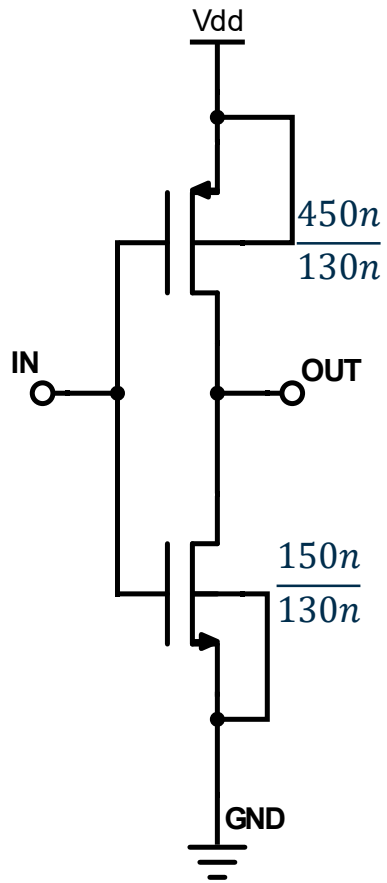
Complementary MOS (CMOS) Side View



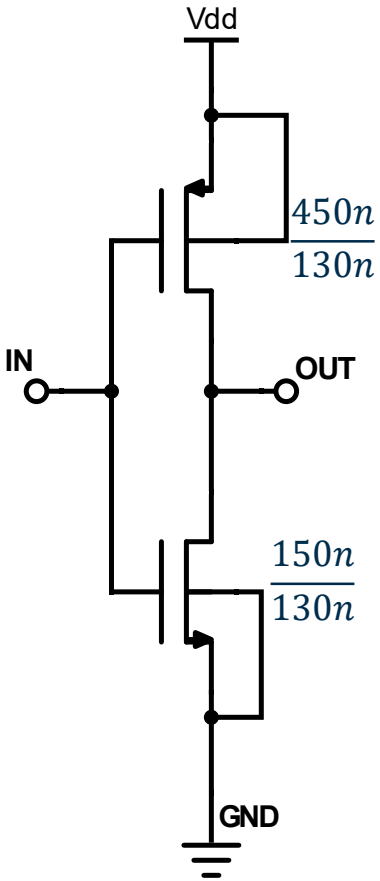
Complementary MOS (CMOS) Side View

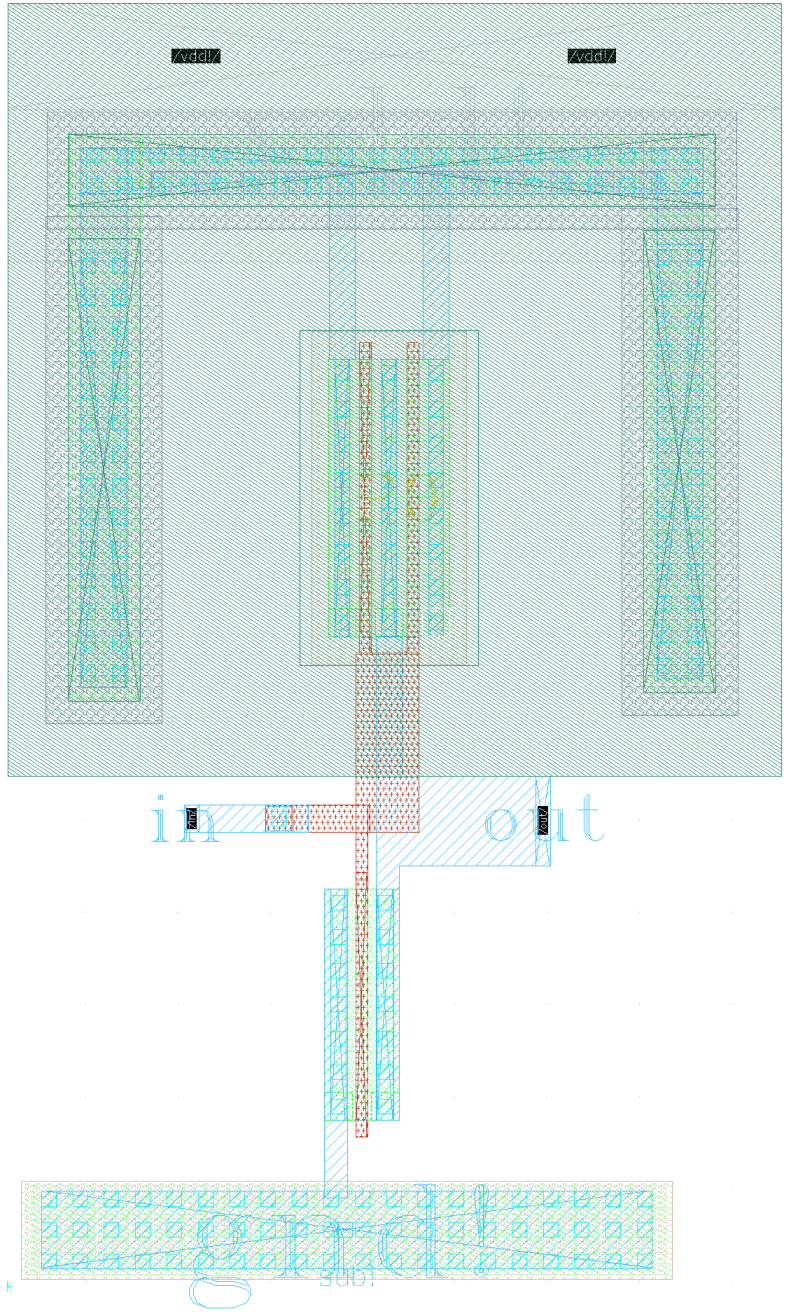


CMOS Inverter

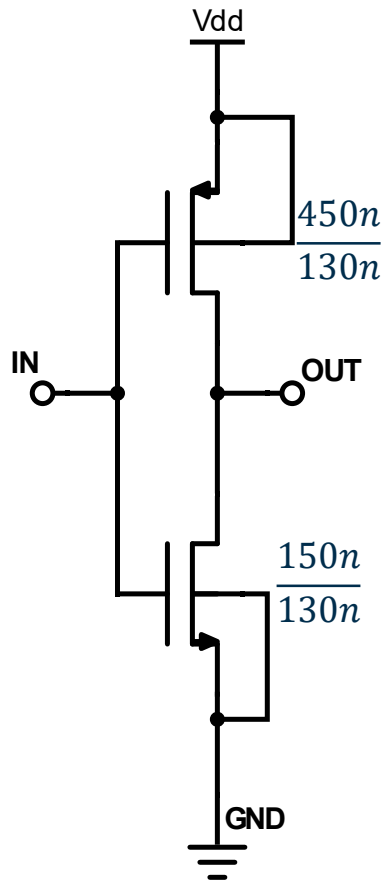


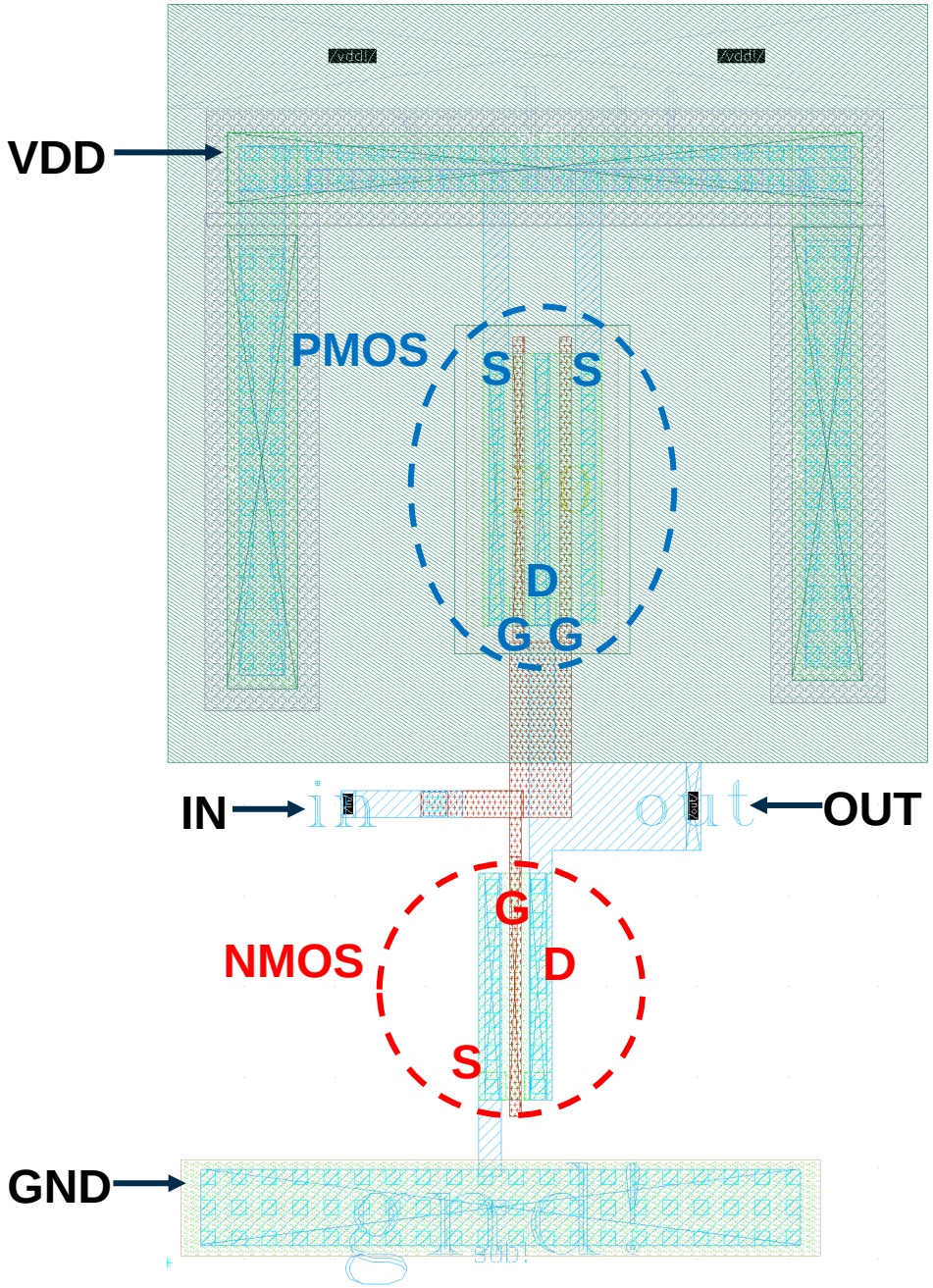
CMOS Inverter Layout



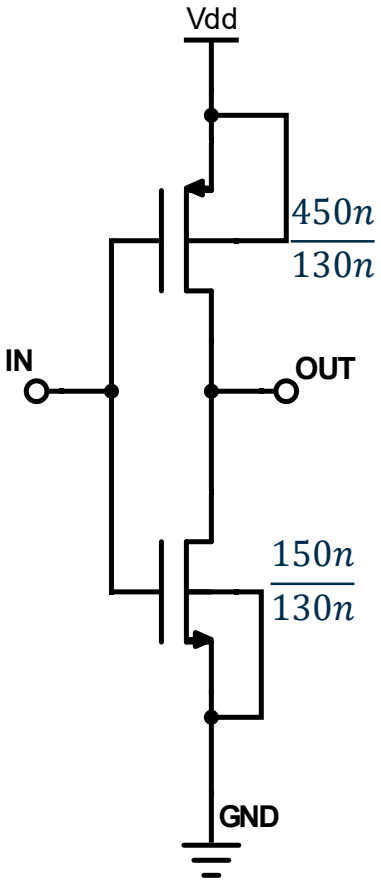


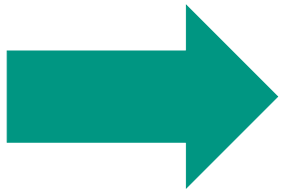
CMOS Inverter Layout

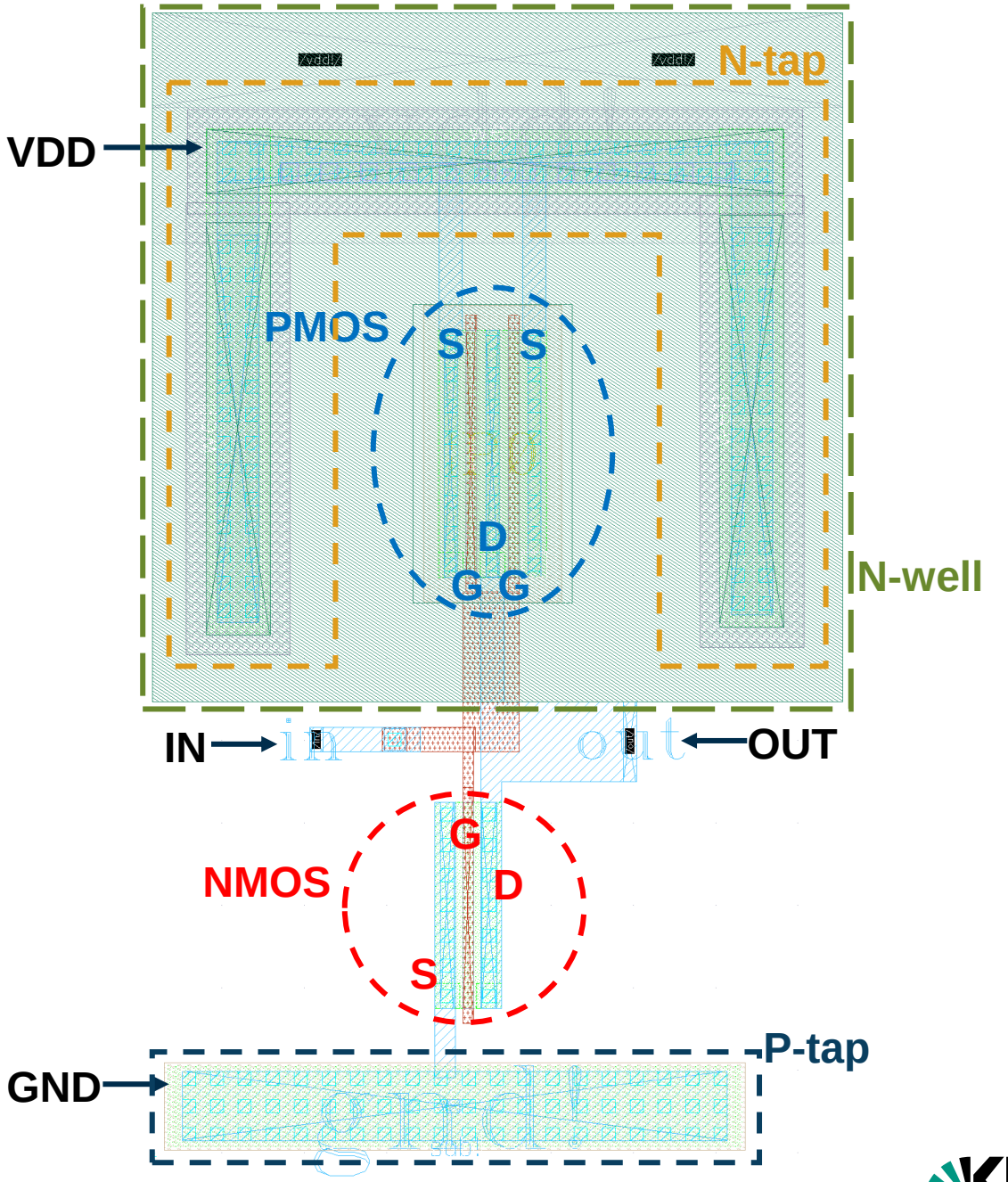




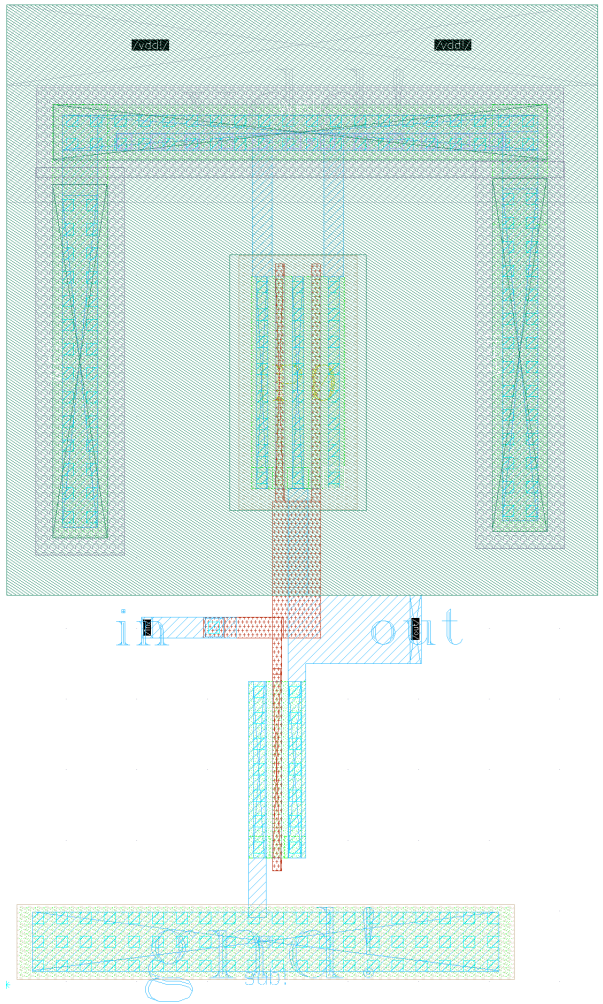
CMOS Inverter Layout

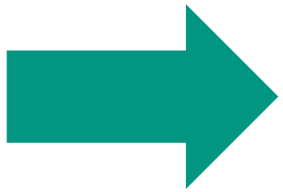


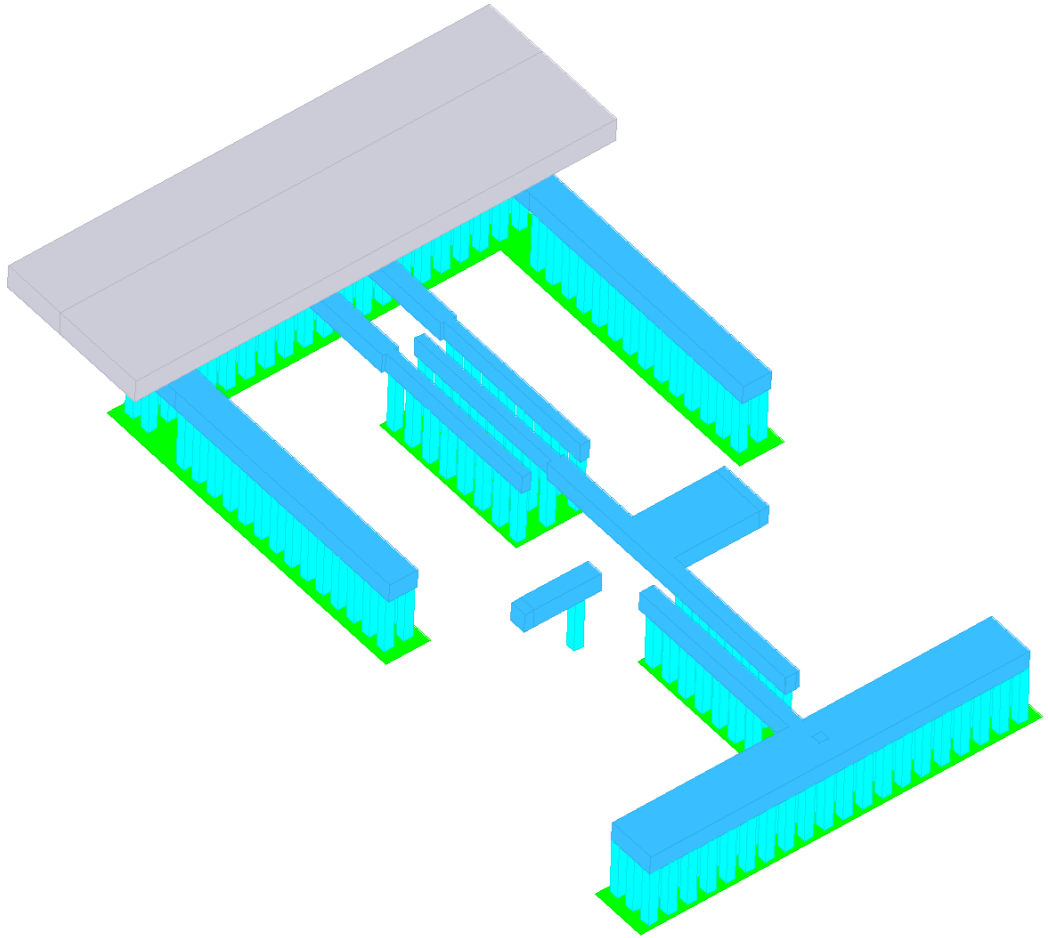




CMOS Inverter Layout BEOL 3D View



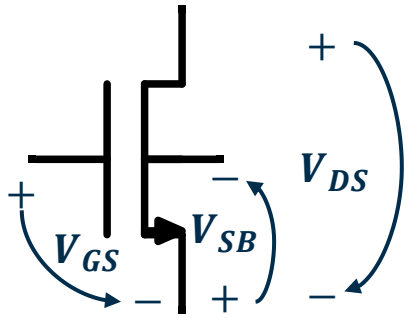




IV Characterisctics of MOSFET

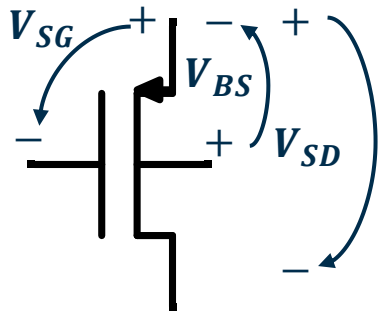
- NMOS

$\lvert V_{GS}\rvert$	$\lvert V_{DS}\rvert$	Region
<< $\lvert V_{THN}\rvert$	-	Cut-off
≤ $\lvert V_{THN}\rvert$	-	Subthreshold
> $\lvert V_{THN}\rvert$	< $\lvert V_{GS}\rvert - \lvert V_{THN}\rvert$	Triode
> $\lvert V_{THN}\rvert$	> $\lvert V_{GS}\rvert - \lvert V_{THN}\rvert$	Saturation

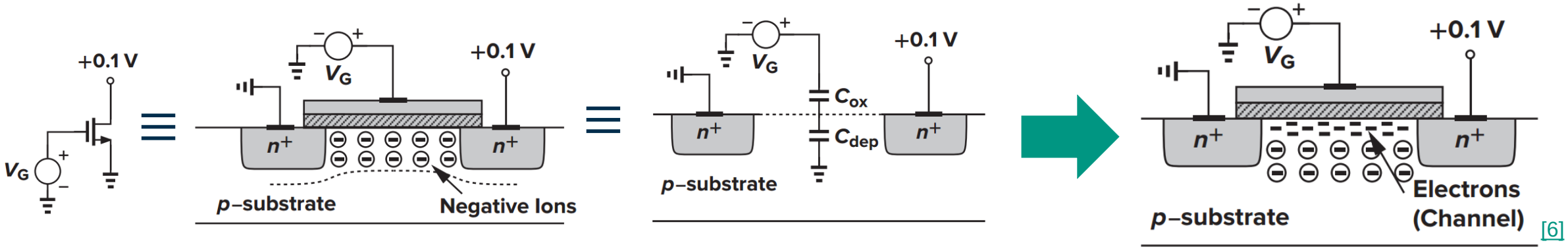


- PMOS

V_{SG}	V_{SD}	Region
<< $\lvert V_{THP}\rvert$	-	Cut-off
≤ $\lvert V_{THP}\rvert$	-	Subthreshold
> $\lvert V_{THP}\rvert$	< $\lvert V_{SG}\rvert - \lvert V_{THP}\rvert$	Triode
> $\lvert V_{THP}\rvert$	> $\lvert V_{SG}\rvert - \lvert V_{THP}\rvert$	Saturation



Threshold Voltage of an N-Channel MOSFET



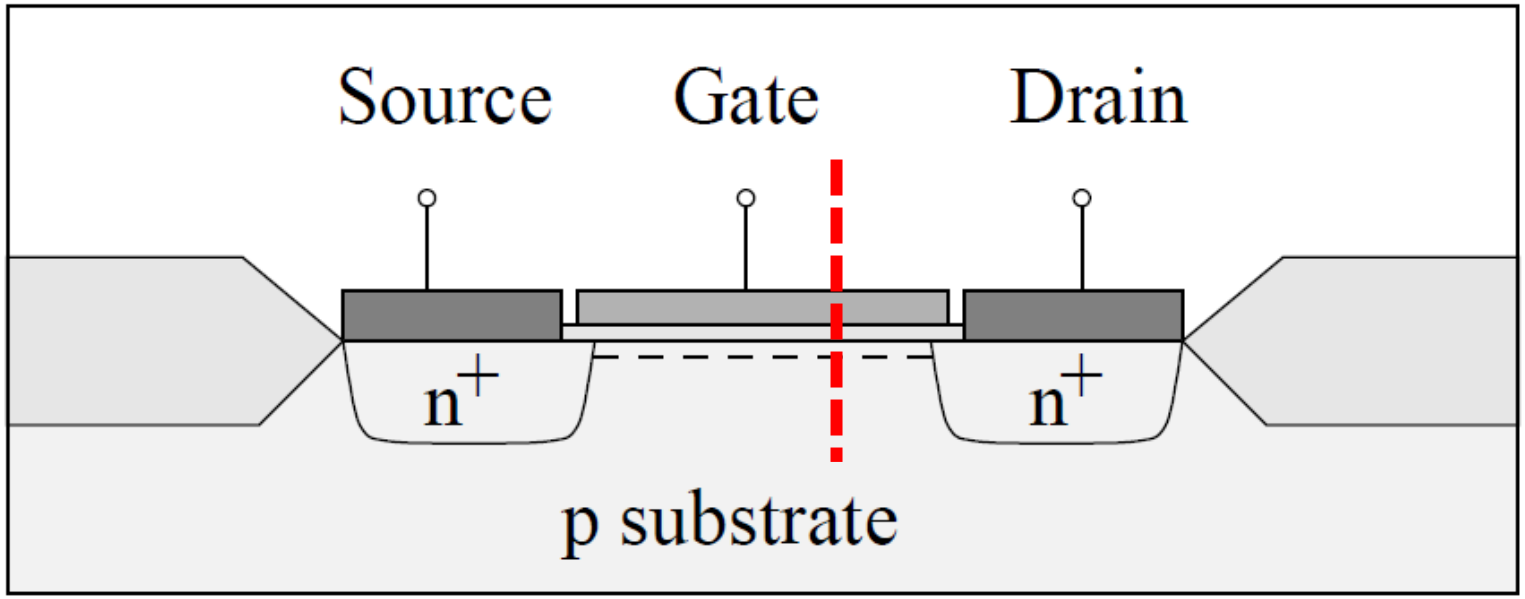
[6]

- The applied gate voltage repels the holes underneath the oxide and forms an N-channel once the voltage reaches a certain level. This voltage level is called the threshold voltage:

$$V_{TH0} = V_{FB} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}$$

- V_{FB}: The difference between work functions (ϕ_{MS}) of the polysilicon gate and the silicon – charge in Oxide layer
- $\phi_F = \left(\frac{kT}{q}\right) ln\left(\frac{N_A}{n_i}\right)$ → k: Boltzmann's constant, q: Electron charge, N_A: Doping density of the substrate, n_i: Density of electrons in undoped silicon
- $Q_{dep} = \sqrt{4.q.\epsilon_{si}.|\phi_F|.N_A}$: Charge in the depletion region
- C_{ox}: Gate-oxide capacitance per unit area

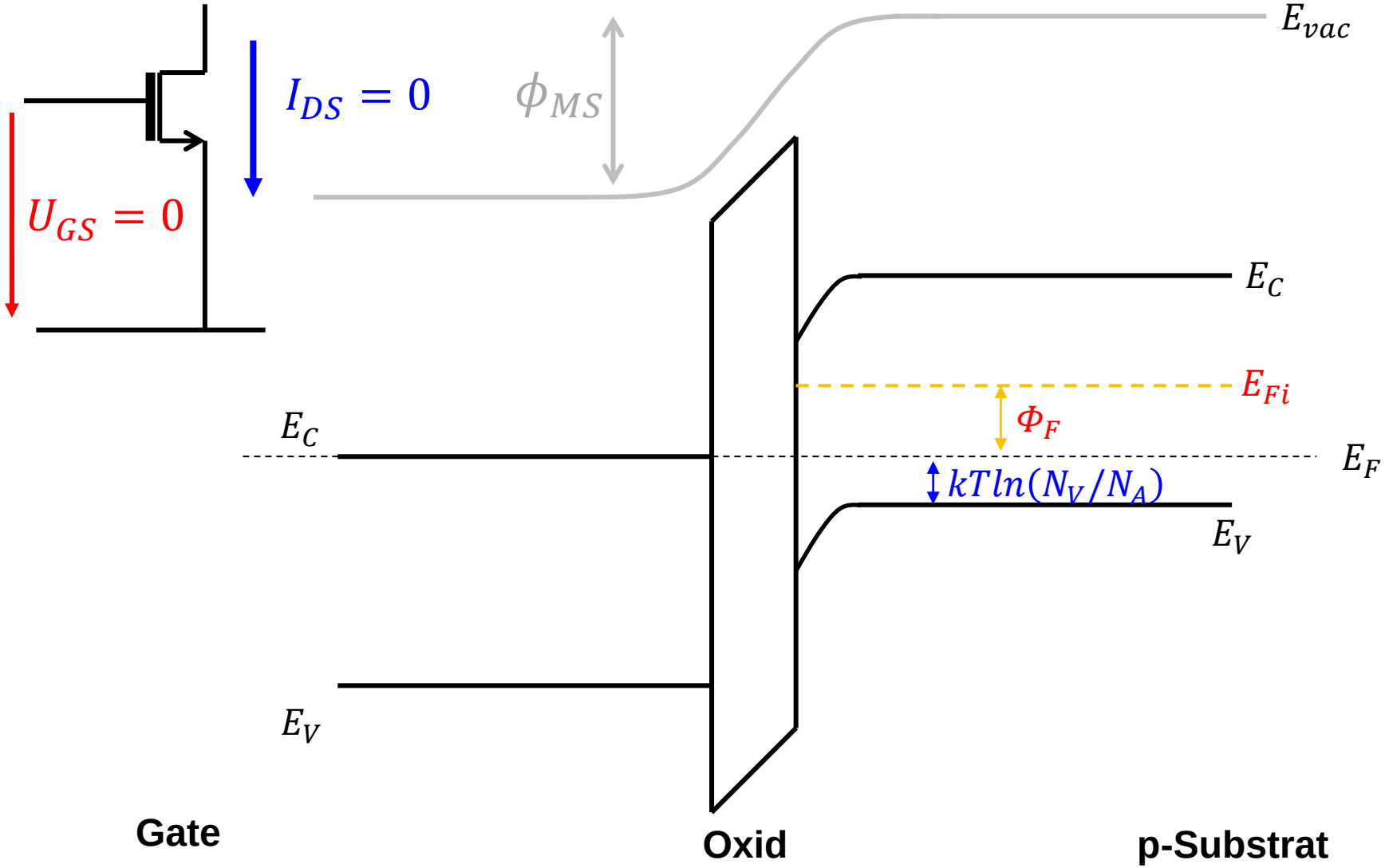
MOSFET (Isolierschicht-Feldeffekttransistoren) Aufbau



Durch eine positive Gate-Spannung werden Elektronen vom Substrat zur Oxid-Silizium-Schnittstelle gezogen, wodurch die Source- und Drain-Anschlüsse mit einem n-Kanal verbunden werden

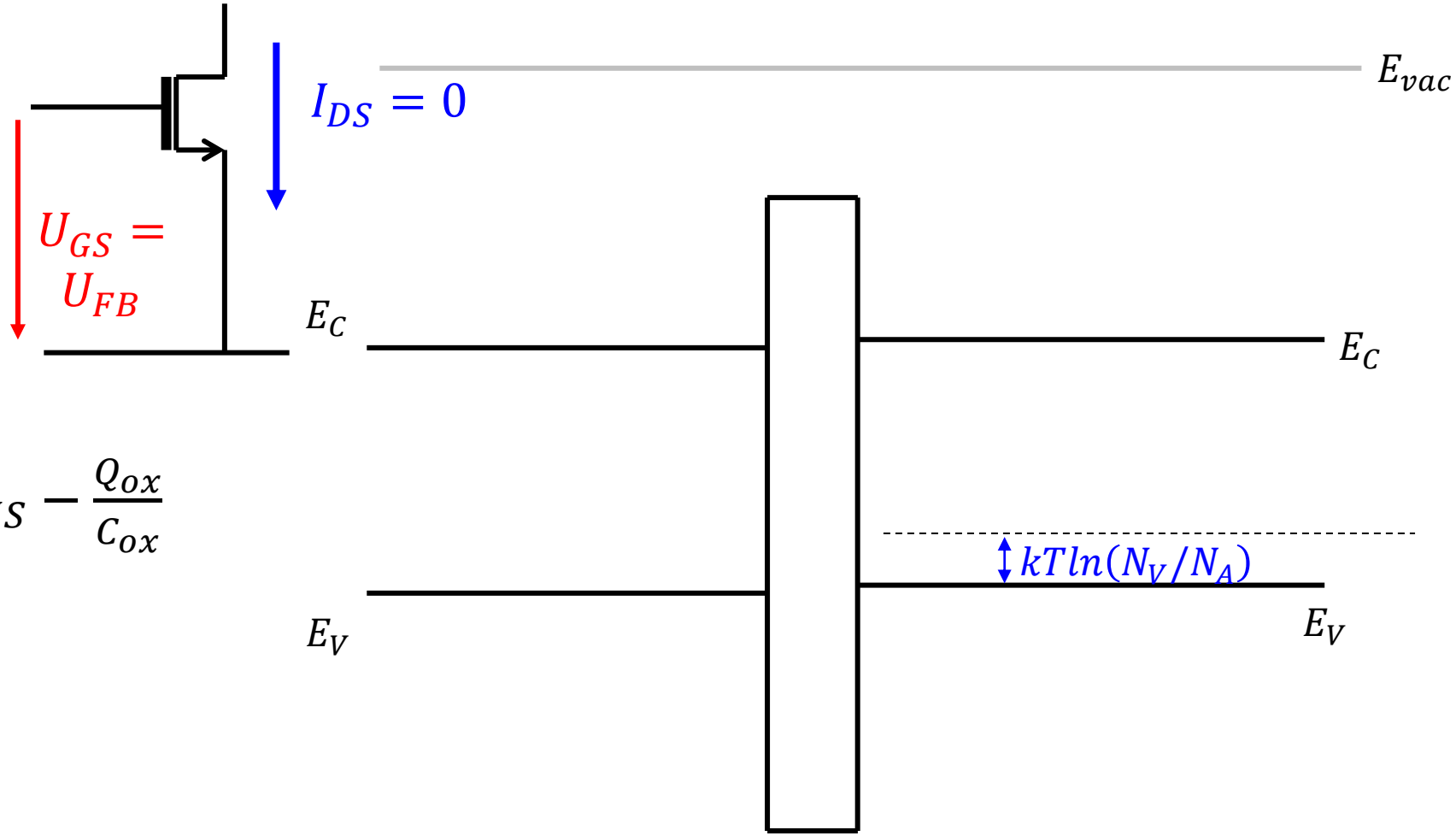
MOSFET (Isolierschicht-Feldeffekttransistor) Aufbau

keine äußere Spannung



MOSFET (Isolierschicht-Feldeffekttransistor) Aufbau

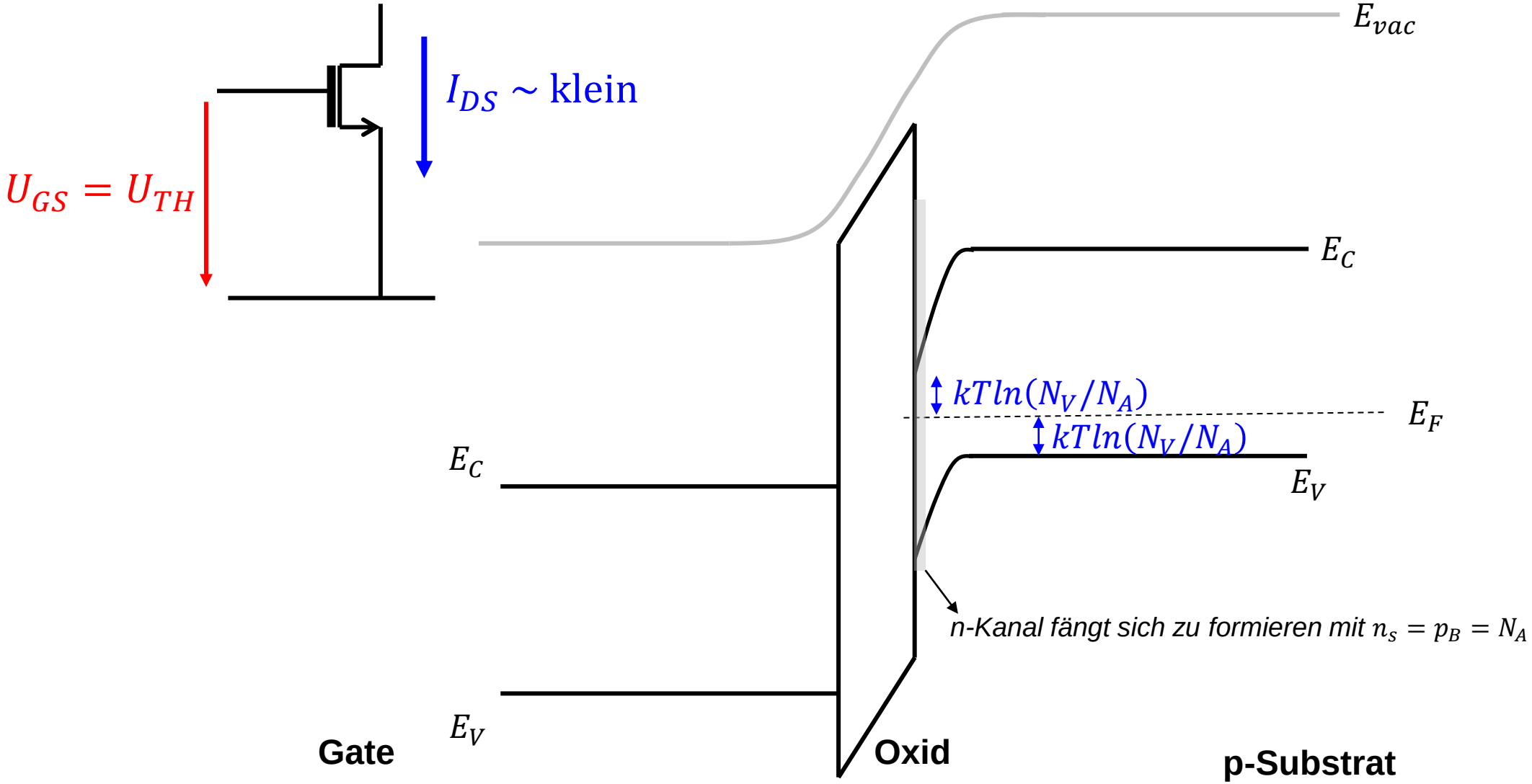
Flachbandzustand



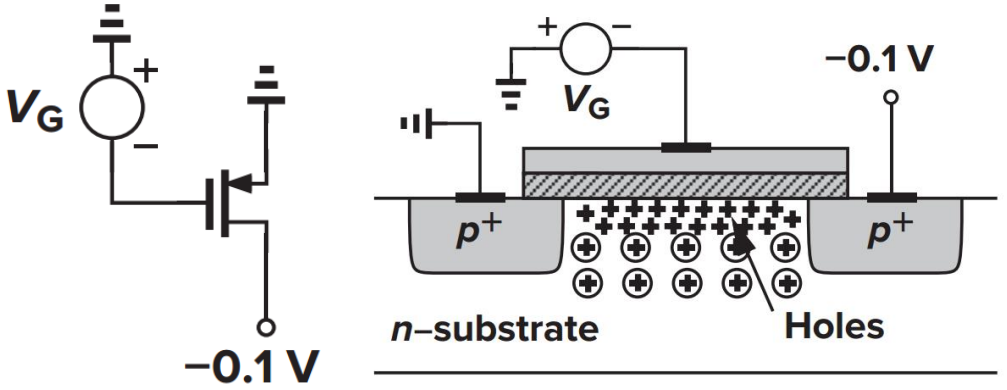
$$V_{FB} = \phi_{MS} - \frac{Q_{ox}}{c_{ox}}$$

MOSFET (Isolierschicht-Feldeffekttransistor) Aufbau

positive Gatespannung



Threshold Voltage of an P-Channel MOSFET

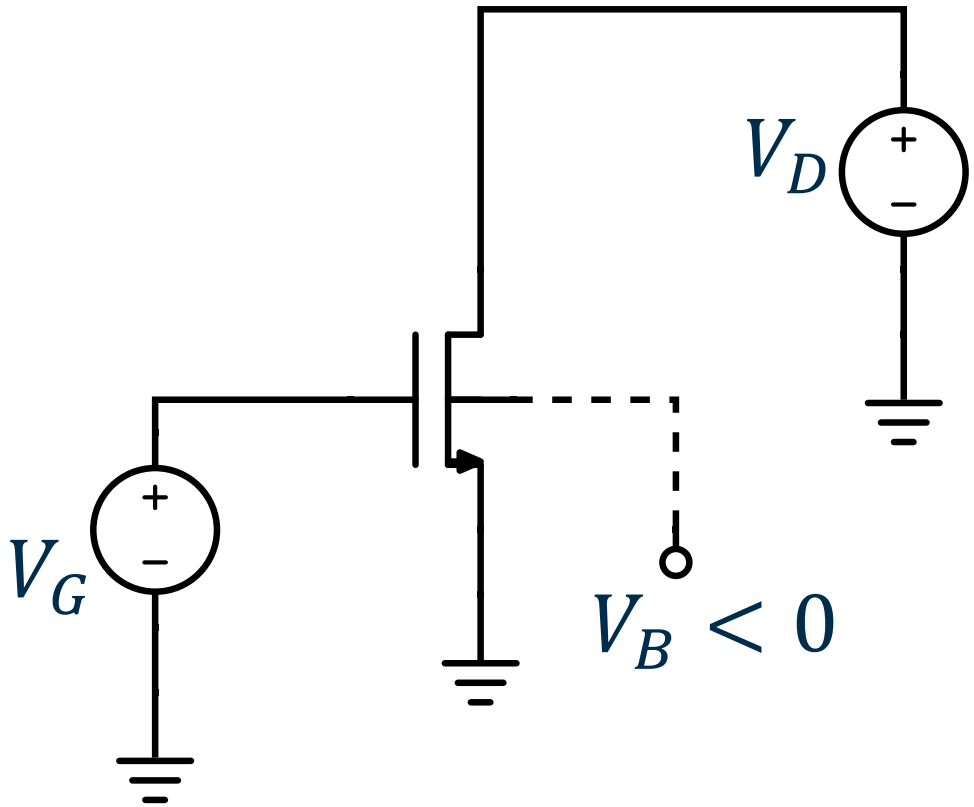


[6]

- The threshold phenomenon is similar in a PMOS device. All the polarities are reversed. The inversion layer consists of holes. The threshold voltage of a PMOS device is typically negative.

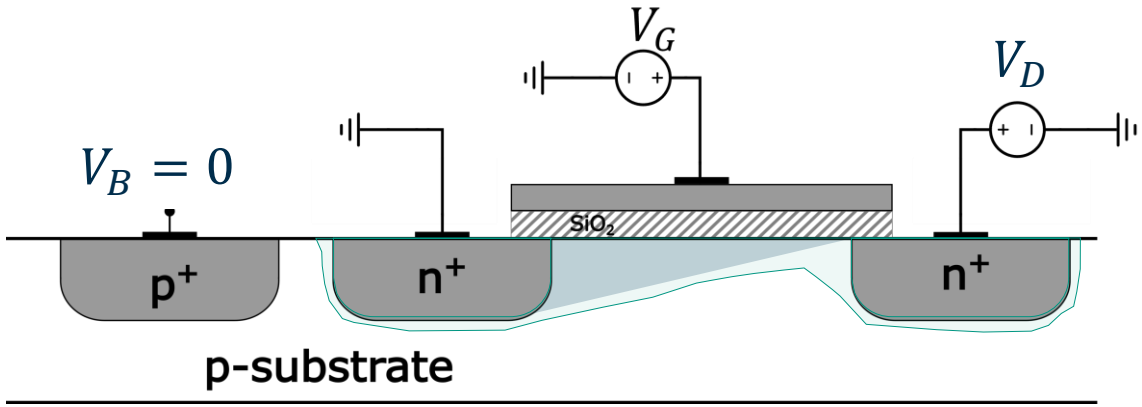
Body Effect

- The analysis so far has assumed that both the bulk and the source of the transistor are connected to ground.
- The bulk pin is typically tied to the lowest voltage in the circuit.
- So, what happens if the bulk voltage is lower than the source voltage?



Body Effect

- As the bulk voltage becomes more negative relative to the source (i.e., V_{SB} increases), the source–bulk junction is further reverse-biased.
- The depletion region under the gate widens, so the magnitude of the depletion charge $|Q_{dep}|$ increases.
- Because the threshold voltage is proportional with Q_{dep}, the threshold increases, too.



Body Effect

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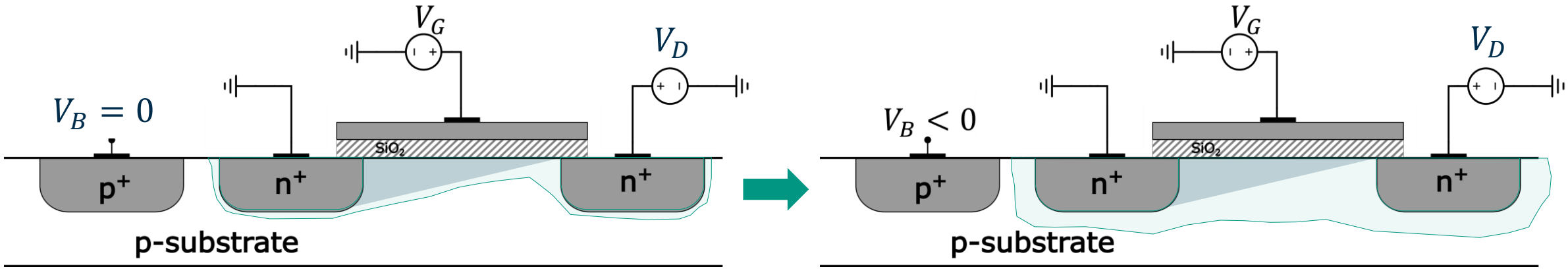


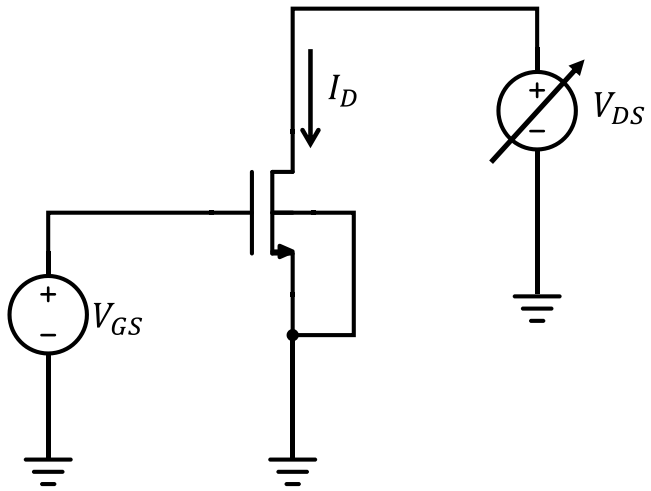
Body Effect

- To sum up, as V_B drops, V_{SB} increases, Q_{dep} increases, therefore V_{TH} increases.
- This effect is called the “body effect” or the “back-gate” effect.” Formulated as:

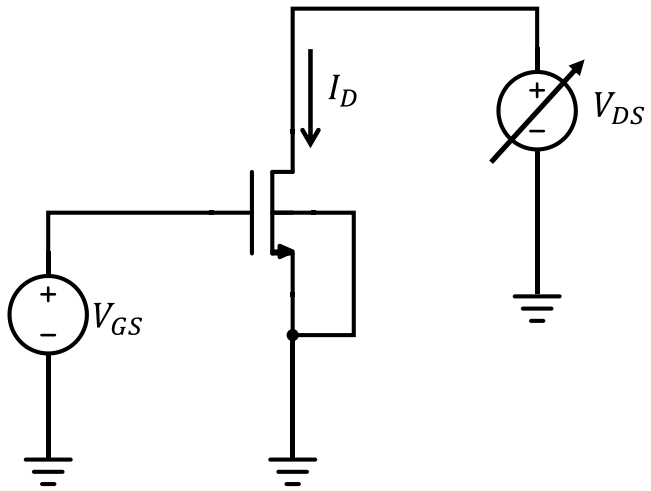
$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{|2\phi_F|}\right)$$

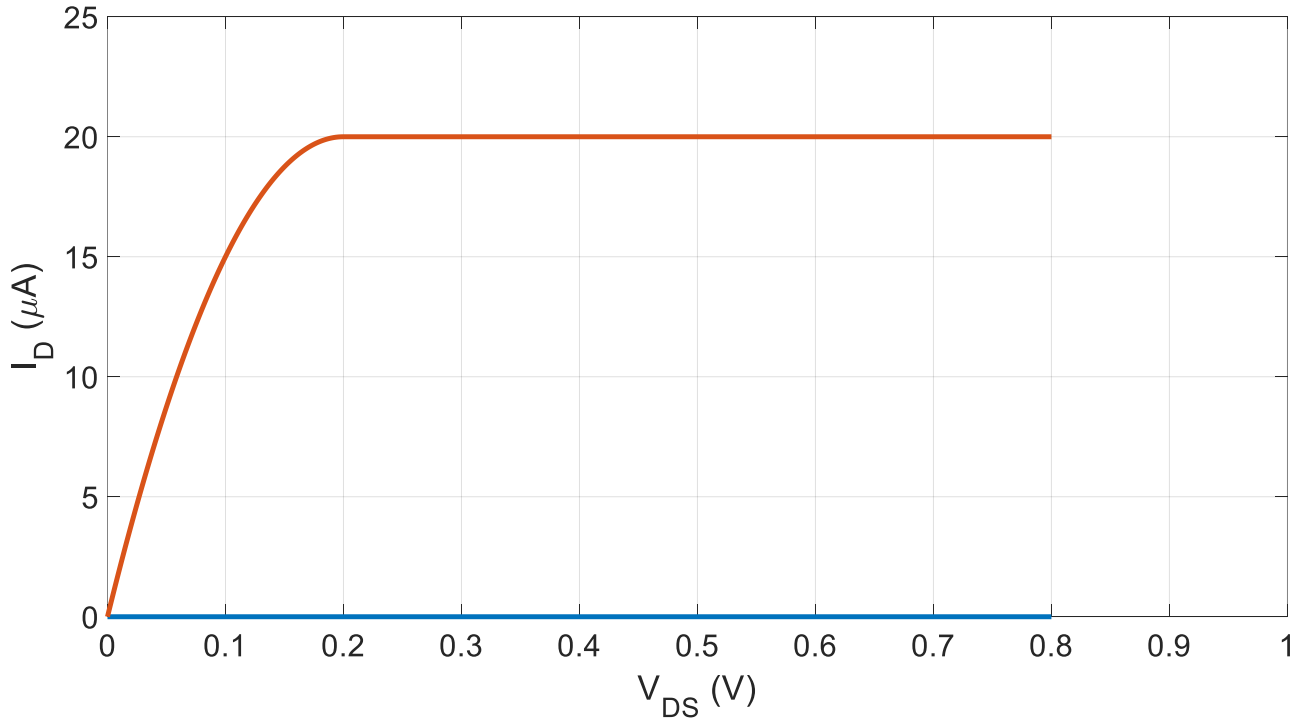
where V_{TH0} was given previously, $\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$ denotes body-effect coefficient, V_{SB} is the source-bulk voltage difference. The value of γ typically lies in the range of 0.3 to 0.4 $V^{1/2}$.

I/V Characteristics of NMOS Transistor - I_D-V_{DS}

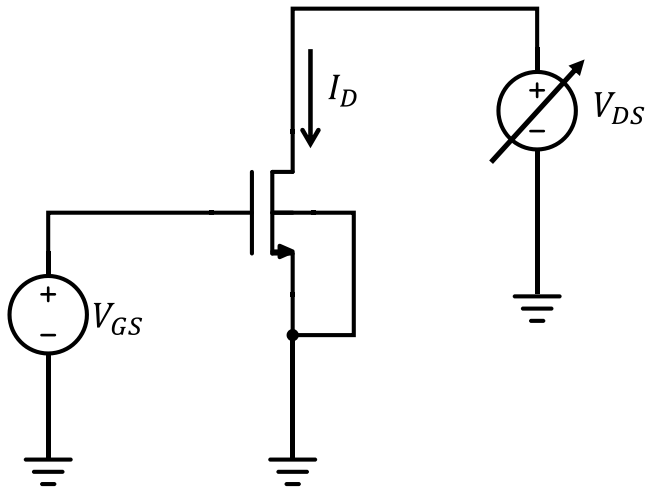


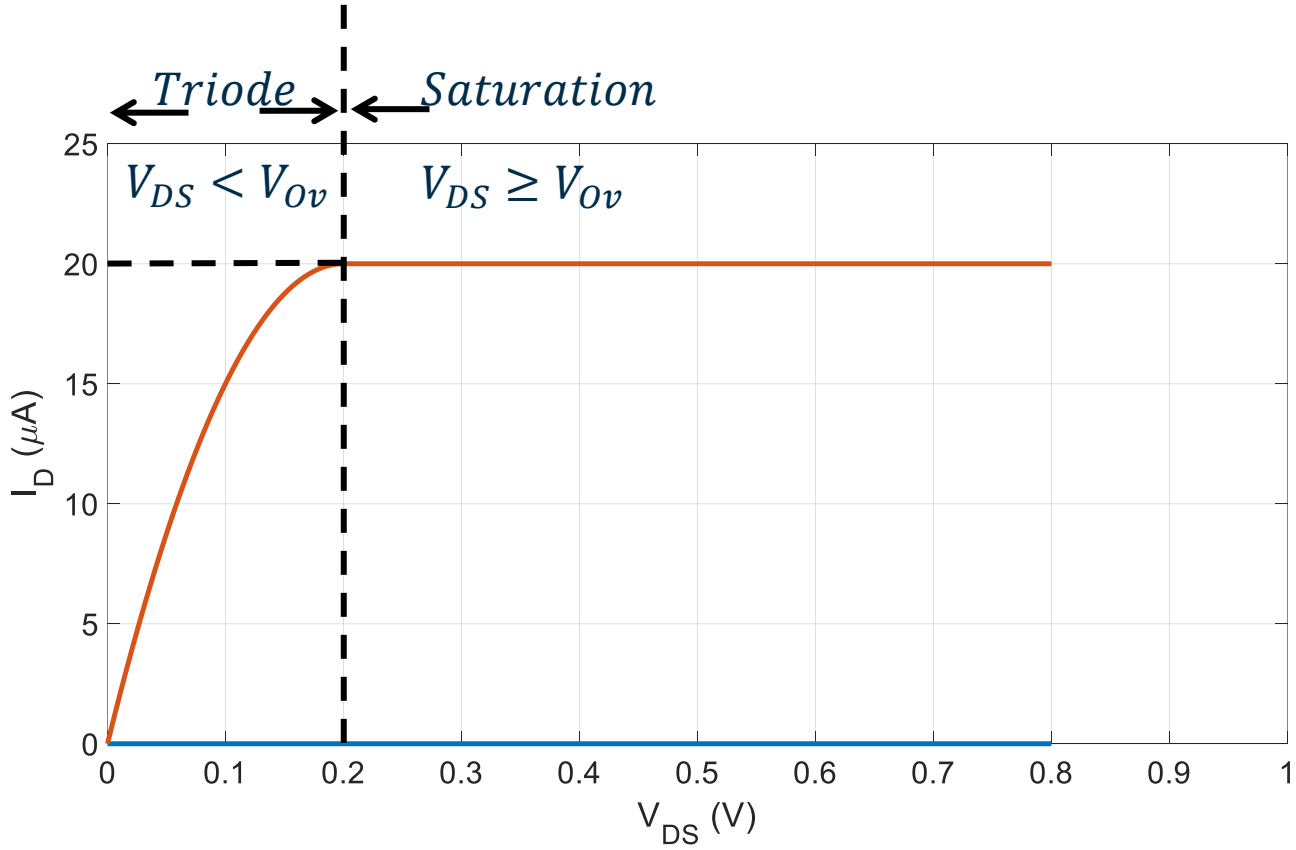
I/V Characteristics of NMOS Transistor - I_D-V_{DS}



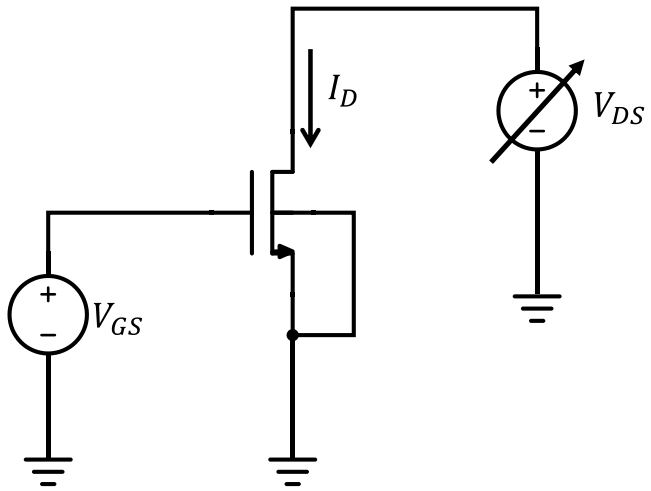


I/V Characteristics of NMOS Transistor - I_D-V_{DS}

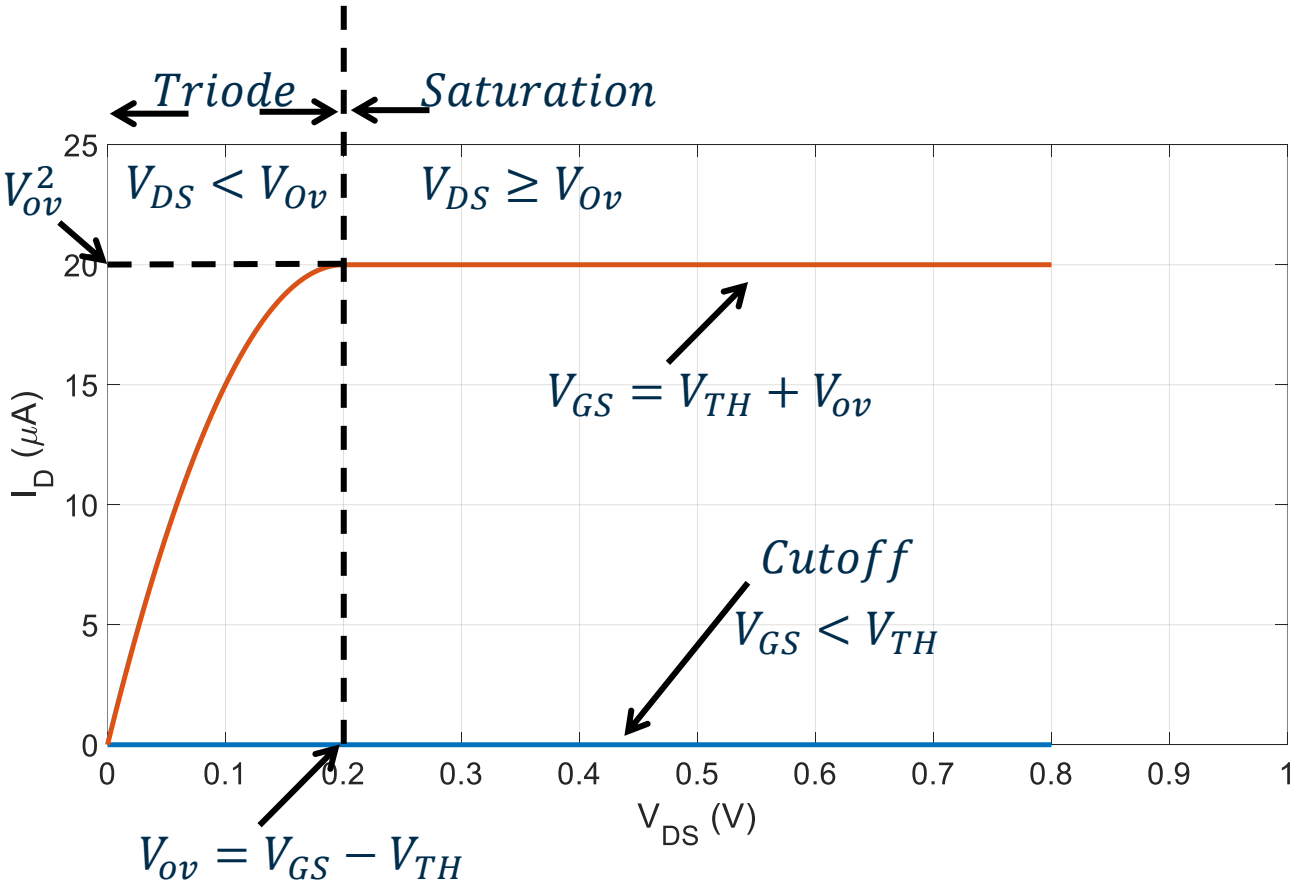




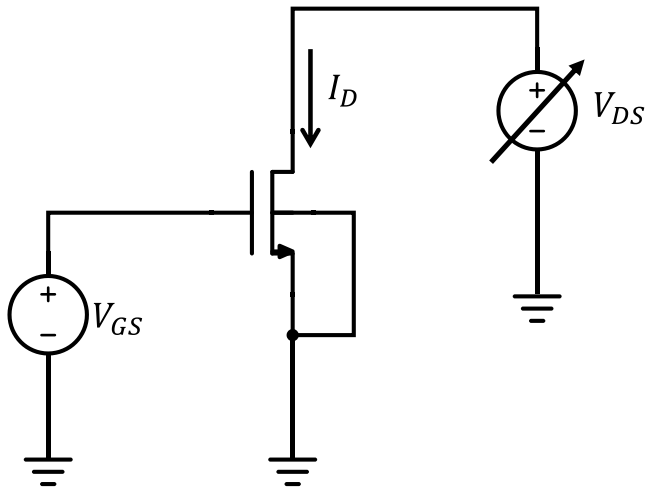
I/V Characteristics of NMOS Transistor - I_D-V_{DS}



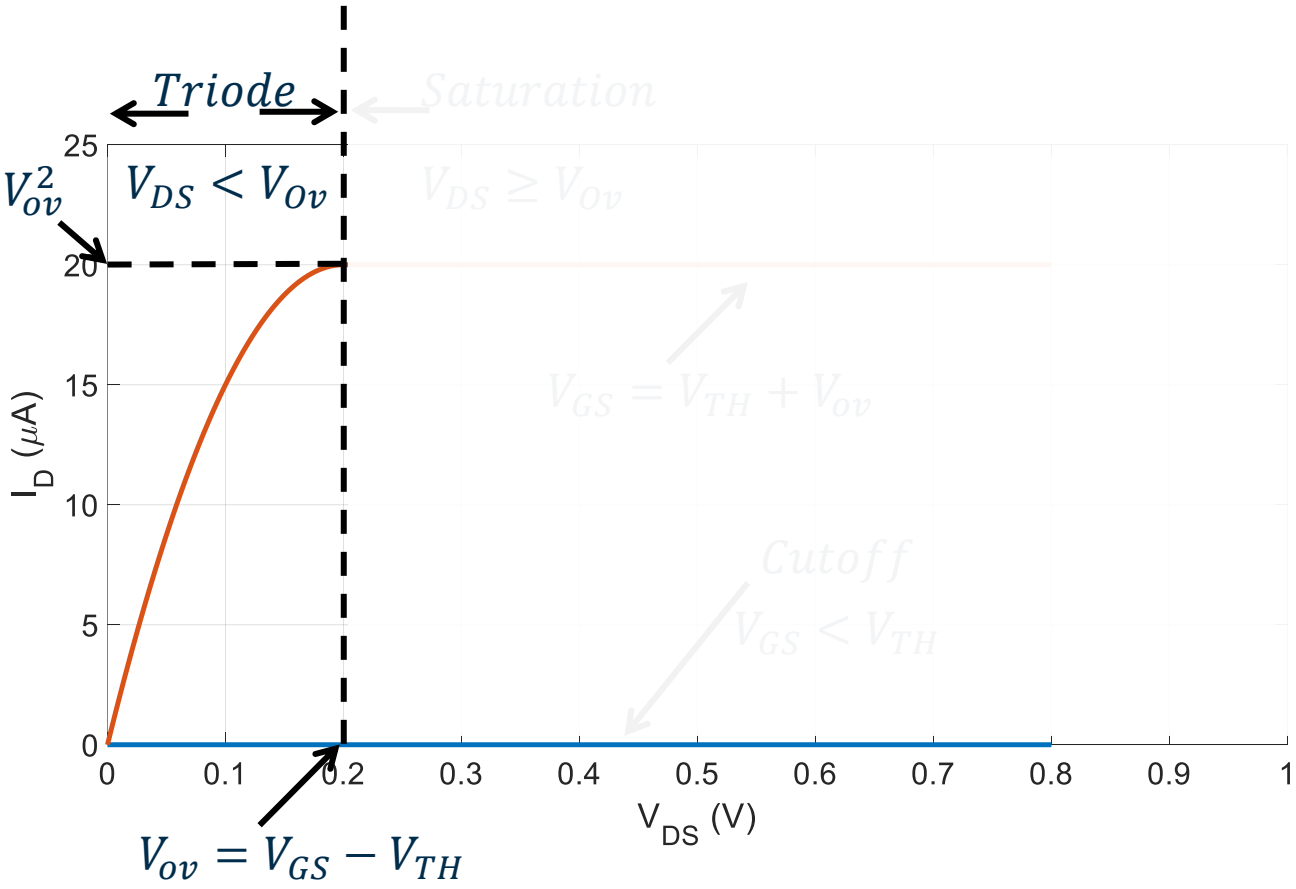
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2$$



I/V Characteristics of NMOS Transistor – I_D-V_{DS} – Triode Region



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2$$



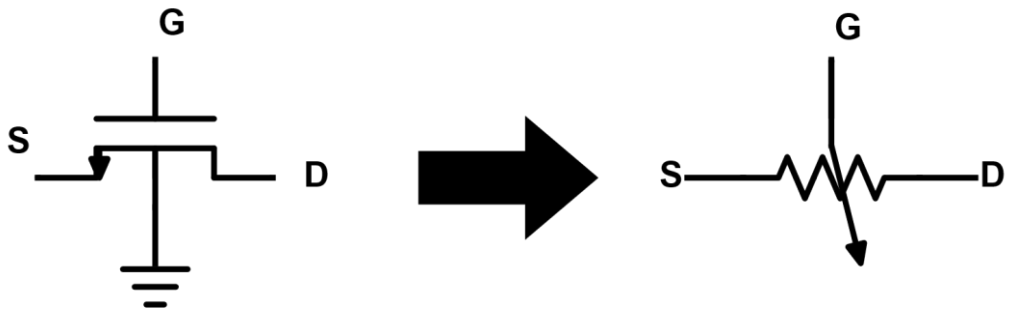
- Triode Region:

$$V_{DS} < (V_{GS} - V_{TH}) = V_{ov}$$

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[V_{ov}V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$= \mu_n C_{ox}\frac{W}{L}\left(V_{ov} - \frac{1}{2}V_{DS}\right)V_{DS}$$

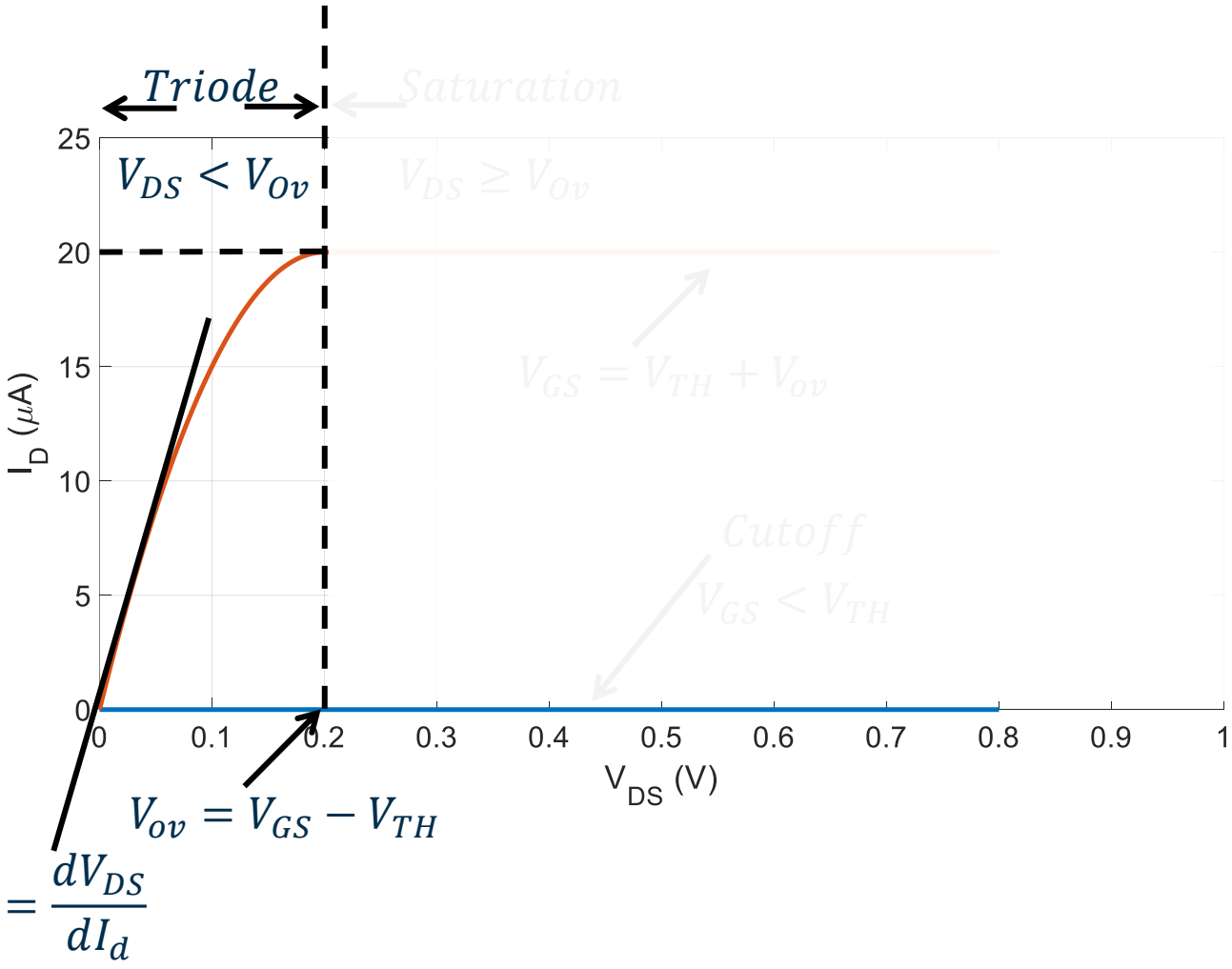
I/V Characteristics of NMOS Transistor – I_D-V_{DS} – Triode Region



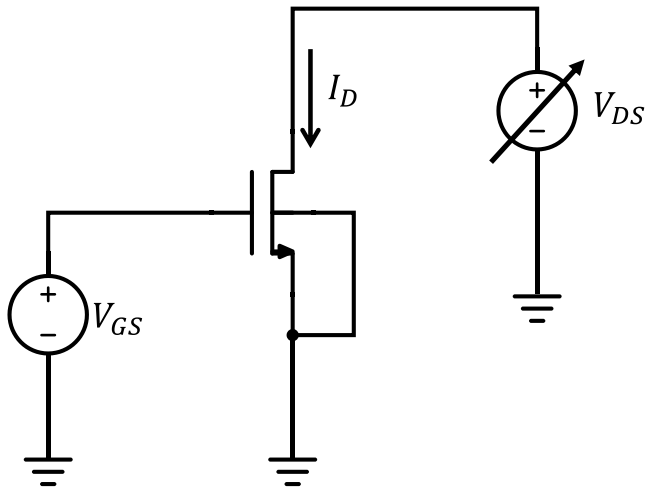
- MOSFET can operate as a voltage controlled resistor in triode region.

$$R_{on} = \frac{dV_{DS}}{dI_d} = \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{ov} - \frac{1}{2}V_{DS}\right)}$$

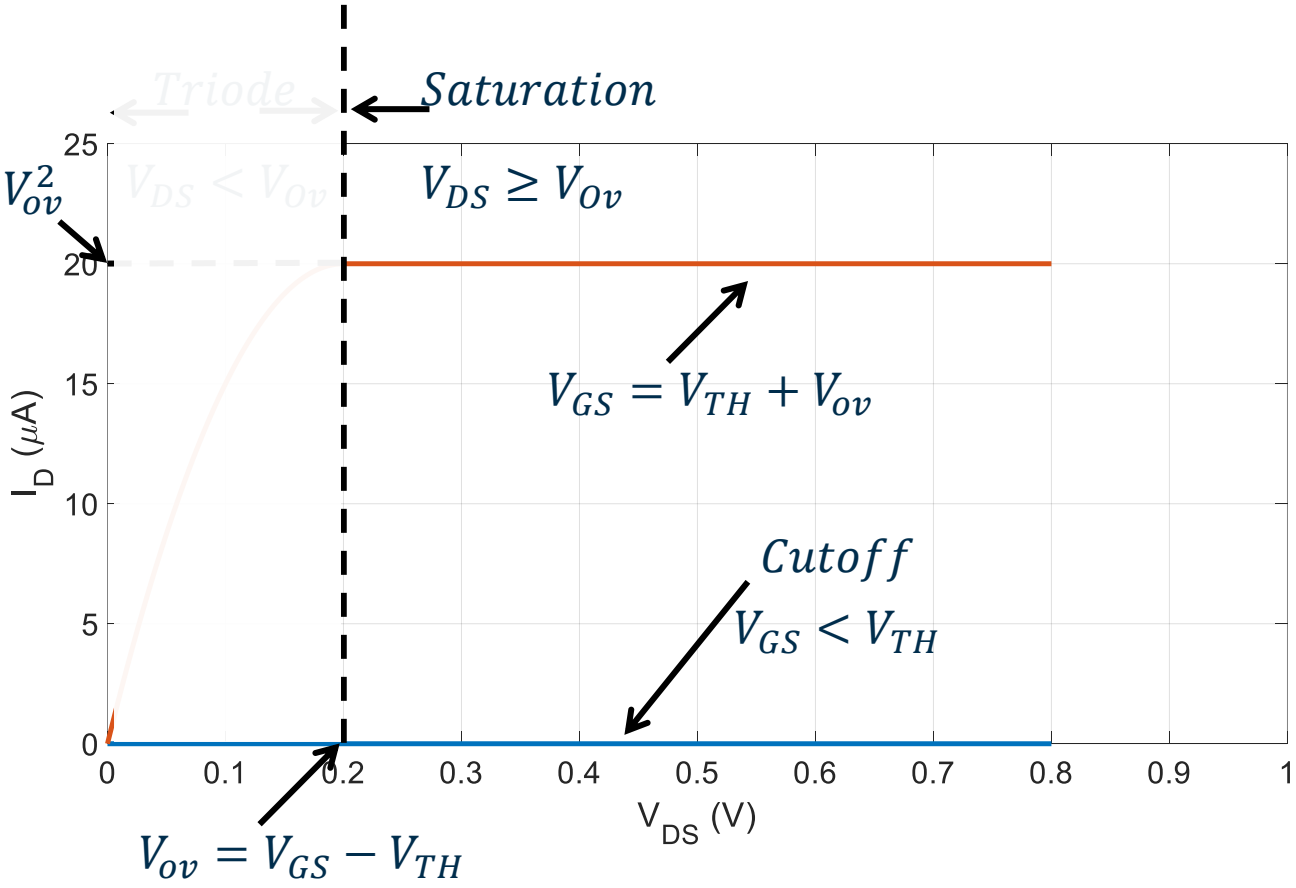
$$\boxed{R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{ov})}}$$



I/V Characteristics of NMOS Transistor – I_D-V_{DS} – Saturation Region



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2$$



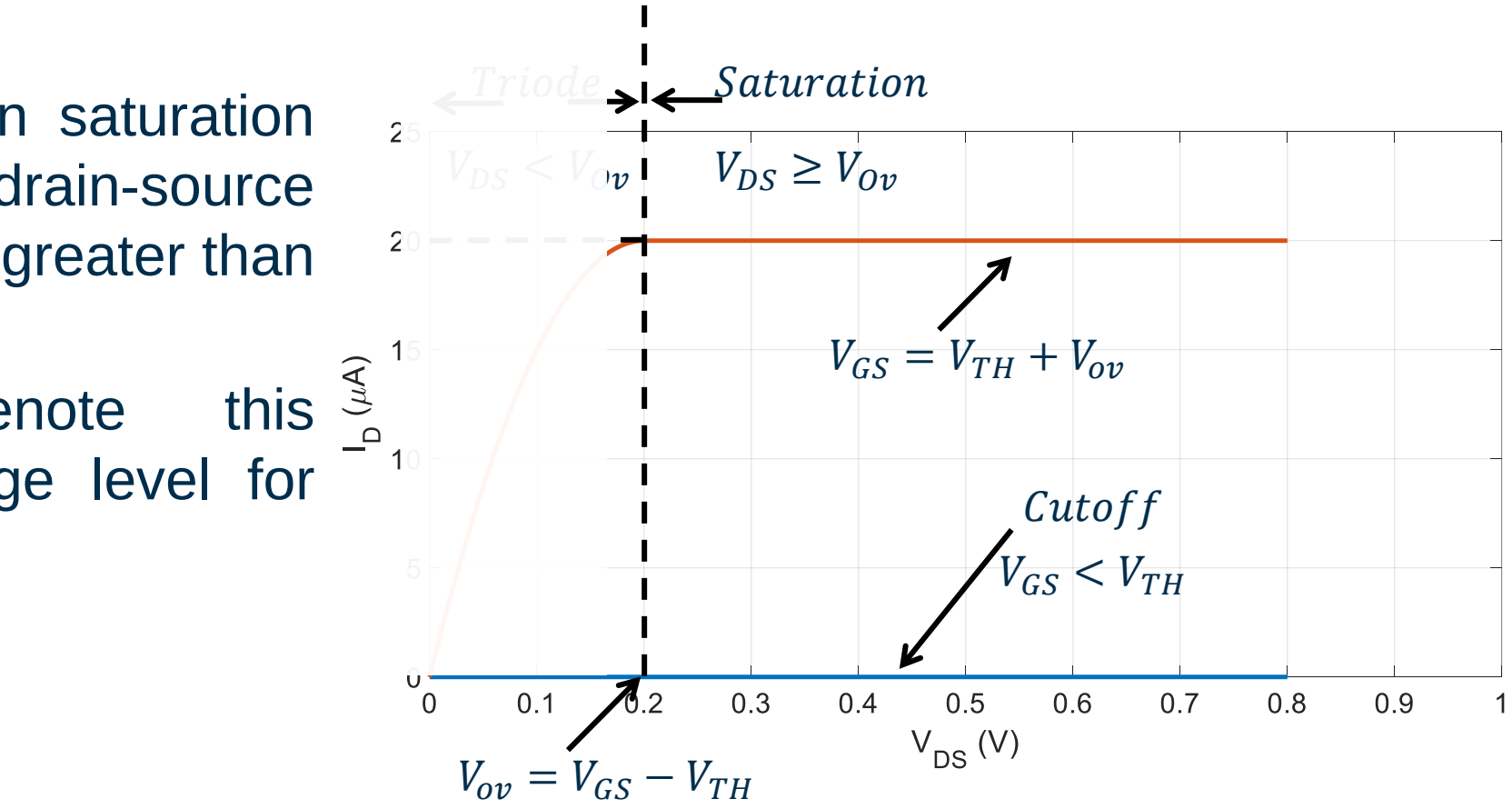
- Saturation Region:

$$V_{DS} \geq (V_{GS} - V_{TH}) = V_{ov}$$

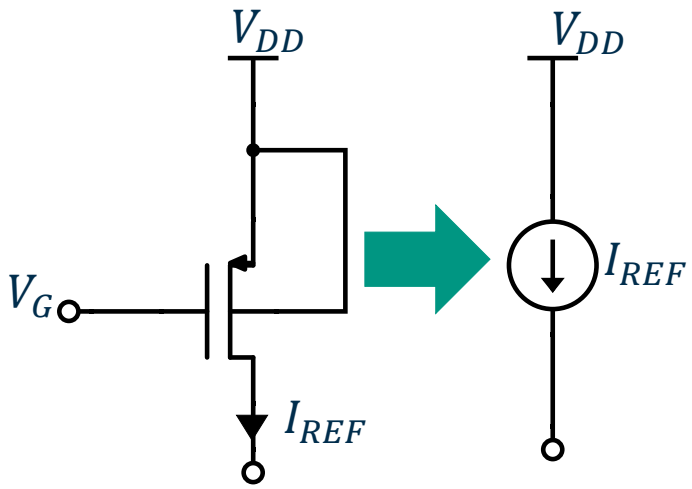
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{ov})^2$$

I/V Characteristics of NMOS Transistor – I_D-V_{DS} – Saturation Region

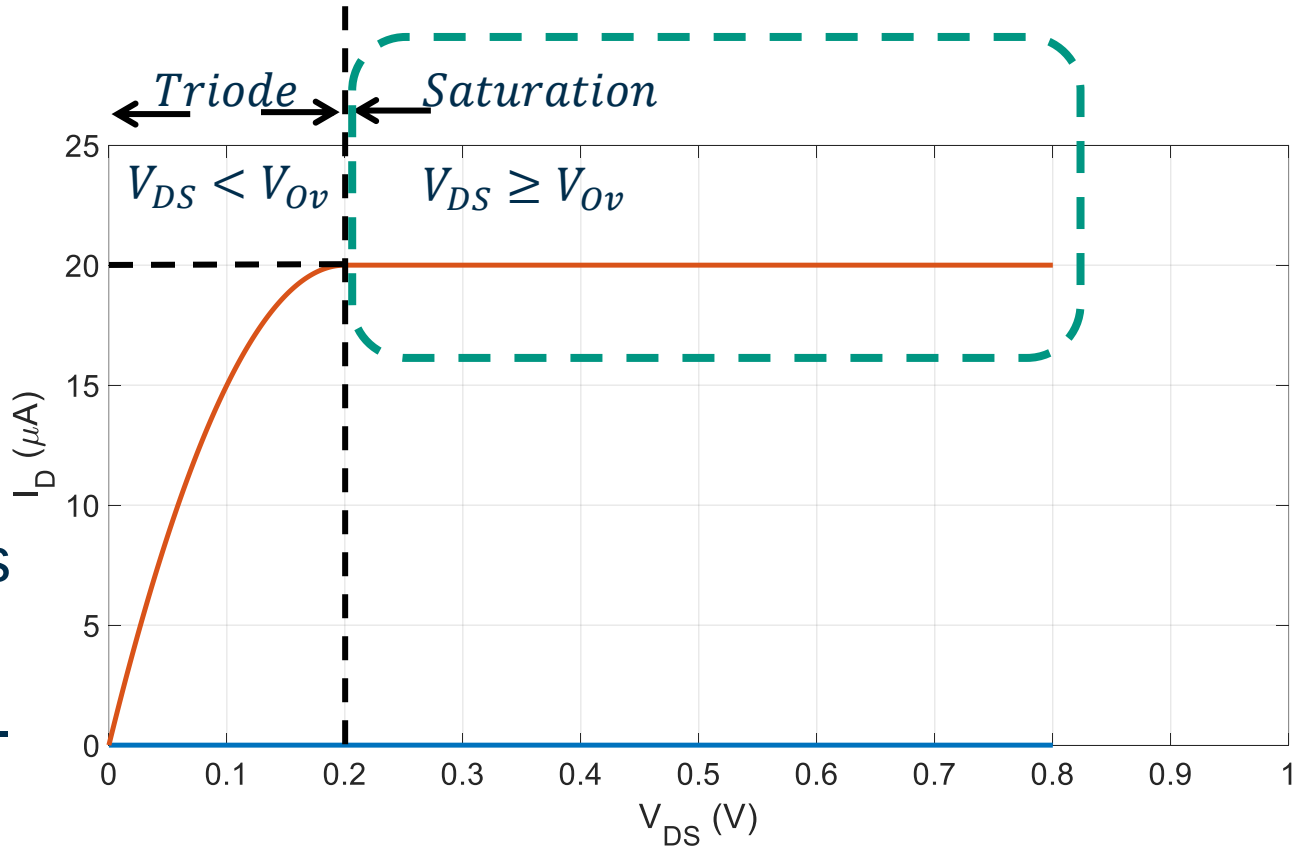
- The transistor remains in saturation region as long as the drain-source voltage V_{DS} is equal to or greater than the overdrive voltage V_{ov}.
- Some resources denote this minimum required voltage level for saturation as $\boxed{V_{D,sat}}$.



I/V Characteristics of NMOS Transistor – I_D-V_{DS} – Saturation Region



- A MOSFET in saturation operates as a current source.
- It can also be viewed as a voltage-controlled current source.



I/V Characteristics of NMOS Transistor – Pinch-off ($V_{DS} > V_{ov}$)

- Consider the drain current equation in triode region:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH} - \frac{1}{2} V_{DS} \right) V_{DS}$$

I/V Characteristics of NMOS Transistor – Pinch-off ($V_{DS} > V_{ov}$)

- Consider the drain current equation in triode region:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{1}{2}V_{DS}\right)V_{DS}$$

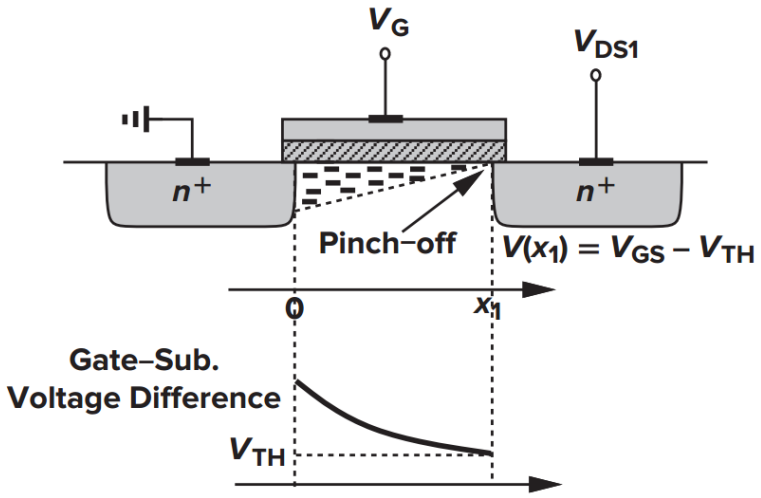
- If we replace V_{DS} by $(V_{GS} - V_{TH})$, we will get the saturation equation:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2$$

- This is a rough equation known as “square law equation„ that assumes the drain current remains independent of V_{DS} voltage after the saturation point.

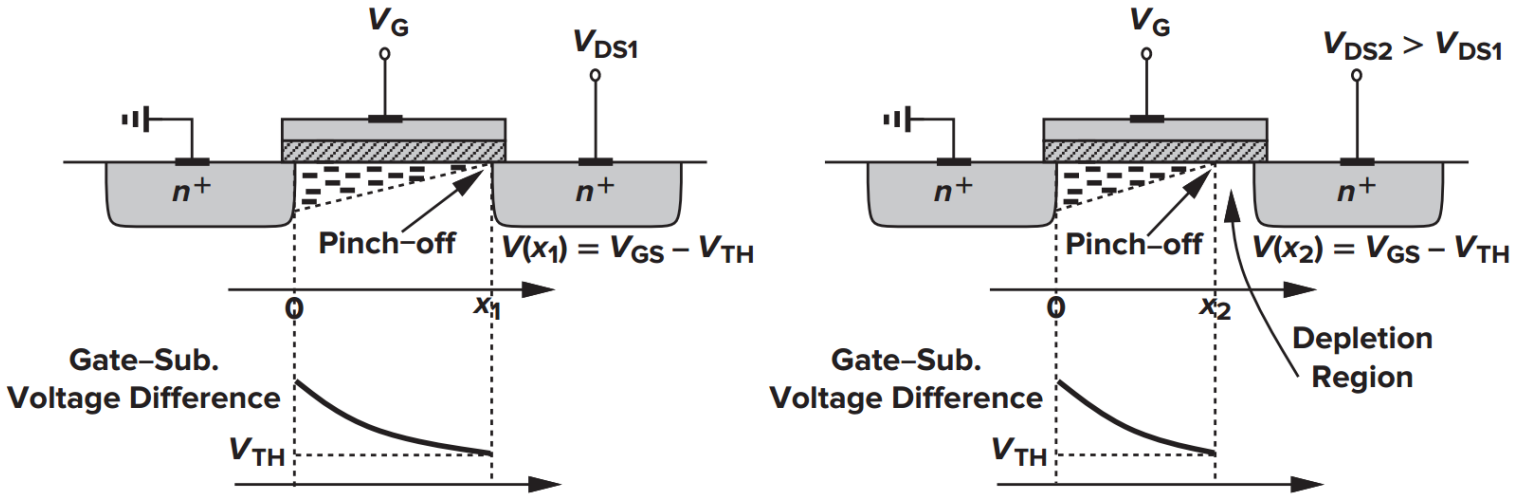
I/V Characteristics of NMOS Transistor – Pinch-off ($V_{DS} > V_{ov}$)

- As V_{DS} increases, the channel near the drain becomes narrower. This phenomenon is known as **pinch-off**.



I/V Characteristics of NMOS Transistor – Pinch-off ($V_{DS} > V_{ov}$)

- As V_{DS} increases, the channel near the drain becomes narrower. This phenomenon is known as **pinch-off**.
- Further increases in V_{DS} push the pinch-off point back toward the source, slightly reducing the effective channel length and causing a small increase in the drain current. This effect is called **channel-length modulation (CLM)**.

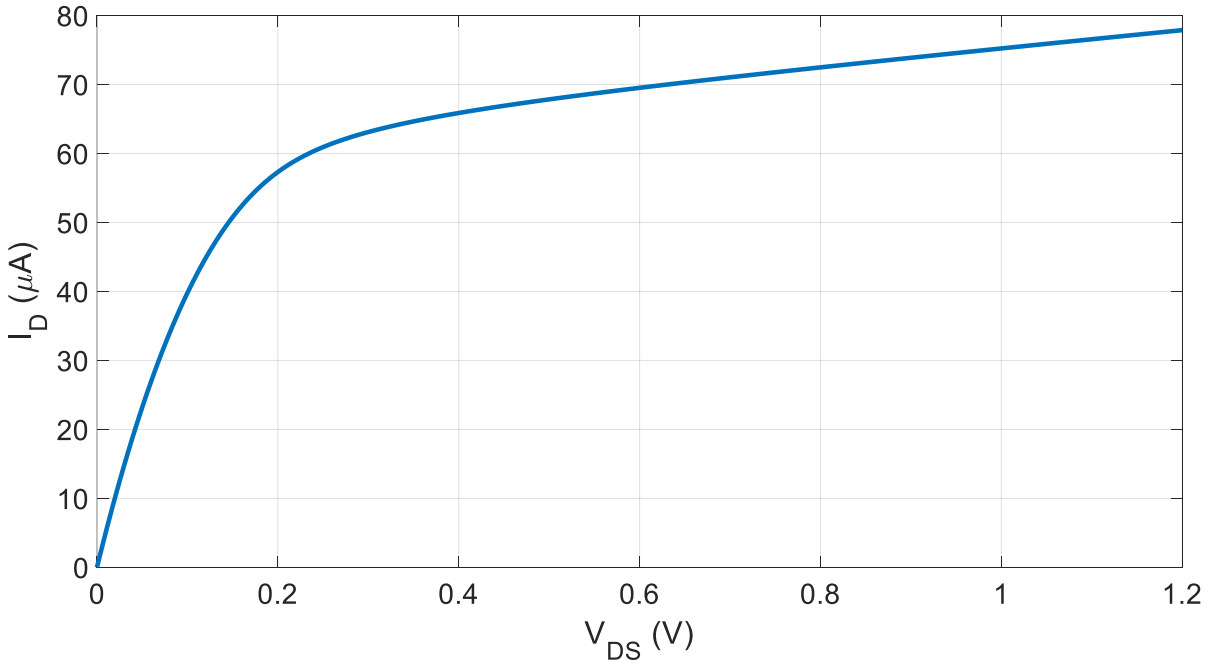


I/V Characteristics of NMOS Transistor – Channel-Length Modulation

- The current equation with channel-length modulation is given as:

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

where λ is the “channel-length modulation coefficient”.



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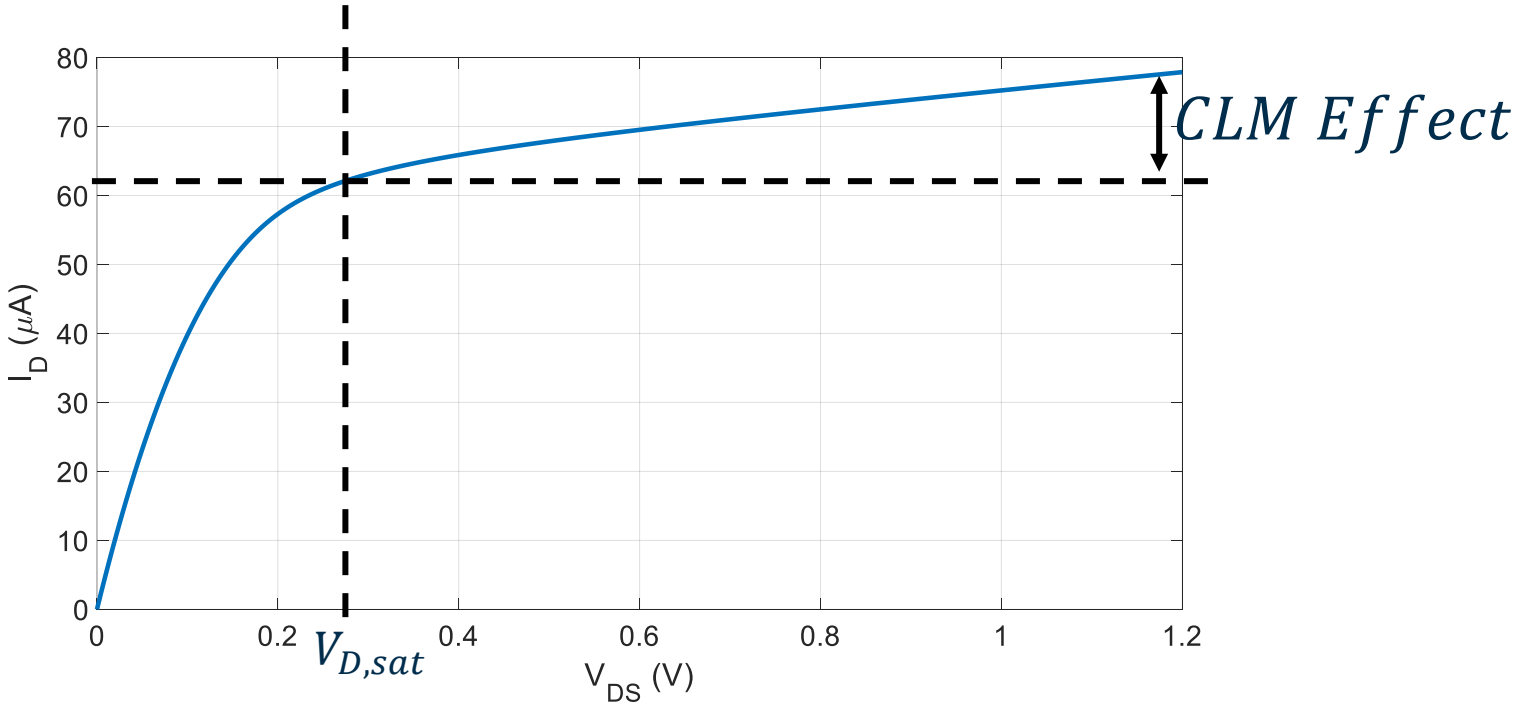
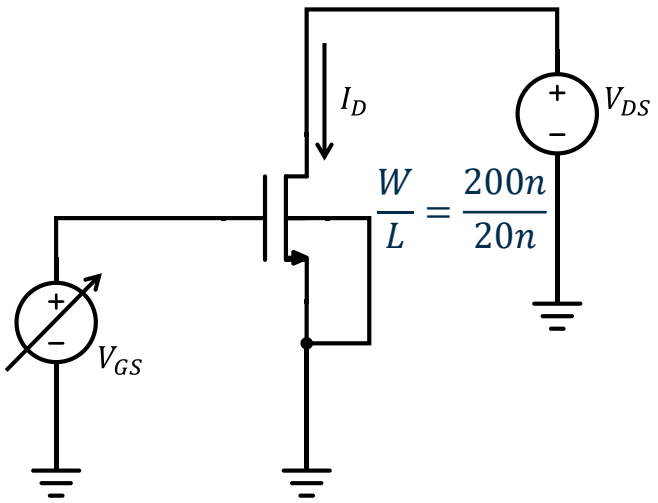
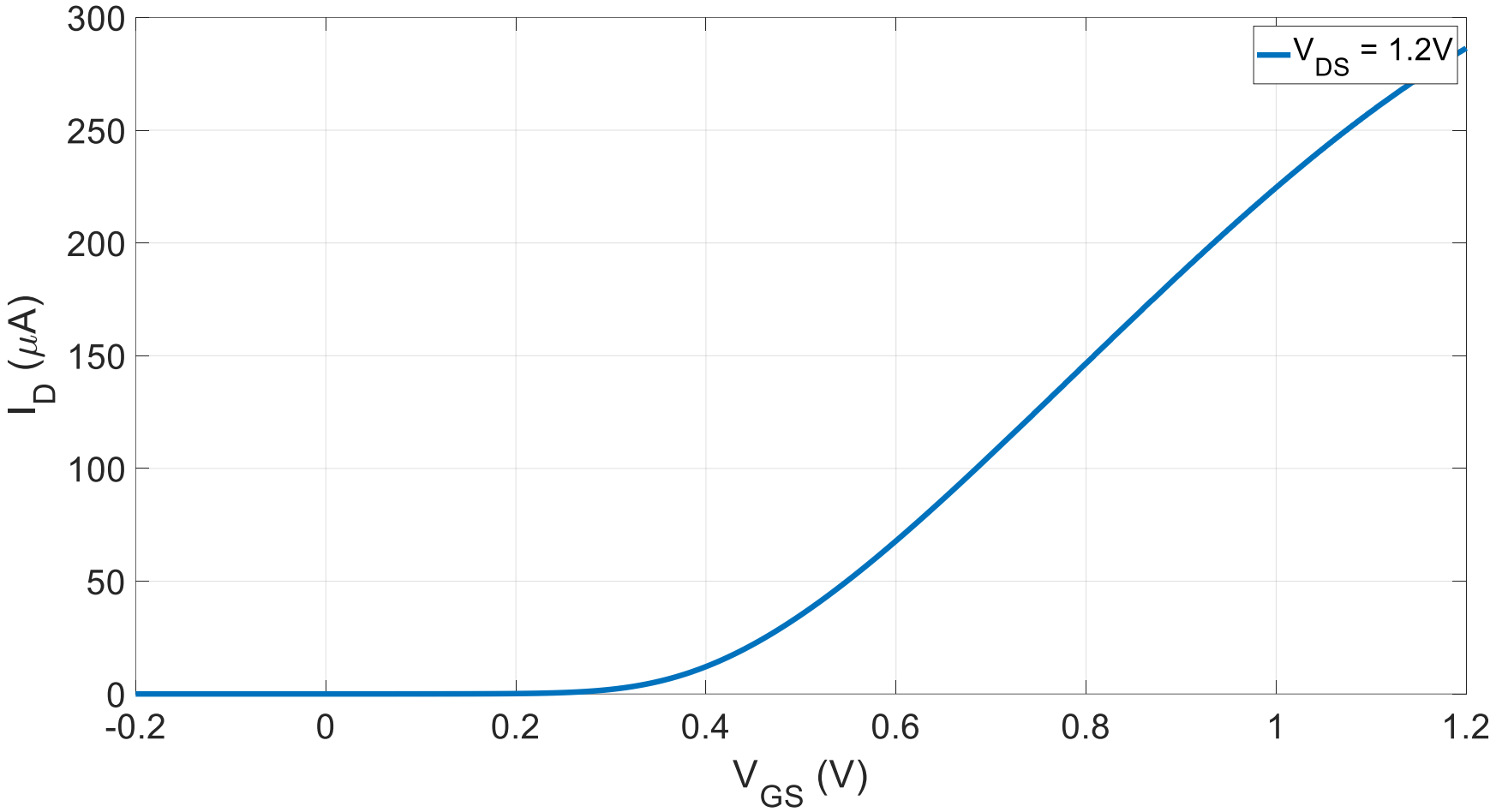


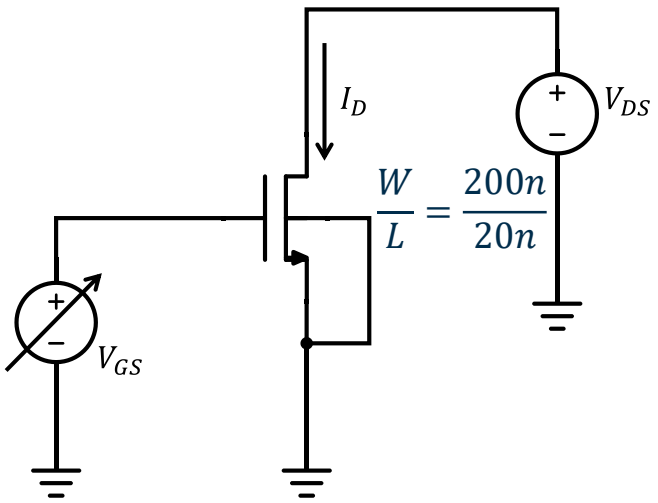
I/V Characteristics of NMOS Transistor – I_D-V_{GS}

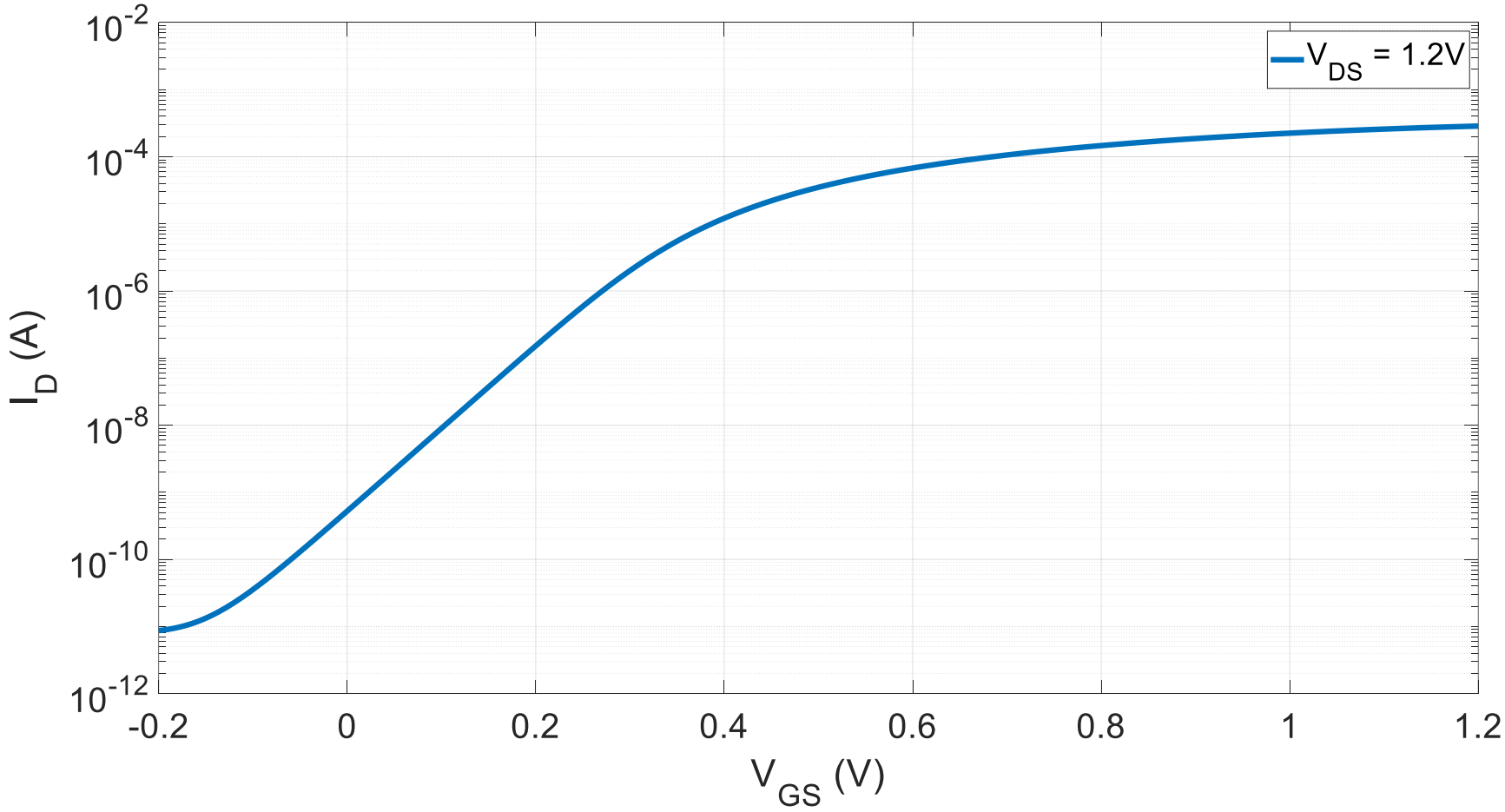
Global Foundries 22 nm CMOS simulation



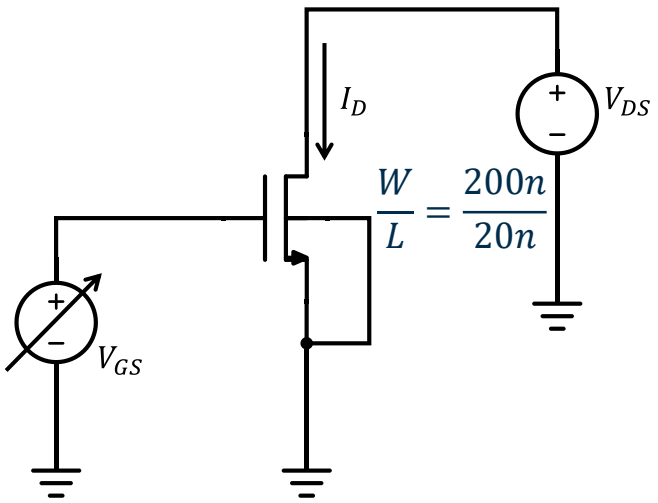


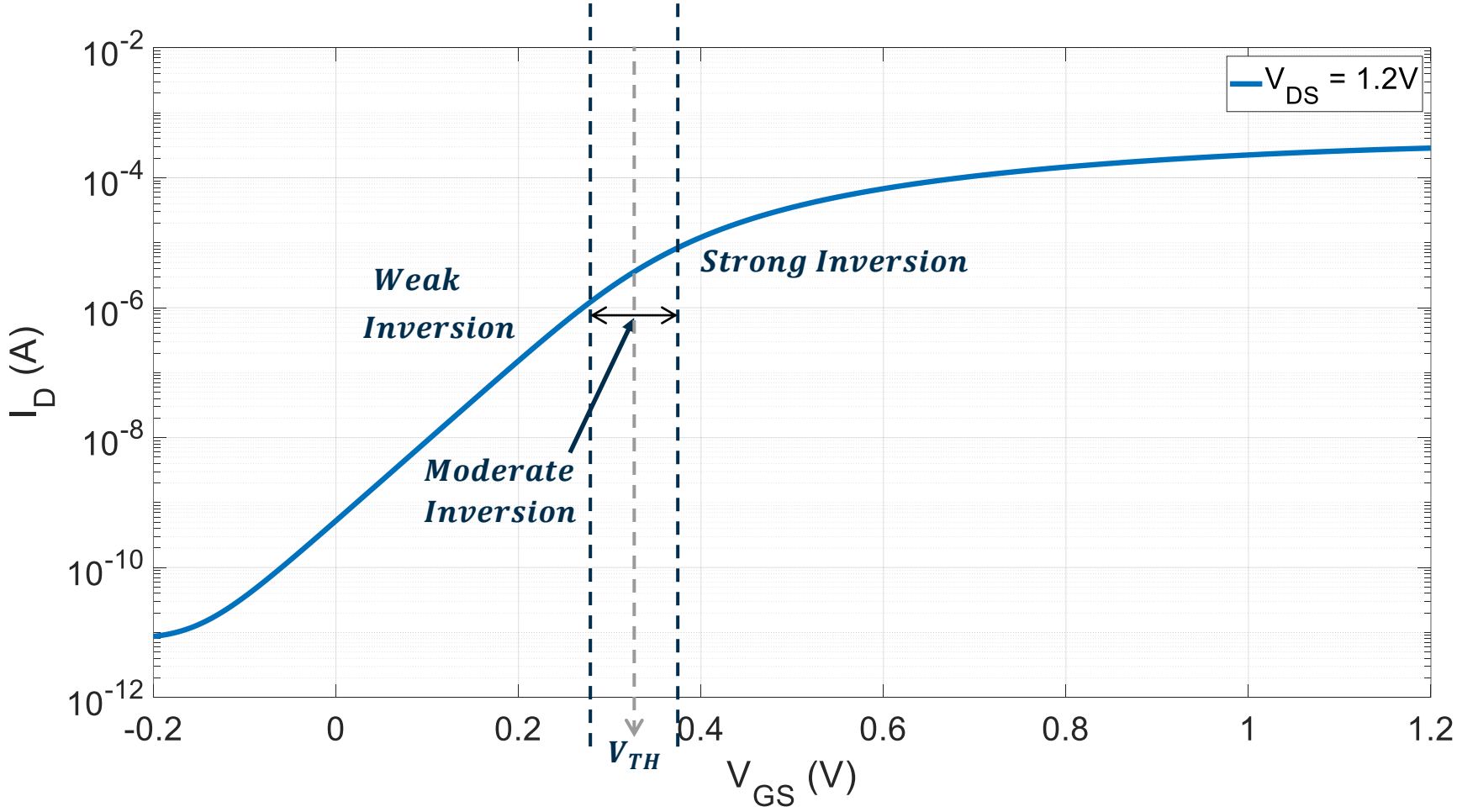
I/V Characteristics of NMOS Transistor – I_D-V_{GS} Log Scale





I/V Characteristics of NMOS Transistor – I_D-V_{GS} Log Scale

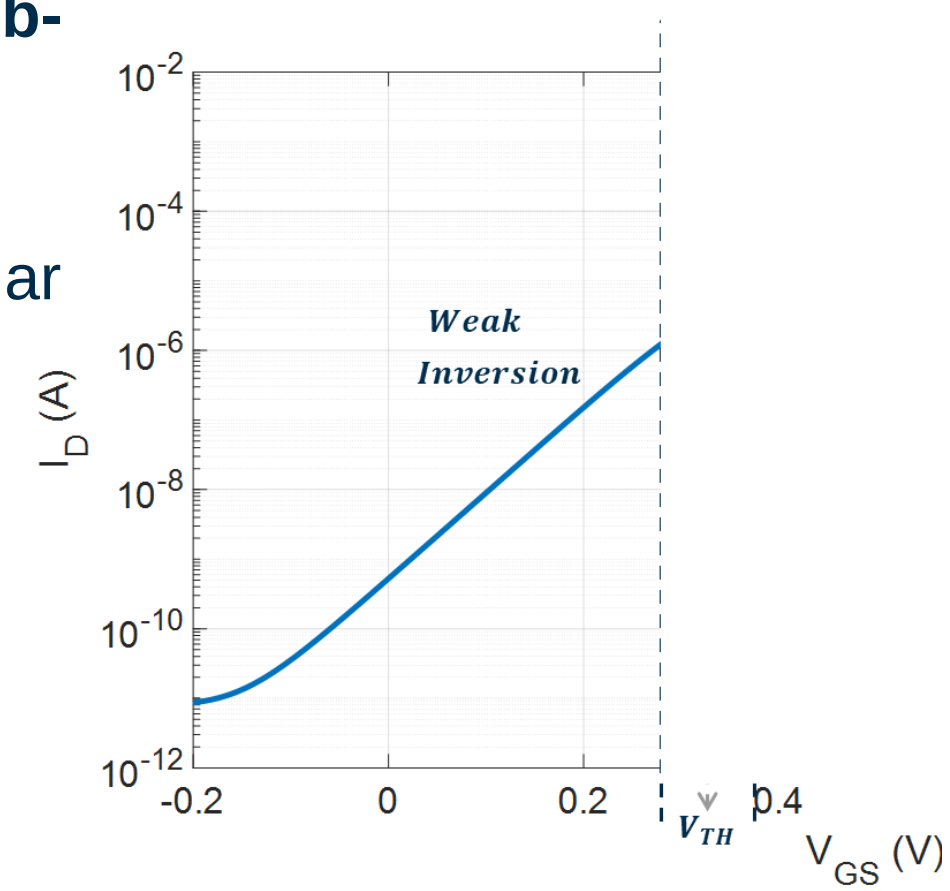




I/V Characteristics of NMOS Transistor – I_D-V_{GS} – Weak Inversion

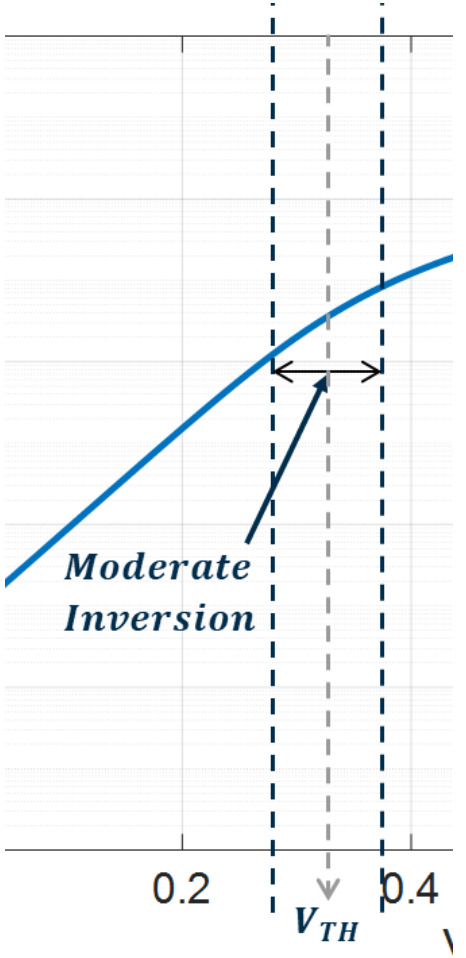
- $V_{GS} < V_{TH}$ in weak inversion (also known as **sub-threshold**).
- The channel is barely formed.
- The current grows exponentially with V_{GS}, a similar behavior with BJTs (but only in sub-threshold).

$$I_D \propto e^{V_{GS}}$$



I/V Characteristics of NMOS Transistor – I_D-V_{GS} – Moderate Inversion

- $V_{GS} \approx V_{TH}$ in moderate inversion.
- Channel is transitioning.
- It is a mix of diffusion and drift, neither exponential nor quadratic, hard to model.

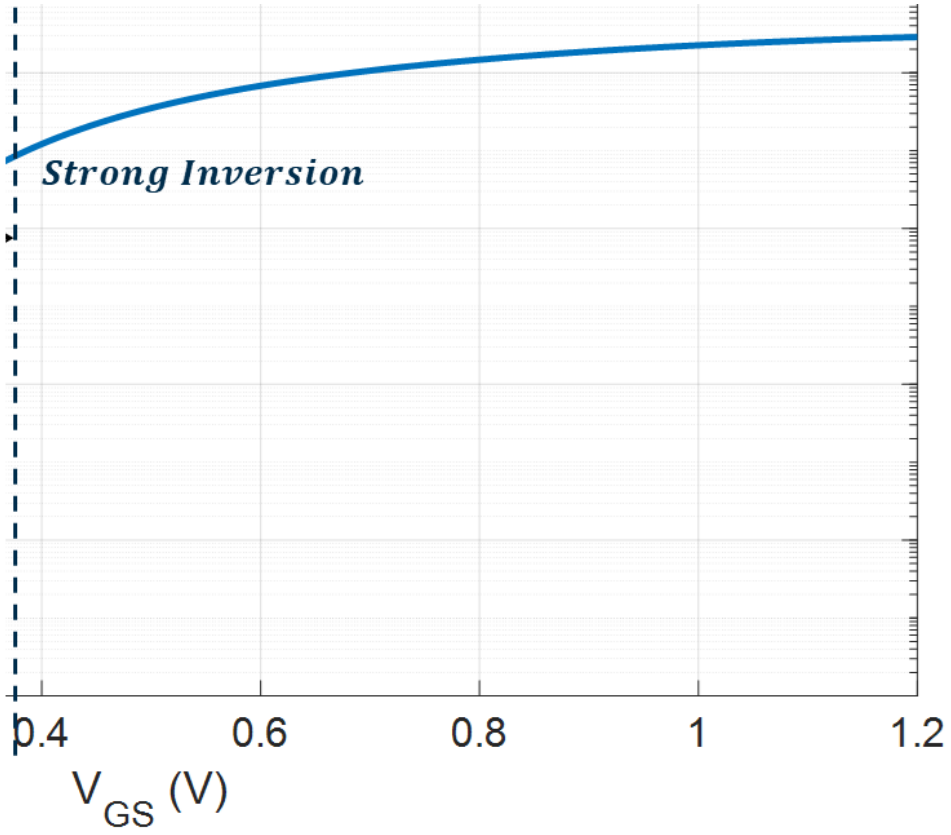


I/V Characteristics of NMOS Transistor – I_D-V_{GS} – Strong Inversion

- $V_{GS} > V_{TH}$.
- Channel is formed.
- Shows a quadratic behavior.

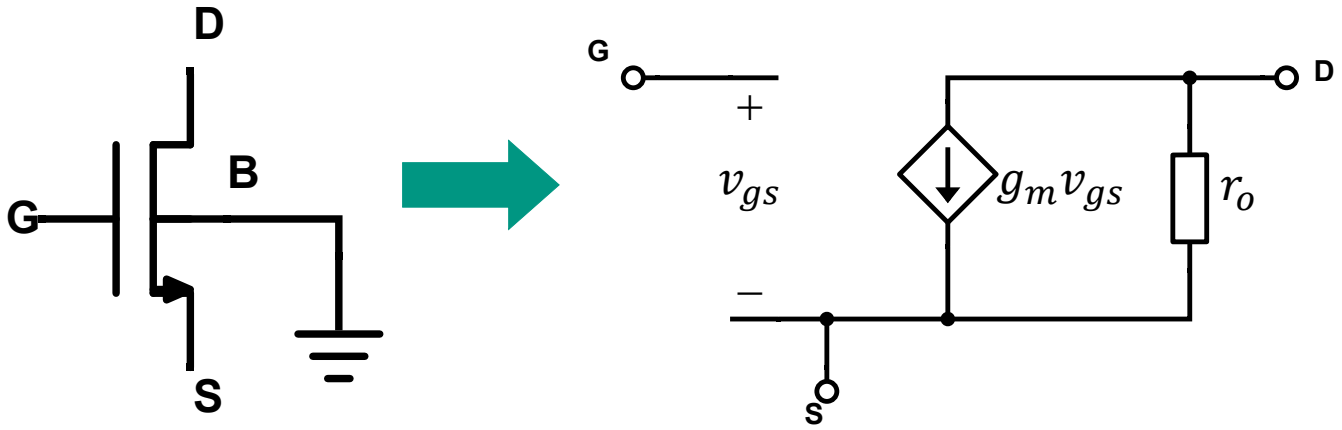
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$I_D \propto V_{GS}^2$$



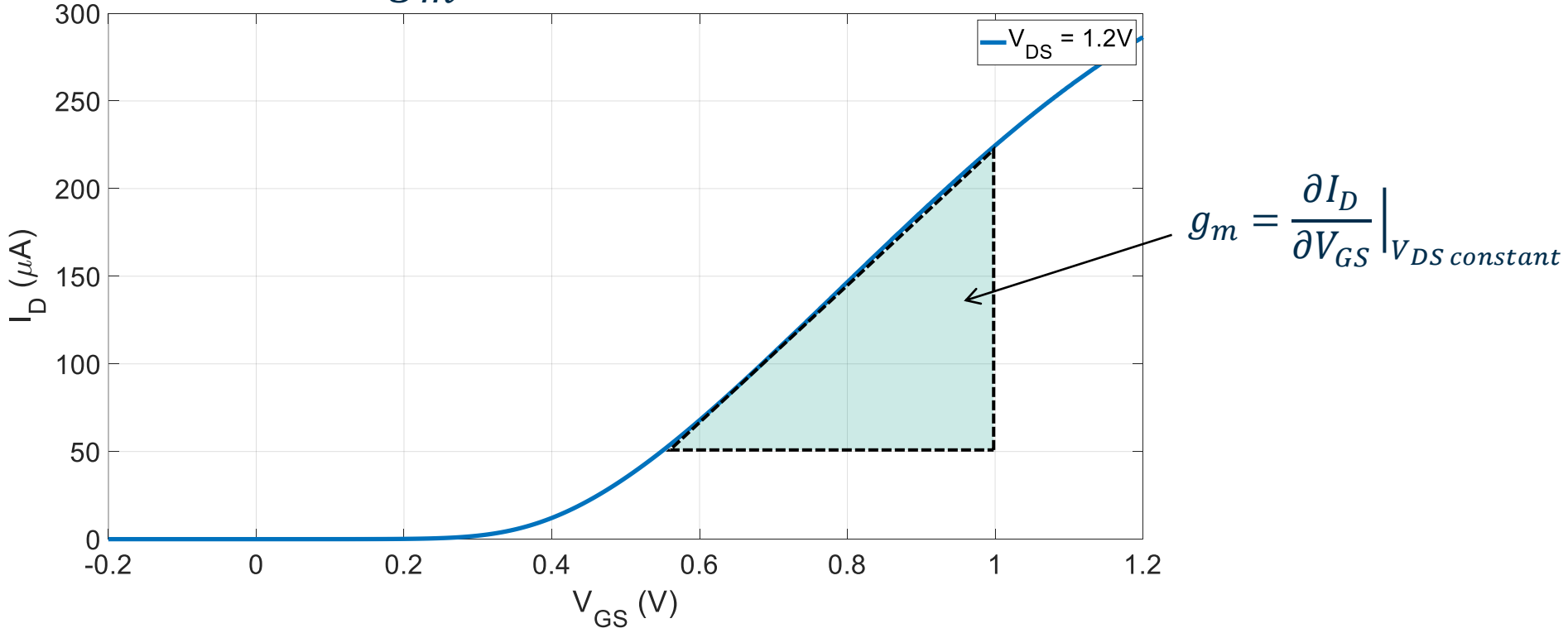
Small Signal Model

- The small-signal model is used after the MOSFET's DC bias has been established. It is commonly used when the transistor is biased in the saturation region (for amplifier analysis). Note that small-signal parameters are conventionally written in lower-case (e.g. v_{gs}, r_o, g_m).



MOS Transconductance (g_m)

- Transistors are highly nonlinear devices, yet with proper biasing and small signal swings, they behave almost linearly, allowing us to model them using quantities like transconductance g_m.



MOS Transconductance (g_m)

- Transconductance measures how effectively the gate voltage controls the drain current. It can be expressed in terms of various device parameters.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}\,constant} = \frac{\partial\left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2\right)}{\partial V_{GS}}$$

$$\boxed{g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})} \qquad \boxed{g_m = \sqrt{2 I_D \mu_n C_{ox}\frac{W}{L}}} \qquad \boxed{g_m = \frac{2I_D}{V_{GS}-V_{TH}}}$$

Output Resistance (r_o)

- We have previously seen that due to the channel-length modulation, the drain current also varies with the drain-source voltage. This effect can be modeled by a voltage-dependent current source, but a current source whose value linearly depends on the voltage across it is equivalent to a linear resistor. This resistor is given by:

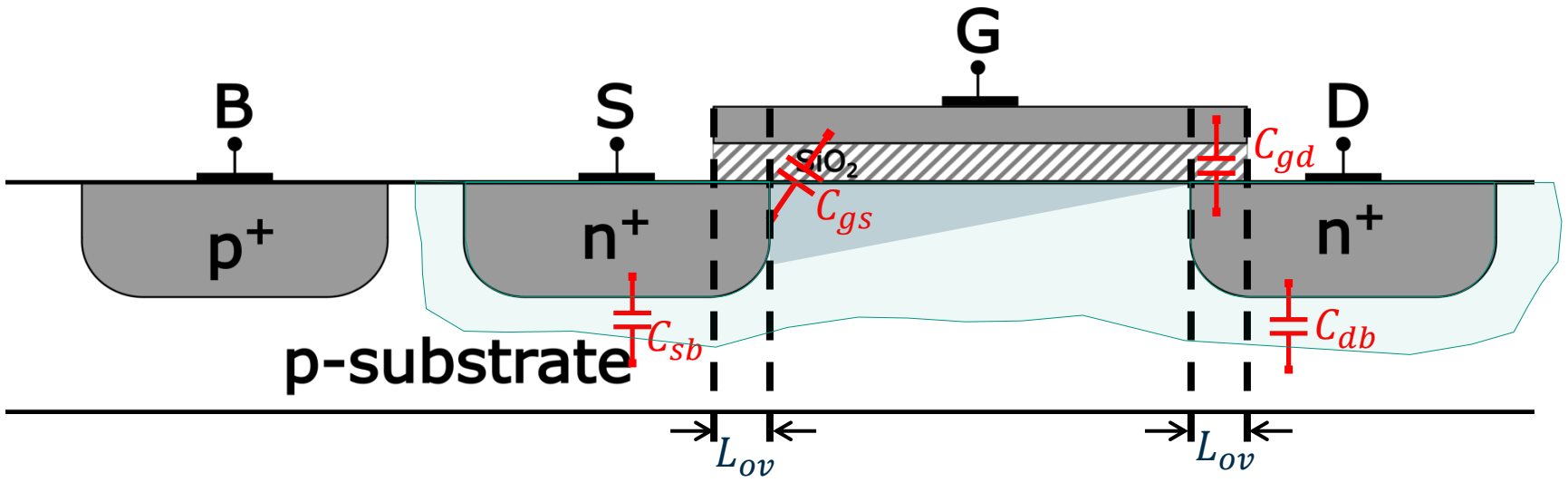
$$r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}}$$

$$= \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \cdot \lambda}$$

$$\boxed{\mathrm{r_o} \approx \frac{1}{\lambda \cdot I_D}}$$

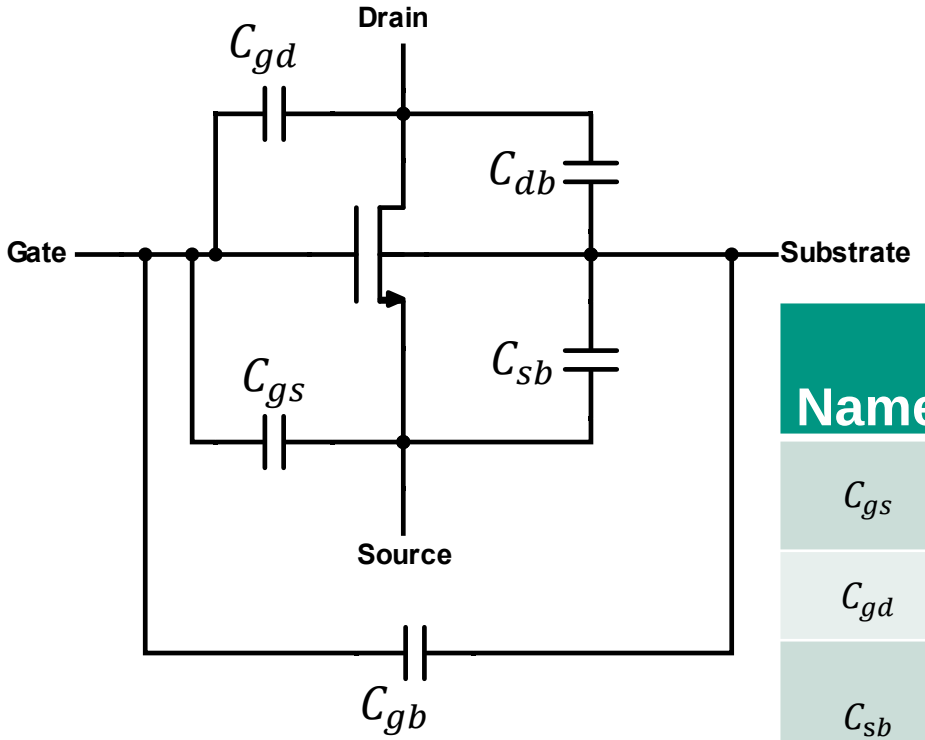
MOSFET Capacitances

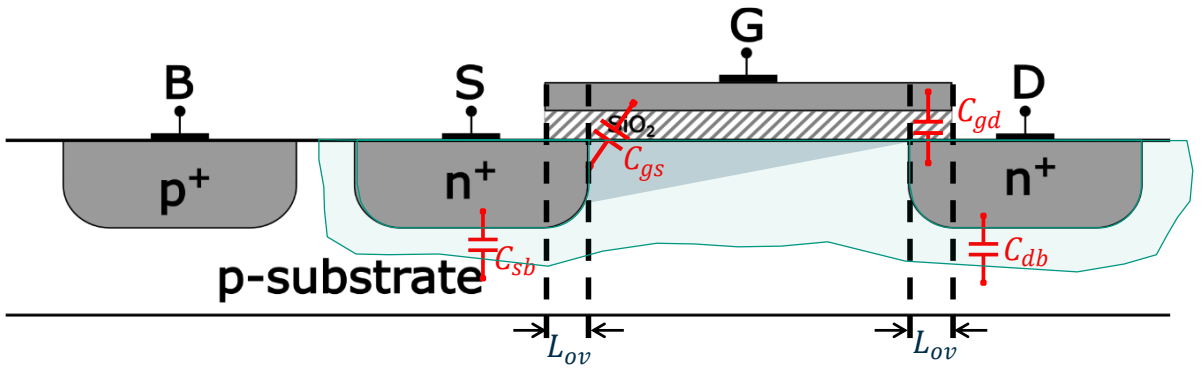
- The cross section of an NMOS operating in the saturation region is given below with the parasitic capacitances.



$$C_{ov} = WL_{ov}C_{ox} \quad C_{gs} = \frac{2}{3}WLC_{ox} + C_{ov} \quad C_{gd} = C_{ov} \quad C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{\phi_0}}} \quad C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{\phi_0}}}$$

MOSFET Capacitances





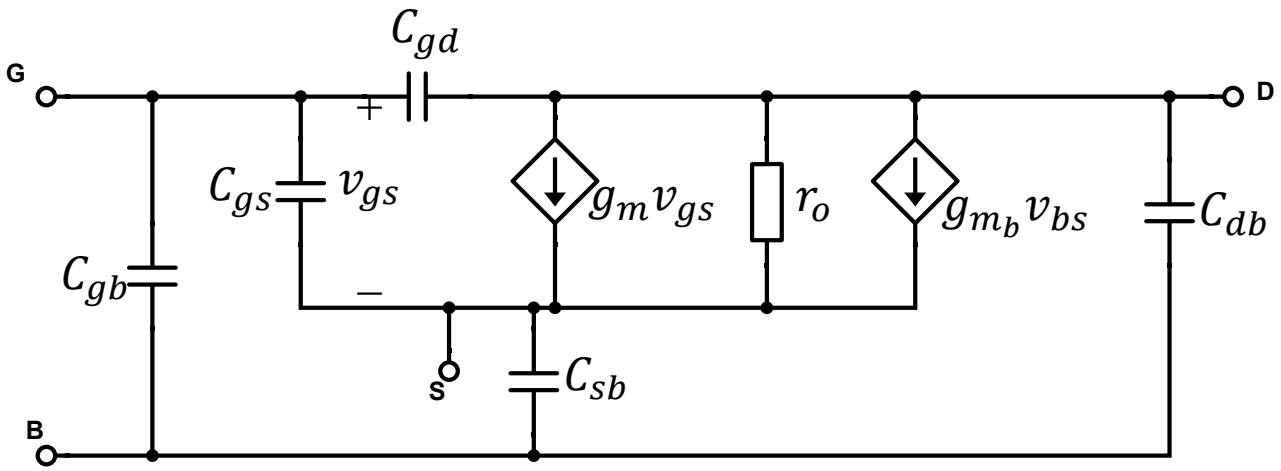
Name	Value in Saturation	Value in Triode
C_{gs}	$\frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$	$\frac{1}{2}WLC_{ox} + WL_{ov}C_{ox}$
C_{gd}	$WL_{ov}C_{ox}$	$\frac{1}{2}WLC_{ox} + WL_{ov}C_{ox}$
C_{sb}	$\frac{C_{sb0}}{\sqrt{1+\frac{V_{SB}}{\phi_0}}}$	$\frac{C_{sb0}}{\sqrt{1+\frac{V_{SB}}{\phi_0}}}$
C_{db}	$\frac{C_{db0}}{\sqrt{1+\frac{V_{DB}}{\phi_0}}}$	$\frac{C_{db0}}{\sqrt{1+\frac{V_{DB}}{\phi_0}}}$
C_{gb}	$Omitted$	$Omitted$

- L_{ov}: Overlap length
- C_{sb0}: The value of C_{sb} at zero body-source bias.
- C_{db0}: The capacitance value at zero reverse-bias voltage.
- ϕ_0: Built-in junction potential

Complete MOS Small Signal Model

- The bulk potential affects the threshold voltage and therefore the overdrive voltage. The small-signal sensitivity of drain current to the bulk voltage is called the body transconductance.

$$g_{m_b} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \left(-\frac{\partial V_{TH}}{\partial V_{BS}} \right)$$



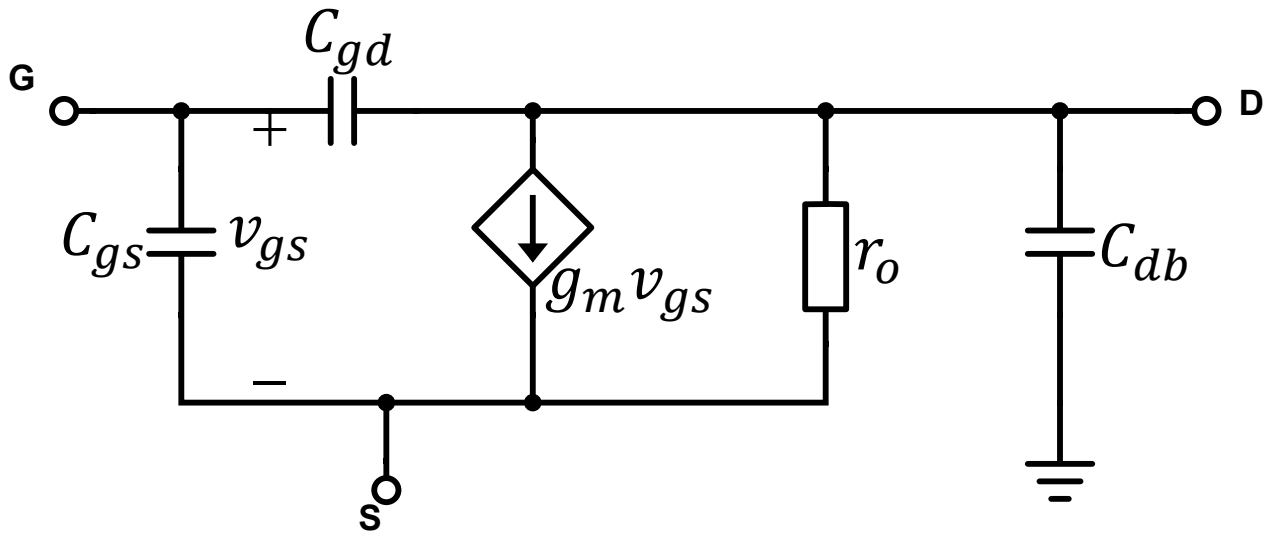
$$g_{m_b} = \eta g_m$$

$$\eta = \frac{g_{m_b}}{g_m}$$

η is typically around 0.1.

Simplified MOS Small Signal Model

- The full MOSFET model is more complex, but it is typically simplified for hand calculations and small-signal analysis.



MOSFET Scaling

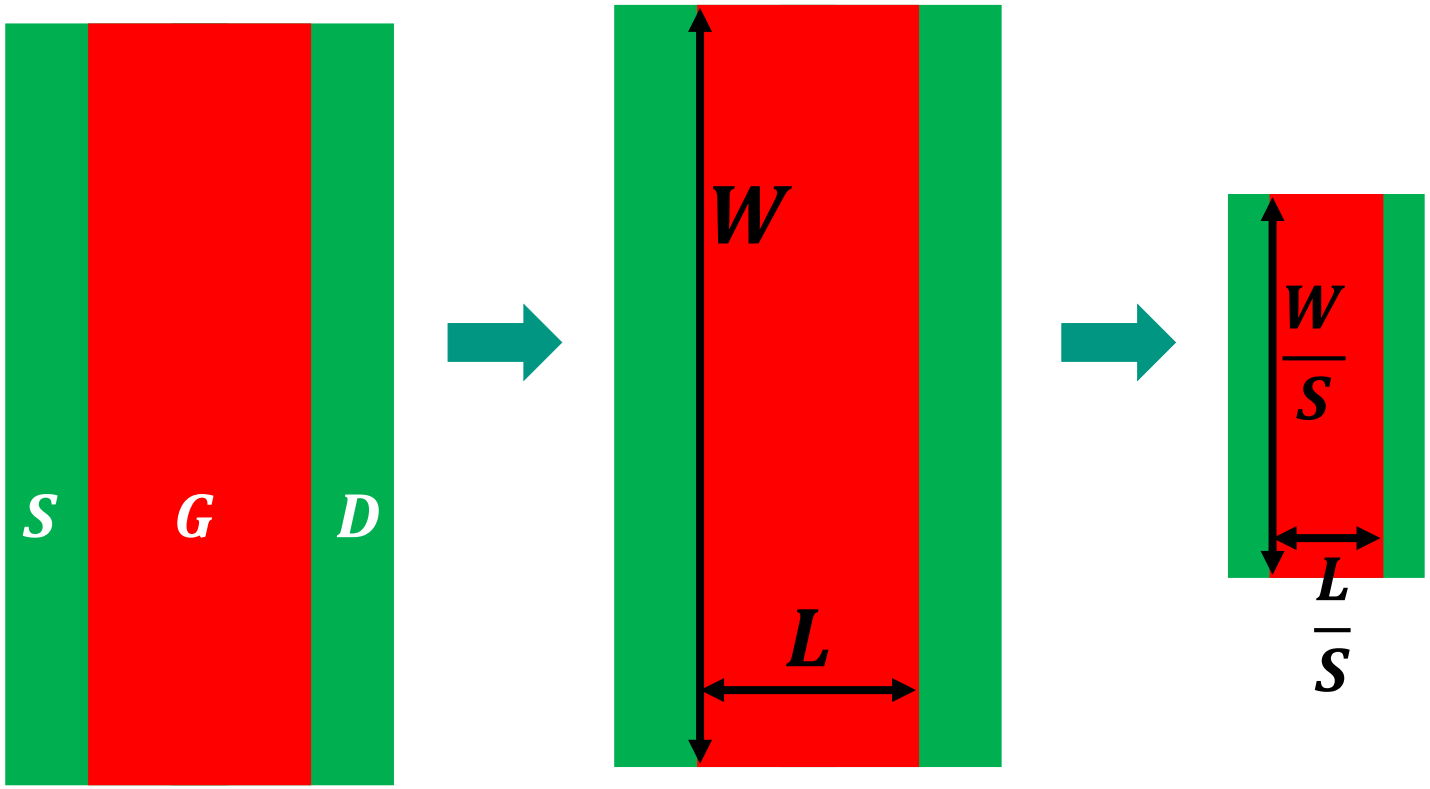
- **Moore‘s Law:** The number of transistors in an integrated circuit doubles roughly every two years.

Why scale transistors?

- Downscaling allows more transistors to fit in the same area.
- Smaller transistors have smaller parasitic capacitances, resulting in faster circuits.
- Higher number of transistors enables more functionality.
- **Downscaling theory:** It was first formalized by Dennard[7]. However, Dennard scaling is no longer fully valid due to short-channel effects and voltage scaling limits.

MOSFET Scaling

Downscaling a Transistor By S



Property	Prameter	Scaled by
MOSFET Length	L	$1/S$
MOSFET Width	W	$1/S$
Oxide thickness	t_{ox}	$1/S$
Supply Voltage	V_{DD}	$1/S$
Substrate Doping	N_A	S
Device Area	$W.L$	$1/S^2$

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