Mikroelektronische Schaltungen und Systeme

Lect 5.
Current Sources

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Mikroelektronische Schaltungen und Systeme

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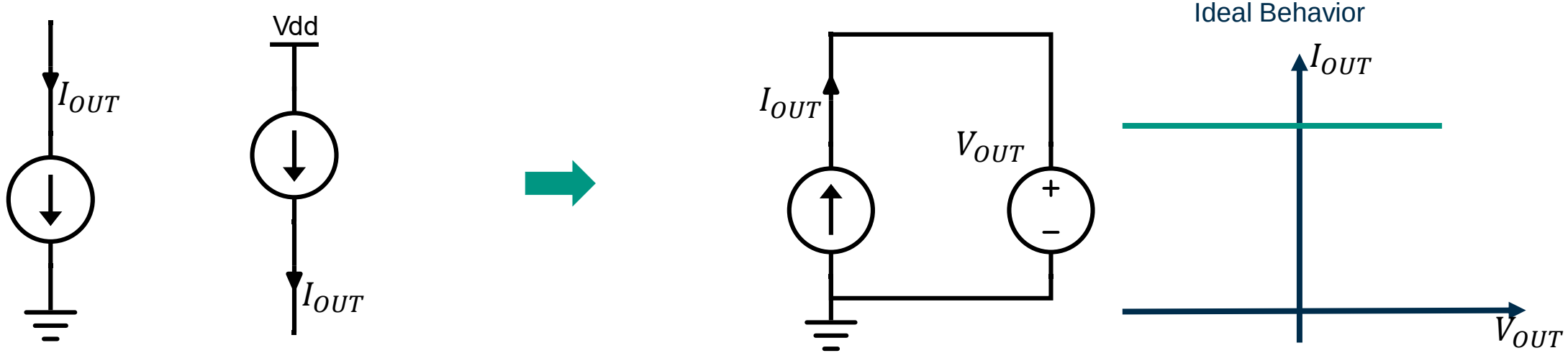
Current Mirror

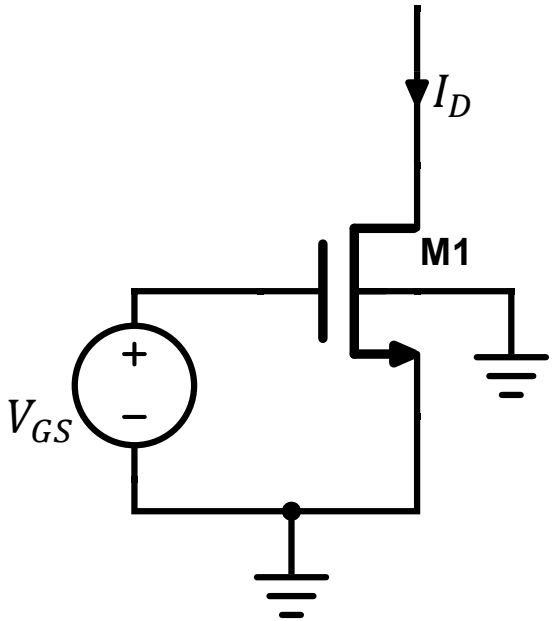
Introduction

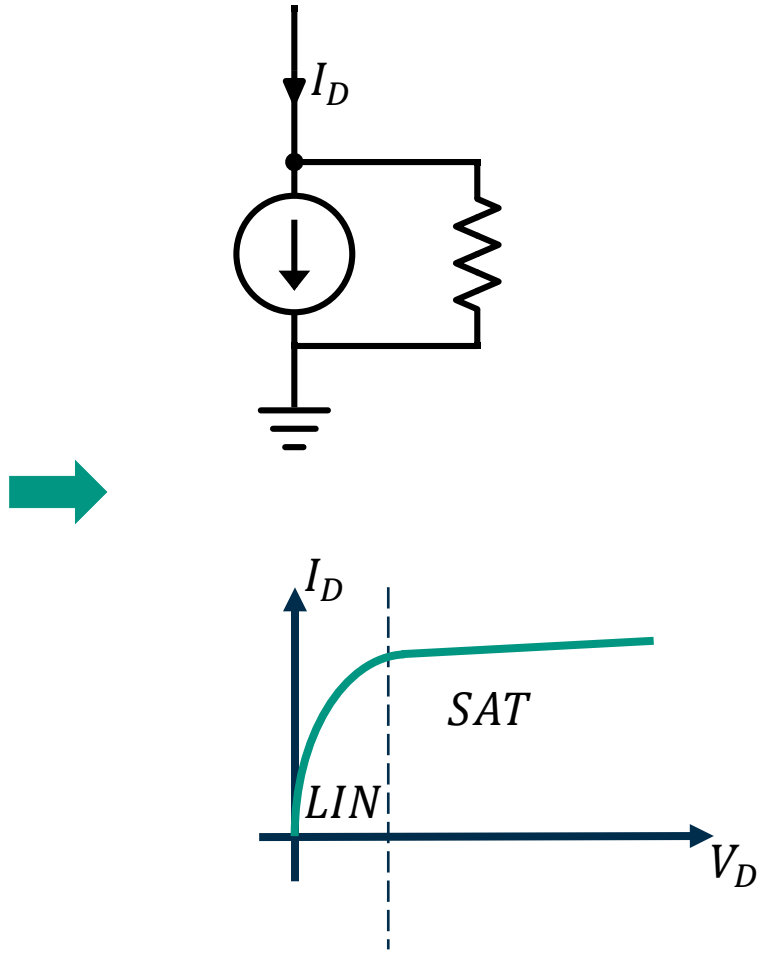
- Current sources are fundamental components for biasing analog circuits.
- Two main types:
  - Current Sink → draws current from the load
  - Current Source → supplies current to the load



Introduction

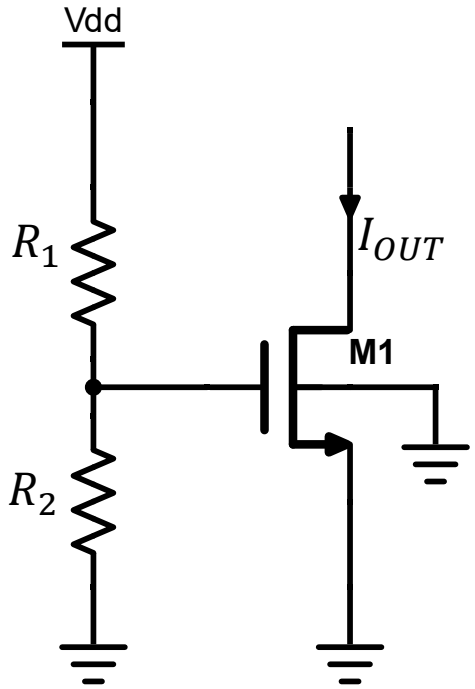
- M1 is at saturation so I_D current is flowing under control of V_{GS}
- Non-ideal MOSFET has finite output resistance, $\frac{1}{\lambda I_D}$
- There is a minimum output voltage for the MOSFET current source, $V_{DS_{sat}}$ to keep M1 in saturation region





Basic Current Source

- A simple current source uses a MOS transistor with a resistive voltage divider.



- Assume M1 operates in saturation.

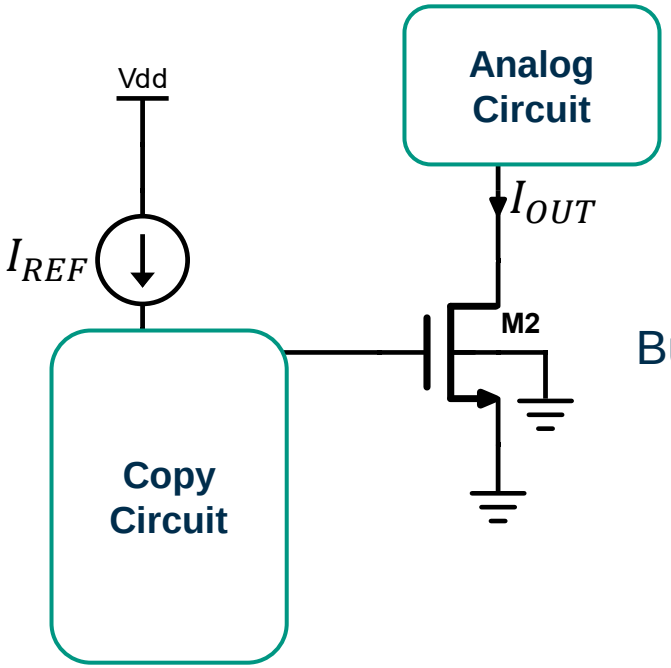
$$I_{OUT} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_1}{R_1+R_2}V_{DD}-V_{TH}\right)^2$$

- R_1 & R_2 values has certain tolerance
- V_{DD} may vary
- R_1 & R_2 vary with temperature

→ No stable current output due to PVT variations!!

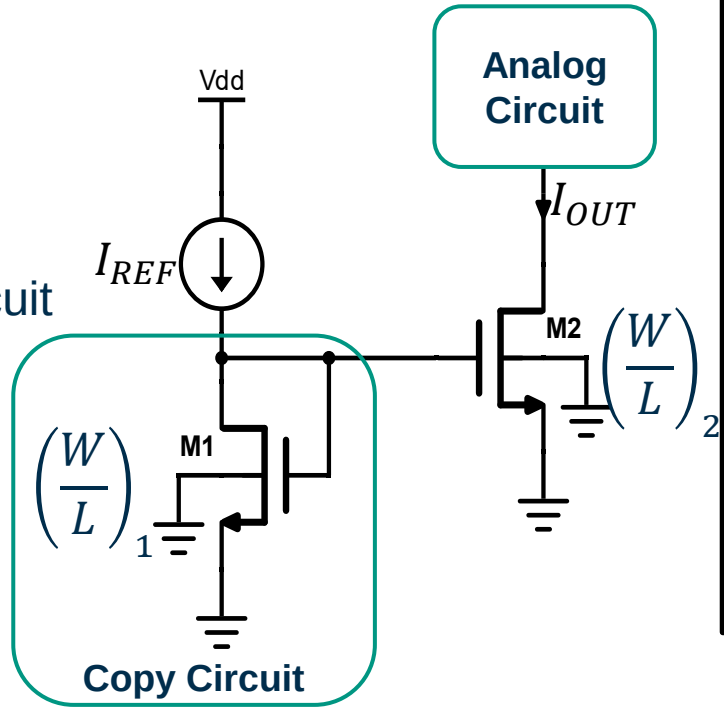
Current Mirror

- The idea of copying current



$I_{OUT} = I_{REF}$

Build „MIRROR“ circuit



$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

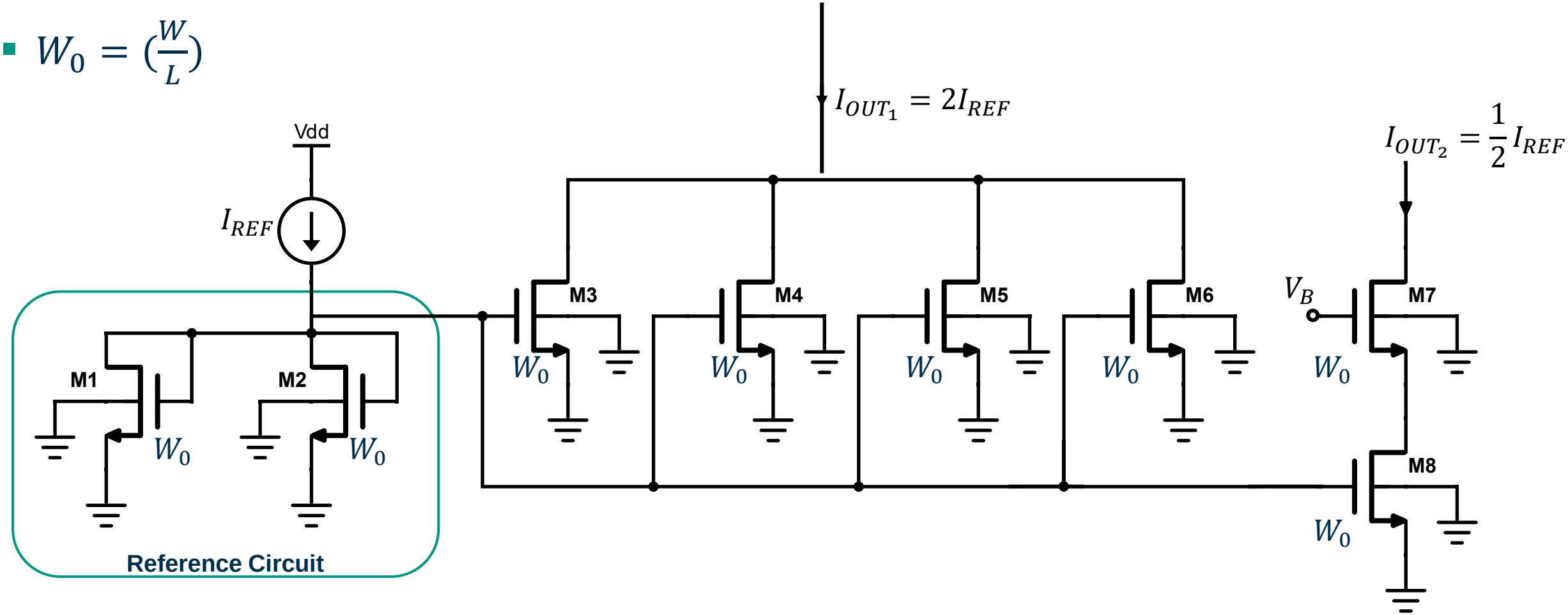
$$I_{OUT} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2$$

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

Scaling the Current Mirror

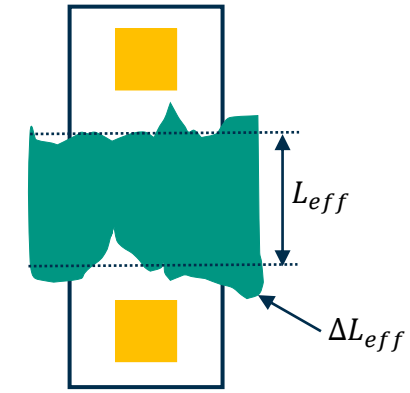
Design Examples

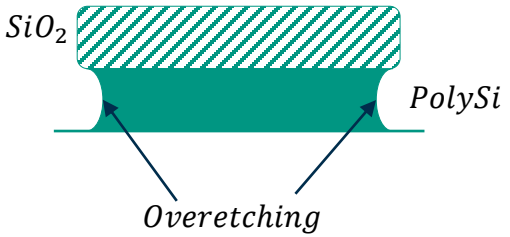
- $W_0 = (\frac{W}{L})$

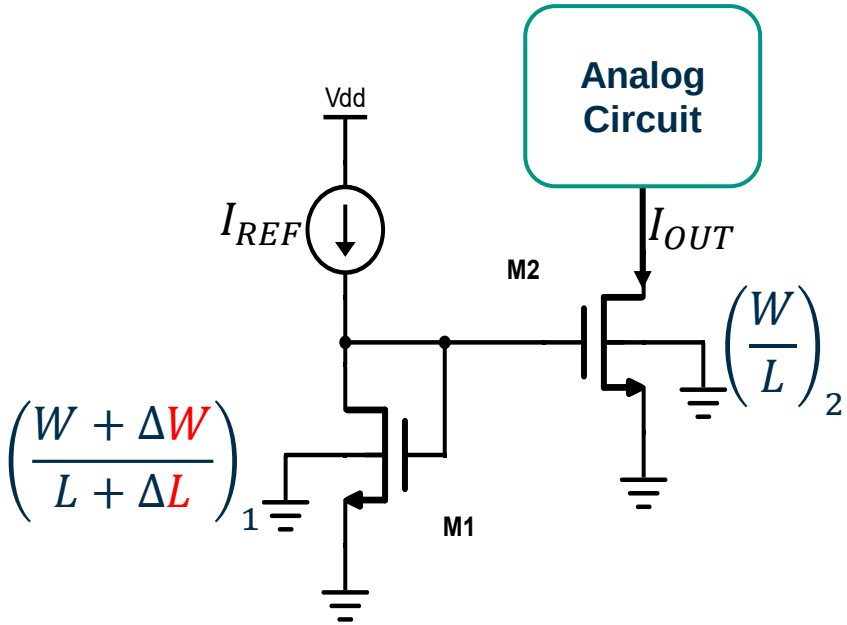


Current Mirror Mismatch

- Causes: Process Variations
  - Mask Misalignment
    - Variations in lithography can shift the transistor gate position.
    - Leads to effective channel width and length difference (ΔW and ΔL) between devices.
  - Diffusion and Etching Effects
    - Lateral diffusion under the mask changes effective channel width and length.
    - Overetching or underetching alters oxide edges and active area dimensions.



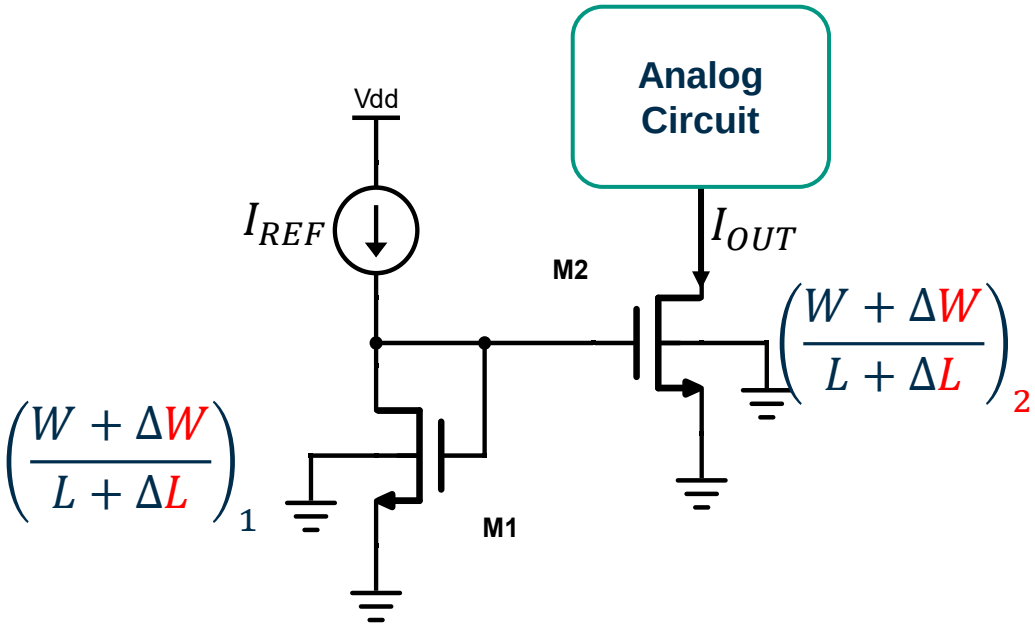




ΔW and ΔL cause I_{OUT} to have mismatch error

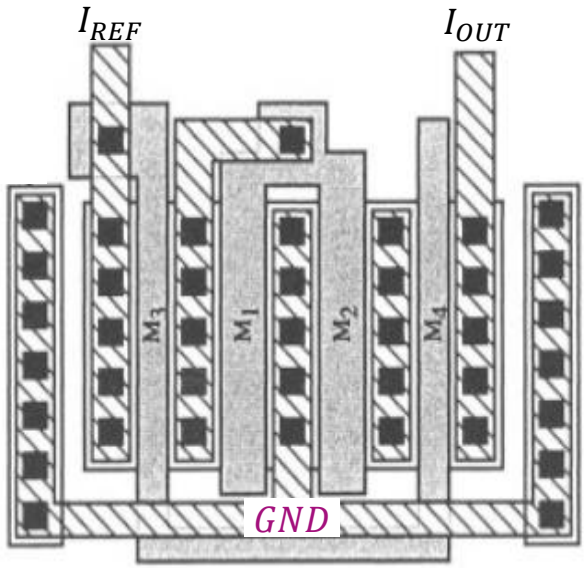
Current Mirror Mismatch

COMMON CENTROID LAYOUT

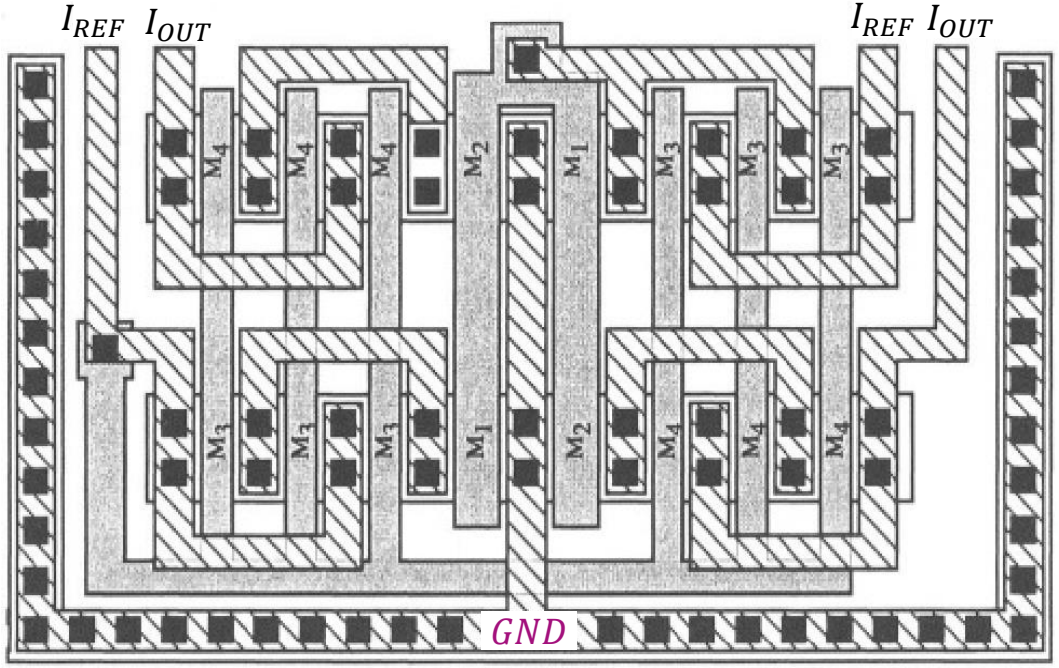


I_{OUT} error is minimized through matched devices

Simple Layout



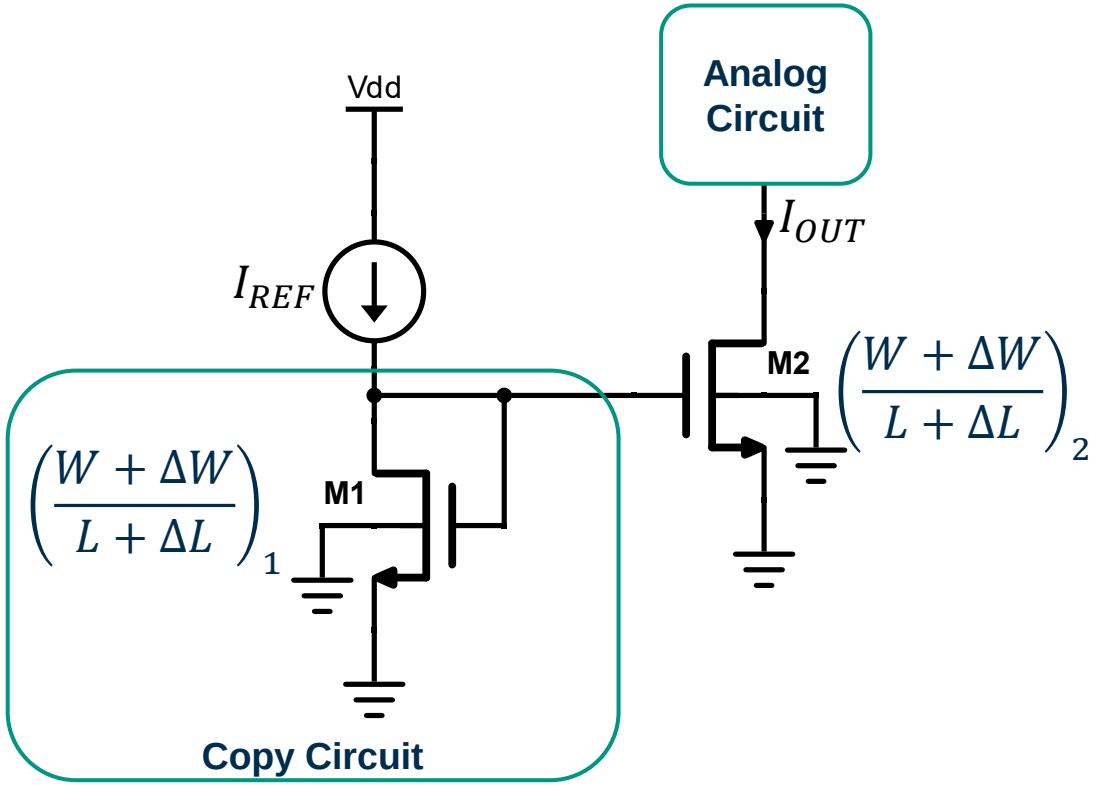
Common Centroid Layout



[1]

Current Mirror Mismatch

- $W \rightarrow W + \Delta W$, $L \rightarrow L + \Delta L$



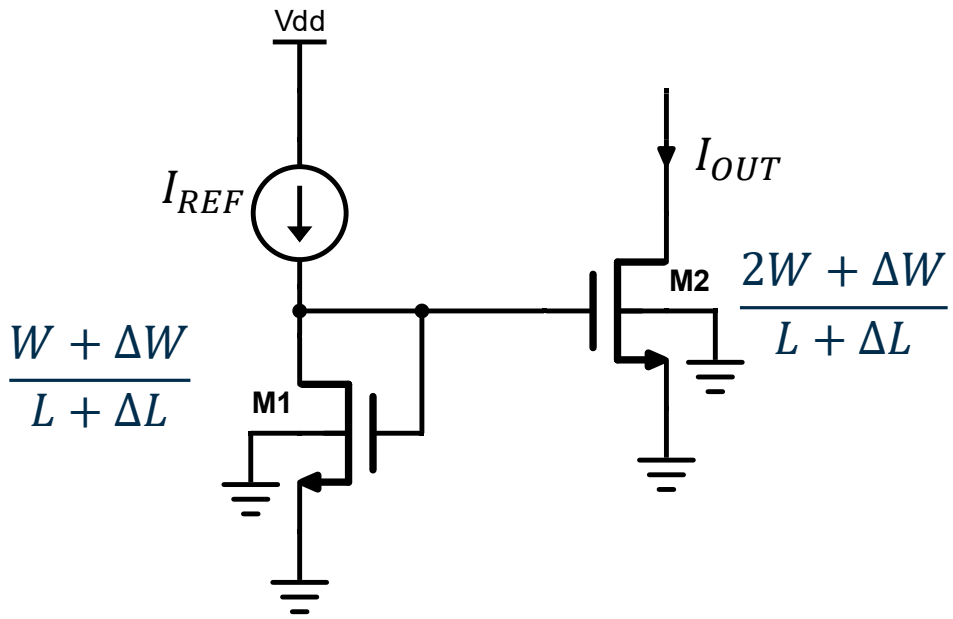
$$I_{REF} = I_{D_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W+\Delta W}{L+\Delta L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{OUT} = I_{D_2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W+\Delta W}{L+\Delta L}\right)_2 (V_{GS} - V_{TH})^2$$

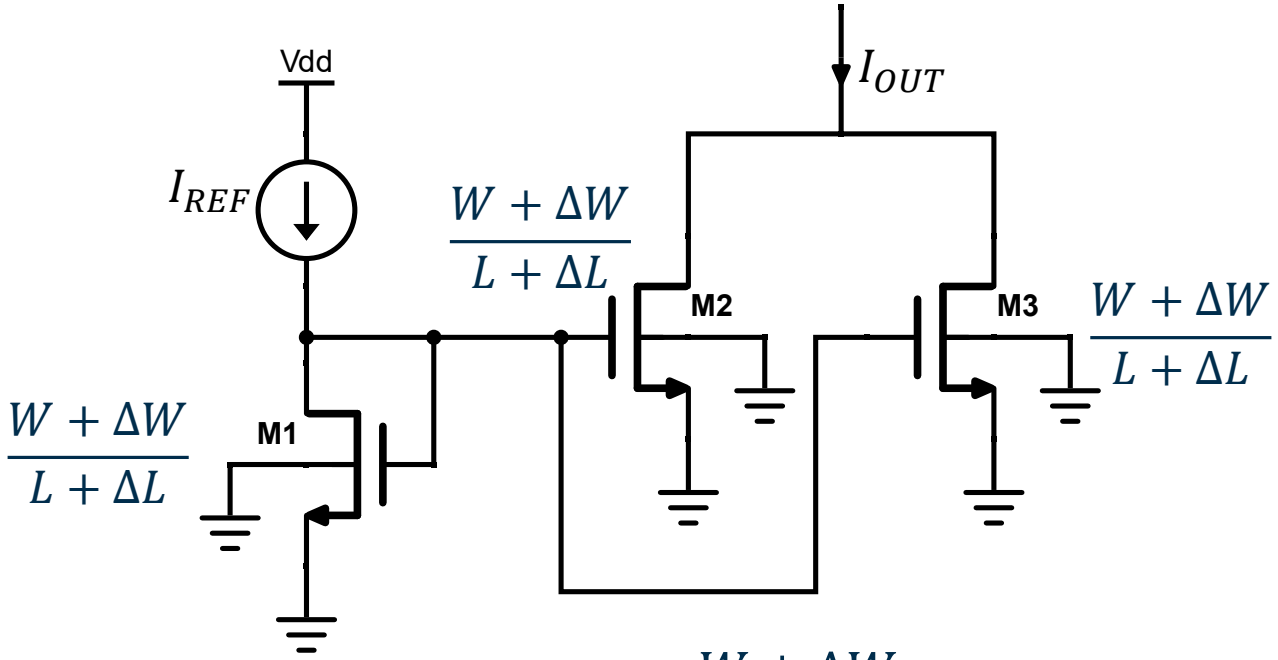
$$\frac{I_{D_2}}{I_{D_1}} = \frac{\left(\frac{W+\Delta W}{L+\Delta L}\right)_2}{(\frac{W+\Delta W}{L+\Delta L})_1}$$

Current Mirror Mismatch

Design Examples



$$\frac{I_{OUT}}{I_{REF}} = \frac{\frac{2W+\Delta W}{L+\Delta L}}{\frac{W+\Delta W}{L+\Delta L}} \neq 2$$

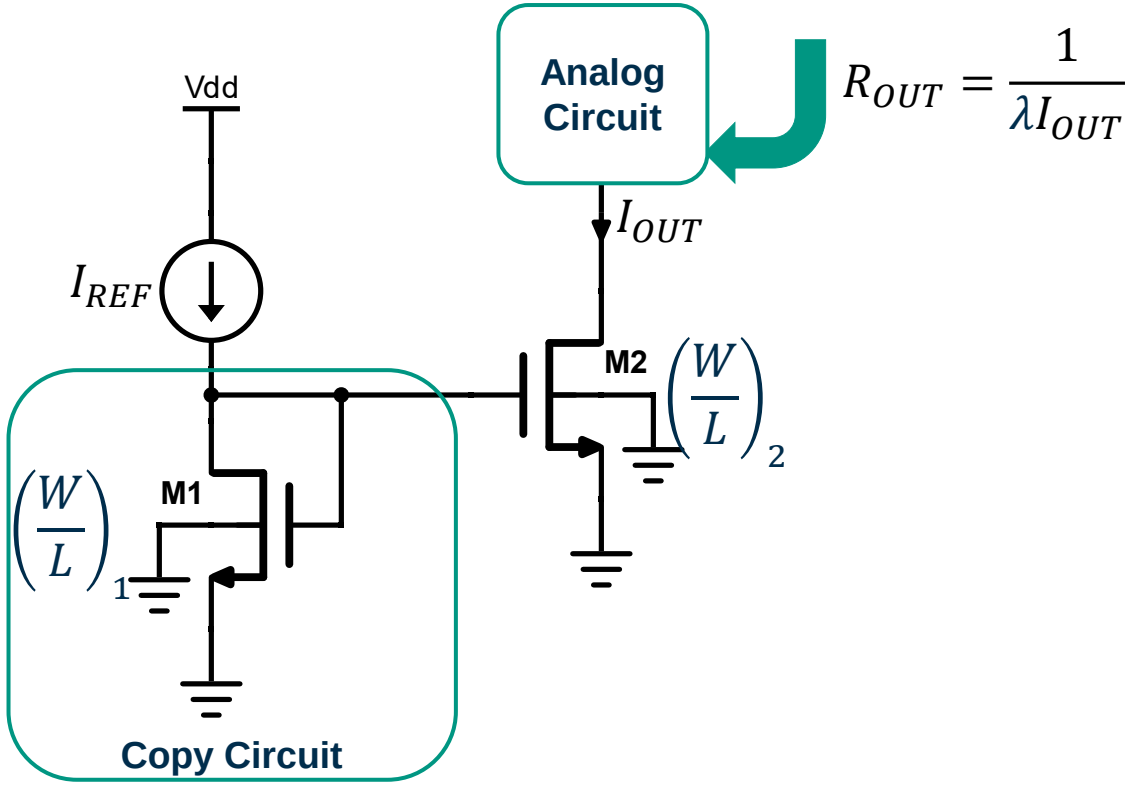


$$\frac{I_{OUT}}{I_{REF}} = \frac{2(\frac{W+\Delta W}{L+\Delta L})}{\frac{W+\Delta W}{L+\Delta L}} = 2$$

Current Mirror

Channel Length Modulation

- Channel length modulation introduces additional current error



$$I_{D_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS_1})$$

$$I_{D_2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS_2})$$

$$\frac{I_{D_2}}{I_{D_1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{(1 + \lambda V_{DS_2})}{(1 + \lambda V_{DS_1})}$$

Mirror Error

- To minimize the effect, ensure $V_{DS_1} = V_{DS_2}$

Cascode Current Mirror

Cascode Current Mirrors

- Ensure $V_{DS_2} = V_{DS_1}$, to eliminate mismatch

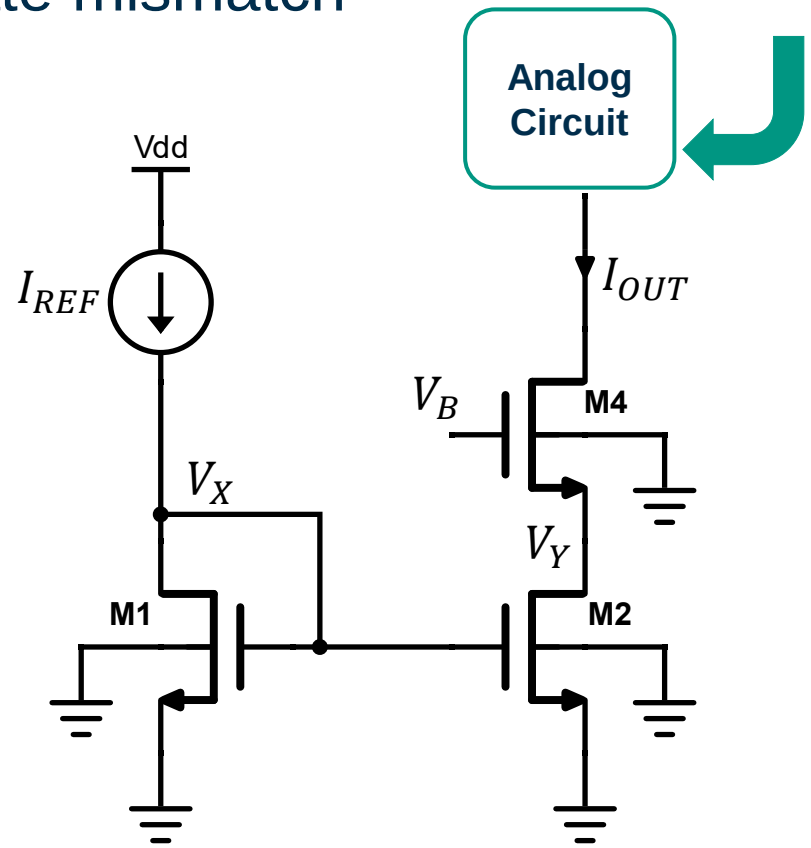
- Biasing Setup

$$V_B = V_{GS_4} + V_X$$

$$V_Y = V_B - V_{GS_4}$$

$$\boxed{V_Y = V_X}$$

$$\frac{I_{D_2}}{I_{D_1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{(1 + \lambda V_Y)}{(1 + \lambda V_X)}$$



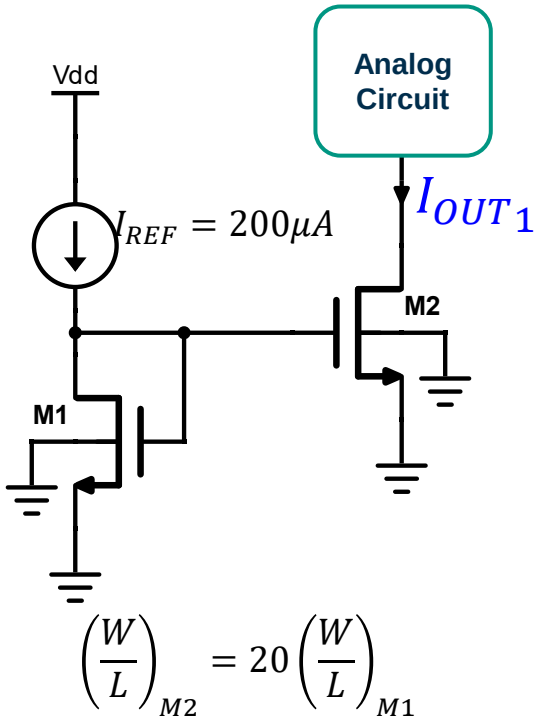
$$R_{OUT} = r_{o_4} + r_{o_2} + gm_4 r_{o_2} r_{o_4}$$

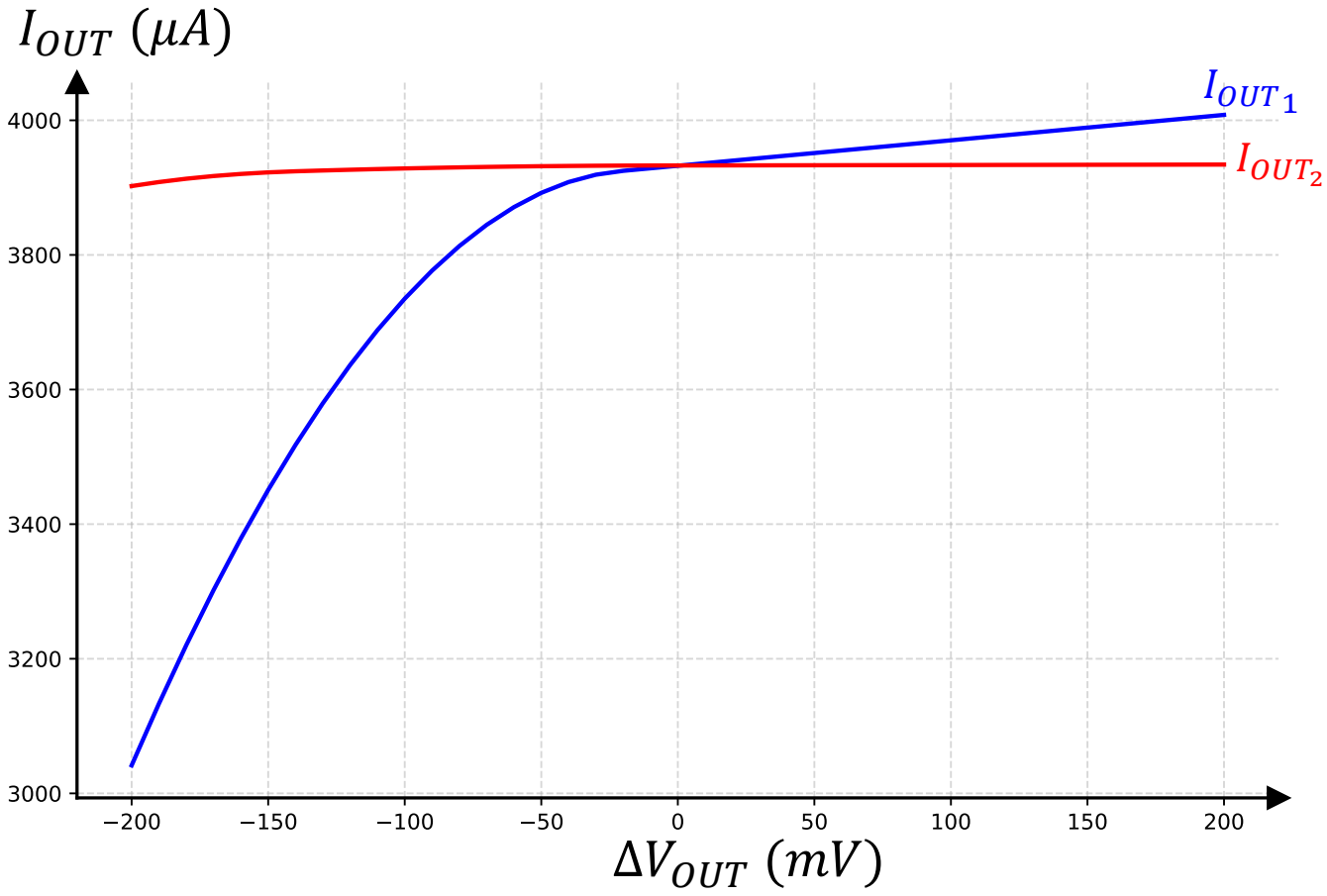
$$\approx gm_4 r_{o_2} r_{o_4}$$

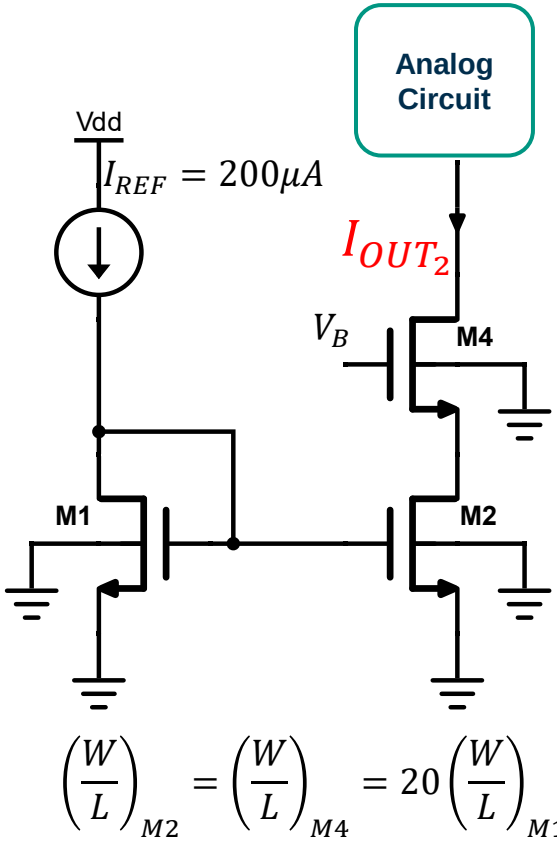
High output resistance & improved accuracy
(suppressed modulation effect !)
(Check on “Single Stage Amplifiers – Slide 37”)

- I_{OUT} marginally depends on V_{OUT}
- $\Delta I_{OUT} = \frac{\Delta V_{OUT}}{R_{OUT}}$
- ΔI_{OUT} leads to minimal modulation of V_Y

Cascode Current Mirrors

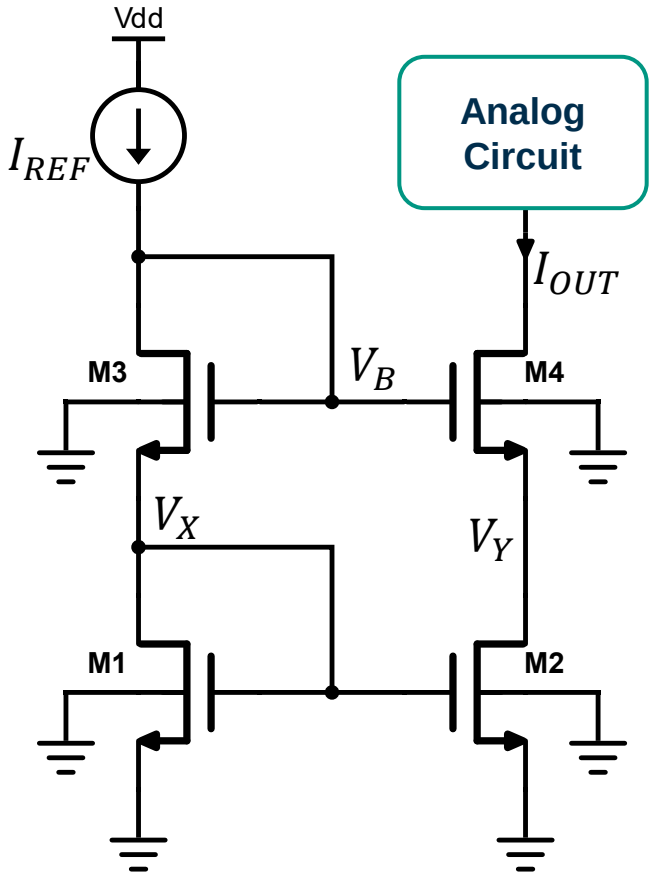






Cascode Current Mirrors

- V_B can be generated by M3 (exact replica of M4)



$$V_{OV} = V_{GS} - V_{TH}$$
$$V_{GS_3} = V_X + V_{TH} = V_{OV} + V_{TH}$$
$$V_{G_3} = V_{GS_3} + V_X = 2V_{TH} + 2V_{OV}$$
$$V_X = V_Y = V_{TH} + V_{OV}$$
$$V_{DS_4} > V_{OV_4}$$
$$V_{OUT} - V_Y > V_{OV}$$

Output Minimum Voltage

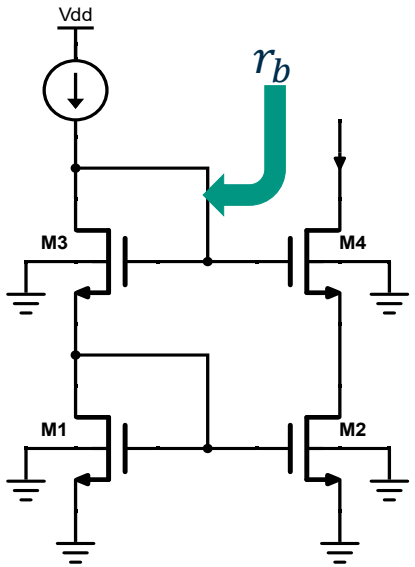
$$\boxed{V_{OUT_{min}} = V_{TH} + 2V_{OV}}$$

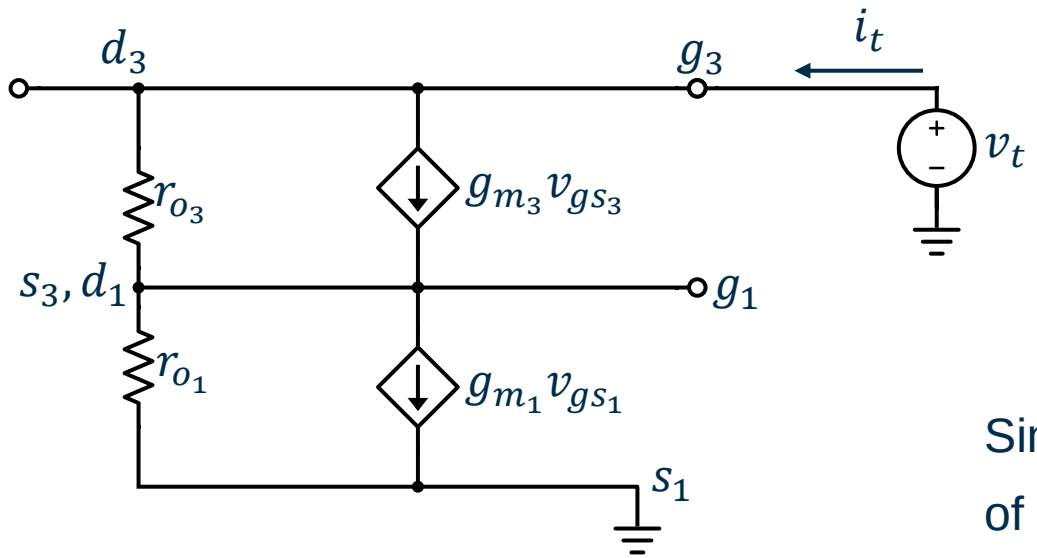
$V_{OUT_{min}}$ is relatively high so,

- Problematic for low-voltage designs
- It limits voltage swing

Cascode Current Mirrors

Output Resistance Calculation





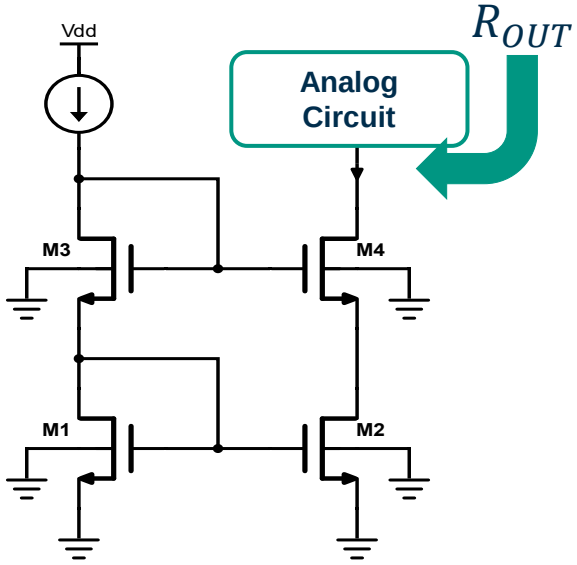
$$\frac{v_t}{i_t} = r_b$$

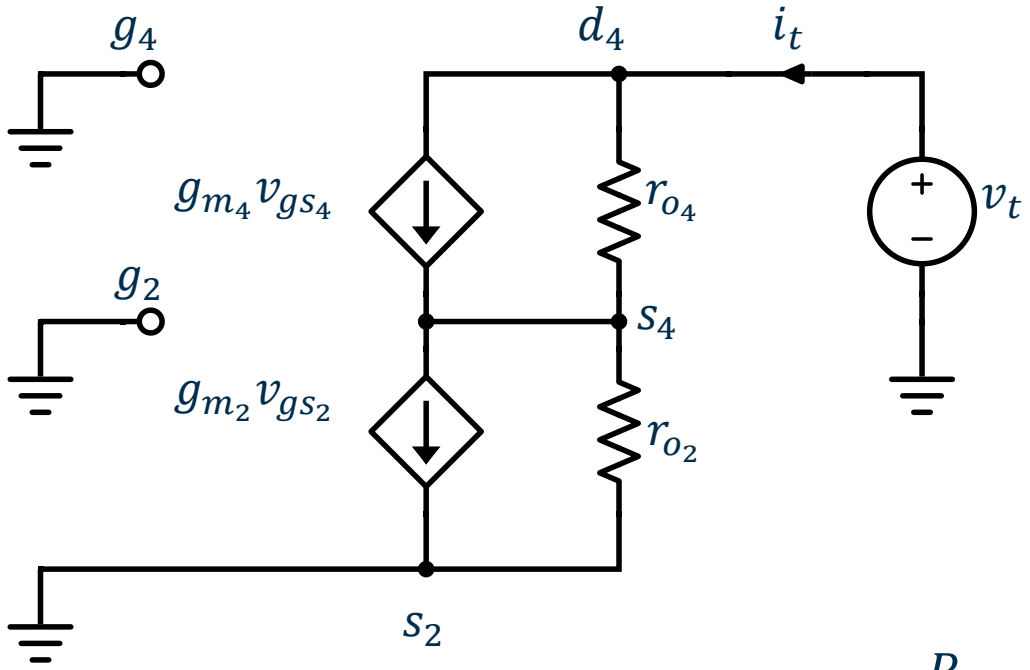
$$r_b \approx \frac{1}{gm} \ll r_o$$

Since $\frac{1}{gm}$ is so small, for easy of calculation of R_{OUT}, node g_3 & g_1 can be considered as grounded.

Cascode Current Mirrors

Output Resistance Calculation





small signal model

$$v_{gs_2} = 0$$

$$v_{gs_4} = -i_t r_{o_2}$$

$$i_t = \frac{v_t - v_{s_4}}{r_{o_4}} - g_{m_4} i_t r_{o_2}$$

$$i_t\left(1 + g_{m_4} r_{o_2}\right) = \frac{v_t - i_t r_{o_2}}{r_{o_4}}$$

$$R_{OUT} = \frac{v_t}{i_t} = r_{o_4}\left(1 + g_{m_4} r_{o_2}\right) + r_{o_2}$$

$$since\ (g_{m_4} r_{o_2} \gg 1)$$

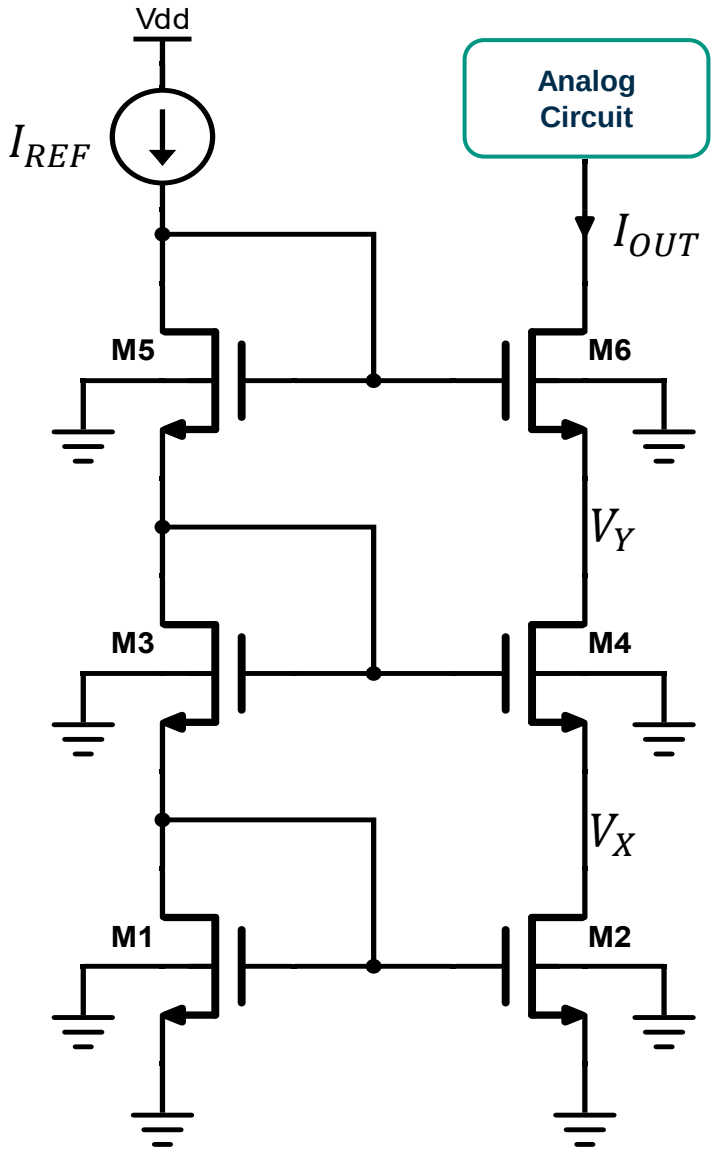
$$\boxed{R_{OUT} = g_{m_4} r_{o_2} r_{o_4}}$$

Triple Cascode Current Mirrors

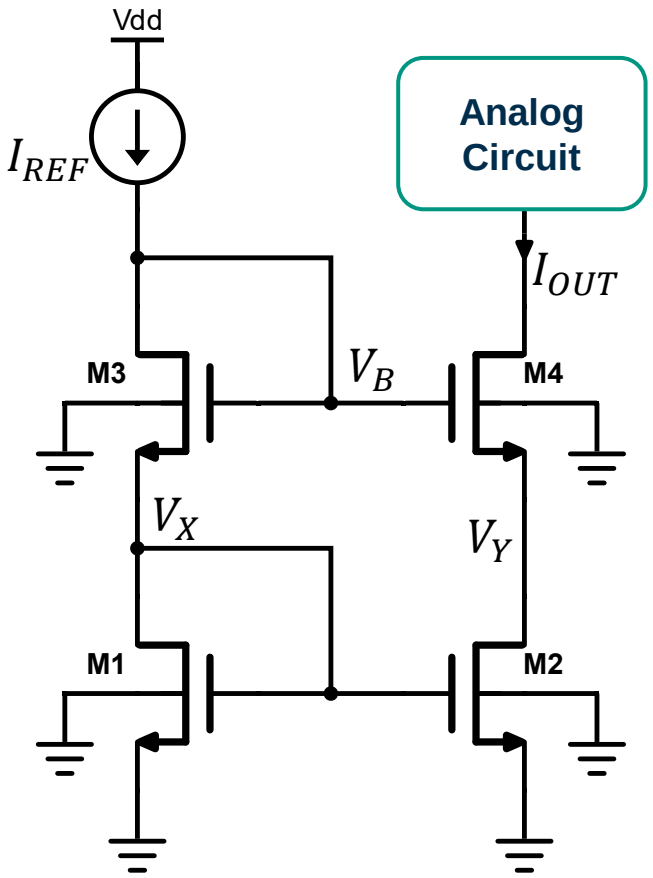
- Each additional cascode transistor (M3–M6) multiplies output resistance by a factor of $g_m r_o$
- Achieves extremely high R_{OUT} for precise current copying and minimal error

$$R_{OUT} = r_{o_6}\{1 + g_{m_6}[r_{o_4}(1 + g_{m_4} r_{o_2}) + r_{o_2}]\}$$
$$+ r_{o_4}(1 + g_{m_4} r_{o_2}) + r_{o_2}$$
$$\approx g_{m_6} g_{m_4} r_{o_2} r_{o_4} r_{o_6}$$

$$V_{OUT_{min}} = V_{OV_2} + V_{OV_4} + V_{OV_6} + 2V_{TH}$$



Low Voltage Cascode Current Mirrors



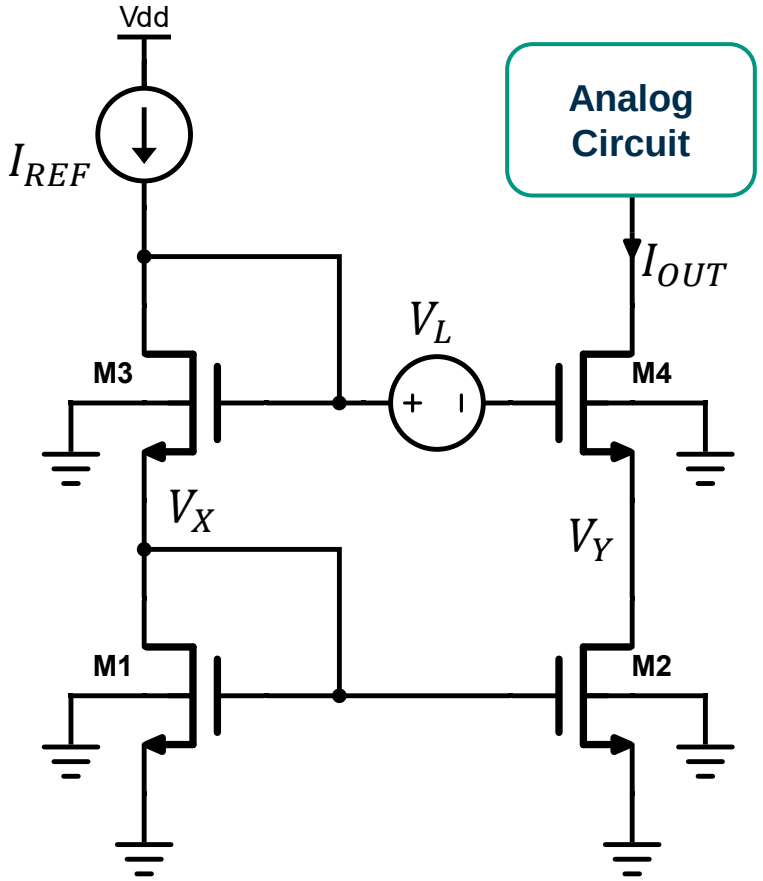
- If we choose $V_X \neq V_Y$ for low output voltage
- Use voltage shifter to equalize drain voltages

$$V_Y = V_X + V_{GS} - V_L - V_{GS}$$

- Choose $V_L = V_{TH}$

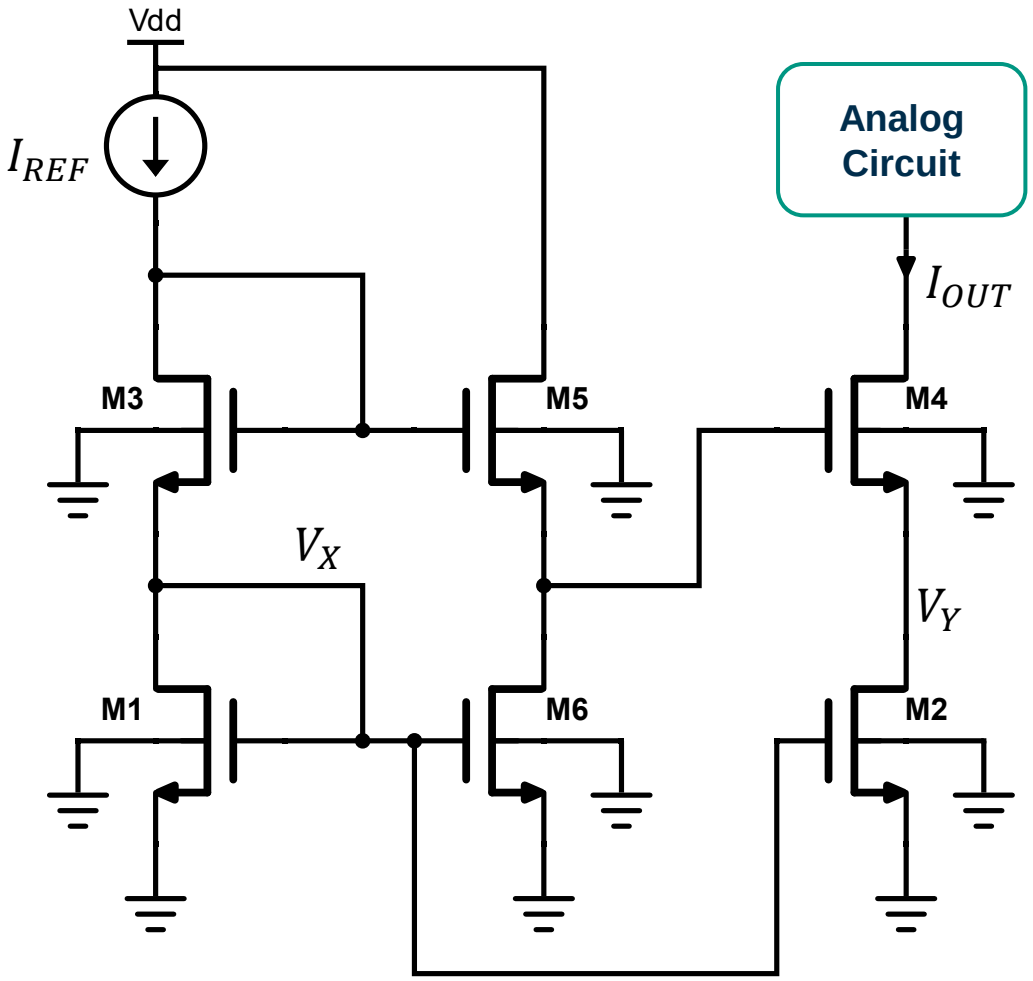
$$V_Y = V_X - V_{TH} = V_{OV}$$

- Still maintains accurate current mirroring for lower $V_{OUT_{min}} = 2V_{OV}$



Low Voltage Cascode Current Mirrors

Design Examples

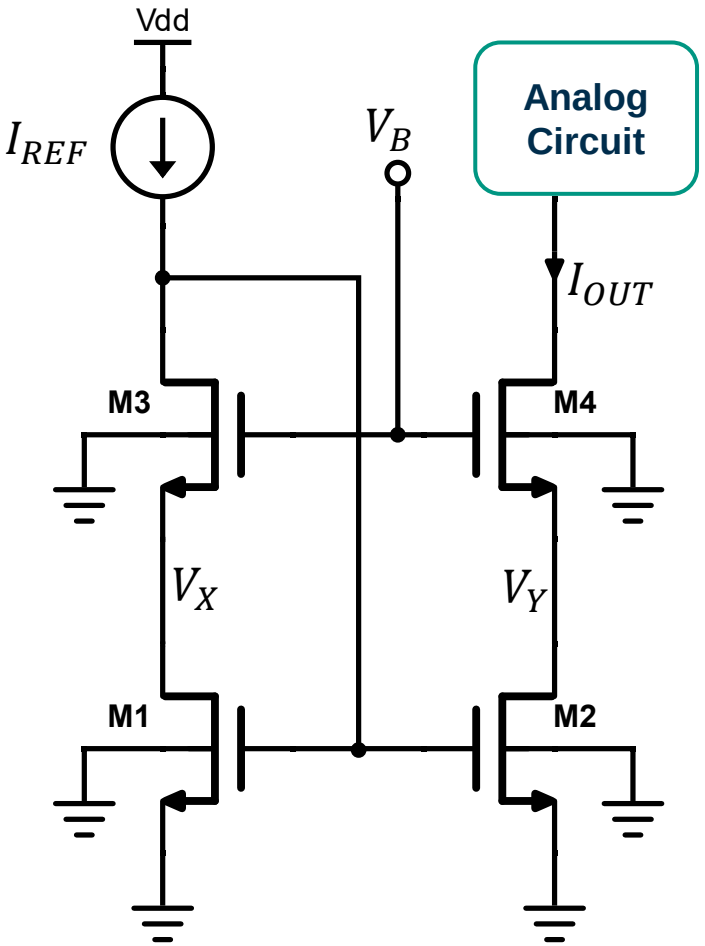


- All transistors share same V_{OV} except M3.
- $V_X = V_{TH} + V_{OV}$
- $W_3 = \frac{1}{4} W_1$, $I_{REF} = \frac{1}{2} \mu_n C_{ox} \frac{1}{4} \left(\frac{W}{L}\right)\left(V_{GS_3} - V_{TH}\right)^2$

- $\left(V_{GS_3} - V_{TH}\right)^2 = 4\left(V_{GS_1} - V_{TH}\right)^2$
- $V_{GS_3} = V_{TH} + 2V_{OV} \rightarrow V_{G_3} = V_X + V_{GS_3} = 2V_{TH} + 3V_{OV}$
- $V_{G_4} = V_{TH} + 2V_{OV} \rightarrow V_Y = V_{OV}$
- $V_{OUT_{min}} = 2V_{OV} \rightarrow$ low min. output voltage
- R_{OUT} remains the same as the cascode current mirror
- But $V_X \neq V_Y \rightarrow$ λ still affects current ratio

Low Voltage Cascode Current Mirrors

Design Examples



- To make sure all transistors operate at saturation.
- For M1;

$$V_B - V_{OV_3} - V_{TH} \geq V_{OV_1}$$

- For M3;

$$V_{OV_1} + V_{TH} - V_X \geq V_{OV_3}$$

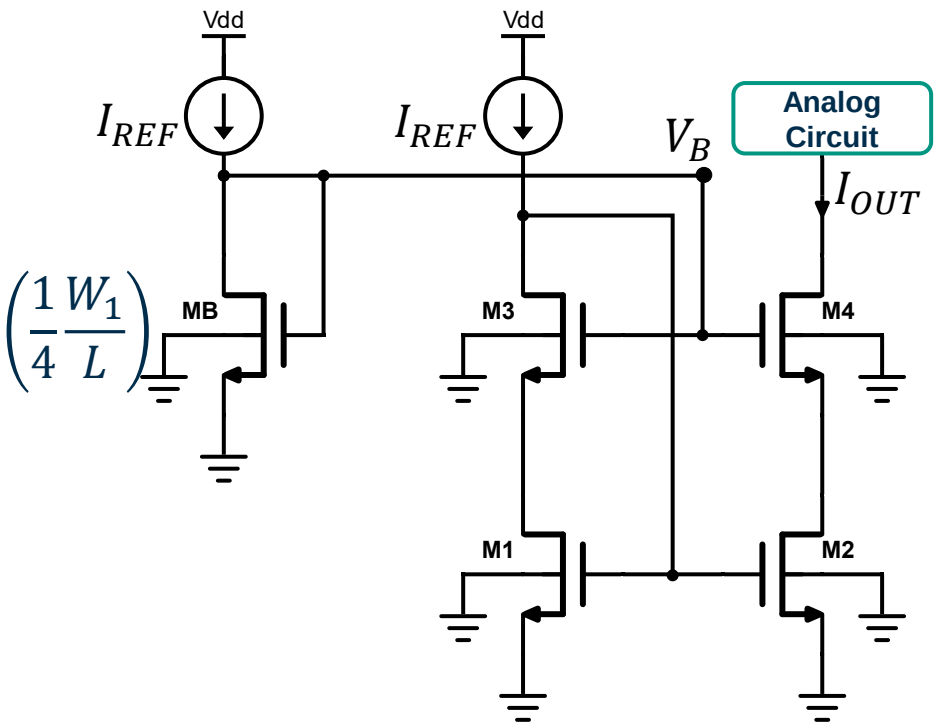
- For $V_{OV_1} = V_{OV_3}$

$$V_B \geq V_{TH} + 2V_{OV}$$

- $V_X = V_Y = V_B - (V_{TH} + V_{OV}) = V_{OV}$
- $V_{OUT_{min}} = 2V_{OV}$ → low min. output voltage.
- And $V_X = V_Y \rightarrow \lambda$, channel length modulation is suppressed

Low Voltage Cascode Current Mirrors

Design Examples



- How to generate $V_B = V_{TH} + 2V_{OV}$?
- $W_B = \frac{1}{4}W_1$,

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\frac{1}{4}\left(\frac{W_1}{L}\right)(V_B - V_{TH})^2$$

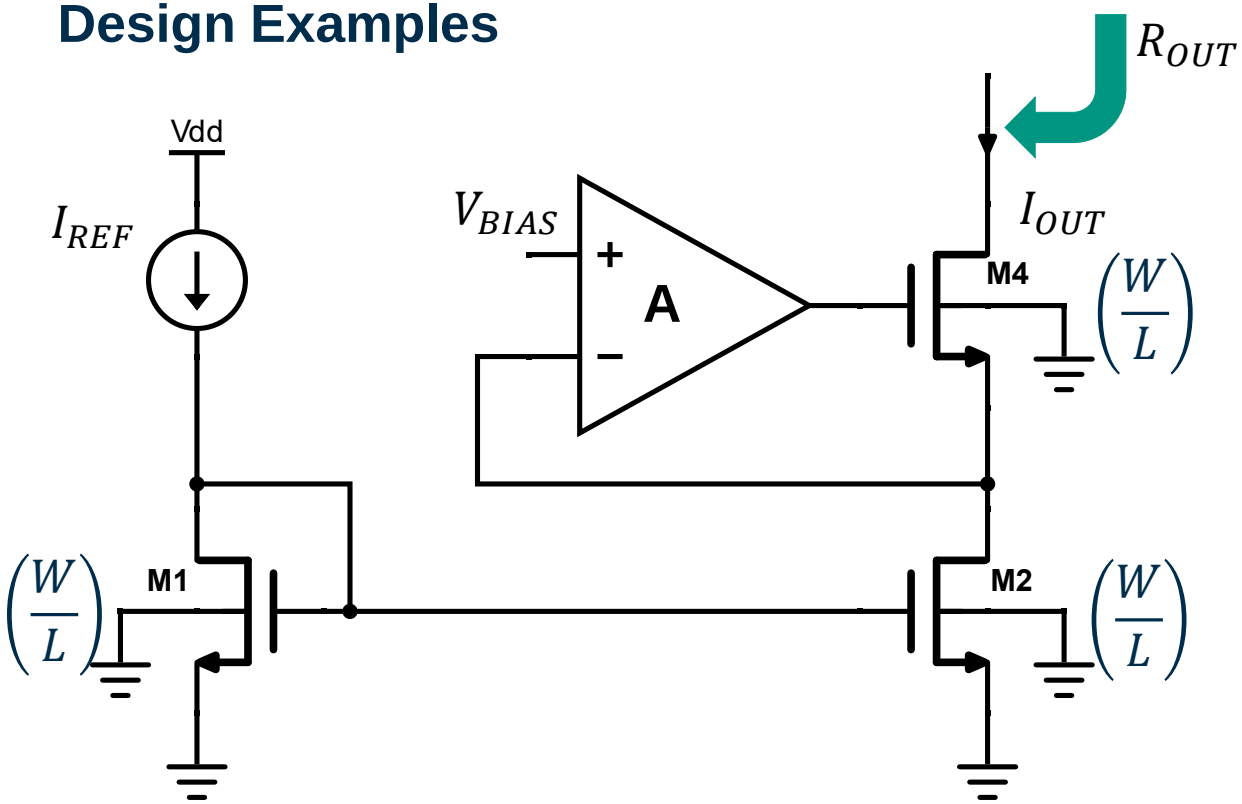
$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_1}{L}\right)(V_{OV})^2$$

$$\rightarrow (V_B - V_{TH})^2 = 4(V_{OV})^2$$

$$V_B = V_{TH} + 2V_{OV}$$

Regulated Cascode Current Mirrors

Design Examples



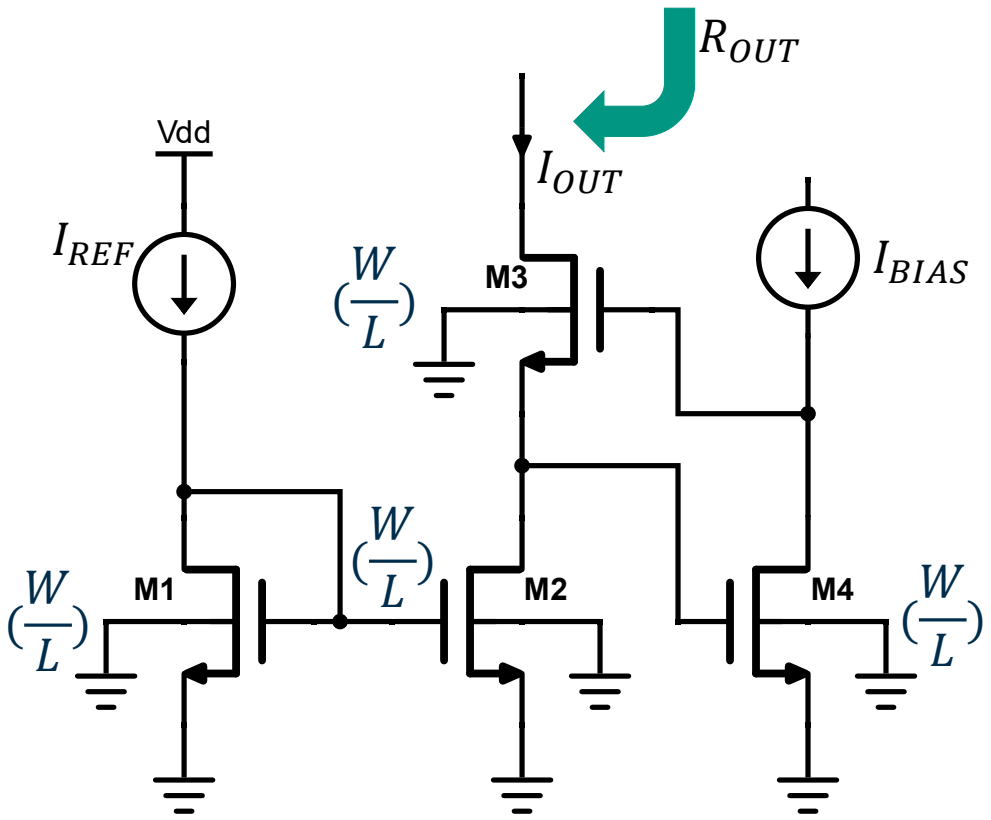
- M1 & M2 act as the basic current mirror
- The op-amp senses V_{D_2} and drives V_{G_4} to keep constant as V_{BIAS}

$$V_{BIAS} = V_{DS_2} > V_{OV_2}$$

- M4 is in saturation → $V_{OUT_{min}} \cong V_{BIAS} + V_{OV_4}$
- $R_{OUT} \cong r_{o_4} + r_{o_2} + (1 + A) g_{m_4} r_{o_2} r_{o_4} \cong A g_{m_4} r_{o_2} r_{o_4}$

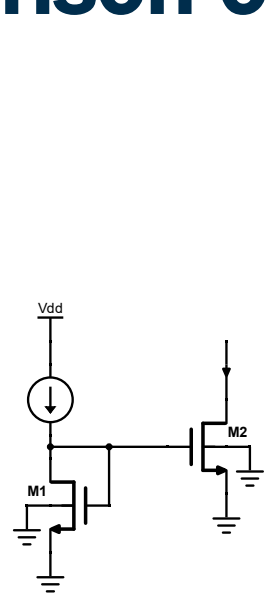
Regulated Cascode Current Mirrors

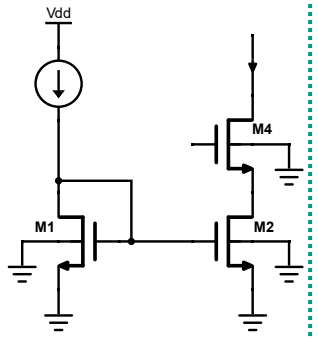
Design Examples

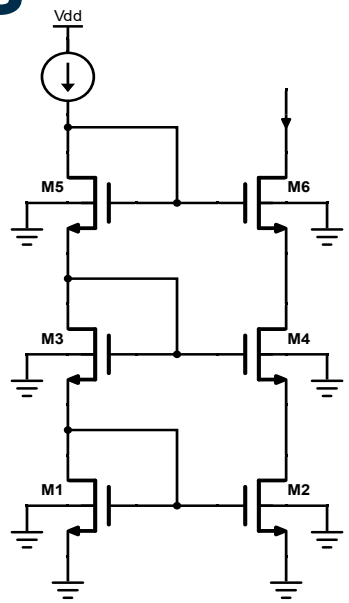


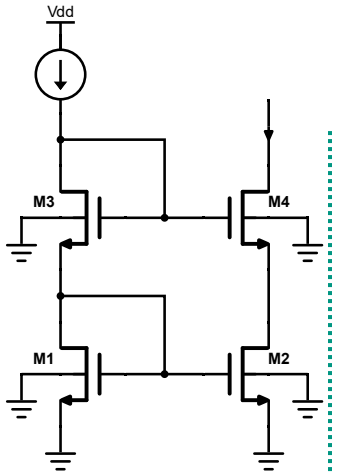
- M1 & M2 act as the basic current mirror
- M3 acts as the cascode device
- M4 is the regulating transistor. It senses V_{D_2} and adjusts V_{G_3} to keep V_{DS_2} constant
- I_{BIAS} provides bias current to operate M4 in saturation
- $R_{OUT} \cong (g_{m_3} r_{o_3}) r_{o_2} (g_{m_4} r_{o_4})$
- $V_{OUT_{min}} = V_{GS_4} + V_{OV_3} \cong V_{TH} + 2V_{OV}$

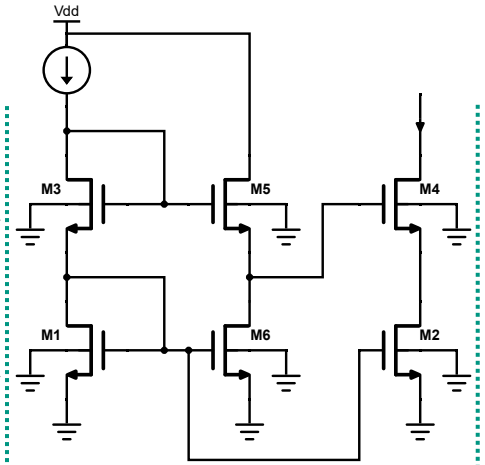
Comparison of Circuits

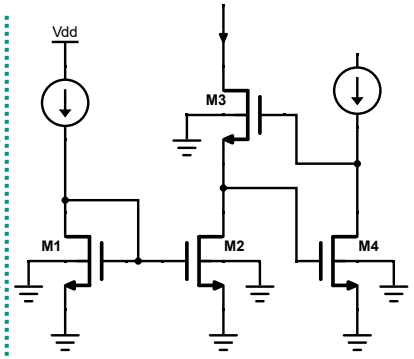












	Simple CM	Cascode CM	Triple Cascode CM	Self-biased Cascode CM	Low Voltage Cascode CM	Regulated Cascode CM
R_{OUT}	r_O	$g_m r_O^2$	$g_m^2 r_O^3$	$g_m r_O^2$	$g_m r_O^2$	$g_m^2 r_O^3$
$V_{OUT_{min}}$	V_{OV}	$2V_{OV}$	$3V_{OV} + 2V_{TH}$	$V_{TH} + 2V_{OV}$	$2V_{OV}$	$V_{TH} + 2V_{OV}$
Additional $BIAS$	No	Yes	No	No	No	Yes
Complexity	Low	$Moderate$	$Moderate$	$Moderate$	$High$	$Very\ High$

REFERENCE

- [1]: Maloberti, F. (2001). Analog design for CMOS VLSI systems. Kluwer Academic.