Mikroelektronische Schaltungen und Systeme

Lect 5.
Current Sources

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Mikroelektronische Schaltungen und Systeme

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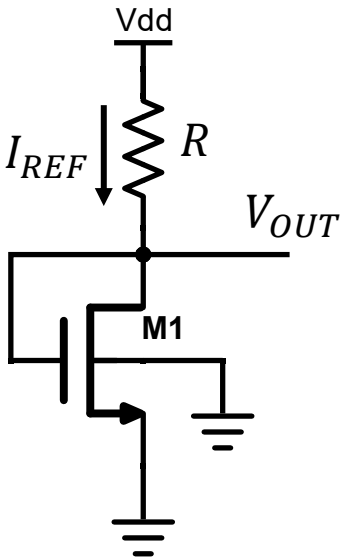
Current Reference

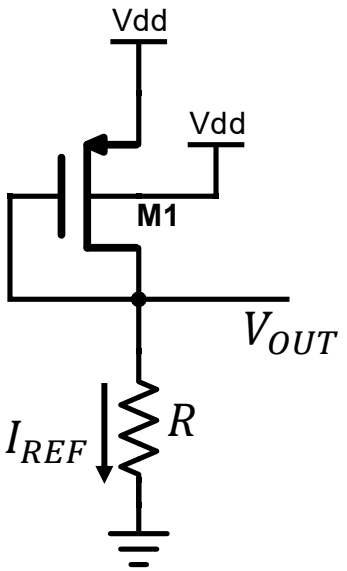
Current Reference

- Purpose:
  - Generate a stable reference current I_{REF} that biases analog circuits.
  - Maintain current independent of supply voltage and temperature variations.
- Resistor-MOS Reference:
  - Current is defined by resistor and transistor bias.

$$I_{REF} = \frac{V_{DD} - V_{GS_1}}{R}$$

  - No stable current output due to PVT variations.





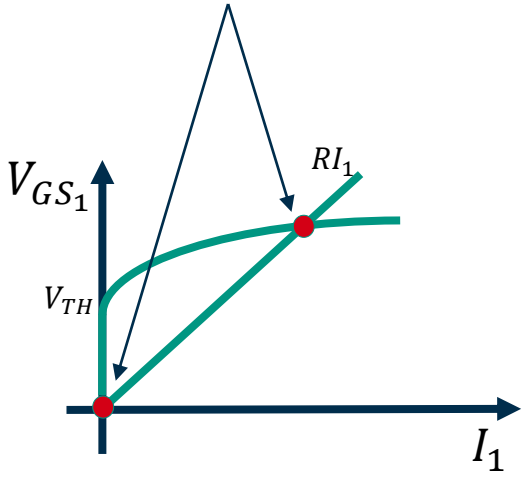
Self-Biased (Bootstrapped) Current Reference

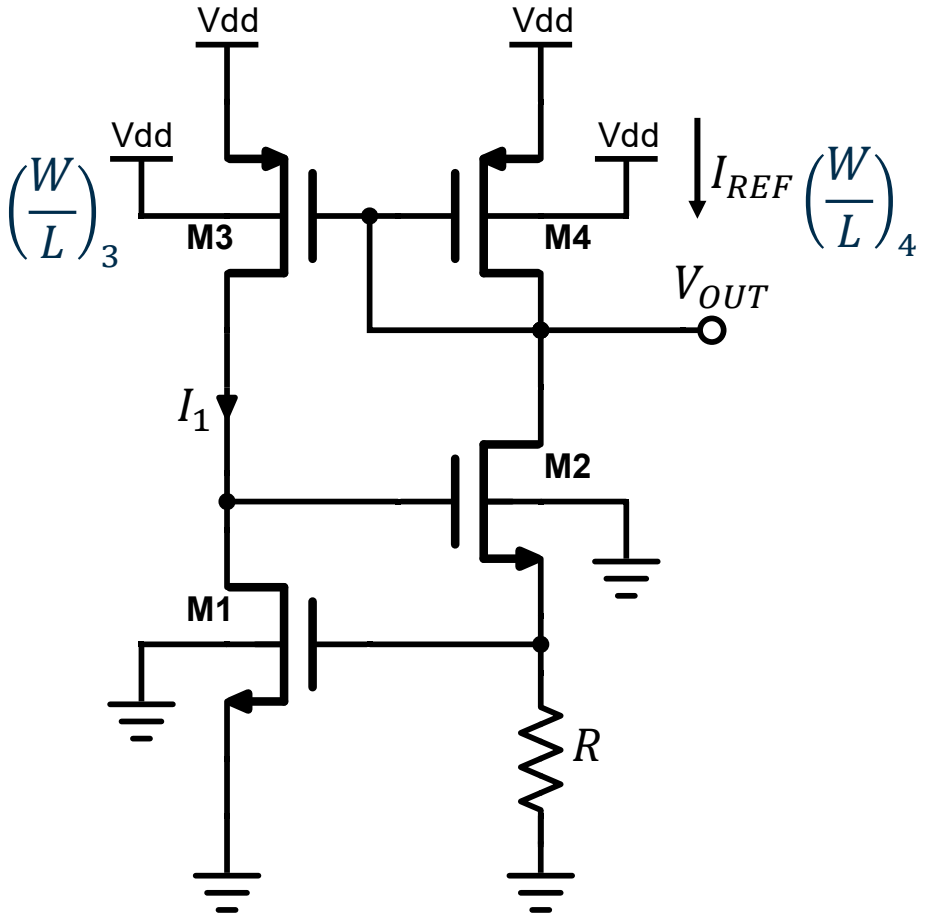
- Operation:
  - M1 and M2 form the core bias loop, where current I_1 is set by resistor R.
  - Transistors M3 and M4 mirror I_1 by creating a self-sustaining loop.

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 \rightarrow I_1 = I_{REF}$$

- $V_{GS_1} = RI_1$
- $V_{GS_1} = V_{TH} + \sqrt{\frac{I_1}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} \quad for\ V_{GS_1} > V_{TH}$
- $I_1 = 0 \quad for\ V_{GS_1} < V_{TH}$

Two operating points





- No dependence on V_{DD}!!
- It requires a **start-up circuit** to avoid zero-current equilibrium.

Self-Biased µ-current Generator

- Operation:
  - Transistors M3 and M4 are matched, (ignore λ)

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 \rightarrow I_3 = I_4$$

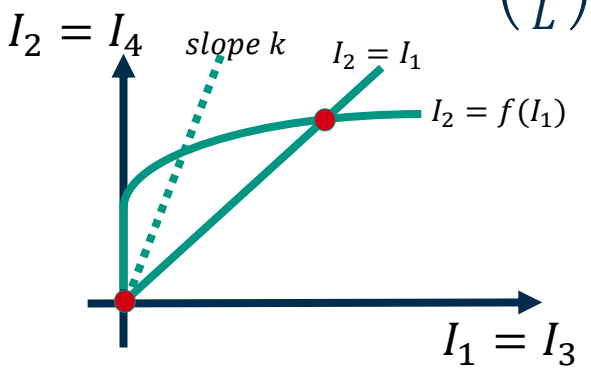
$$I_1 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \left(V_{GS_1} - V_{TH_1}\right)^2$$

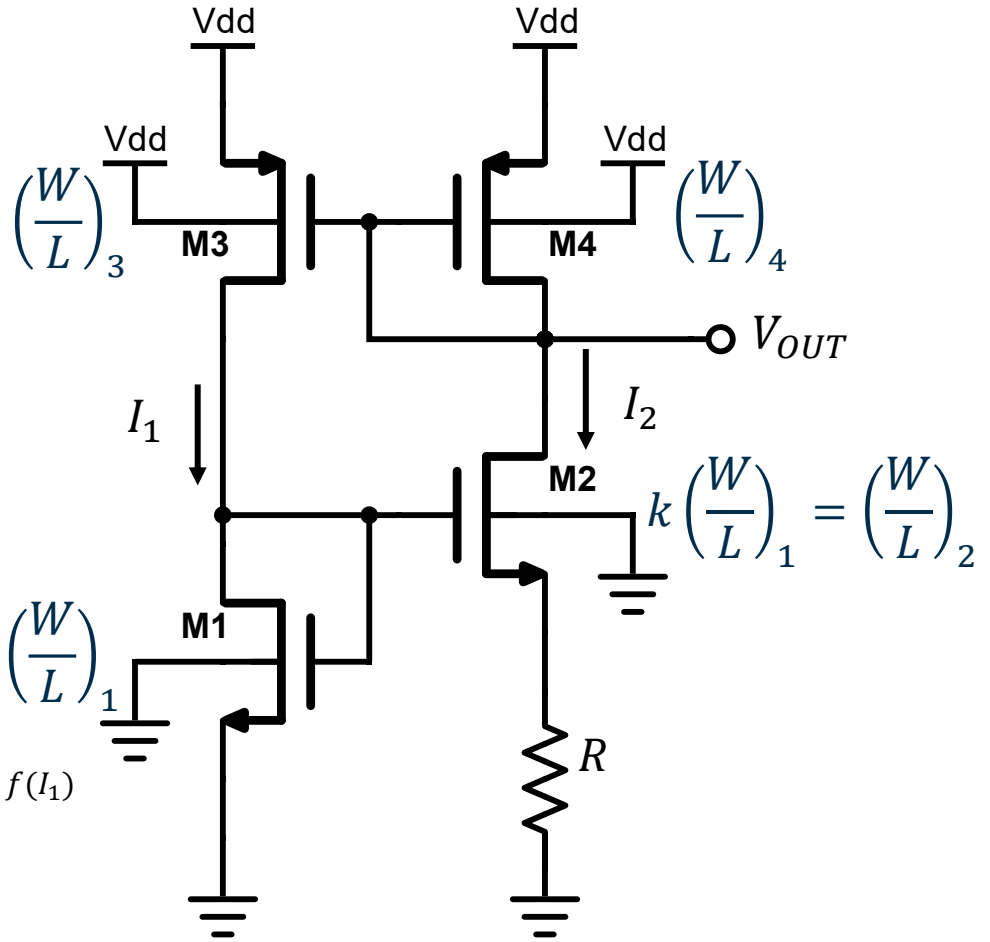
$$I_2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left(V_{GS_2} - V_{TH_2}\right)^2$$

  - $V_{GS_1} = V_{GS_2} + RI_2 \quad \& \quad V_{TH_1} = V_{TH_2}$

$$\sqrt{\frac{I_1}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} = \sqrt{\frac{I_2}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} + RI_2$$

  - No dependence on V_{DD}!!
  - R does not need to be very large for small I_2
  - It requires a **start-up circuit**

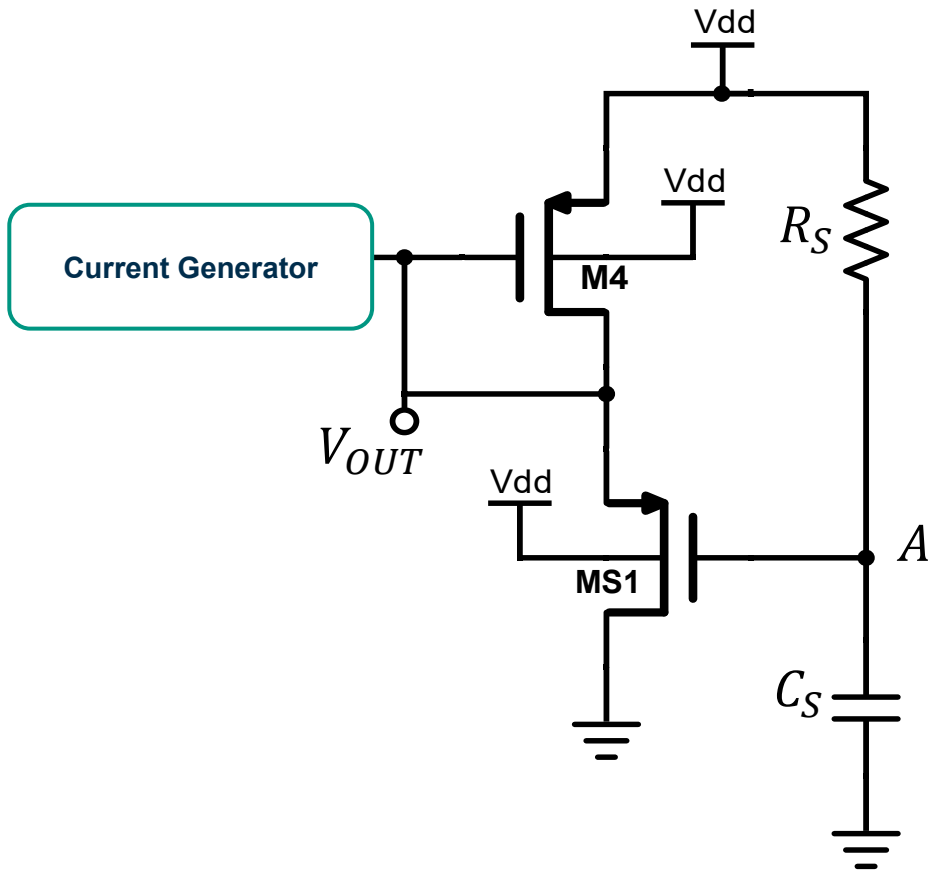




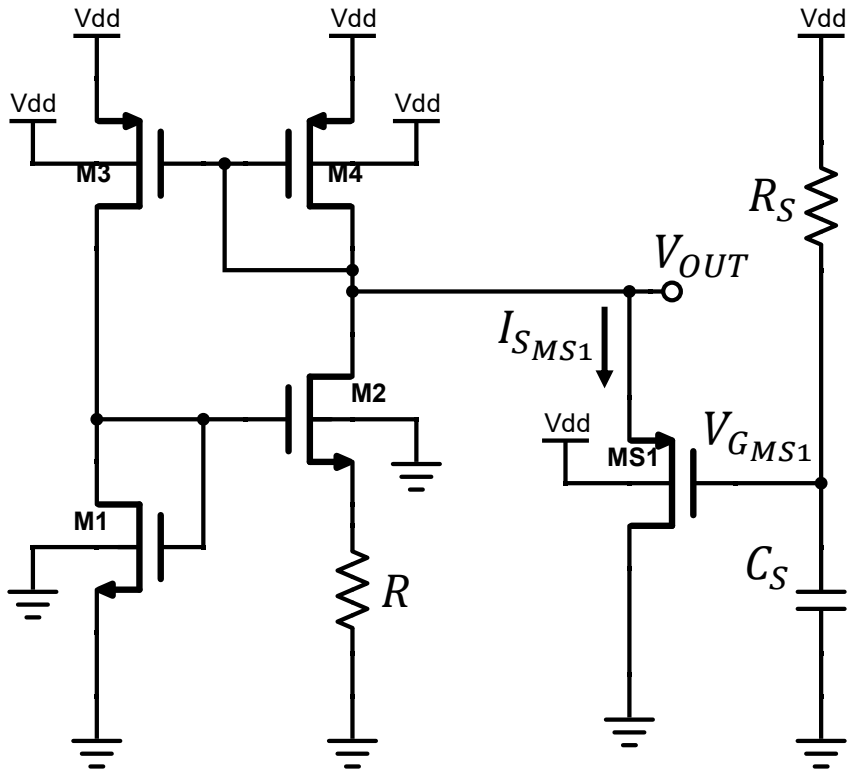
Start-Up Circuit

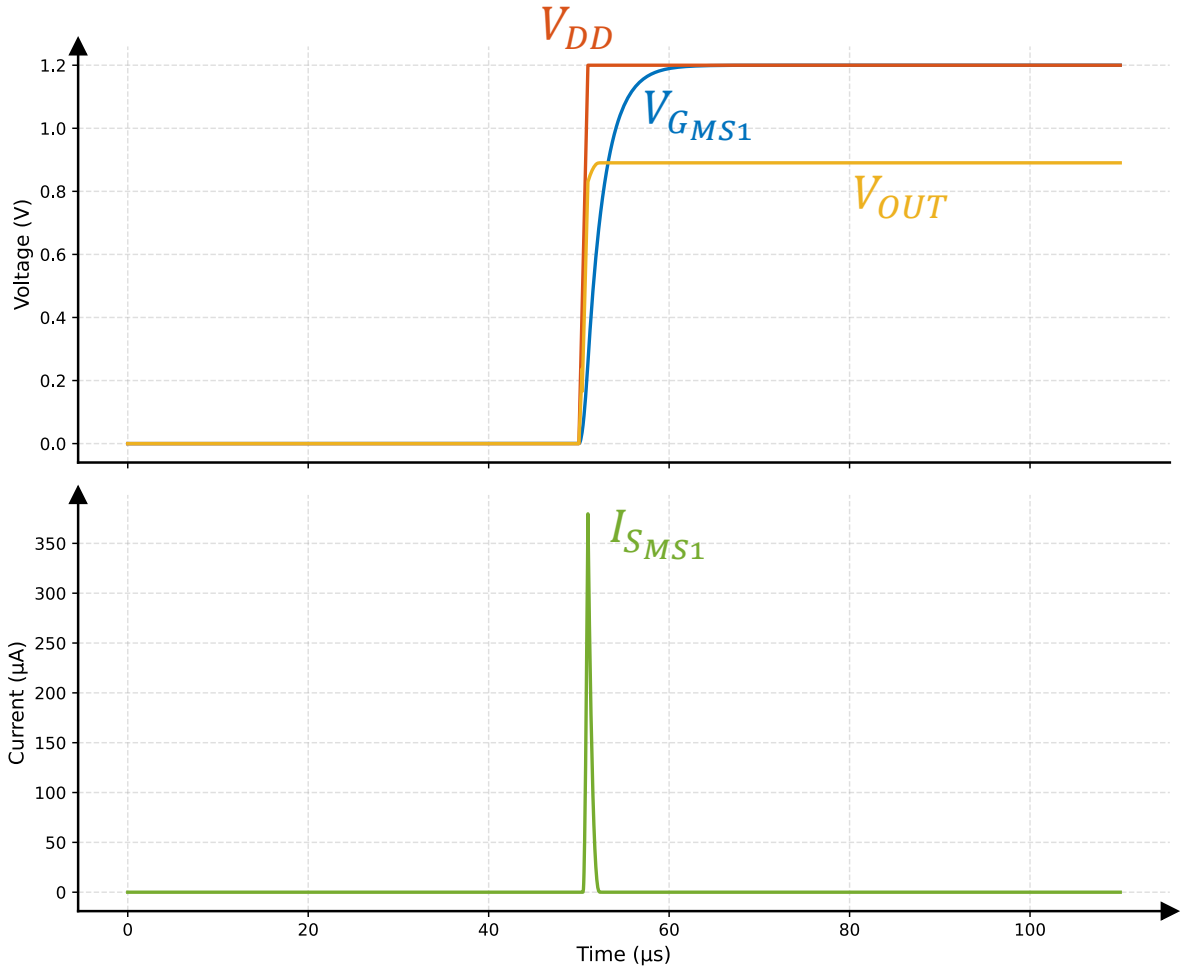
- Purpose:
  - Ensures the bias or reference circuit starts correctly after power-up.
  - Prevents the system from staying in the zero-current state.
- Dynamic Start-up:
  - Uses an RC network to momentarily inject current at power-on.
  - The capacitor, C_S, charges during start-up. Initially V_A is ground.
  - Until C_S charges MS1 is on.
  - $\tau = R_S C_S$. For 1µs start-up duration,

$$C_S = 1\text{pF}, R_S = 1\text{M}\Omega$$



Dynamic Start-up Circuit





V_{BE} –based Current Generator

- Purpose:
  - Generates a reference current derived from V_{BE} of a bipolar transistor.
  - Provides a current with predictable temperature dependence.
- Operation Principle:
  - The op-amp forces nodes A and B to the same voltage:

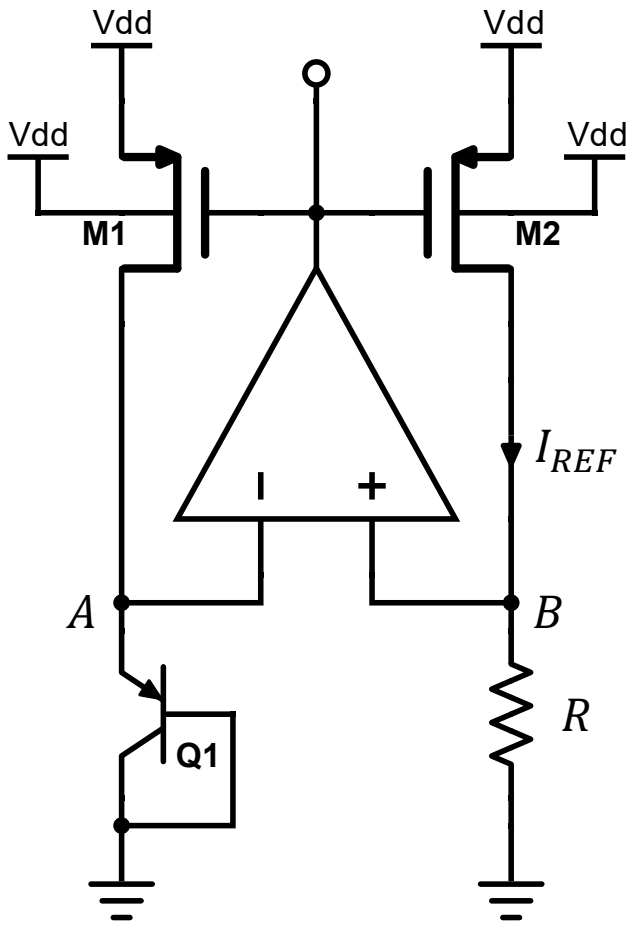
$$V_A = V_B$$

  - Hence, the resistor current is defined by the transistor's V_{BE}.

$$|V_{BE_1}| = V_T \ln\left(\frac{I_1}{I_S}\right)$$

$$I_{REF} = \frac{V_{BE_{Q_1}}}{R}$$

  - $V_{BE_{Q_1}}$ decreases by ≈2 mV/°C → **CTAT (Complementary to Absolute Temperature)** current behavior .
  - Simple implementation using one BJT.



V_T –based Current Generator

- Purpose
  - To generate I_{REF} that is independent of V_{DD} but has a specific relationship with temperature.
  - MOS Transistors are in saturation,

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2$$

- Operation Principle:

$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_1 \rightarrow I_1 = I_2 = I_{REF} \quad ; \quad \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 \rightarrow V_A = V_B$$

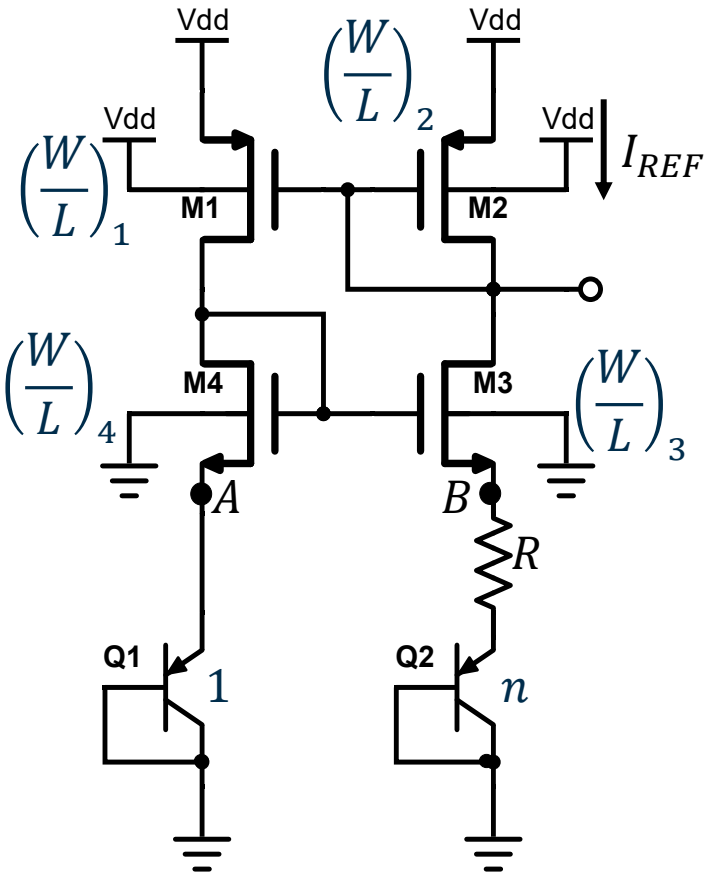
$$I_S = qA\left(\frac{D_n n_i^2}{N, W}\right)$$

$$|V_{BE_1}| = V_T \ln\left(\frac{I_1}{I_S}\right); |V_{BE_2}| = V_T \ln\left(\frac{I_1}{\boldsymbol{n} I_S}\right)$$

$$RI_1 = |V_{BE_1}| - |V_{BE_2}| = V_T \ln\left(\frac{I_1}{I_S}.\frac{\boldsymbol{n} I_S}{I_1}\right)$$

$$I_1 = \frac{V_T}{R}\ln(n)$$

  - V_T & R have positive temperature coefficient.



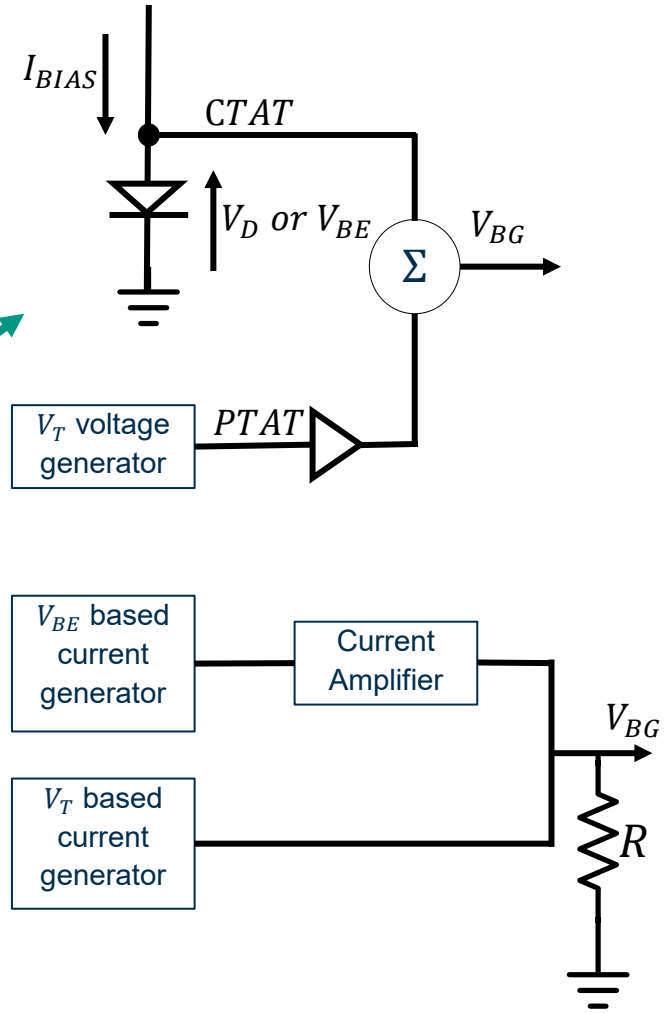
Voltage Reference

Bandgap Reference Voltage

- Purpose:
  - Generates a temperature-independent reference voltage (≈ 1.2 V for silicon).
  - Achieved by combining two voltages with opposite temperature coefficients:
    - V_{BE} :negative temperature coefficient (CTAT)
    - V_T :positive temperature coefficient (PTAT)

$$V_{BG} = V_{BE} + mV_T$$

- Bandgap Idea
  - Voltage addition approach: combines V_{BE} (CTAT) and scaled V_T (PTAT) voltages.
  - Current addition approach: generates PTAT and CTAT currents, converts their sum to voltage.



Bandgap based on Voltage Processing

- Generates temperature stable reference voltage by combining V_{BE} (CTAT) and ΔV_{BE} (PTAT).
- The amplifier forces the two transistor base voltages to satisfy:

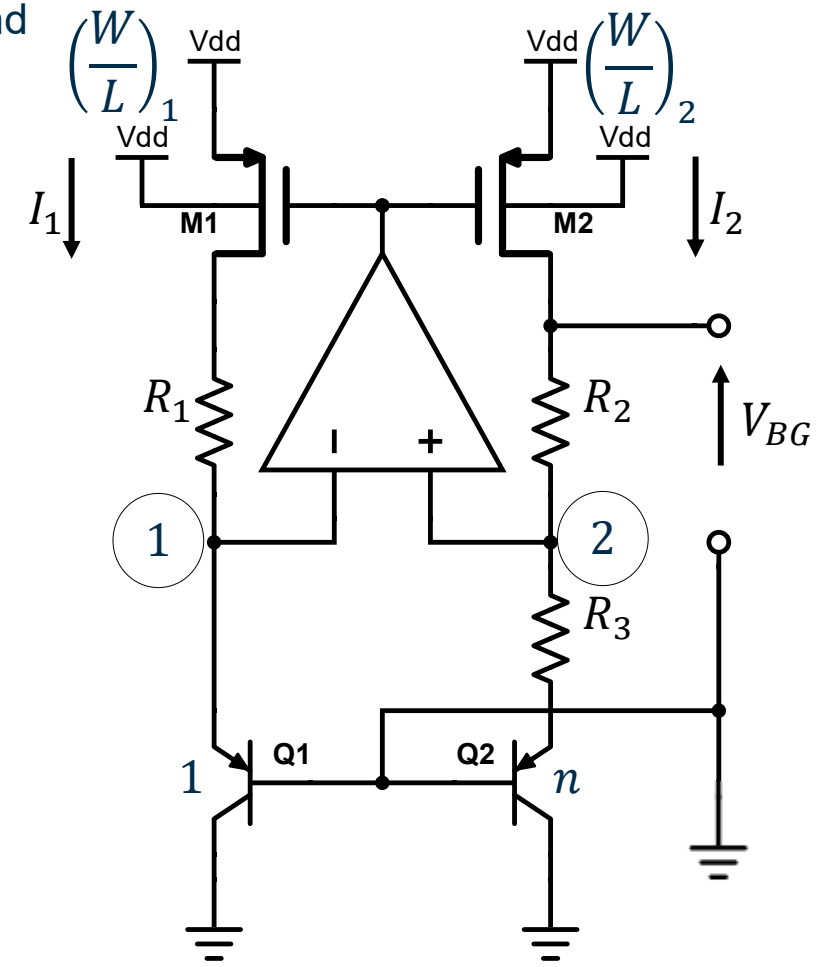
$$|V_{BE_1}| - |V_{BE_2}| = \Delta V_{BE} = V_T \ln\left(\frac{I_1}{I_S}.\frac{nI_S}{I_2}\right) = R_3 I_2$$

- The reference voltage is formed as:

$$V_{BG} = V_2 + R_2 I_2 - V_{AG}; \qquad \frac{I_1}{I_2} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2};$$

$$V_{BG} = |V_{BE_1}| + V_T \frac{R_2}{R_3} \ln\left(\frac{\left(\frac{W}{L}\right)_1 n}{\left(\frac{W}{L}\right)_2}\right) = |V_{BE_1}|(CTAT) + m.V_T(PTAT)$$

- The scaling factor $m = \frac{R_2}{R_3} \ln\left(\frac{\left(\frac{W}{L}\right)_1 n}{\left(\frac{W}{L}\right)_2}\right)$.
- Achieves a zero temperature coefficient for the correct resistor and area ratios.



Bandgap based on Current Processing

- Q_1 & Q_2 generate a PTAT current through R_1:

$$I_1 \cong I_S e^{\left(\frac{|V_{BE_1}|}{V_T}\right)}$$

$$|V_{BE_1}| - |V_{BE_2}| = \Delta V_{BE}$$

$$= V_T \ln\left(\frac{I_1}{I_S}.\frac{kI_S}{I_2}\right) = V_T \ln(k)$$

$$I_1 = \frac{V_T \ln(k)}{R_1}$$

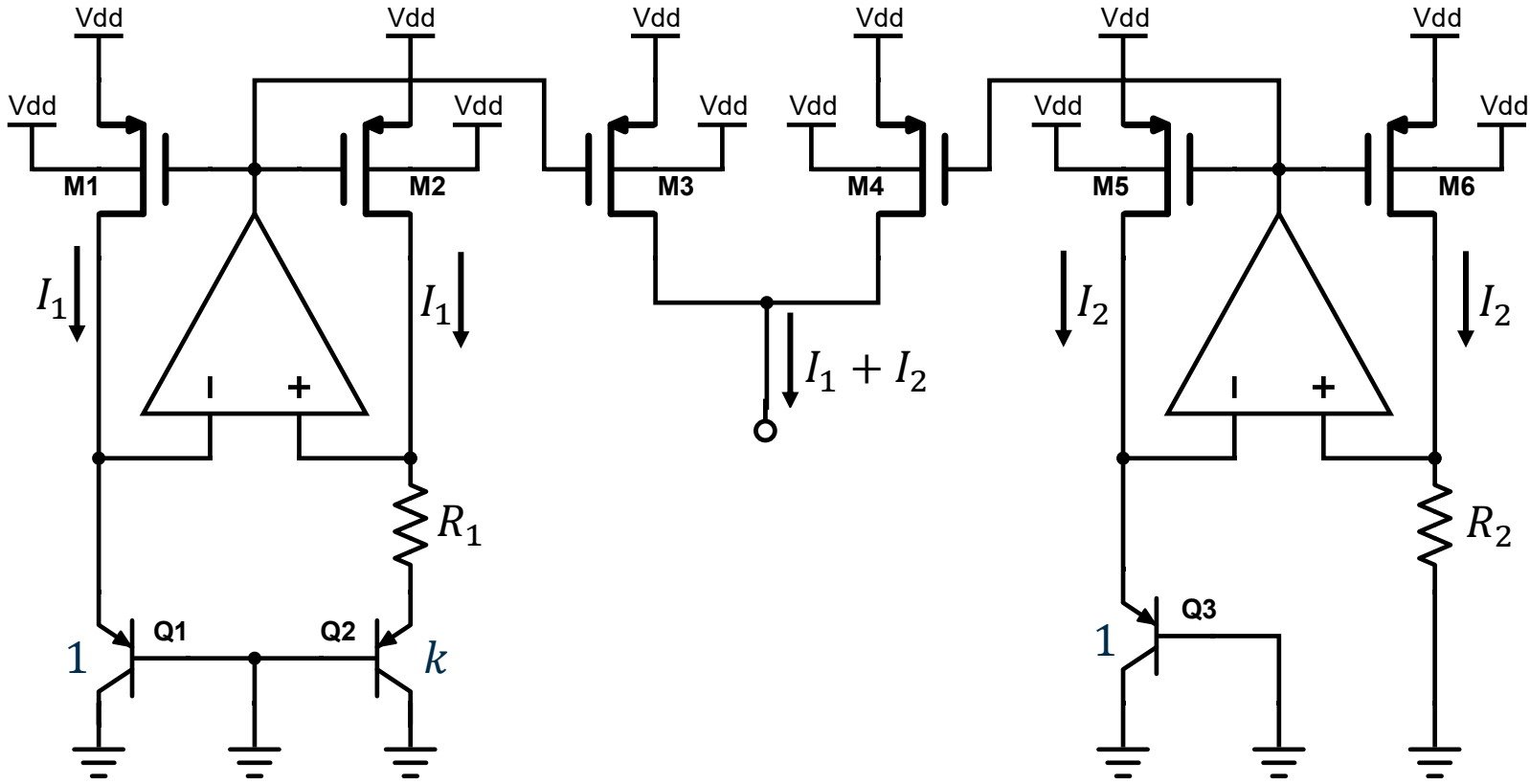
- The CTAT current is derived from the base-emitter voltage V_{BE}:

$$I_2 \cong I_{C_3} = I_S e^{\left(\frac{|V_{BE}|}{V_T}\right)}$$

$$|V_{BE}| = V_T \ln\left(\frac{I_2}{I_S}\right) ; I_2 = \frac{|V_{BE}|}{R_2}$$

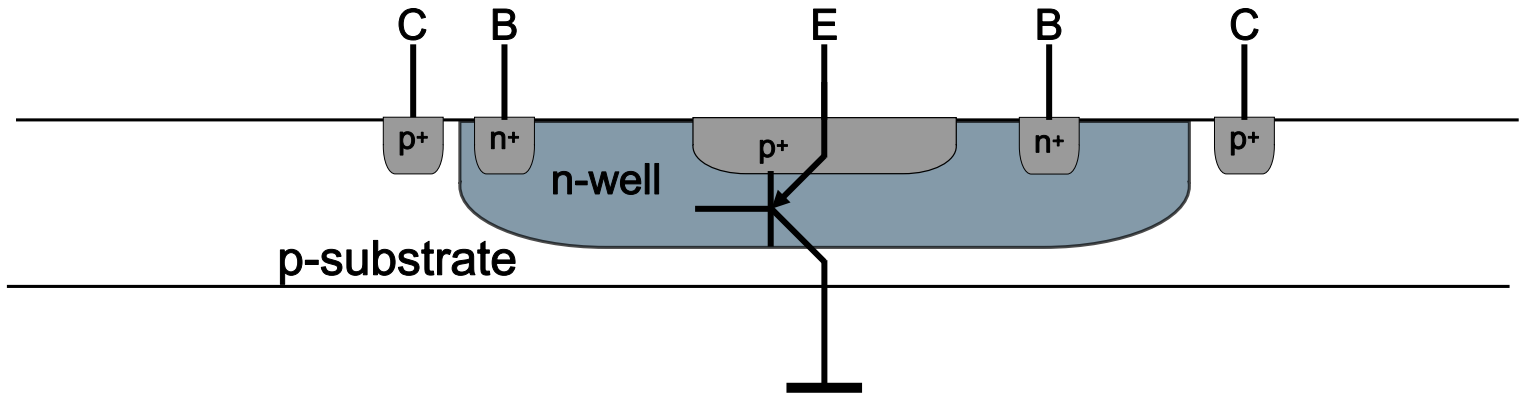
- Output current:

$$I_1 + I_2 = \frac{V_T \ln(k)}{R_1} + \frac{|V_{BE}|}{R_2}$$



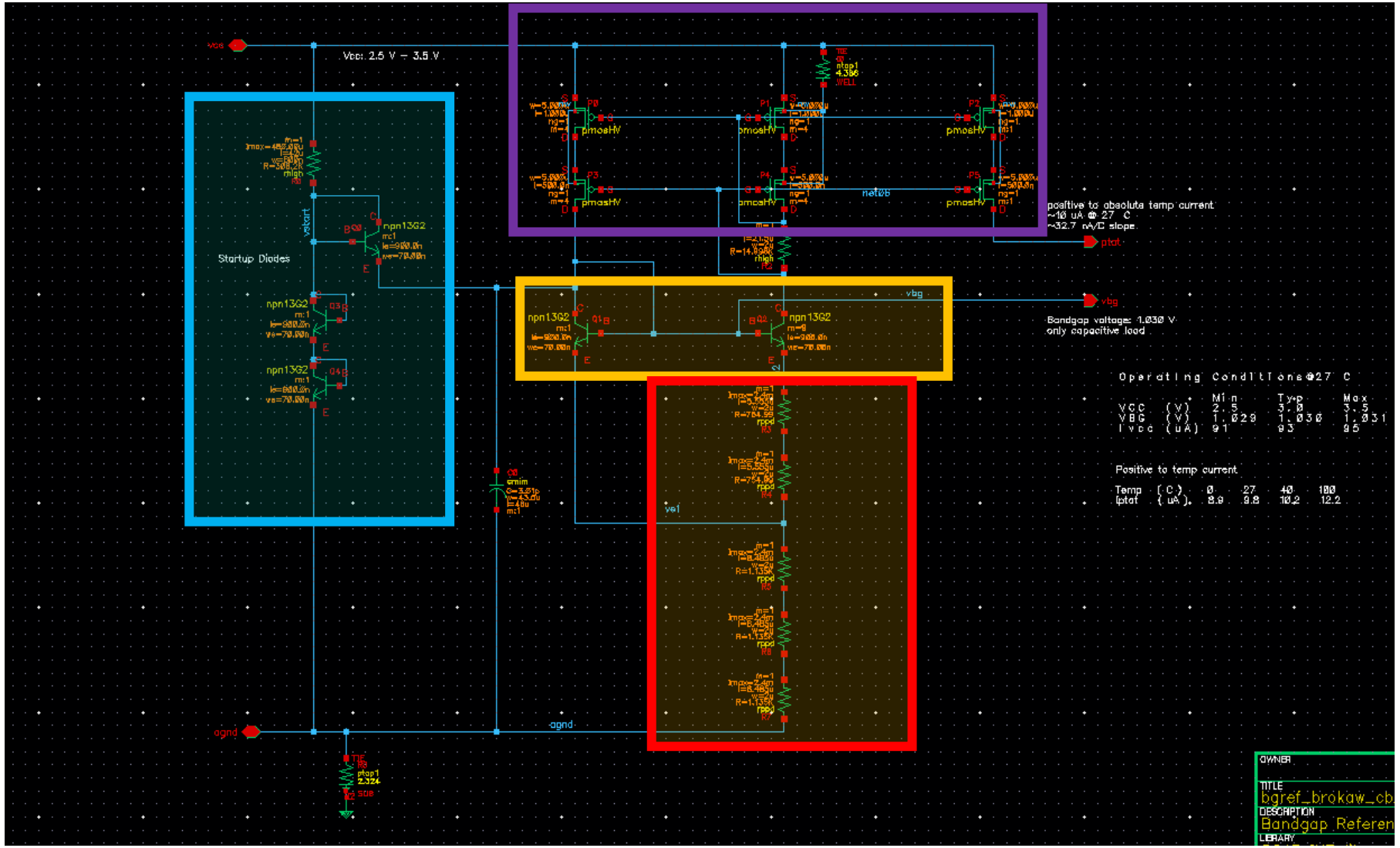
Compatibility with CMOS Technology

- In CMOS technologies, where the independent bipolar transistors are not available, parasitic bipolar transistors are used.
- Realization of PTAT voltage from the difference of the source-gate voltages of two MOS transistors biased in weak inversion is also reported in the literature.

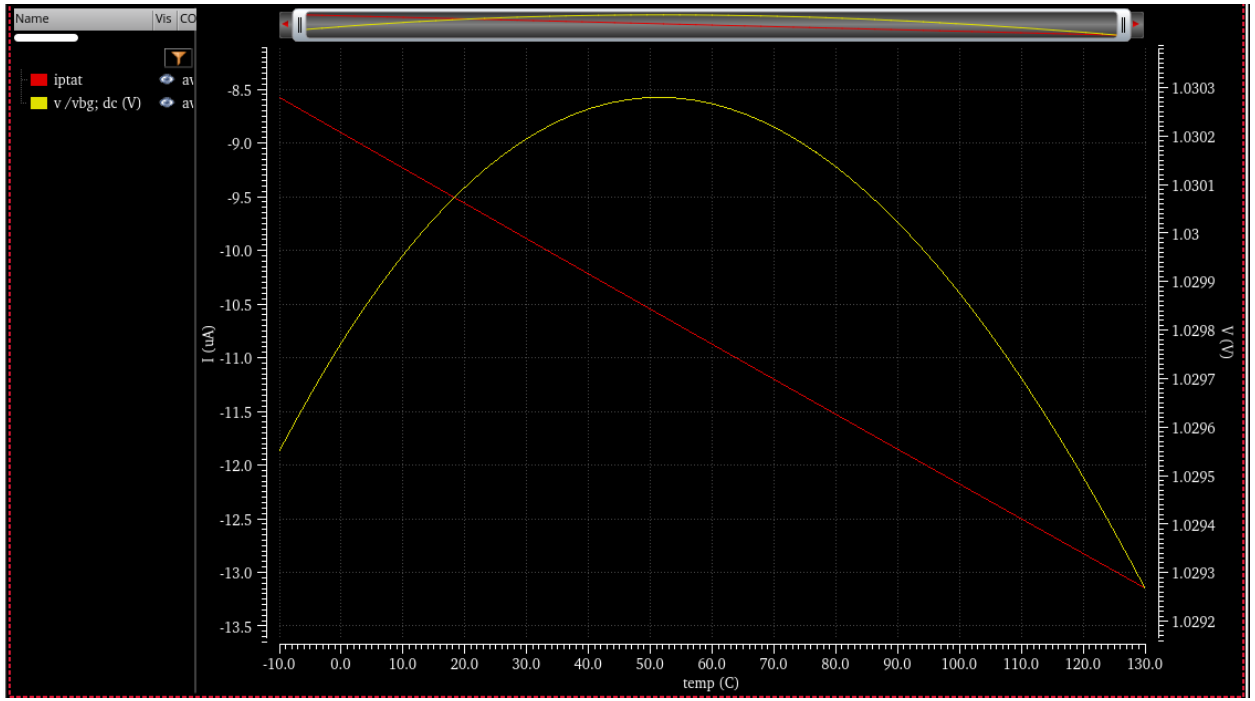


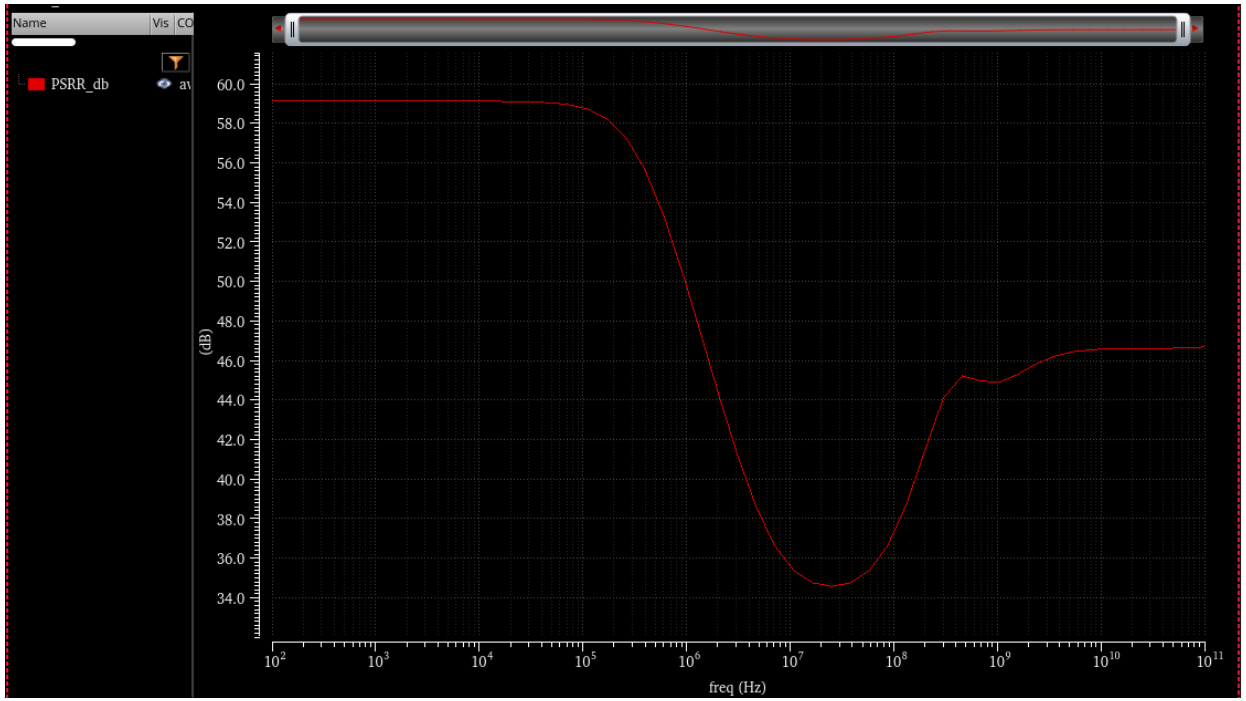
“parasitic“ substrate PNP transistor
available in any CMOS technology

Bandgap Circuit Schematic



Simulation Results



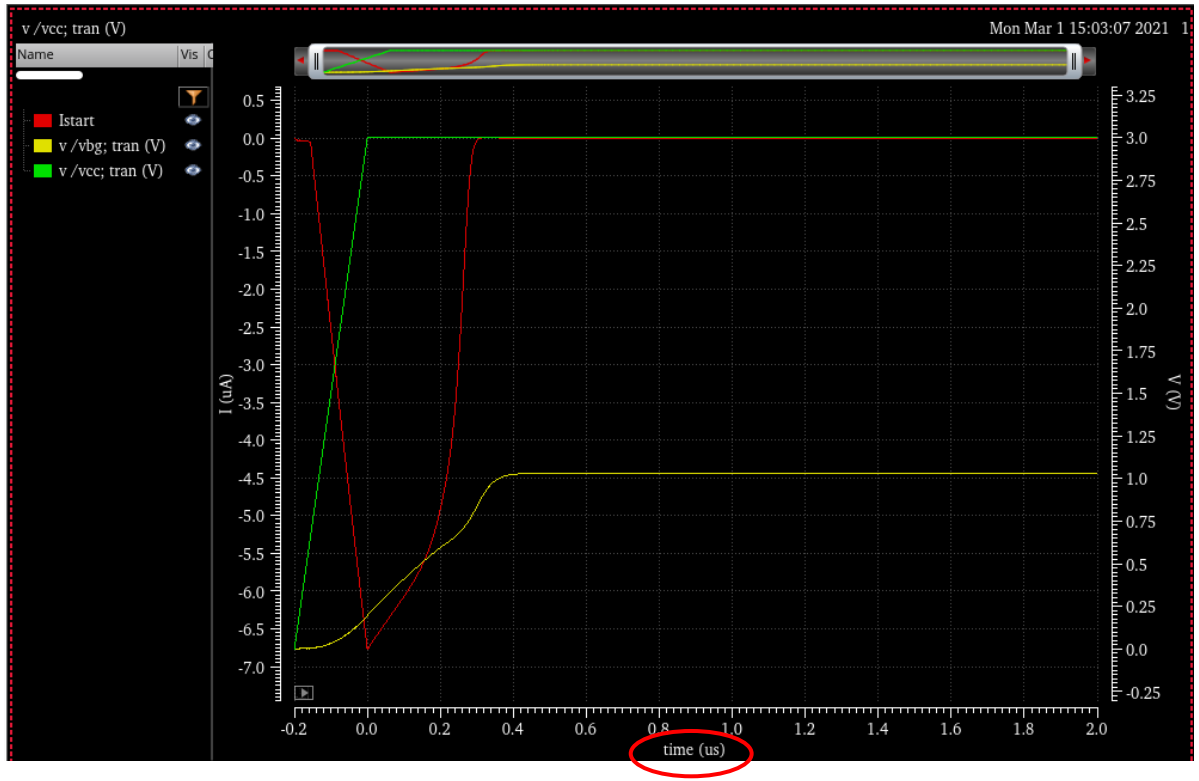


- Vbg = 1.03 V with less 1 mV Output Voltage variation (0 - 100°C)
- Iptat ≈ 10µA @27°C with 32.7nA/°C slope
- good PSRR > 34 dB
- Vcc = 2.5 – 3.5 V
- I(Vcc) = 93 µA @27°C ; 116 µA @100°C

Why Start-up Circuit ?

- Startup diodes help to bring the circuit in a defined bias point

With Startup Diode

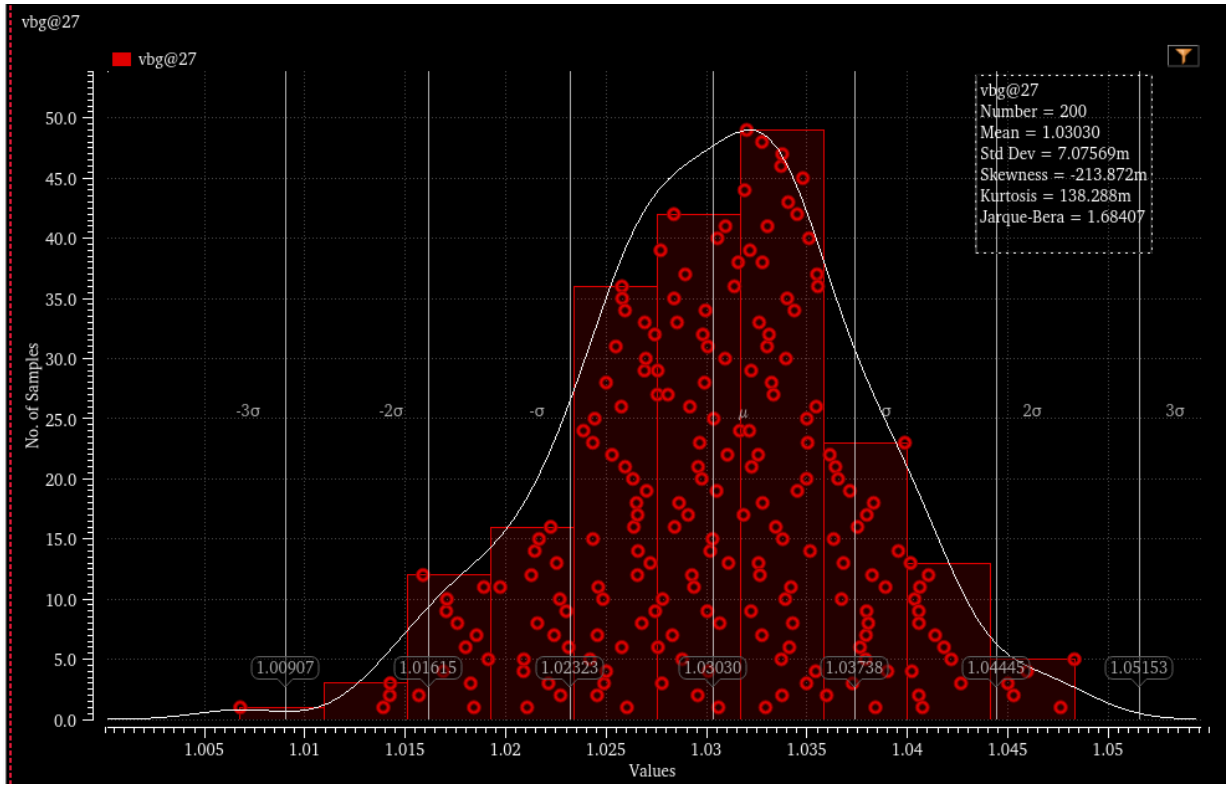


No Startup Diode

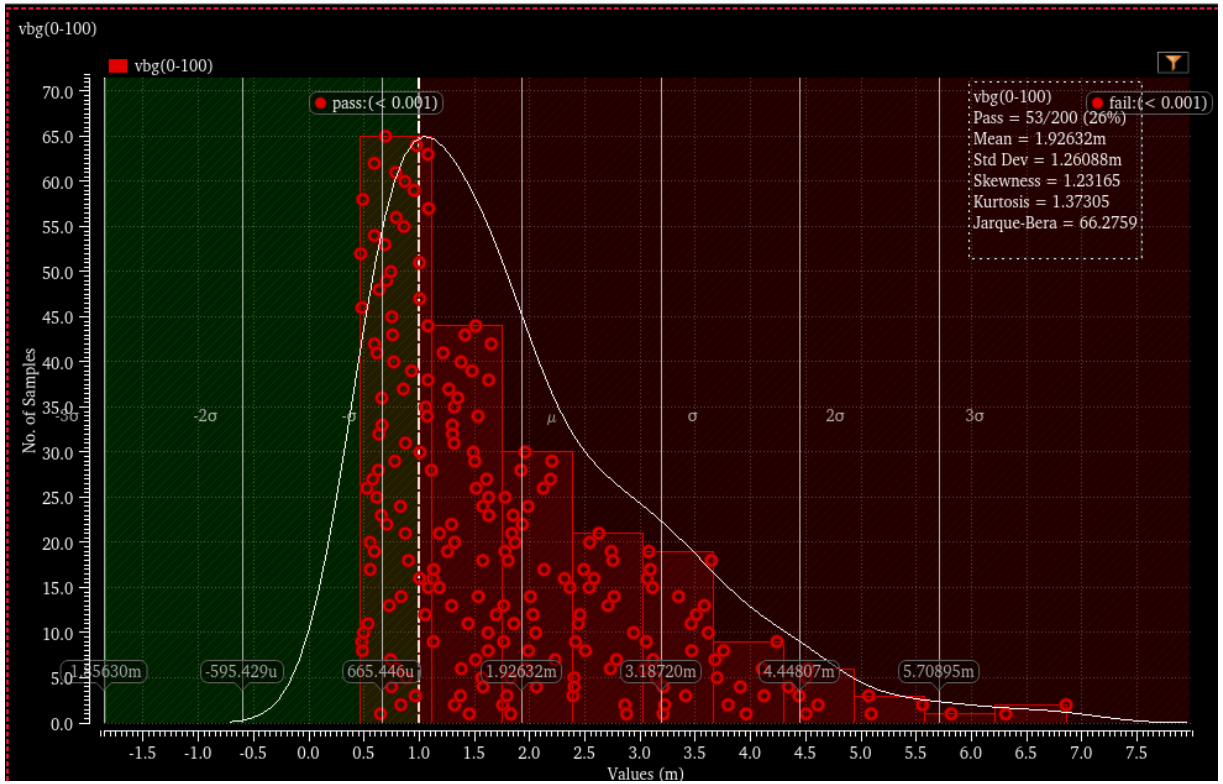
- Almost no current through the npn transistors is also a somewhat stable bias point!

Process and Device Mismatch

Output Voltage@27° C

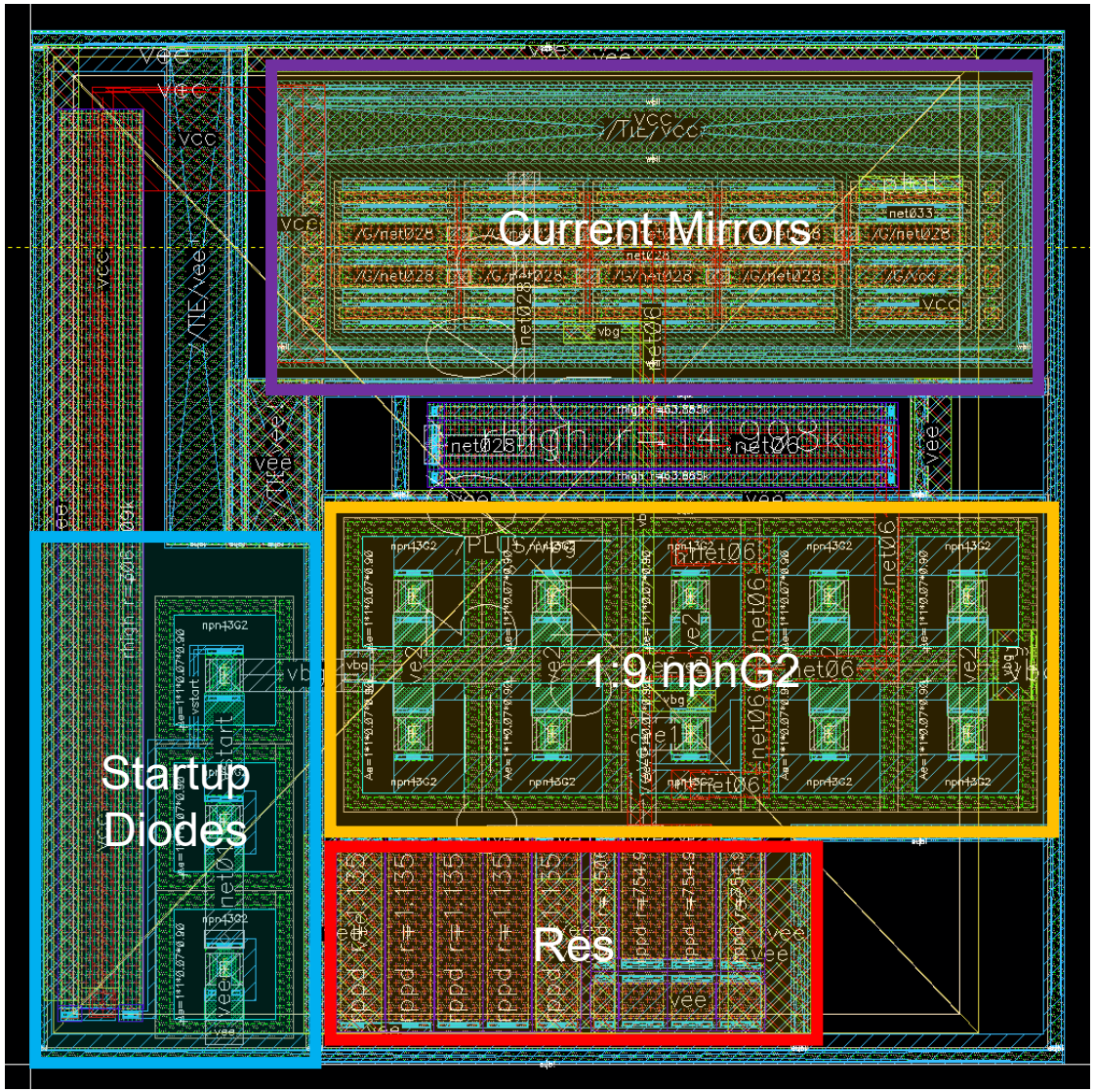


Variation 0 - 100 ° C



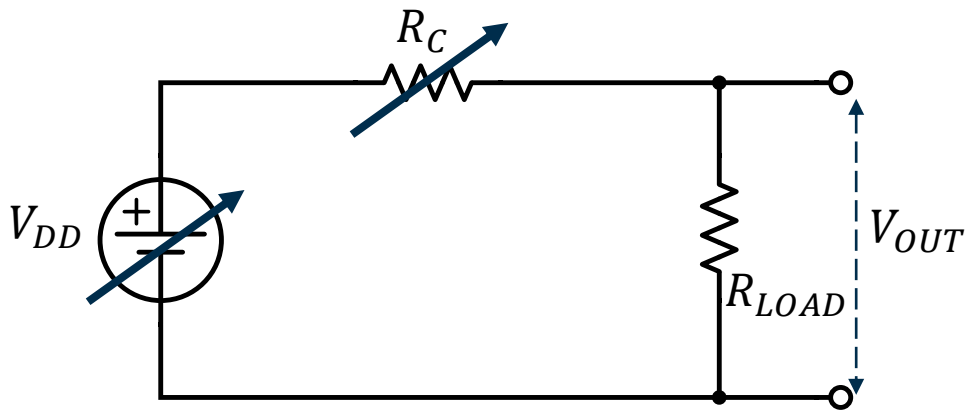
Layout

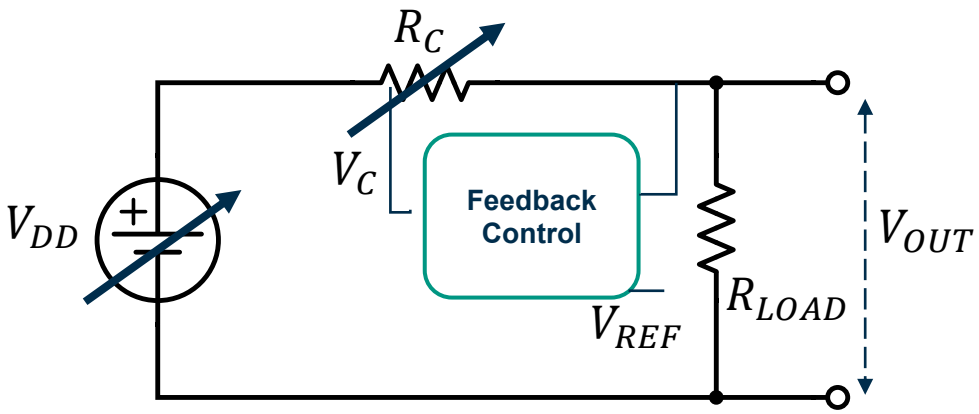
- 50 µm x 50 µm
- M1 - TM1 (Covered with a CMIM)
- Possible improvements
  - Resistor matching
  - Use only same sized resistors
  - Investigate effect of noise coupled into output
  - Higher order temp compensation
  - Pin for a voltage proportional to temp



Low Dropout Voltage (LDO)

Linear Regulator





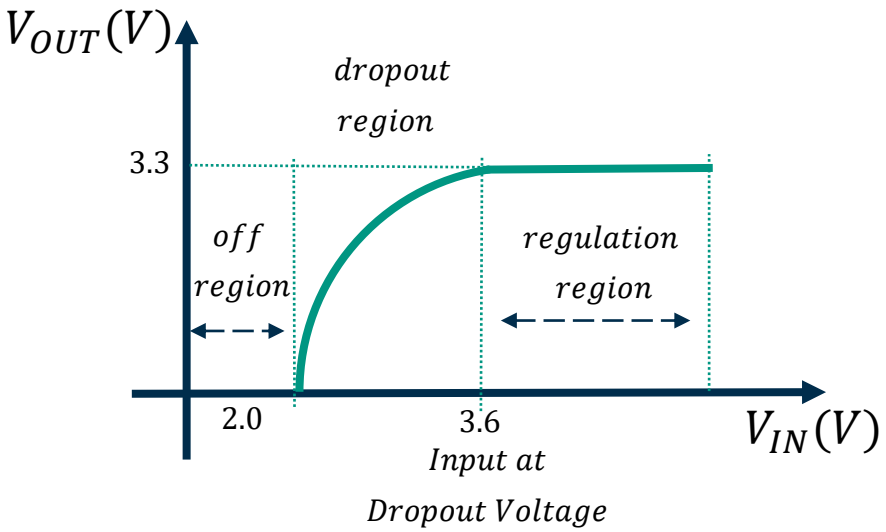
- V_{OUT} must be constant.
- V_{DD} is not constant. Over time, it will change
- R_{LOAD} can be anything.

$$V_{OUT} = \frac{R_{LOAD}}{R_{LOAD}+R_C} V_{DD}$$

- Solution is control R_C to have continuous desired V_{OUT} value

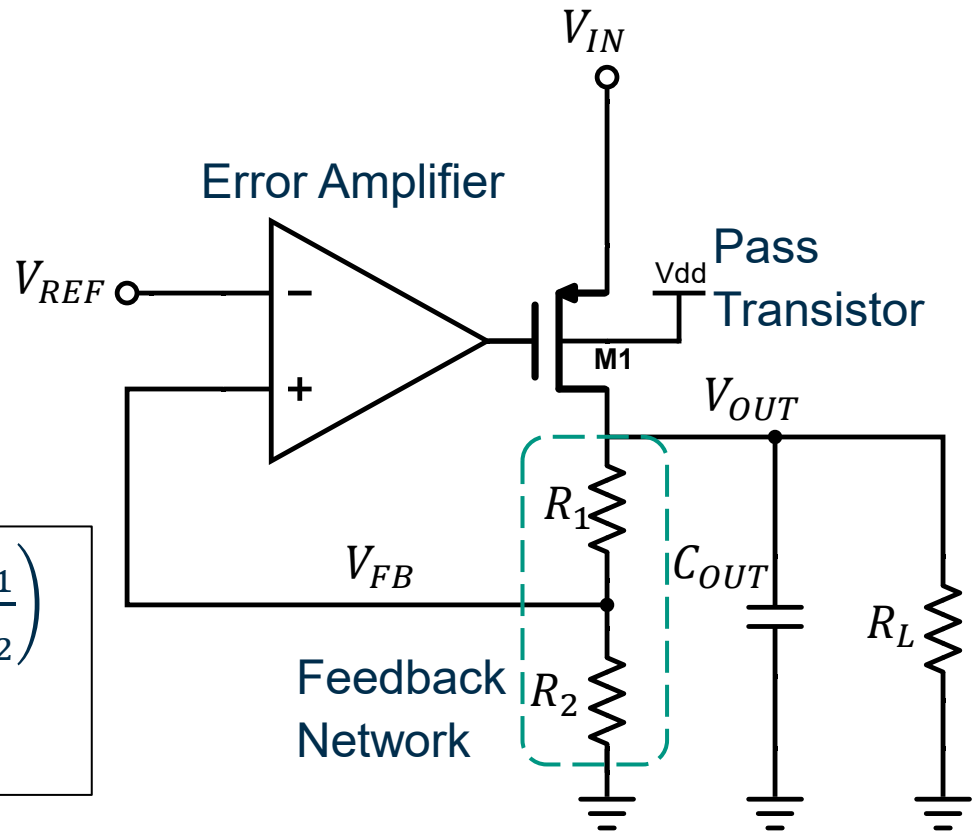
Low Dropout Regulator (LDO)

- A Low Dropout (LDO) regulator is a DC linear voltage regulator that can regulate the output voltage even when the supply voltage is very close to the output voltage.
- Low dropout voltage, $V_{DO} = V_{IN} - V_{OUT}$ only by the R_{ON} of the PMOS.
- As an example, the dropout voltage of the TPS76733 is typically $350\ mV$ at $1\ A$.

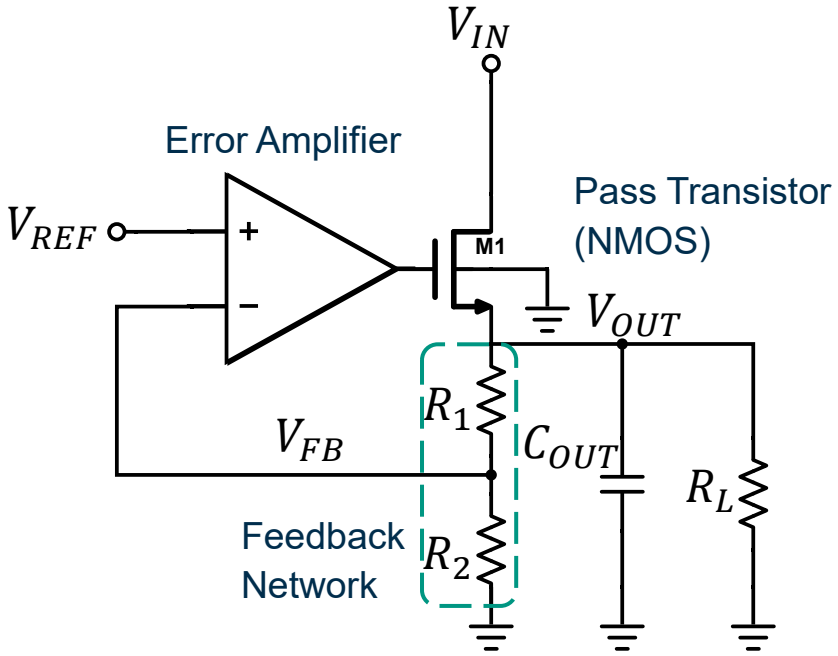


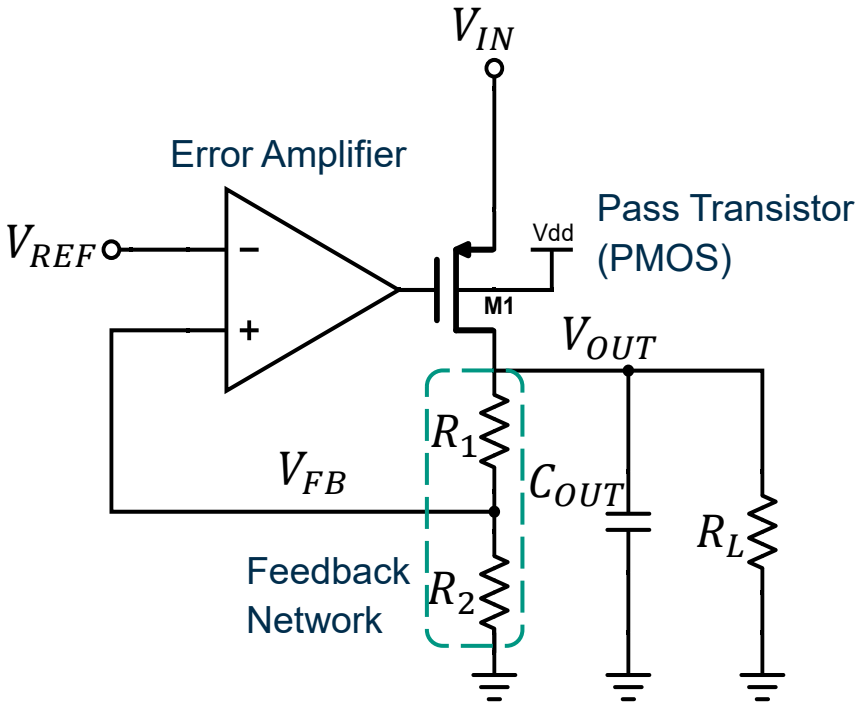
$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

$$\eta \approx \frac{V_{OUT}}{V_{IN}}$$



Pass Transistor





- Standard Linear Regulator with NMOS
  - The gate voltage (V_G) must be higher than the output (V_{OUT}) by the threshold voltage (VGS).
  - Since the Op-Amp cannot drive the gate above V_{IN}, the minimum voltage drop is large.

$$V_{IN_{min}} \approx V_{OUT} + V_{TH} + V_{OV}$$

  - Typical Dropout: 1.5V−2.0V.

- Low Dropout Regulator with PMOS
  - The Pass Transistor operates as a variable resistor. The minimum drop is determined only by the on-resistance ($R_{DS_{ON}}$), not the threshold voltage.

$$V_{dropout} = I_{LOAD}\, R_{DS_{ON}}$$

  - Typical Dropout: 100mV−300mV.