Proposed Product of "Multi-chiplet CPU Module for Gaming Computers"

1.0 The Abstract

[a] The proposed product, "Multi-Chiplet CPU Module for Gaming Computers," addresses the constraints of conventional CPUs by enhancing scalability, customization, and efficiency for gaming and AI applications. [b] Traditional CPUs face limitations due to Moore's Law, leading to power leakage, overheating, and lower production yields [1,4]. [b] Their development is both costly and time-intensive, with general-purpose solutions creating performance bottlenecks in specialized areas like gaming and artificial intelligence. [b] Additionally, they suffer from restricted memory bandwidth, minimal flexibility for rapid changes, and inefficient heat management as power consumption grows [2]. [c] The Multi-Chiplet CPU Module's design allows for greater scalability, flexibility, and personalized optimization for gaming and AI market requirements [3]. [c] Smaller 5nm chiplets improve yields and reduce costs, while heterogeneous cores and integrated AI units boost performance, solving inefficiencies in older CPUs. [d] This product pushes beyond Moore's Law by employing modular chiplets, enhancing yields, cutting costs, and scaling up efficiently. [d] Its adaptable architecture, including an AI processing unit, eliminates bottlenecks and expands memory bandwidth, while modularity accelerates customization with advanced thermal management optimizes heat dissipation and power use. [e] The "Multi-Chiplet CPU Module for Gaming Computers" surpasses traditional CPU limitations

with modular chiplets, elevating scalability, performance, and customization for gaming and AI tasks.

[f] Key words: Chiplet, CPU, AI, Gaming, DCRA, Architecture, Dynamic Configuration, Heterogeneous, Adapt-NoC

2.0 The Executive Summary

[g] Traditional monolithic CPU designs are encountering growing challenges in meeting the demands of modern gaming PCs, particularly in terms of scalability, thermal management, and production efficiency. [h]As gaming demands grow, monolithic CPUs begin experiencing performance bottlenecks, power usage, and rising manufacturing costs. [h] Production of traditional monolithic CPUs has also increased massively, advanced nodes have been priced around 20% higher [4]. [h] On identical chips, the tested monolithic chip is currently worth approximately $567/unit due to the complexity and lower yields associated with large single-die architectures [16]. [h] In contrast, the Multi-Chiplet chip will be a more economical option as units of production would cost around $215 — a 37% saving over monolithic alternatives [16]. The chiplet design provides greater production yields and design flexibility by disaggregating the CPU into smaller and more controllable chiplets [3]. This

arrangement also increases heat dissipation and performance by scaling computation to a number of chiplets, and addresses the drawbacks of a CPU. [i] The cost savings and increased efficiency of the multi-chiplet design are expected to recoup initial investment within 2.5 years, enabling a competitive price point in the market[11,12,13]. [j] As a result, advancing the development of the Multi-Chiplet CPU Module is highly recommended, as it presents a more cost-effective and performance-driven alternative to conventional monolithic CPUs. [j] By taking advantage of the enhanced manufacturing cost-efficiency and scalability of chiplet architecture, this module has a unique chance to compete successfully in the high-end gaming CPU market by bringing an intelligent next-generation solution that solves many of the issues facing current CPU designs while maintaining competitive pricing.

3.0 The Product Description/Proposed Business Concept

[k] The "Multi-Chiplet CPU Module for Gaming Computers" incorporates essential features like dynamic chiplet configuration, customizable chiplet designs, and the Adapt-NoC, all based on Heterogeneous Manycore Architectures. This modular framework boosts performance, scalability, and future-proofing by facilitating easier updates and upgrades to individual components. [i] Heterogeneous Manycore Architectures improve performance by leveraging diverse computing resources and efficient communication systems and is more

efficient than single- and homogenous multi-core architectures [5]. [i] The Dynamic Chiplet Configuration allows real-time adjustments within the multi-chiplet architecture, enabling the addition or removal of chiplets based on workload demands, optimizing performance, energy efficiency, and resource utilization and will be implemented through DCRA (Distributed Chiplet-based Reconfigurable Architecture) [6]. As the manycore systems often face memory and interconnect inefficiencies when handling such tasks, the DCRA provides flexible memory hierarchy designs, allowing DRAM to be integrated or interleaved between chiplets as needed [6]. In Heterogeneous Manycore Architectures, static Network-on-Chip (NoC) configurations frequently result in inefficiencies during inter-chiplet communication, especially when dealing with dynamic and diverse workloads [7]. [i] Adapt-NoC addresses this by enabling dynamic partitioning and reconfiguration of sub-NoCs, allowing routers and links to adapt in real time to workload changes [7]. [i] Customizable chiplet designs play a crucial role in semiconductor innovation, where multiple chiplet is built in separate functional blocks, specialized for tasks like CPU processing, GPU acceleration, AI computation, memory control, and power management. This method enables manufacturers to combine chiplets from different process technologies, maximizing performance and reducing manufacturing costs by reusing existing chiplets. With these groundbreaking features and advanced chiplet technology, the product stands out against competitors and is poised for unrivaled success.

[i][6] The DCRA architecture addresses the need for a reconfigurable design to meet varying performance, power, area (PPA), and cost targets for irregular applications. The Torus NoC (Network-on-Chip), is designed to span multiple dies and packages, allowing scalability. DCRA manages the tile's SRAM as either a cache or scratchpad, providing prefetching support via a task-based execution model. DRAM dies can be interleaved with DCRA dies for enhanced memory configuration. DCRA builds upon the task-based execution model of Dalorex, where tasks are managed by the Task-Scheduling Unit (TSU) and routed through the NoC to the appropriate tile that owns the data. This task-based approach shifts the challenge from irregular memory accesses to irregular inter-tile communication. To handle this, DCRA employs a 2D torus network, which provides better uniformity than a 2D mesh for handling irregular traffic, as demonstrated in Dalorex. However, unlike Dalorex's monolithic wafer-scale design, DCRA solves the issue of implementing the torus NoC across different grid sizes and dies. The DCRA aims to efficiently handle variable workloads, such as data traversal algorithms, which have non-uniform compute demands. It achieves this by offering several configuration options at different stages (pre-silicon, packaging, compile-time) to balance performance, cost, and energy efficiency.

[i][7] Heterogeneous manycore architectures in "Multi-chiplet CPU module for Gaming Computers" enable handling of large number of applications, by combining computing resources from CPUs, GPUs and accelerators and communication channels for

cache and memory coherence. Yet static NoC designs have trouble coping with heterogeneous traffic streams generated by concurrent applications, which results in a deficient system. These shortcomings are mitigated by chiplet-based manycore architectures that utilize a silicon interposer to divide the monolithic chips into smaller chiplets connected by micro-bumps (μbumps). While passive interposers underutilize wiring resources, active interposers integrate wires and transistors using cost-effective technologies like 65nm, improving both economic efficiency and performance. Enhanced communication between chiplets and capacity demands on memory can be met by active interposers that facilitate double-layer NoC design. Techniques such as SMART, which bypasses multiple hops in one cycle, and Panthre, which reconfigures NoC topology to avoid power-gated routers, further enhance performance and energy efficiency, and can be integrated into adaptive designs like Adapt-NoC for additional optimization.

[i][7] Adapt-NoC provides dynamic subNoC partitioning and reconfiguration in order to optimize inter-chiplet communication in multi-chiplet CPU. By designing flexible routers and links, it enables workload-aware real-time reconfiguration that optimises the flow of data without slowing down the system. This provides for dynamic chiplet set up and workload scalability. As Adapt-NoC creates multiple sub-networks, each subNoC can handle various traffic and workloads at a time, which reduces cross-chiplet collisions and boosts performance across mixed architectures of AI chiplets, CPU chiplets, and memory

controllers. The sharing of memory controllers among subNoCs ensures efficient use of memory resources and reduces bottlenecks. Reconfigurable routers and links adjust link connections as the traffic peaks, so PCIe 5.0, DDR5 memory, and inter-chiplet communication flow seamlessly. Internal lock mechanisms prevent deadlock and keep the system running during chiplet changes. Additionally, power-gating is compatible with dynamic voltage and frequency scaling (DVFS), enabling efficient energy use under various loads.

[i][8] Customizable Chiplet Designs like Memory Controller Chiplets, AI Processing Chiplets, CPU Chiplets, and Power Management Chiplets are included in the product artechieture and delivers major performance, efficiency, and scalability benefits. The Memory Controller Chiplets control access and allocation of memory to ensure optimum bandwidth utilization, as the workload requires. This prevents bottlenecks for memory intensive applications such as AI and gaming. AI Processing Chiplets are specially designed resources for machine learning computation, by disassociating the AI computations from standard CPU cores allowing for faster AI processing without depleting CPU cycles. CPU Chiplets rely on heterogenous cores, whereby high performance cores do heavy workloads, and efficiency cores do background work and thus optimize the resource consumption of the tasks. Finally, Power Management Chiplets automatically control voltage and frequency, so power is deployed as needed depending on the load, reducing energy costs without compromising

performance. The task-based modularity ensures performance, but also easy updates and upgrades to individual components, giving more flexibility and future-proofing for the future.

[i][9, 10] Other highlights of the Multi-Chiplet CPU Module include scalable chiplet architecture (based on TSMC's 5nm process), DDR5 and PCIe 5.0 support, dynamic chiplet design to adapt to workloads in real time, and robust thermal management that helps make it both powerful and cost effective with 16 heterogeneous cores. Multi-Chiplet CPU Module designed on chiplet architecture featuring multiple CPU chiplets (CCDs) and an I/O die (IOD) to scale. It's manufactured with TSMC's cutting-edge 5nm process and comes with DDR5 memory and PCIe 5.0. With a temperature-dependent TDP of 180W, the module runs entirely on external GPUs without integrating graphics. Its dynamic chiplet structure allows real-time workload adjustment through CCIX inter-chiplet communication protocols. AI processing chips and chiplet designs are specialised to particular purposes. The module also encapsulates advanced thermal management and security features for optimal performance and protection. The design consists of 16 heterogenous cores with cache levels L1: 64KB, L2: 1MB, and L3: 32MB that is connected through mesh, PCIe, and Infinity Fabric.

4.0 Market Research & Analysis

The U.S. market for Multi-Chiplet CPU Modules plays a critical role in the gaming hardware sector, fueled by strong consumer demand and the growing sophistication of gaming

technologies. The U.S. market for Multi-Chiplet CPU Modules for Gaming Computers is currently valued at approximately $9 billion annually, primarily driven by the gaming PC and laptop segments [11]. With an estimated 14 million users and a per capita income of around $650, this results in a market penetration rate of 4.1%. This market includes B2C gaming hardware, covering both online and offline sales, consumer spending, and taxes [12]. Significant growth potential exists within both the CPU and GPU sectors. Specifically, CPU spending is projected to increase from $773.5 per person in 2024 to $1,102 by 2029, while GPU spending is expected to rise from $689.5 to $1,260 within the same period [11,12,13]. Globally, the gaming market is expected to grow from $59.2 billion in 2024 to $79.58 billion by 2029, with the number of gamers projected to increase from 136 million to 156 million over these five years [11,12,13]. Establishing a foothold in the U.S. market will allow the Multi-Chiplet CPU Module to expand its reach globally, capitalizing on its early success to dominate the international gaming hardware sector. Financial and economic considerations are crucial for this endeavor, requiring substantial initial investments in research and development, advanced manufacturing processes, and marketing strategies to build market presence. With an anticipated initial market penetration rate of 1% in Year 1, revenues could reach $90 million, climbing to $135 million in Year 2, $180 million in Year 3, $270 million in Year 4, and $450 million by Year 5, assuming a market penetration rate of 5%. Cumulatively, this would generate an estimated total revenue of $1.125 billion over five years, presenting a

favorable economic environment for new market entrants. Leveraging economies of scale in production could help drive down costs, improving profit margins. Additionally, offering innovative features and customizable designs could support premium pricing, attracting gamers who prioritize high-performance systems. As CPU spending is forecasted to increase from $773.5 per person in 2024 to $1,102 by 2029, the Multi-Chiplet CPU Module could position itself as a premium choice in the evolving gaming hardware market [11,12,13]. Careful financial planning, market analysis, and strategic execution will be essential to navigating competitive pressures and maximizing returns on investment in this dynamic industry.

On performance front, with its chiplet architecture, adaptive setup and customizable chiplet layout, the Multi-Chiplet CPU Module is able to match AMD Ryzen 7000 series or Intel Core i9-13900K processors. The product's innovations arise from the product's Dynamic Chiplet Configuration, powered by Distributed Chiplet-based Reconfigurable Architecture (DCRA) and Heterogeneous Manycore Architectures, which are superior to AMD Ryzen and Intel Core CPUs in breaking a fundamental limitation of manycore systems: processing odd workloads such as graph processing [6,7]. The DCRA has the flexibility of adjusting memory resources dynamically to achieve the best performance in unregular workloads, varying power, performance, and area (PPA) targets [6]. A 2D torus NoC ensures a uniform flow of traffic between different dies without bottlenecks typical of the traditional

processor [7]. The Heterogeneous Manycore Architecture combines CPUs, GPUs and accelerators with a double-layer NoC on active interposers to further facilitate flexibility. In contrast to static architectures, the design allows partitioning and reconfiguration in real time through Adapt-NoC, enabling optimal communication paths and load allocation in real time [7]. Other configurable chiplet patterns like Memory Controller Chiplets, AI Processing Chiplets, and Power Management Chiplets add efficiency. Memory Controller Chiplets scale memory bandwidth, AI Processing Chiplets perform faster machine learning, and Power Management Chiplets control power via dynamic voltage and frequency scaling (DVFS). With its 5nm manufacturing technology, the Multi-Chiplet CPU Module easily competes with AMD Ryzen 7000 series and Intel Core i9-13900K for enhanced performance and efficiency. Heterogenous architecture allows real-time chiplet addition/removal for dynamic workload optimization versus Ryzen's fixed 16 core, 5.7 GHz model with 16 heterogeneous cores and estimated 4.5 GHz [14,15]. With a TDP of 253W, the Intel i9-13900K is beaten by the Multi-Chiplet's 180W TDP and high-performance cooling [15]. Featuring DDR5 memory and PCIe 5.0 connectivity, this design delivers high performance and customization to ensure its viability within U.S. and international markets for gaming hardware.

5.0 Finance & Economics:

[4,16] The cost of developing a prototype Multi-Chiplet CPU Module utilizing

TSMC's advanced 5nm process, chiplet integration, and specialized components, can amount to approximately $122,000, driven by high manufacturing, packaging, and hardware deployment expenses. The deployment of TSMC’s powerful 5nm process for CCD and IOD multiplexing is expensive, often upwards of $17,000 per wafer. If we take as an underlying model the prototyping of four CPU chiplets and one IOD, the overall chip manufacturing expense can exceed $50,000, minus mask sets and fabrication. Extras such as chiplet integration packaging using a silicon interposer adds $20,000 and dynamic chiplet deployment with Distributed Chiplet-based Reconfigurable Architecture (DCRA) for an additional $15,000 for hardware and connectors like CCIX. Combining AI processor chiplets, power management, and memory controller chiplets adds another $25,000. Private-label cooling — necessary for the 180W variable TDP, as well as thermal management and security — adds about $5,000. The PCIe 5.0 and DDR5 memory support also brings additional costs up around $7,000 on the controllers and other parts needed. The approximate cost of creating a prototype is $122,000 including design, testing, and packaging.

6.0 Technical Team Skills:

To manufacture the Multi-Chiplet CPU Module, it takes a dedicated 16-25 person team including architects, engineers, software engineers and security professionals to plan, design, optimize and validate chiplets, interconnects and firmware. Architects (1-2): System

Architect will build the architecture with chiplet interconnect and communication protocols such as CCIX. Chip Design Engineers (3-5) design CPU chiplets, AI processors, memory controllers and power management chiplets. Verification Engineers (2-3) check chip functionality, especially DCRA and heterogeneous cores. Interconnect Engineers (2-3) improve chiplet communication through Torus NoC/Adapt-NoC. Temperature Control Engineers (2-3) apply adjustable TDP and thermal control. Chiplet and memory management firmware development by Software Developers (3-5). Physical Design Engineers (2-3) – layout and manufacturing; Testing Engineers (2-3) – performance evaluation; Security Engineers (1-2) – security aspects.

7.0 Risks & Assumptions

[17] The Multi-Chiplet CPU Module is threatened by manufacturing issues, thermal management problems, inter-chiplet communication bottlenecks, and software optimisation while having to satisfy market needs in order for AI and gaming to be viable. Some of the risks of manufacturing the Multi-Chiplet CPU Module include making it difficult with the TSMC 5nm process, the 180W TDP can have issues with thermal and power management, and the inter-chiplet communication with CCIX and Adapt-NoC will lead to latency or bottlenecks. In combination with the fluid hierarchies, memory and cache consistency risk high-load drunkeling. It requires custom firmware/software tweaking for exploitation of the

architecture and vulnerabilities in inter-chiplet communication can break the system. And higher production cost, market pressure and uncertainty of software ecosystem support are also major threats. The blueprint assumes robust requirements for AI/gaming optimization, thermal management, scalability of NoC and the flexibility to futureproof with adaptable chiplets are all critical to the success of the product.

8.0 Conclusions and Recommendation

"Multi-Chiplet CPU Module for Gaming Computers" is a groundbreaking processor design, offering better scalability, customizability and performance compared to monolithic CPUs. The proposed product changes the way CPUs are designed by overcoming monolithic CPU architecture and provides modular and scalable architecture for high-density games and AI environments. Module utilizes dynamic chiplet architecture that allows instant chiplet addition and deletion with the shift in workload. In addition to the flexibility, power usage and scalability are increased and the CPU can handle multiple high-performance, hard workloads easily such as 4K gaming, raytracing, artificial intelligence tasks like NPC behavior or advanced physics simulations. Its architecture is further optimized through 5nm manufacturing technology that results in transistor density and also high thermal efficiency and power consumption improvement. Apart from that, having AI-based processing chiplets dedicated to ML workloads will ensure future-proofability of the module as AI already enters

every gaming and general-purpose computing context. With the market conditions, which are driving demand for gaming hardware and AI applications sparked by it, this module is emerging as an in its own category against big players like AMD and Intel. Market entry time also depends on economy and technologies. [m] To contend, however, attention needs to be focused on specific R&D, on chiplet communication and thermal management, to increase performance without compromising efficiency. [m] In addition, proper marketing will be necessary to inform consumers on the benefits of multi-chiplet design versus conventional CPUs. [m] If the Multi-Chiplet CPU Module can successfully combine both technology and market need, it has the potential to revolutionize the gaming hardware market in the world and provide gamers and AI enthusiasts with a new sense of performance, scalability and flexibility.

Reference:

[1] T. Li, J. Hou, J. Yan, R. Liu, H. Yang, and Z. Sun, “Chiplet heterogeneous integration technology—status and challenges,” Electronics, vol. 9, no. 4, Article 670, Apr. 2020. [Online]. Available: https://doi.org/10.3390/electronics9040670. [Accessed: Oct. 19, 2024].

[2] V. Gujar, “Chiplet technology: revolutionizing semiconductor design—A review,” Saudi Journal of Engineering and Technology, vol. 9, no. 2, Article 006, Feb. 2024. [Online].

Available: https://saudijournals.com. [Accessed: Oct. 19, 2024].

https://www.researchgate.net/publication/378156097_Chiplet_Technology_Revolutionizing_Semiconductor_Design-A_Review

[3] Chiplets — the inevitable transition

(AMD, Intel CPU MCM structure)

https://blog.apnic.net/2023/11/07/chiplets-the-inevitable-transition/

[4] Y. Feng and K. Ma, “Chiplet actuary: A quantitative cost model and multi-chiplet architecture exploration,” arXiv, vol. 2203.12268v4 [cs.AR], Apr. 2024. [Online]. Available: https://arxiv.org/html/2203.12268v4. [Accessed: Oct. 19, 2024].

[5] G. Shan, Y. Zheng, C. Xing, D. Chen, G. Li, and Y. Yang, “Architecture of computing system based on chiplet,” Micromachines (Basel), vol. 13, no. 2, Article 205, Jan. 2022. doi: 10.3390/mi13020205. [Online]. Available: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC8877588/. [Accessed: Oct. 19, 2024].

[6] M. Orenes-Vera, E. Tureci, M. Martonosi, and D. Wentzlaff, “DCRA: A distributed

chiplet-based reconfigurable architecture for irregular applications," presented at Princeton University, Princeton, NJ, USA. [Online]. Available: https://ar5iv.labs.arxiv.org/html/2311.15443v2. [Accessed: Oct. 19, 2024].

[7] H. Zheng, K. Wang, and A. Louri, "A versatile and flexible chiplet-based system design for heterogeneous manycore architectures," presented at the Department of Electrical and Computer Engineering, George Washington University, Washington, D.C. [Online]. Available: https://par.nsf.gov/servlets/purl/10229858. [Accessed: Oct. 19, 2024].

[8] Y. Kwon et al., "Chiplet heterogeneous-integration AI processor," in 2023 International Conference on Electronics, Information, and Communication (ICEIC), Singapore, 2023, pp. 1–2. doi: 10.1109/ICEIC57457.2023.10049867. [Accessed: Oct. 19, 2024]. https://ieeexplore-ieee-org.libaccess.sjlibrary.org/document/10049867

[9] A. Fogli, B. Zhao, P. Pietzuch, M. Bandle, and J. Giceva, "OLAP on modern chiplet-based processors," presented at Imperial College London, London, U.K., and TU Munich, Munich, Germany. [Online]. Available: https://zbjob.github.io/VLDB24.pdf. [Accessed: Oct. 19, 2024].

[10] Liu, Y., Li, X. & Yin, S. Review of chiplet-based design: system architecture and interconnection. Sci. China Inf. Sci. 67, 200401 (2024). https://doi.org/10.1007/s11432-023-3926-8

https://link.springer.com/article/10.1007/s11432-023-3926-8

[11] No Author, "Gaming Hardware - United States," 2024. [Online]. Available: https://www-statista-com.libaccess.sjlibrary.org/outlook/amo/media/games/gaming-hardware/united-states. [Accessed: Oct. 19, 2024].

[12] No Author, "Gaming Accessories - United States," 2024. [Online]. Available: https://www-statista-com.libaccess.sjlibrary.org/outlook/amo/media/games/gaming-hardware/gaming-accessories/united-states. [Accessed: Oct. 19, 2024].

[13] No Author, "Gaming Hardware - Worldwide," 2024. [Online]. Available: https://www-statista-com.libaccess.sjlibrary.org/outlook/amo/media/games/gaming-hardware/worldwide#analyst-opinion. [Accessed: Oct. 19, 2024].

[14] No Author, "Ryzen 5 7500F: Performance Tests in Benchmarks and Full Specs," 2024. [Online]. Available: https://nanoreview.net/en/cpu/amd-ryzen-5-7500f. [Accessed: Oct. 19, 2024].

[15] K. Hinum, "Intel Core i9-13900K Processor - Benchmarks and Specs," Nov. 4, 2022. [Online]. Available: https://www.notebookcheck.net/Intel-Core-i9-13900K-Processor-Benchmarks-and-Specs.666495.0.html. [Accessed: Oct. 19, 2024].

[16] Dylan Patel, "Die Size and Reticle Conundrum – Cost Model With Lithography Scanner Throughput," [Online]. Available: https://www.semianalysis.com/p/die-size-and-reticle-conundrum-cost. [Accessed: Oct. 19, 2024].

[17] G. H. Loh, S. Naffziger and K. Lepak, "Understanding Chiplets Today to Anticipate Future Integration Opportunities and Limits," 2021 Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 2021, pp. 142-145, doi: 10.23919/DATE51398.2021.9474021.
https://ieeexplore-ieee-org.libaccess.sjlibrary.org/document/9474021

[18] W. T. Beyene, “Chiplet technology and heterogeneous integration,” IEEE, Senior Member, [Online]. Available: https://eps.ieee.org/images/files/enews/EDMS_TC_-_Chiplet_Technology_and_Heterogenous_Integration.pdf

Chiplet Technology and Heterogeneous Integration. [Accessed: Oct. 19, 2024].

[19] S. Naffziger et al., “Pioneering chiplet technology and design for the AMD EPYC™ and Ryzen™ processor families: Industrial product,” in 2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA), Valencia, Spain, 2021, pp. 57–70. doi: 10.1109/ISCA52012.2021.00014.

https://ieeexplore-ieee-org.libaccess.sjlibrary.org/document/9499852

Check list:

✔	[a] Abstract: Motivation Sentence
×	[b] Abstract: Problem Statement
×	[c] Abstract: Approach Statement
×	[e] Abstract: Conclusions Sentence

×	[d] Abstract: Results Sentence
×	[f] Abstract: Keywords
×	[g] Executive Summary: Proposal Background
×	[h]Executive Summary: Problem Statement
×	[i] Executive Summary: Financial statement related to the proposal
×	[j]Executive Summary: Recommended action for “boss”
×	[k] Product Description: Product Description (underline only the topic sentence of the paragraph)
×	[l] Product Description: Product Differentiators (what is “special” about the proposed product?

×	[m] Conclusion: Recommendation Statement

	EE295 Grammar Checklist
✓	1. No personal pronouns "I, we, our, my, ..etc"
✓	2. Avoid passive voice "The work was done by engineers"-instead "Engineers did the work"
✓	3. No use of "very"
✓	4. Structure--Confirm that the paragraph has a proper structure with a single topic sentence (most likely the first sentence) with body/supporting sentences and a conclusion sentence