PCB REVIEW RUBRIC

Group name: _____ Section: _____ Examiner: _____

This course requires that all teams design, order, populate, and test a printed circuit board (PCB). It is expected that the final demonstration will be conducted using as much of the PCB as possible. If after extensive debugging, hot fixing, etc. your TA may allow you to use a solder- or bread- board circuit in the final demonstration without loss of points on **this** assignment; however, you will have to convincingly explain why the PCB design is no longer a viable option. The course staff reserves the right to exempt the PCB requirements for only certain components.

This assignment is officially completed at the final demonstration; however, the first step has earlier due date. Please consider all manufacturing, shipping, parts sourcing, etc. lead times to ensure that your team fully completes the assignment by the due dates. *This is your responsibility.*

Perform the following steps, in sequence:

1. **[15%, pass/fail] Initial TA review of Schematics [Due Monday March 15, recommended ASAP]**
    a. **complete** layout-ready schematics (in PDF format), and
    b. a **complete** bill-of-materials (BOM)

2. **[35%, pass / fail] Initial TA review of PCB Layout [Due Second Lab Period (March 18/19)]**
   Ask your TA how they would like you to submit your PCB design for review. Each may require a different collection of documents, but at a minimum your team must provide:
    a. **complete** and **final** schematics (in PDF format),
    b. **fully** routed PCB(s) exported as Gerbers,
    c. A 1:1 scale printout of the PCB (in PDF with only top and bottom copper layer),
    d. proof of DRC/ERC checks,
    e. centroid file (only if getting assembly done by manufacturer),
    f. print-out of planned order from fabricator's website (PDF),
    g. a **complete** and **final** bill-of-materials (BOM), and
    h. a printout of this rubric with the answers to the below questions.
    Note that I am answering some of these questions with the knowledge that **I will only have 1 copper layer**. This also resulted in there only being the top copper layer (didn't show the bottom) when I exported my 1:1 printout from KiCAD.

    What manufacturer do you plan to use: JLCPCB
    What is the lead + shipping time: 1-2 days + 2-4 days shipping
    What quantity do you intend to order: 2
    Manufacturer specifications
        Maximum number of layers: 6
        Surface finish: HASL (with lead)
        Copper weight: 1 oz

Minimum solder mask clearance:	.05 mm	
Minimum drill hole size:	0.20 mm	
Minimum trace width:	0.127 mm	
Minimum trace spacing:	0.127 mm	
Minimum via to trace spacing:	0.254 mm	
Blind / Buried vias:		Yes / No
Have you configured your tools DRC based on these specifications:		Yes / No
Does your PCB require a stencil to populate:		Yes / No
If so, do you have a plan to order one:		Yes / No
All components fit on PCB printed 1:1 scale:		Yes / No
Checked for and corrected issues from appendix 1 checklist:		Yes / No
Your team name and number is clearly visible in the silkscreen:		Yes / No

3. **[50%] Assemble, test, and debug PCB (Waivers must be submitted, reviewed, and approved by April 11)**
   Fully populate the team's PCB design. We suggest starting with the power components and then moving to the next sub-system, one at a time. Be sure to test between each population. You may be forced to populate the entire board at once if a stencil is required. Attempt to debug and fix all design issues. Consider techniques such as trace cutting, fly wiring, etc. Consult with the course staff if a solution is not obvious.

   If the PCB design is proven to be unworkable, then start a conversation with your TA, Professor, and other course staff about how best to proceed. We may recommend a second PCB design and/or allow a solder- or bread- board based final demo. Unless an exemption is granted, the final demo is expected to be on a PCB. Use the attached waiver request form to officially request an exemption.

Notes:

Appendix 1: Systematic PCB Verification Approach:

1. Parts Completion Check
    a. Major components
        i. Microcontroller/FPGA/SoC/Microprocessor/CPLD
        ii. Power supply, regulators, battery management
        iii. Sensors
        iv. User interface elements (LCDs, buttons, switches, etc.)
        v. Actuator drivers and control: Motor control, LED driver circuitry, audio filters and amplifiers, Etc.
    b. Support components
        i. Microcontroller manufacturer's guidelines followed?
        ii. All relevant application notes for major components followed?
        iii. Support components have proper package and value? (Power circuit support components designed to handle necessary voltages and currents?)
        iv. All ICs have decoupling capacitors as close to ***every*** power pin on the package?
    c. Other components included?
        i. Programming header?
        ii. Reset circuit?
        iii. Power connector(s)?
        iv. Packaging mounting holes in PCB?
        v. Power on indicator(s)?
        vi. Heartbeat LED?
        vii. Oscillator/clocking circuitry?
        viii. Debugging LEDs or interfaces?
2. Parts Placement Check:
    a. Oscillator close to microcontroller?
    b. Decoupling caps close to/under related ICs?
    c. Connectors on board edges?
    d. Parts grouped by system and/or in reasonable way that minimizes routing?
3. Mechanical/Space Conflict Check:
    a. All x- and y- footprint space around electrical pins and pads are accounted for?
    b. Has z-height of all parts been accounted for?
    c. Has clearance been provided for the bolt heads of all mounting holes?
    d. Have connectors been placed on the outer edges of boards where appropriate? Are they overhanging board edge where appropriate? Are they oriented in the correct direction?
    e. Are all mounting and mechanical support holes free of traces and other items?
4. Routing Completion Check:
    a. All traces routed?
    b. Oscillator traces clear of interfering signals?
    c. Traces of appropriate widths to handle current being passed? (Including power traces)
5. Routing Minimization Check:
    a. Trace lengths have been minimized where possible?

    b. Octagonal (45-degree constrained) layout mode has been utilized, where possible?
    c. Right angles have been removed, except where necessary?
    d. Acute angles have been eliminated from all board routing?
6. Via Minimization Check:
    a. Vias have been eliminated to extent reasonable?
    b. Planes on opposite sides of boards are connected by vias at reasonable intervals?
7. Plane Check:
    a. Planes have been included, where reasonable?
    b. Analog ground (AGND), has been separated from the main ground net?
    c. Isolation on all planes has been set to at least 12 mils?
8. Silkscreen check
    a. Silkscreen labels have been provided for all components and connectors?
    b. Silkscreen labels have been appropriately placed near components, but not on top of pads or pins?
    c. Pin 1 of all ICs and other polarity-sensitive components (such as diodes) are clearly marked?
    d. Board silkscreen layer includes course and team name?
    e. Board silkscreen layer includes names of all team members, if possible?
    f. Board silkscreen layer includes a descriptive name to identify the board?
    g. Board silkscreen layer includes a revision number and/or last modified date?
9. Gerber Check
    a. Gerber files have been inspected by a gerber viewer program (e.g. gerbv) to check for any last-minute software CAM-processing defects.

Appendix 2: PCB Waiver Request

Team name: _____ TA: _____

Portion of project that will not be demonstrated on a PCB:

Explanation of the PCB design fault:

What steps were taken in attempt to overcome the design fault:

How will you demonstrate the affected portion?

TA Approval/Comments:

Professor Approval/Comments: