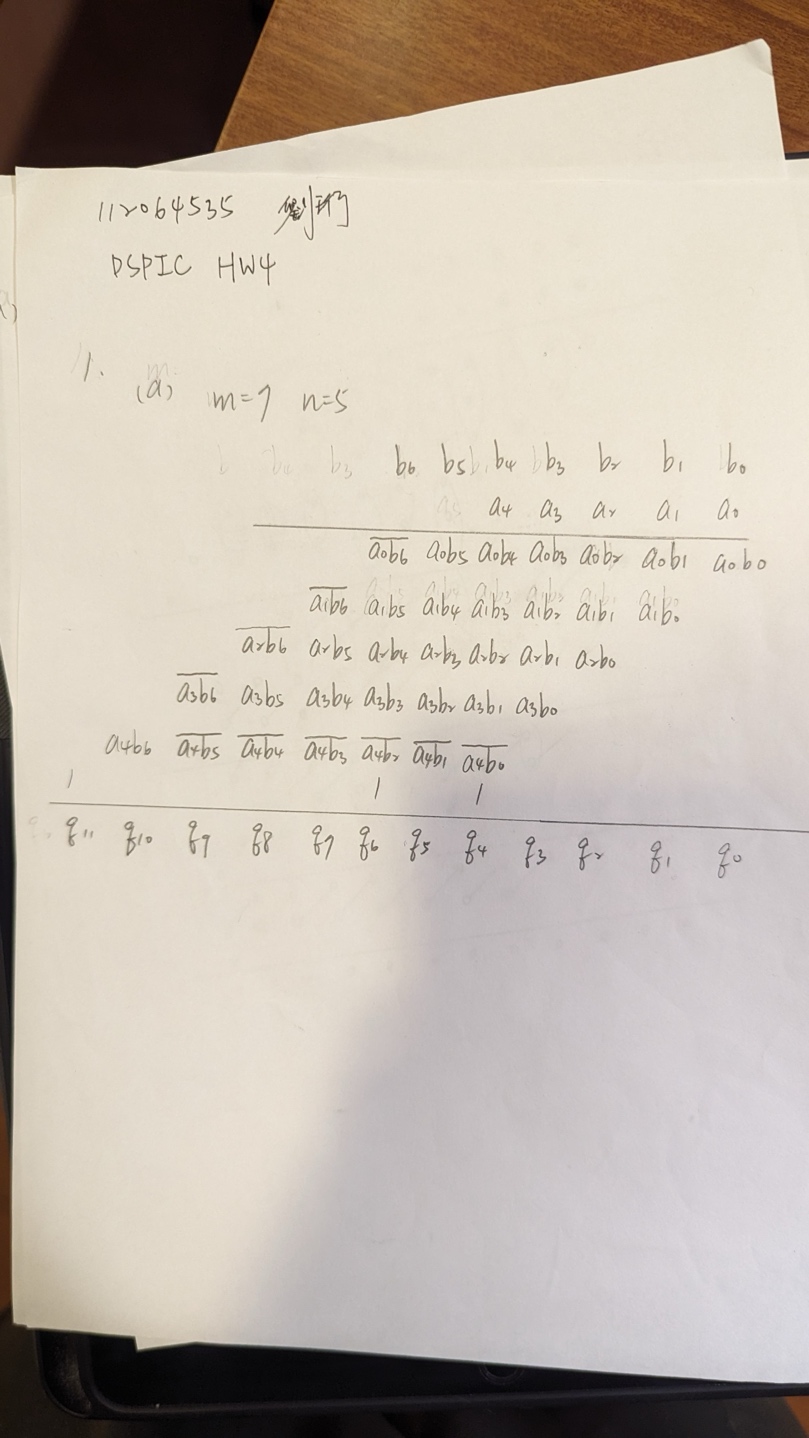
**DSPIC HW4**

**學號：112064535**

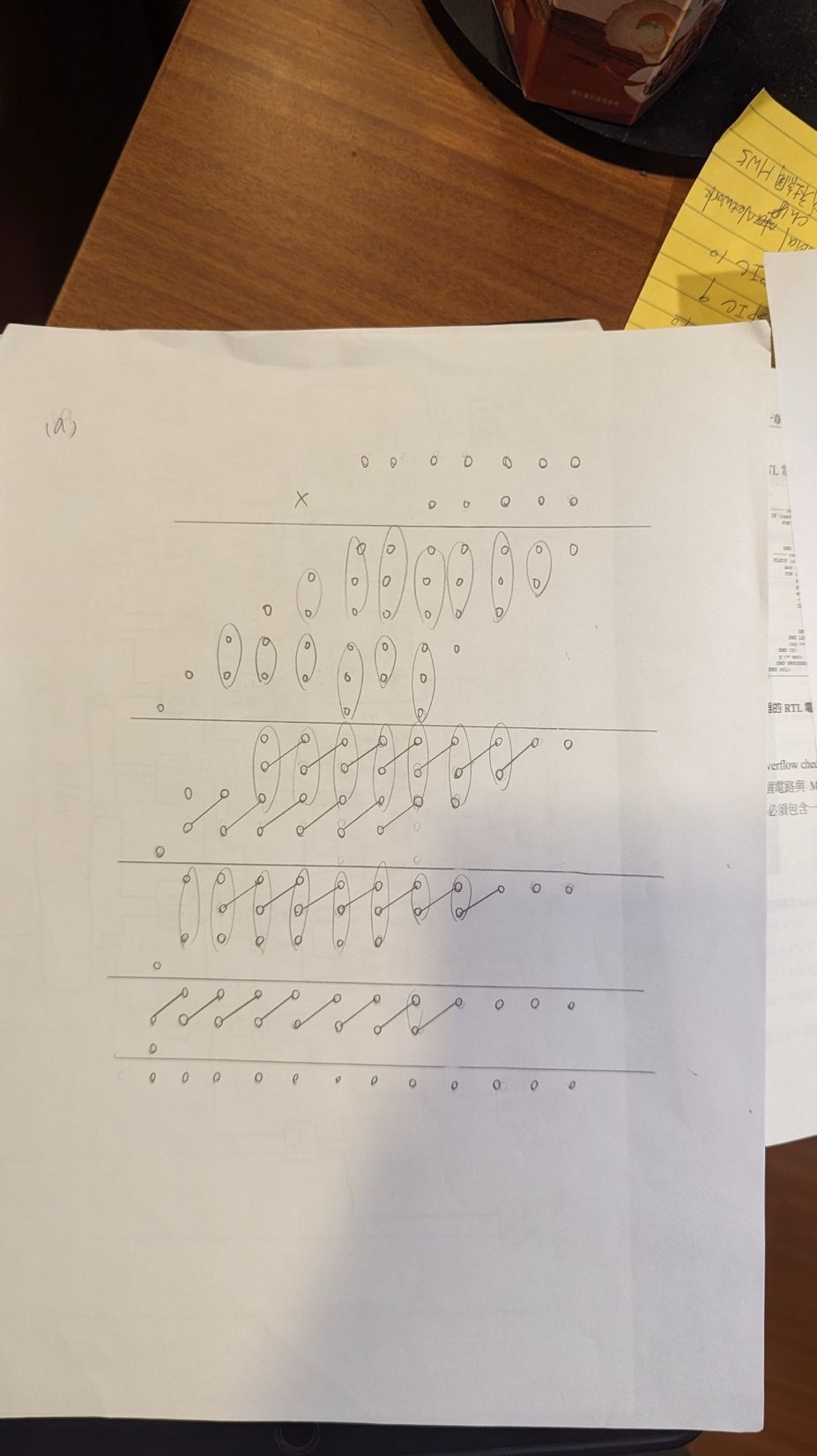
**姓名：劉珩**

1.

(a)

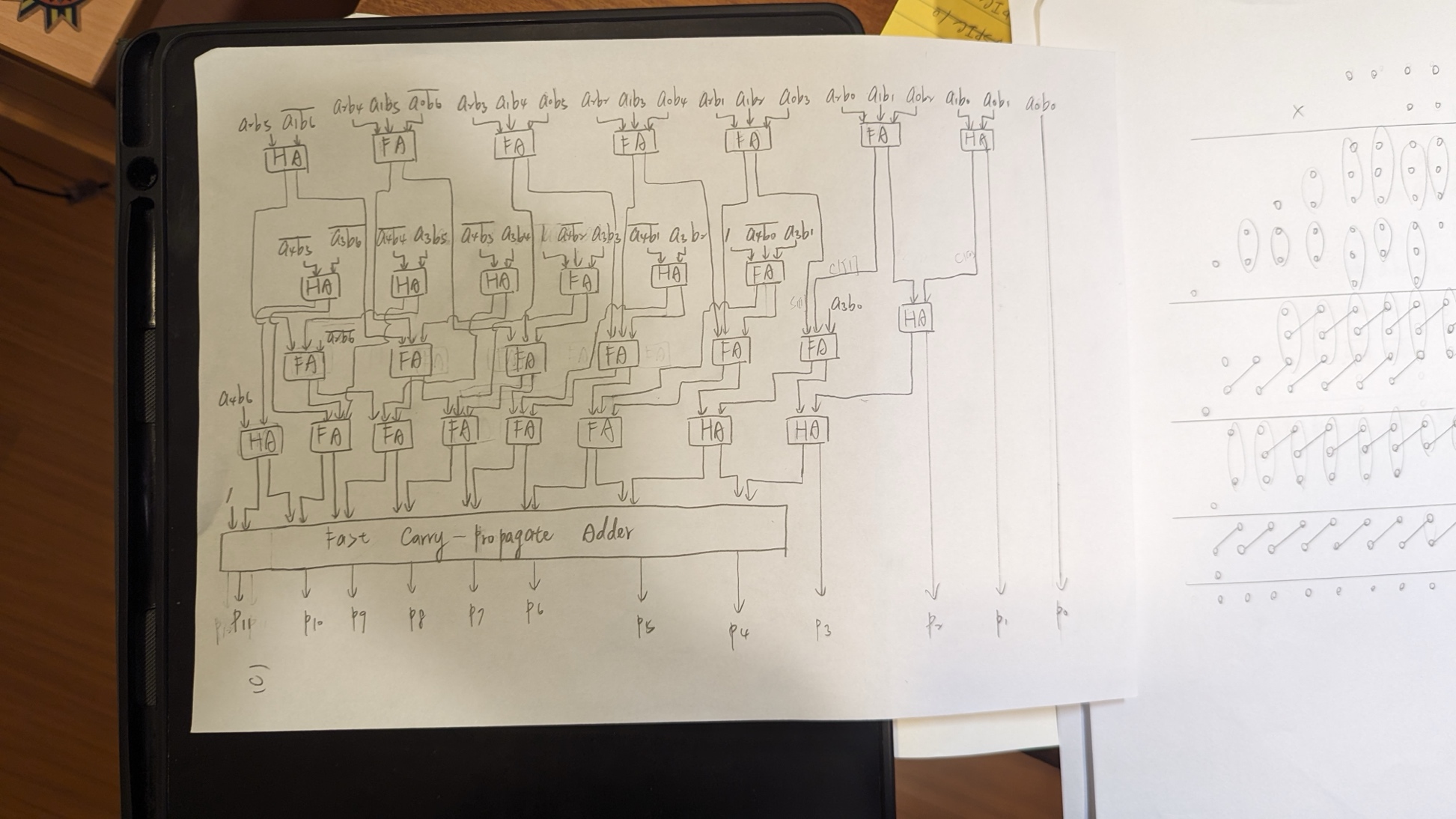


(圖一) 7✕5 乘法器運算流程



(圖二) 運作流程(包含18個FA及11個HA)

(b)

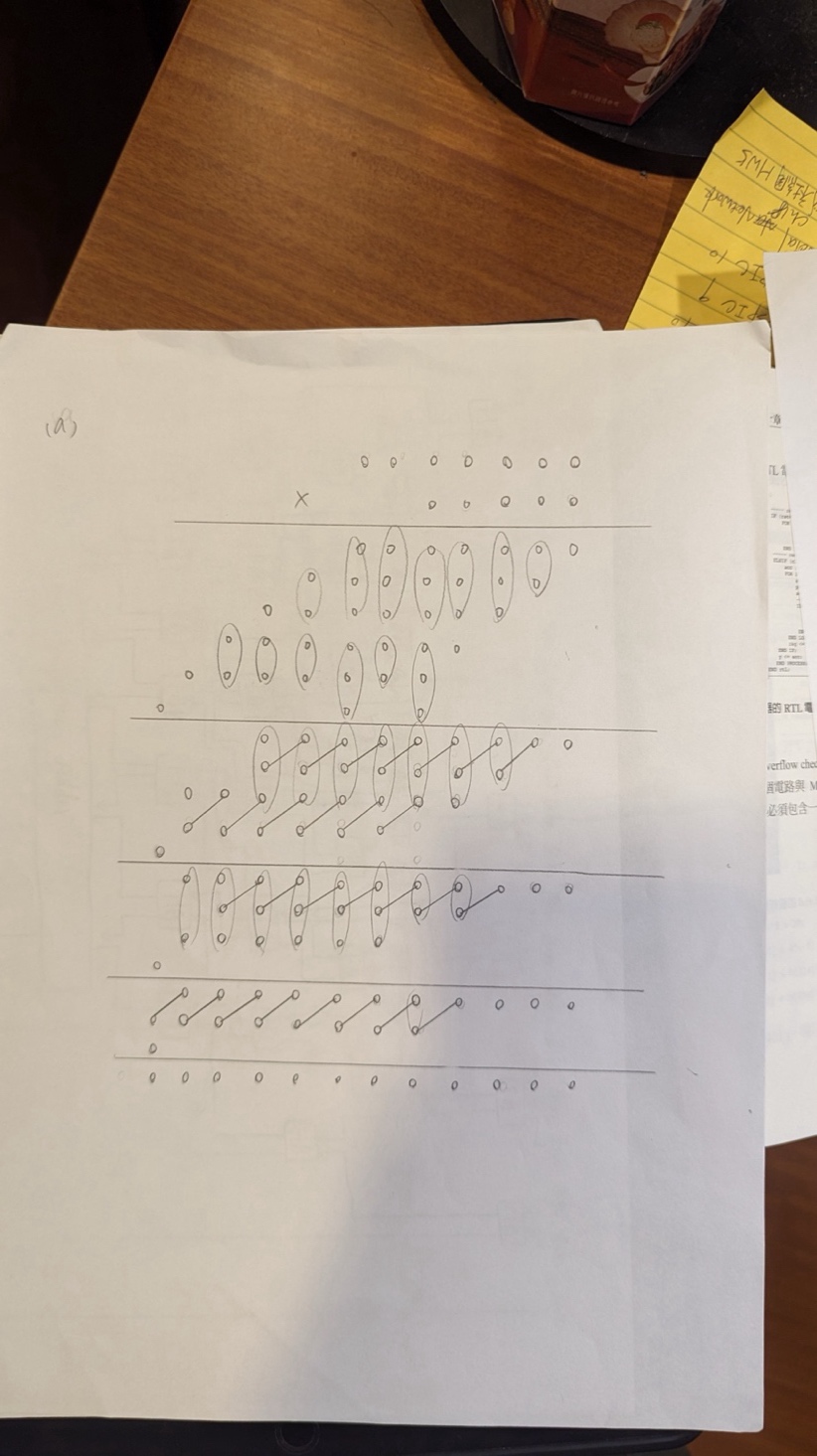


(圖三) Wallance-Tree結構

(c)

Verilog code:

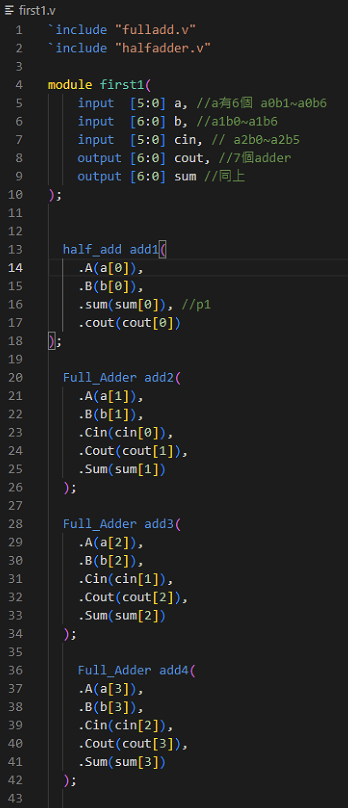
1. 把加法器分成四層，第一層有兩個部分:

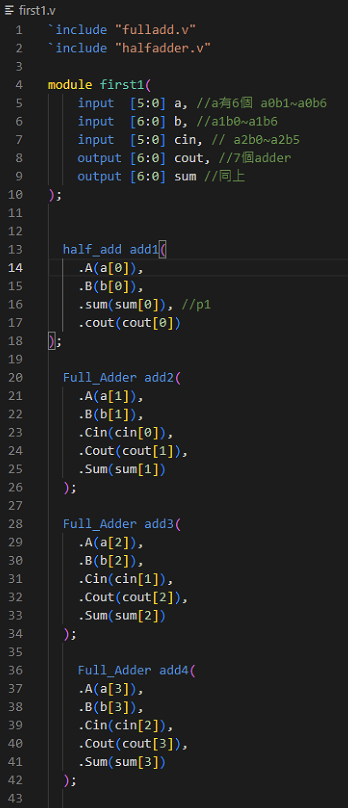


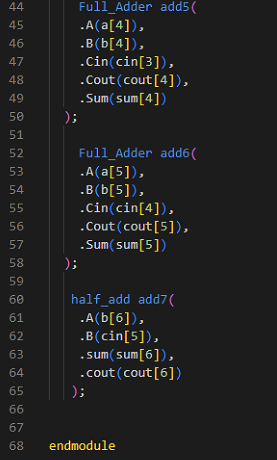
first1

first2

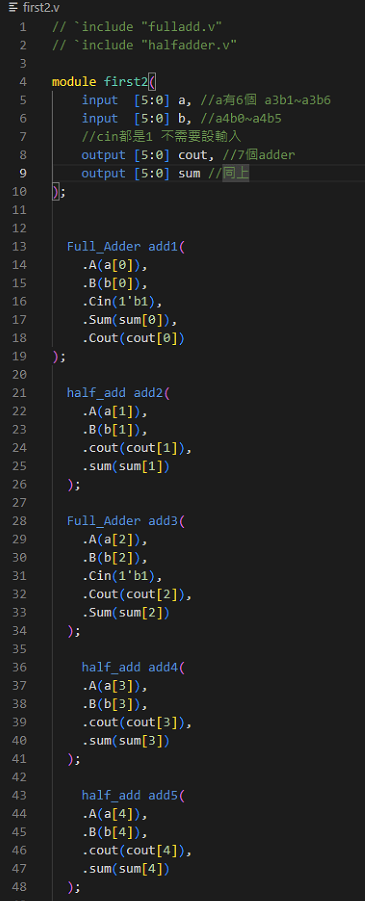
first1.v:

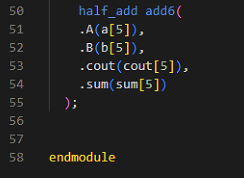




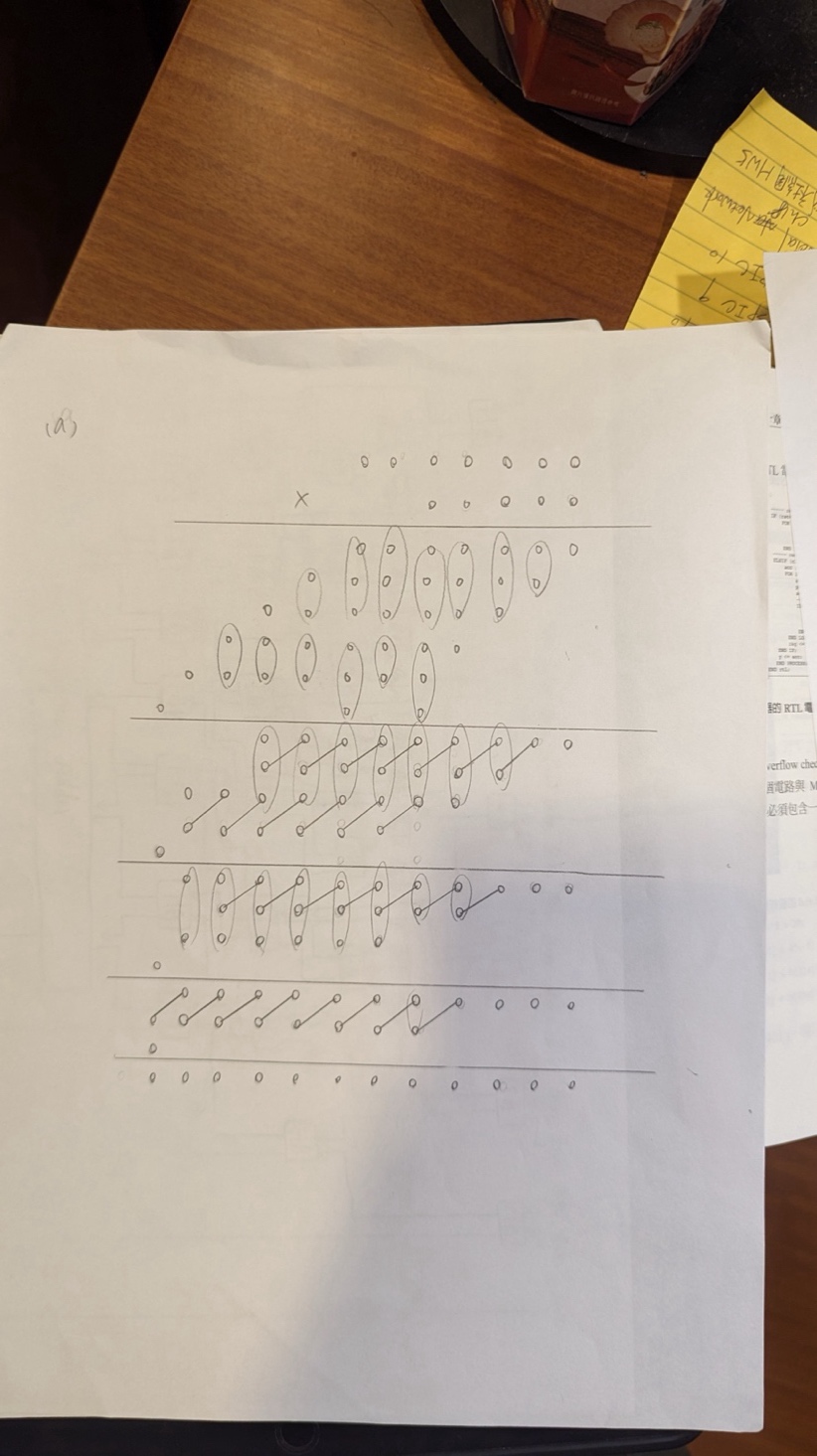


first2.v:



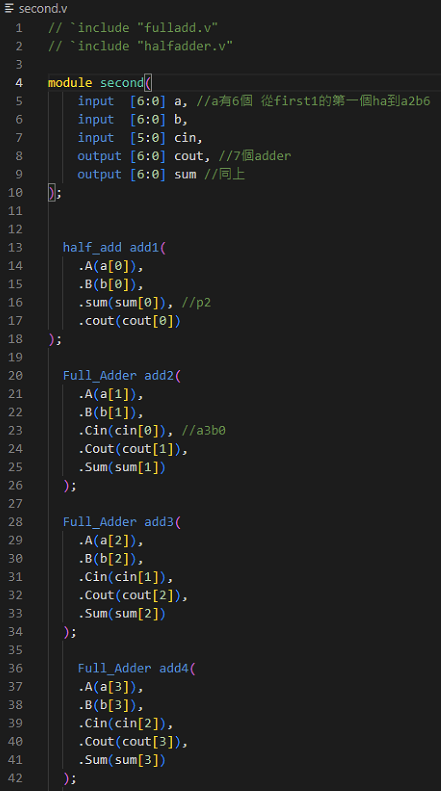


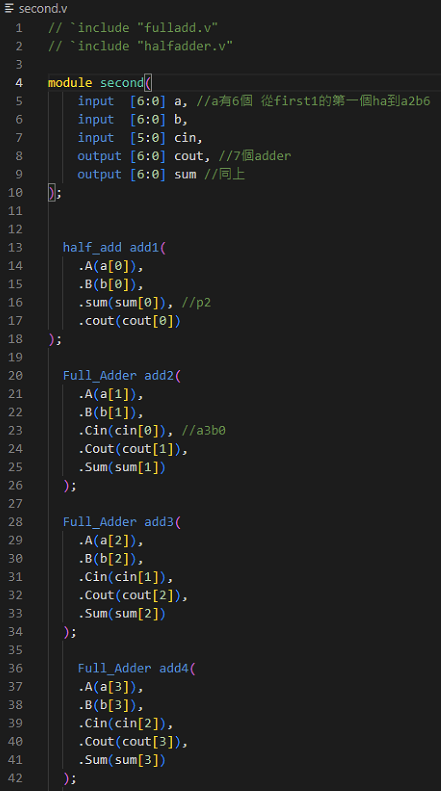
1. 第二層:

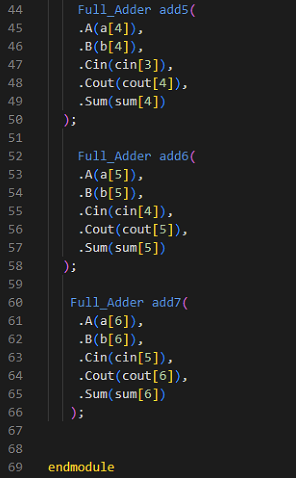


second

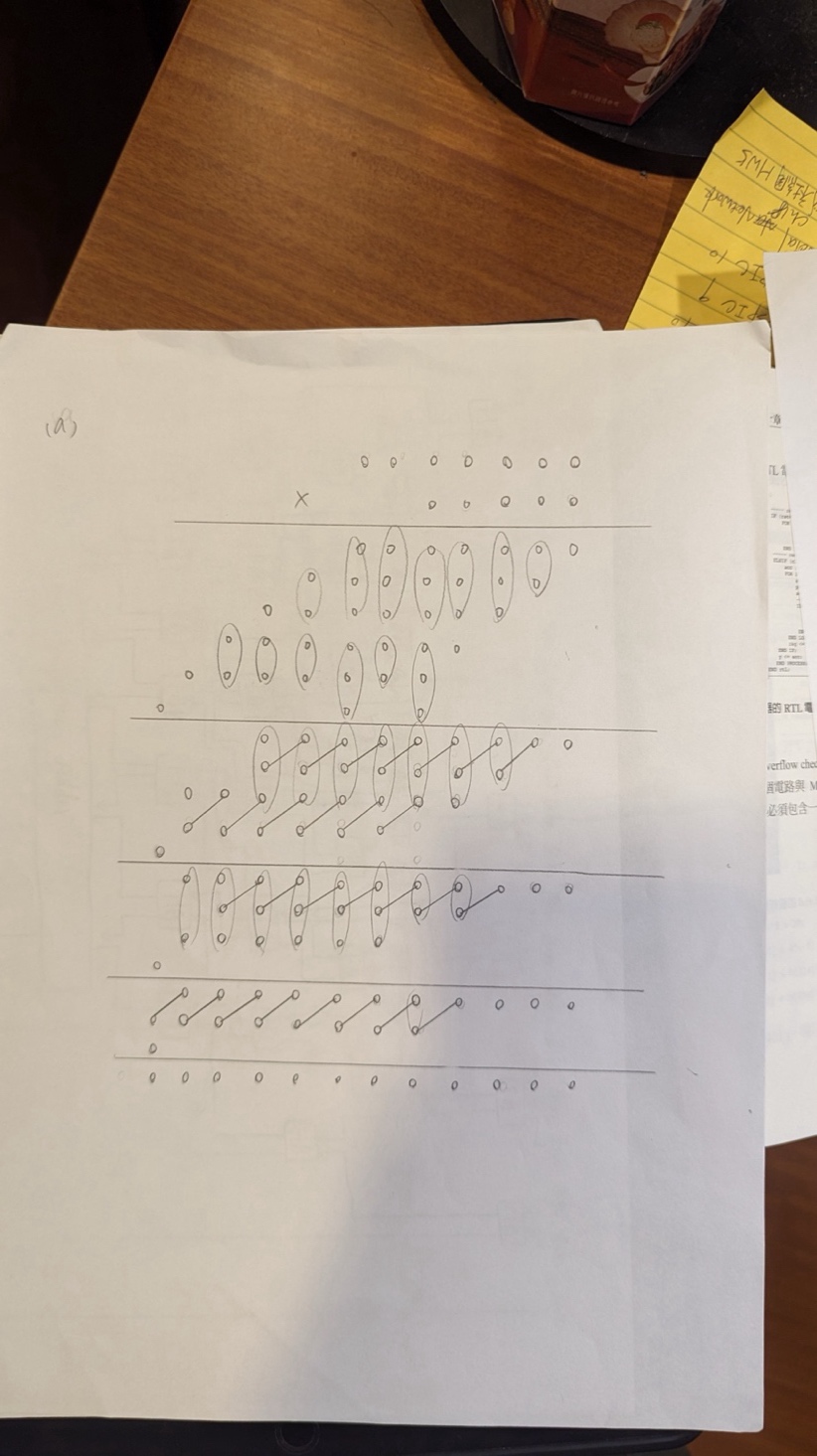
second.v:





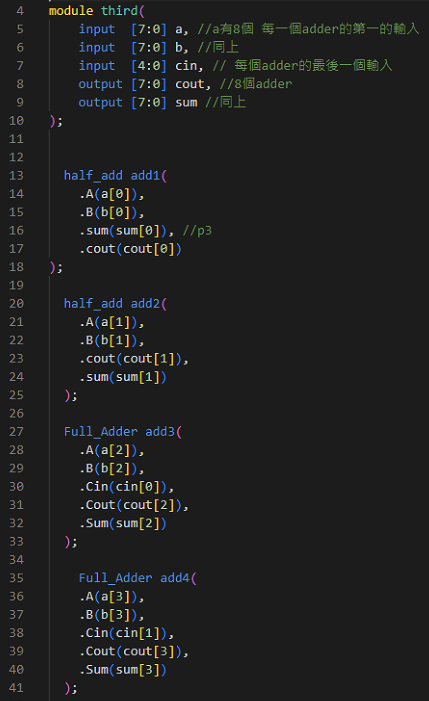


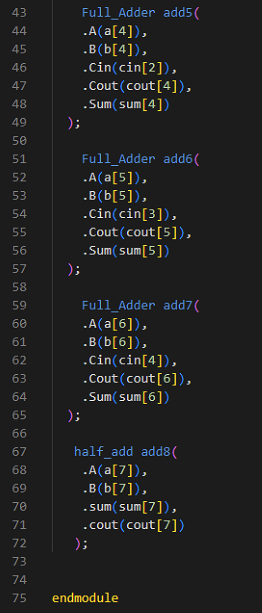
1. 第三層:



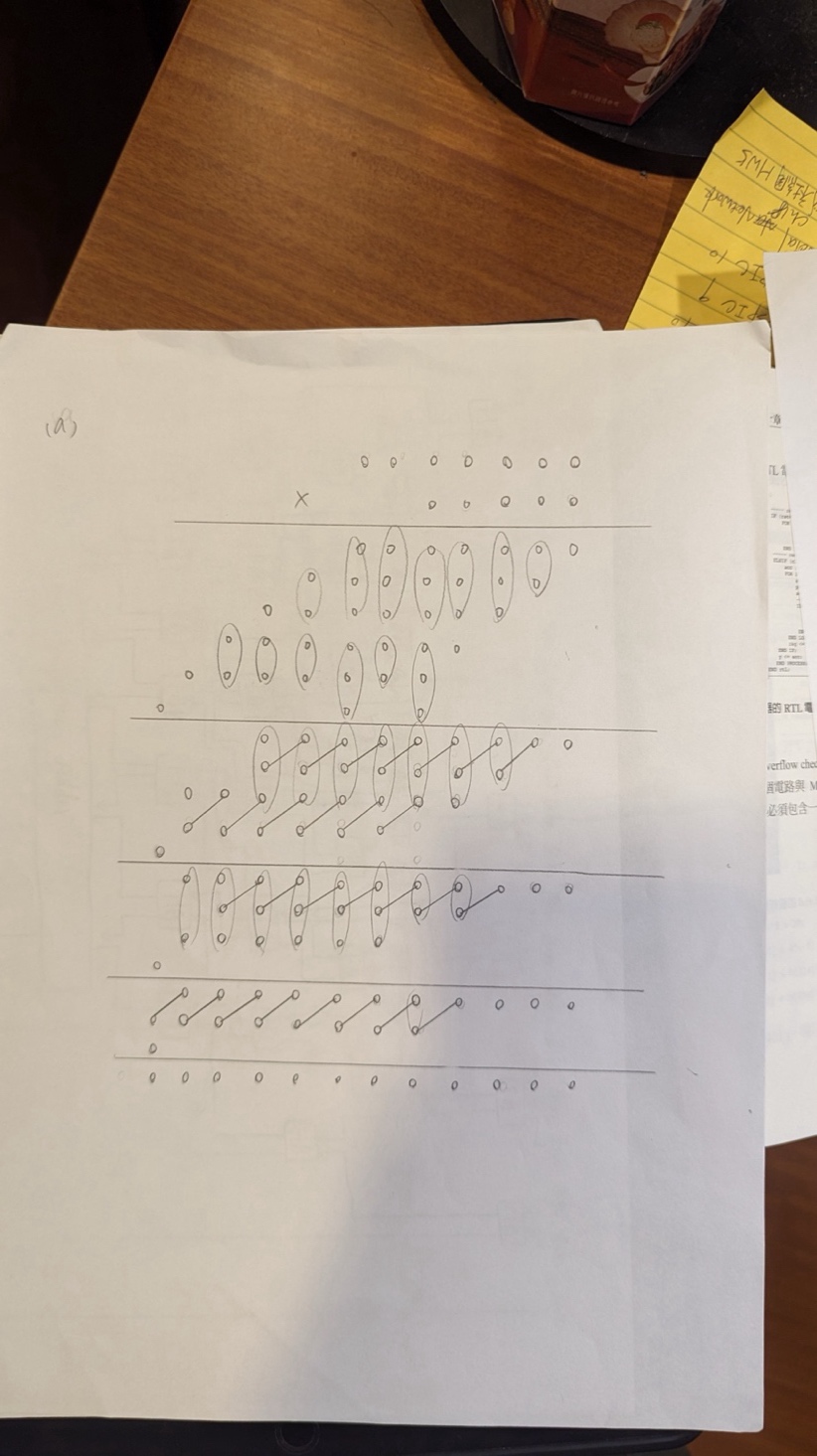
third

third.v:



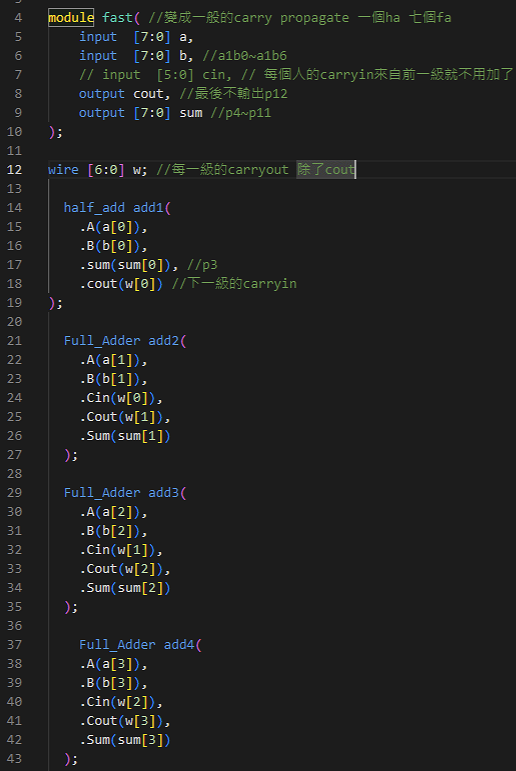


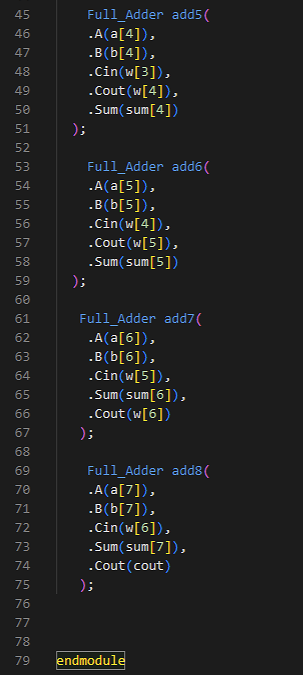
1. 第四層:



fast carry propagation

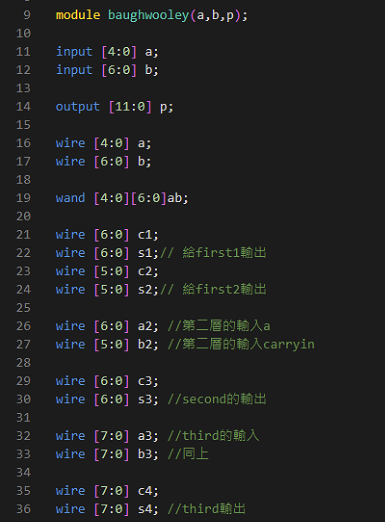
fast\_carry\_prop.v:



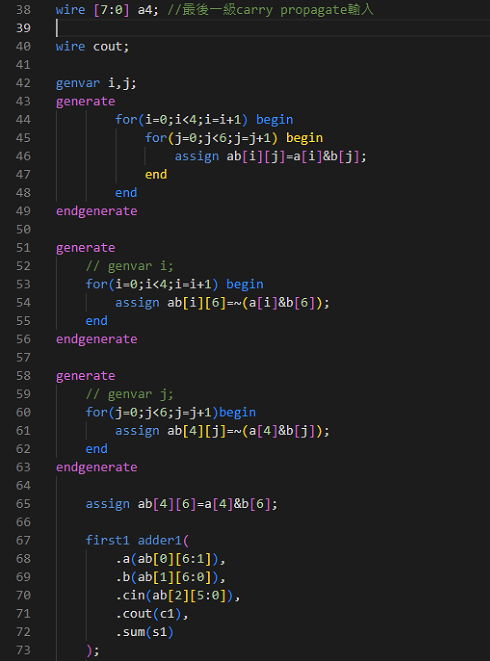


1. 在top module裡將所有input a跟b乘好再運算:

baugh\_wooley.v:

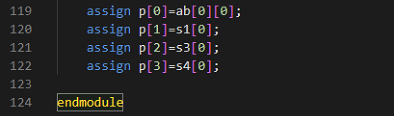


(圖四) 定義輸入及輸出



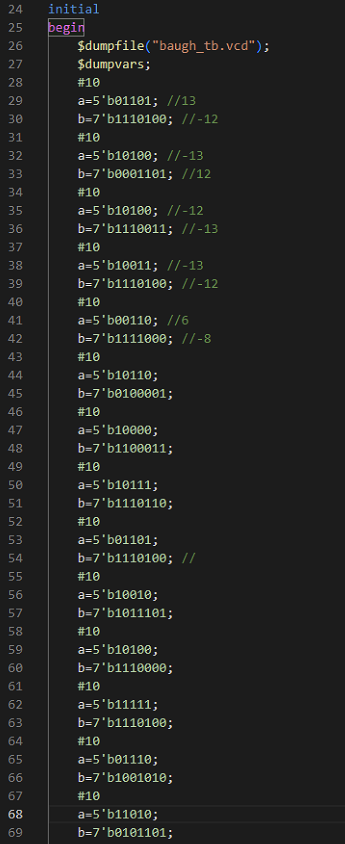
(圖五) 配置所有的ab對

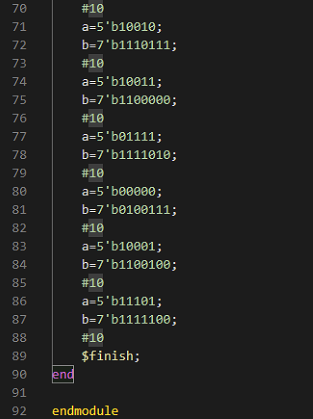


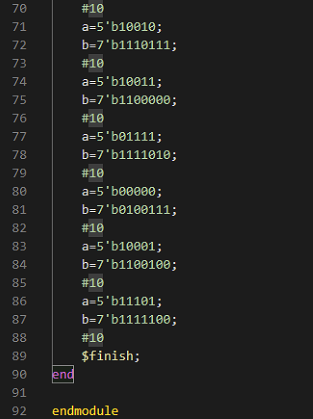


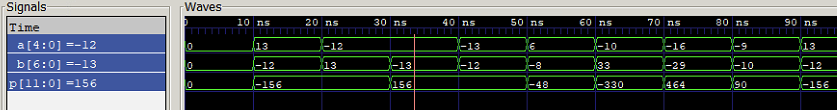
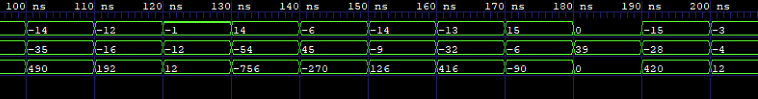
(圖六)(圖七) 運算後決定輸出

1. test bench輸入及輸出結果:









2.

(a)

(i)利用matlab產生21個tap的filter coefficient，以符合規定的filter constrains，coefficient為:

-0.0105963997986059

-0.0380214361435444

-0.0365217681824527

0.00336388262116807

0.0454851577619937

0.0194242970434525

-0.0610882554173864

-0.0752620124582160

0.0734976427892512

0.307268070442418

0.421992848704956

0.307268070442418

0.0734976427892512

-0.0752620124582160

-0.0610882554173864

0.0194242970434525

0.0454851577619937

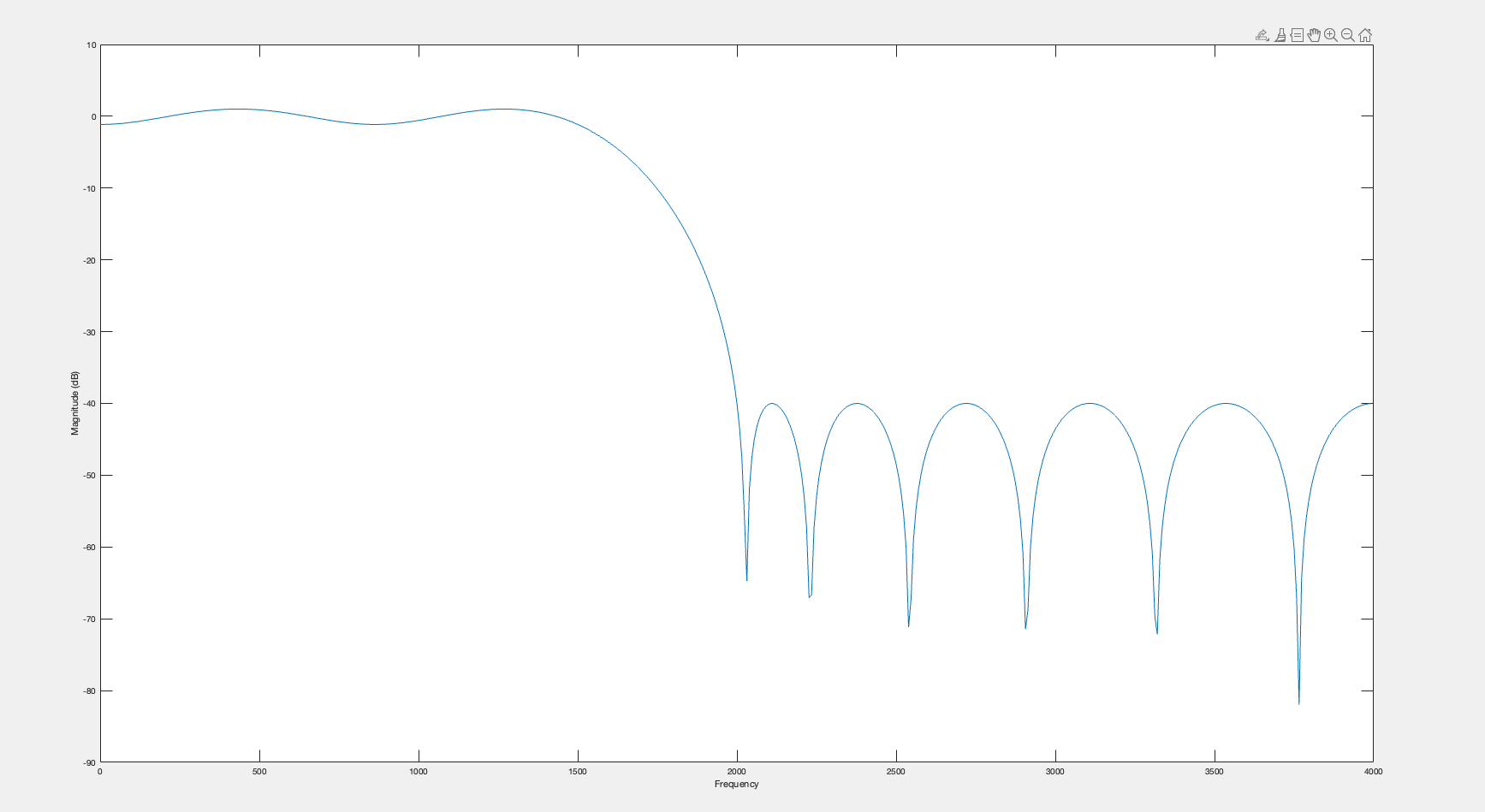
0.00336388262116807

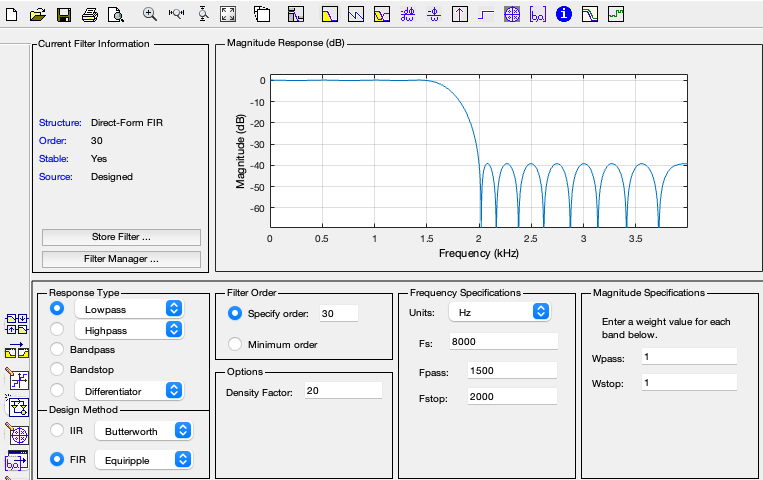
-0.0365217681824527

-0.0380214361435444

-0.0105963997986059

(ii)21 tap的FIR low pass filter頻率響應為:





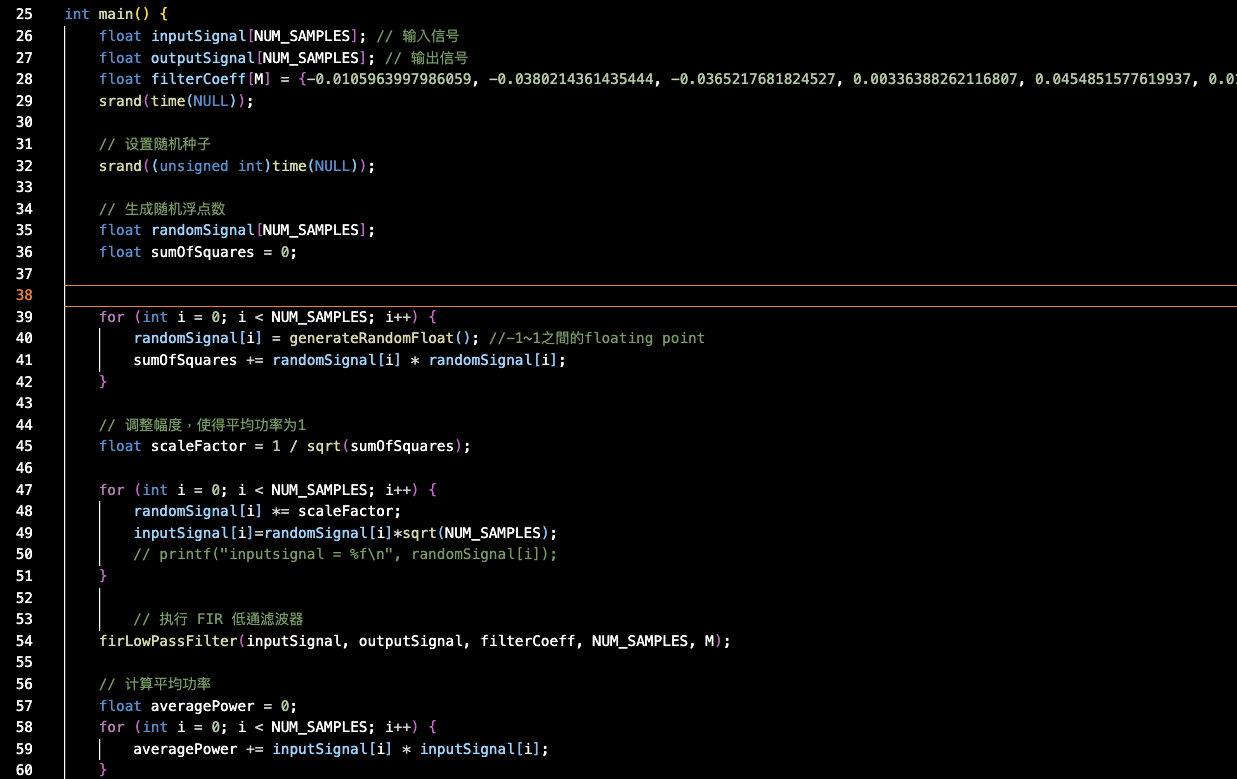
可以看到tap數更高的filter在transition band上更加sharp

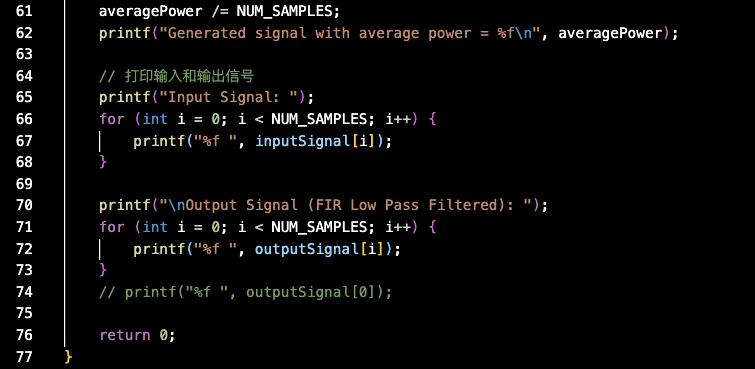
(b)

(i) c program:

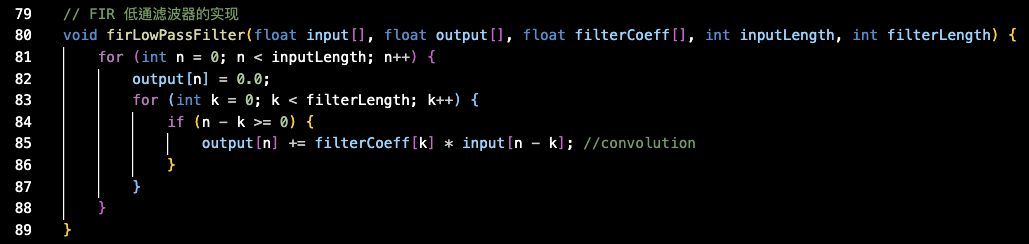


(圖八)生成亂數之副函式

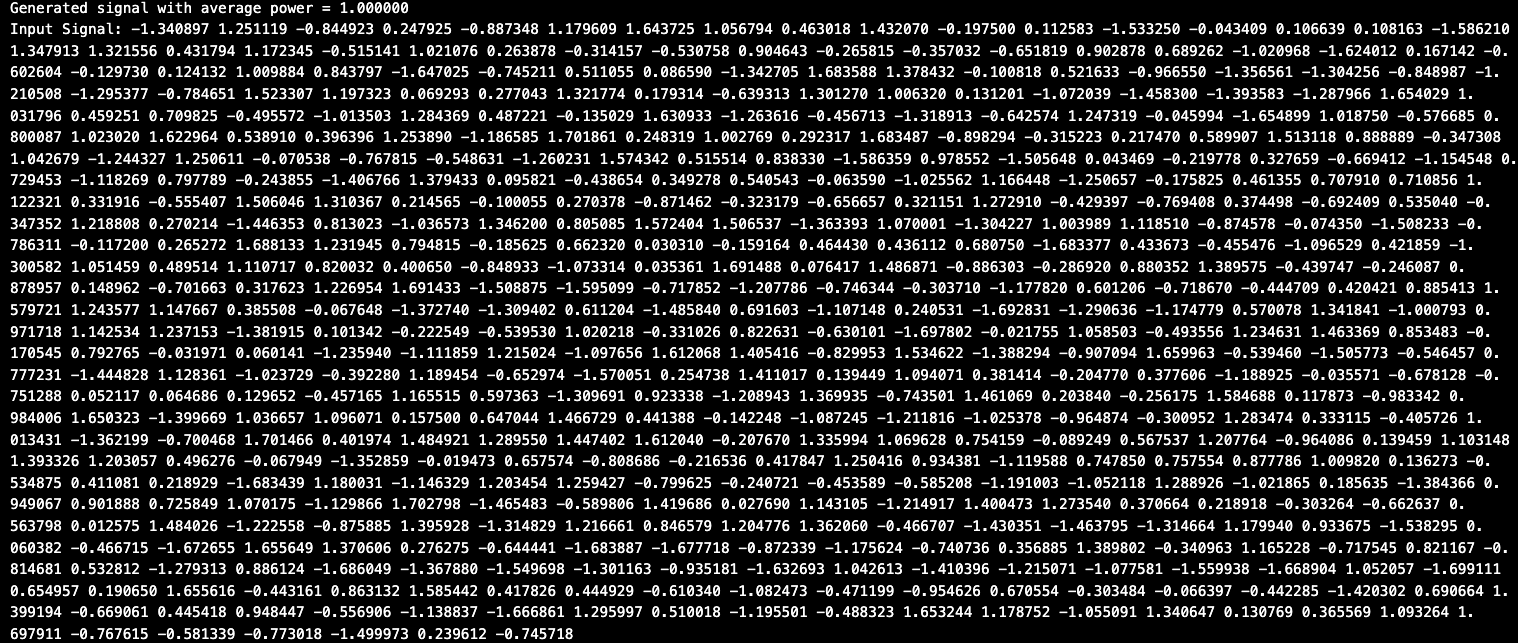


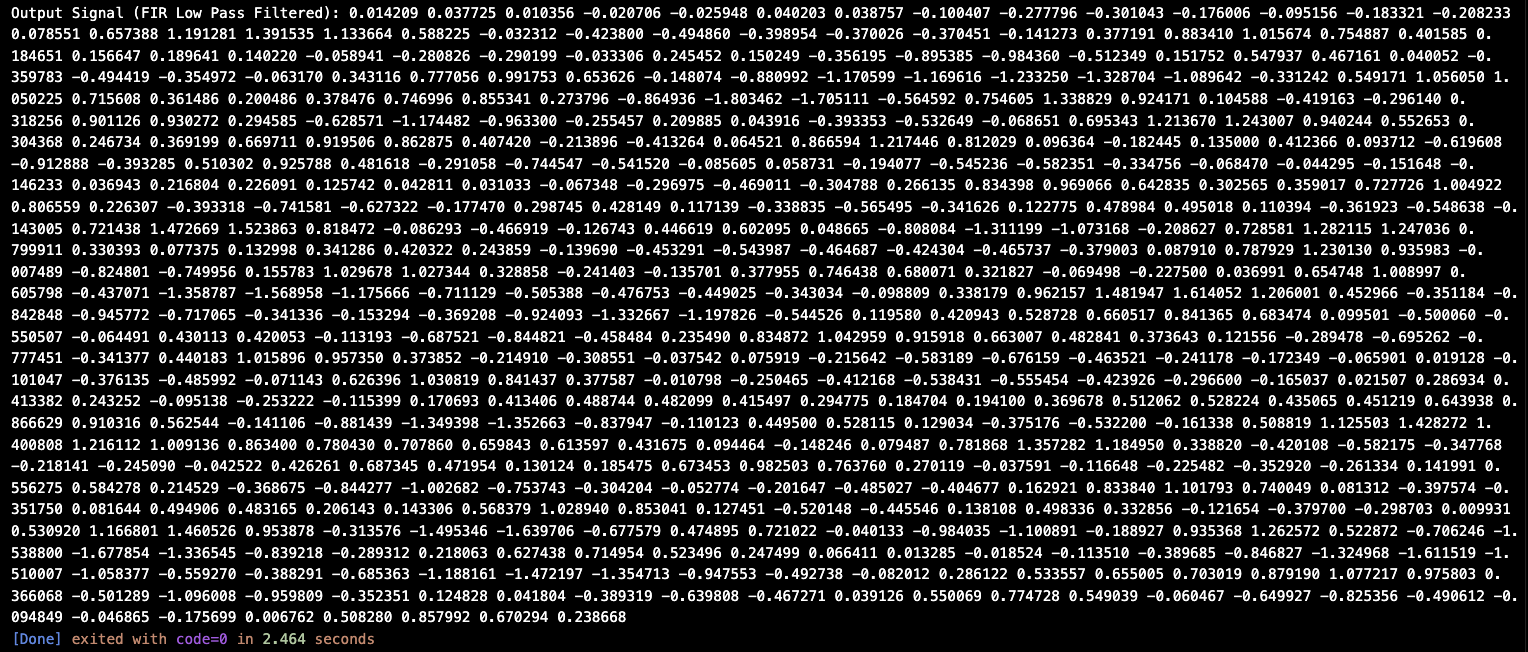


(圖九)(圖十)將隨機生成的512筆資料scaling成power為1的input

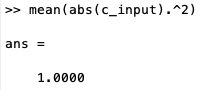


(圖十一)convolution

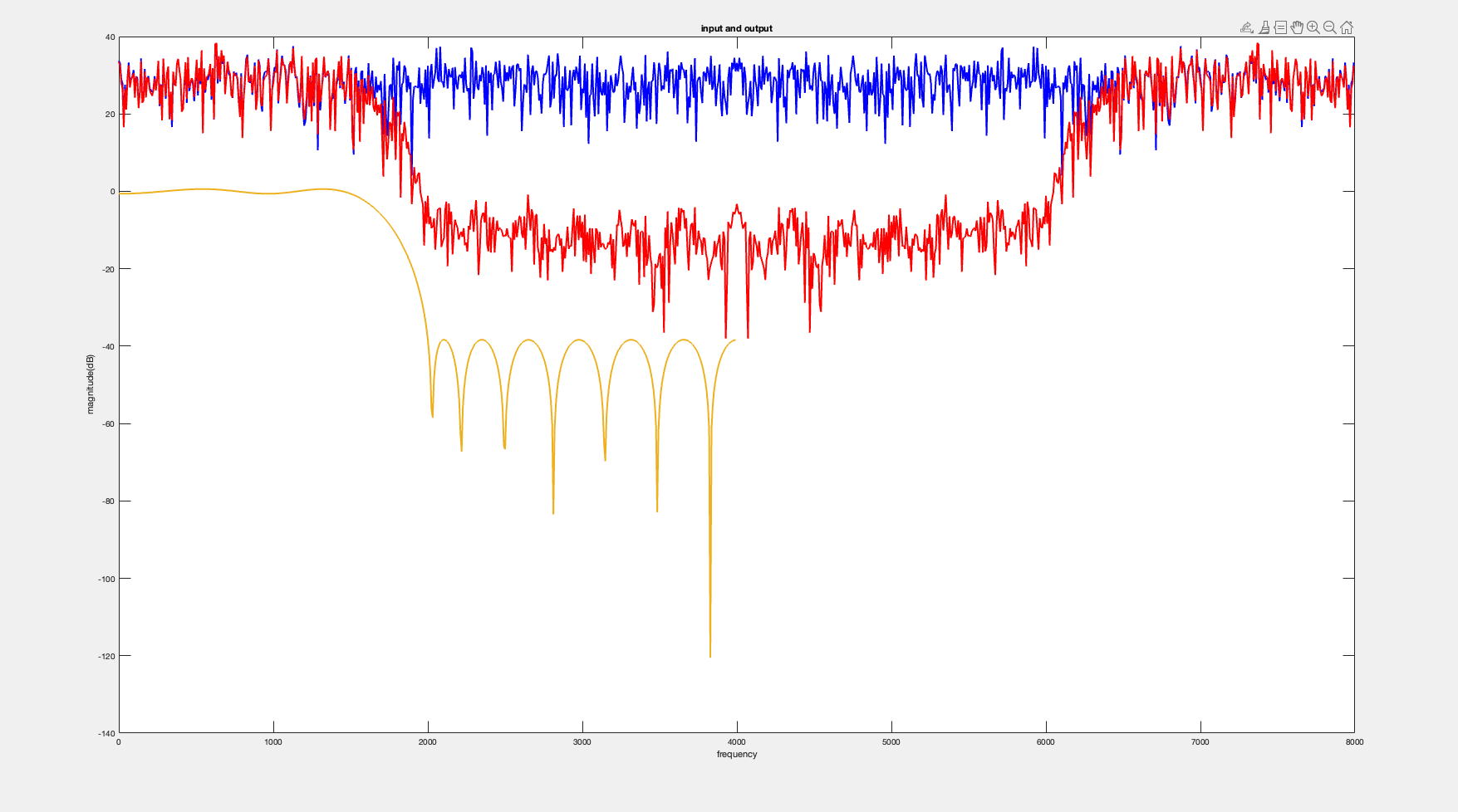




(圖十二)輸出結果



在matlab中驗證c產生的input average power為1



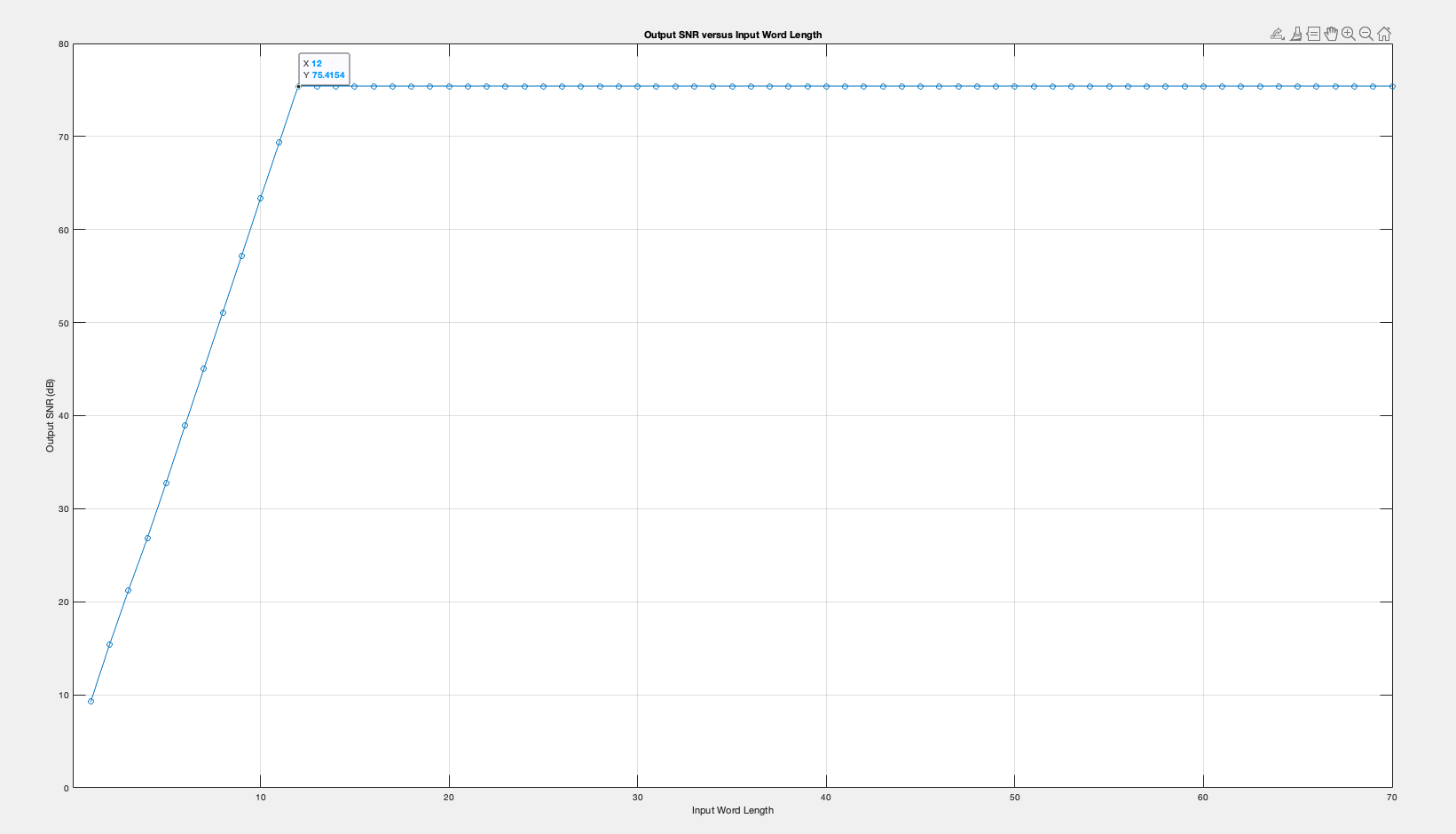
(圖十三)輸入與輸出頻譜對比

(ii)

1. 先將input word-length quantize為fix point，整數為4bits，小數為12bits，共16bits ，再把fix point input跟floating point input比較:

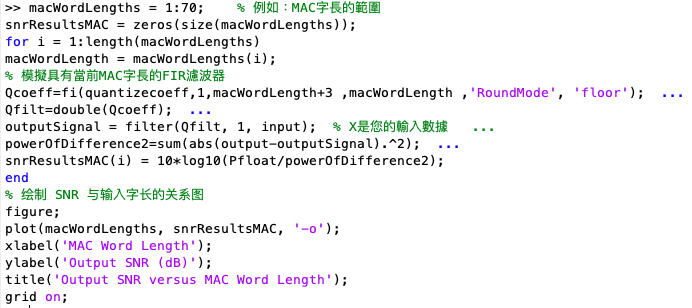


小數點位數

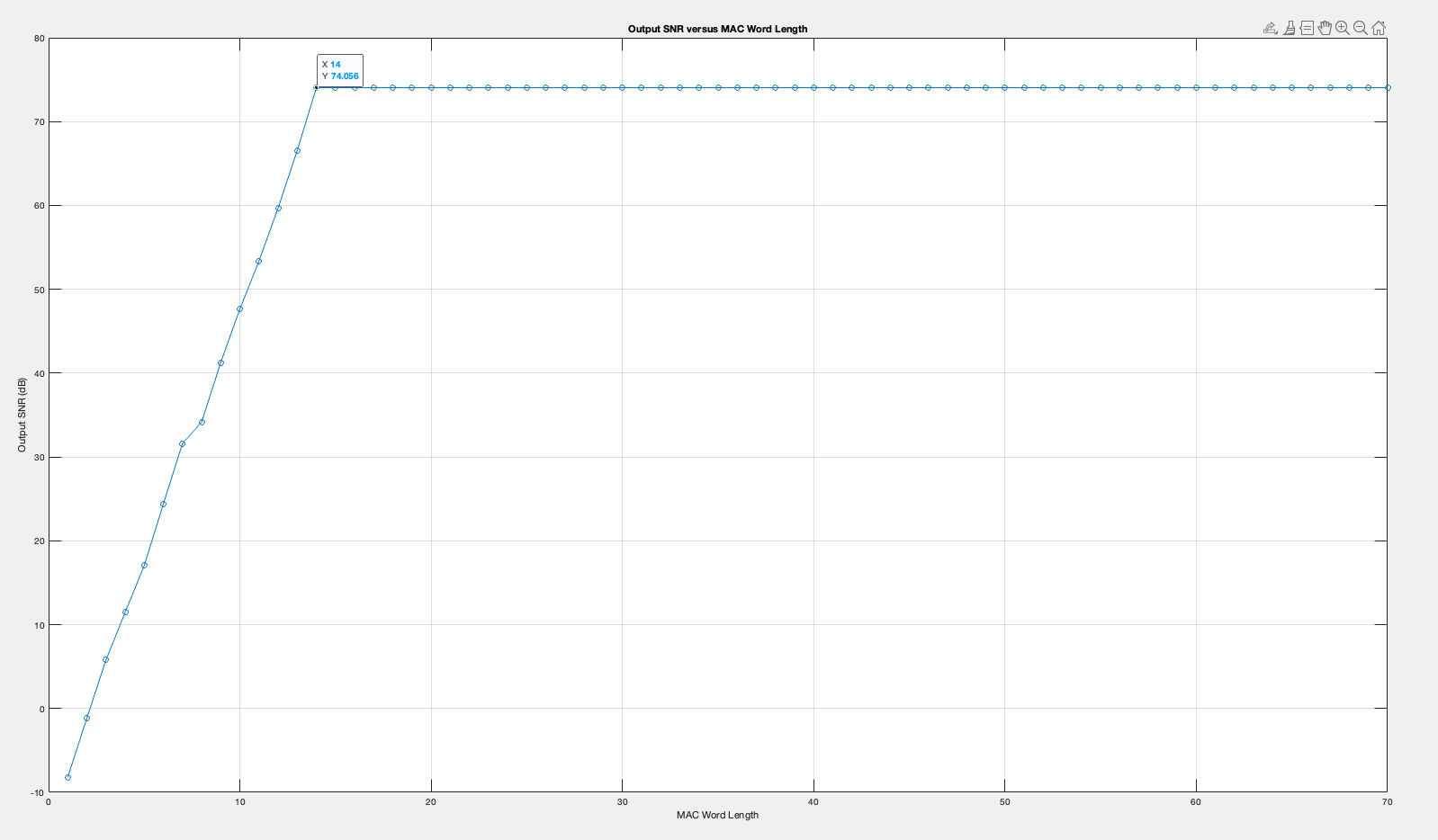


發現在小數點為12bits時開始saturate，因此決定fix point word-length為16bits，小數為12bits

1. 將filter coefficient quantize為16bits word-length的fix point，小數位為14bits，跟floating point 的filter coefficient比較:



小數點位數



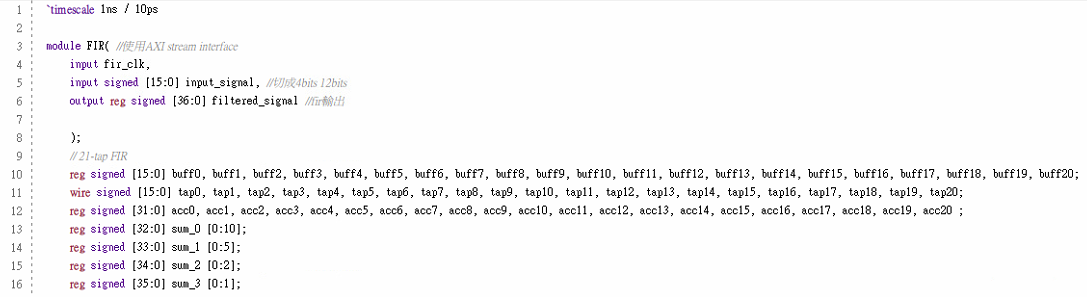
發現在小數點為14bits時開始saturate，因此決定MAC word-length為16bits，小數為14bits

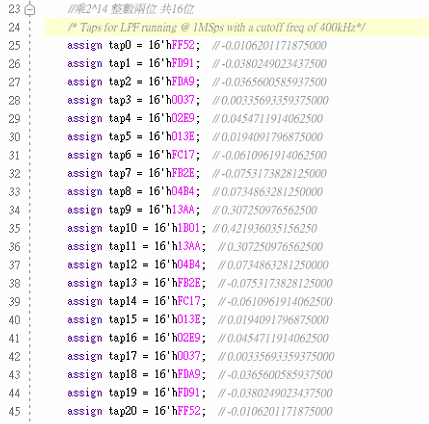
(c)

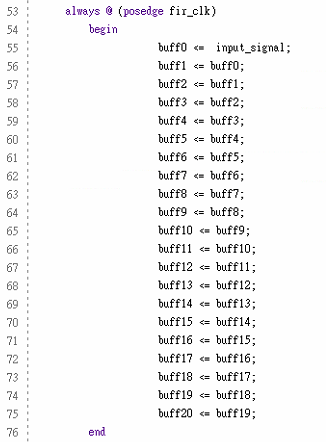
(i)Verilog code:

1. fir.sv:

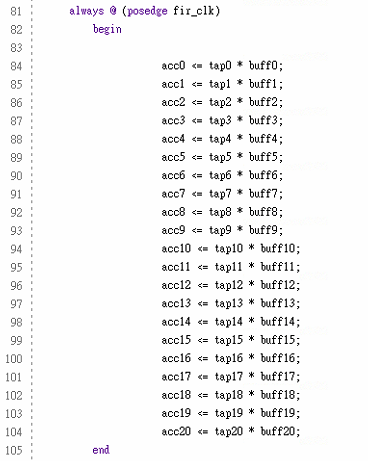
先將每個coefficient存在reg tap裡，coefficient的形式根據上一題的結果，先將所有小數換成整數，例如：0.307250976562500換成十進制(包含sign bit)是00.01001110101010，將小數點去掉後十六進制為13AA。每個tap相乘完的結果兩兩相加，最後到output總共有37bits，其中小數位為26 bits(input 12bits+coefficient 14bits)，再將輸出結果設為26bits小數。

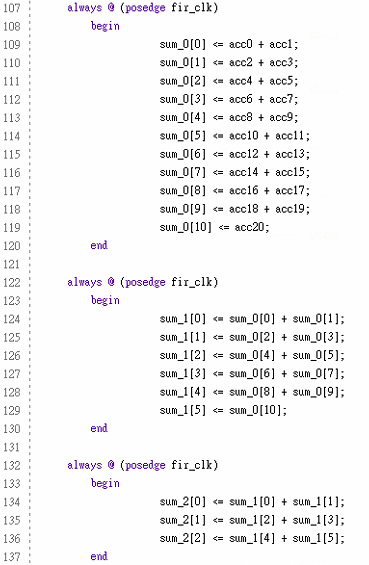




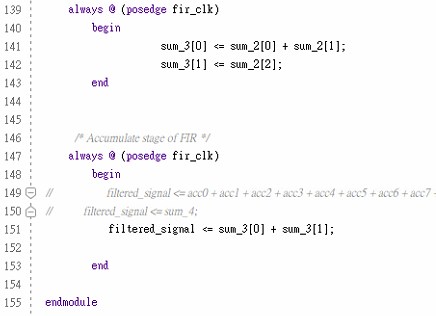


每一級tap的delay





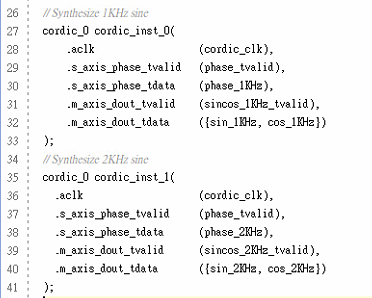
tap的輸出兩兩相加

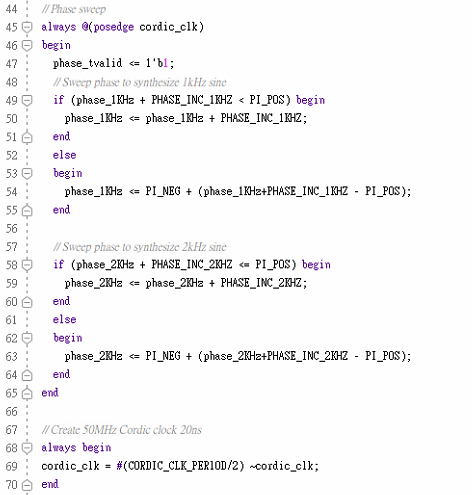


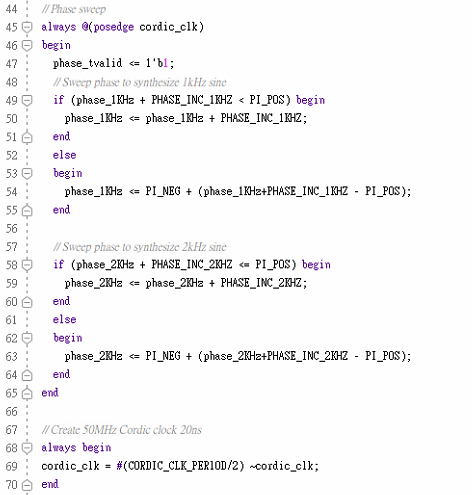
1. fir\_tb.v:

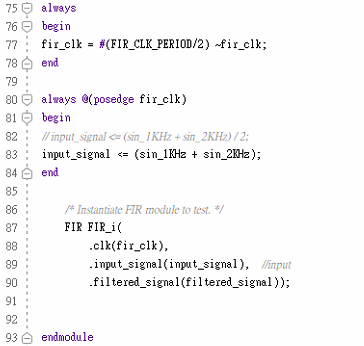
在這裡使用cordic IP產生兩個分別為1kHz及2kHz的sine wave，cordic clock為50MHz，取樣頻率8kHz，input用兩個sine wave相加表示，sine wave為15 bits，因此input最多可以用16 bits表示。



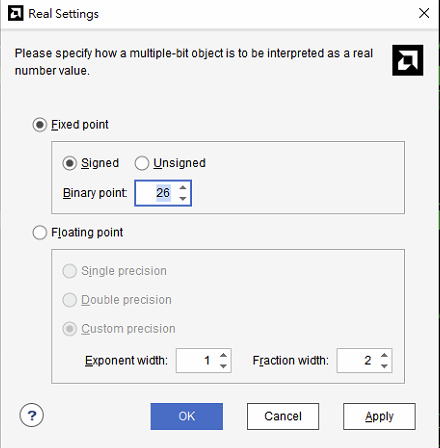


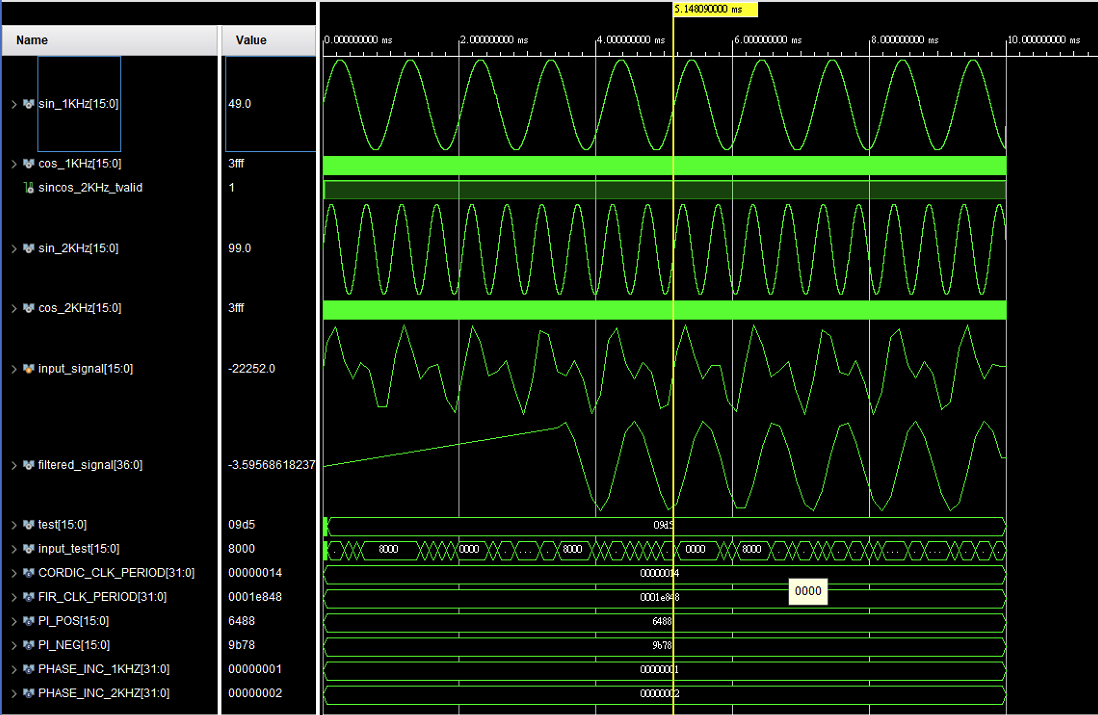
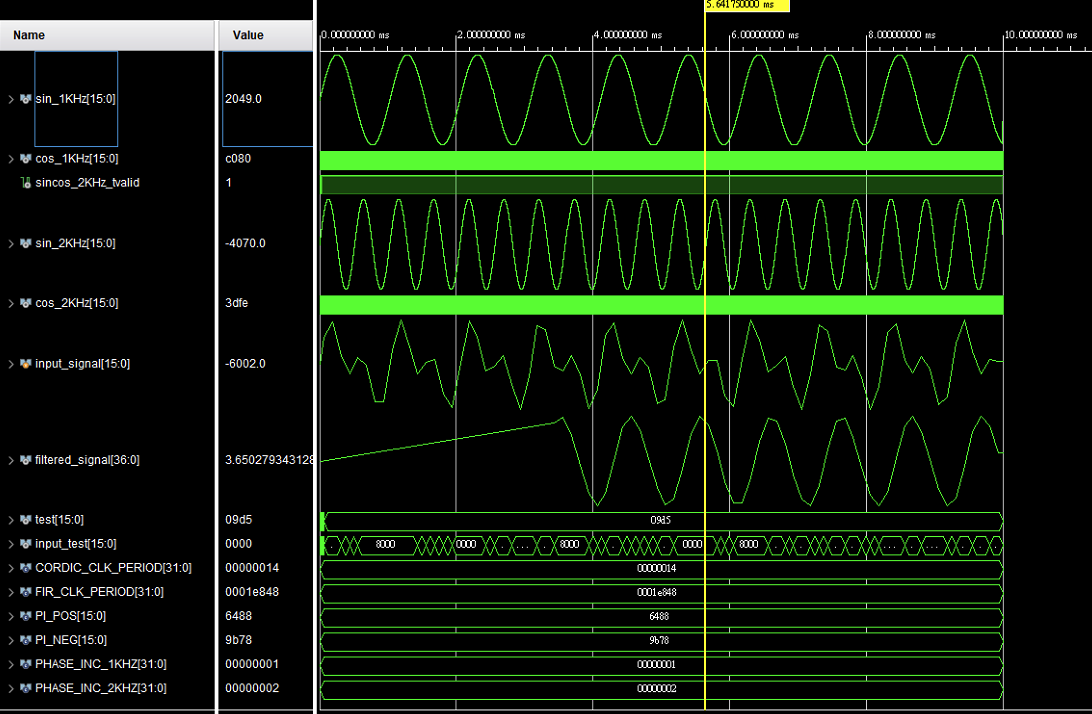






1. output waveform:





(ii)circuit speed and resource number:



