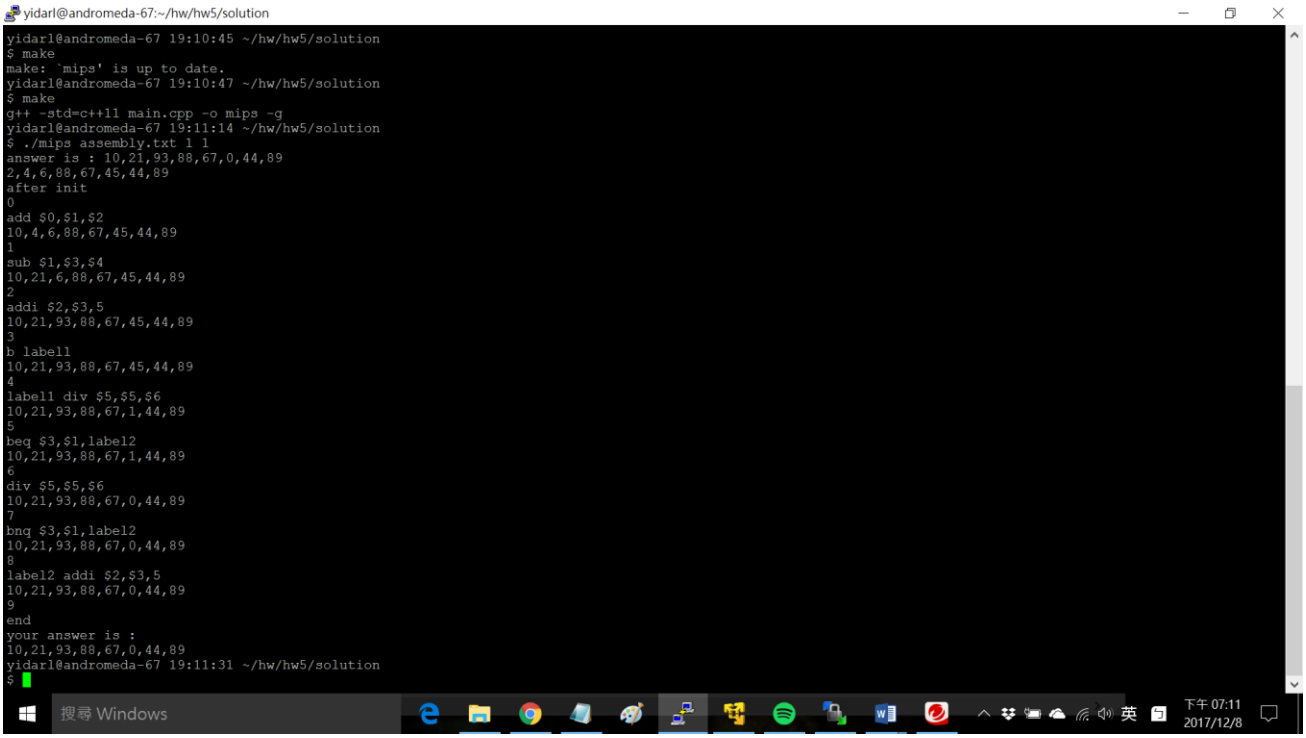
hw5-report

screenshot of output of compiling and running the program:

Part 1: MIPS simulator without Pipelining

assembly.txt

```
answer is : 10,21,93,88,67,0,44,89
2,4,6,88,67,45,44,89
after init
0
add $0,$1,$2
10,4,6,88,67,45,44,89
1
sub $1,$3,$4
10,21,6,88,67,45,44,89
2
addi $2,$3,5
10,21,93,88,67,45,44,89
3
b label1
10,21,93,88,67,45,44,89
4
label1 div $5,$5,$6
10,21,93,88,67,1,44,89
5
beq $3,$1,label2
10,21,93,88,67,1,44,89
6
div $5,$5,$6
10,21,93,88,67,0,44,89
7
bnq $3,$1,label2
10,21,93,88,67,0,44,89
8
label2 addi $2,$3,5
10,21,93,88,67,0,44,89
9
end
your answer is :
10,21,93,88,67,0,44,89
```


yidarl@andromeda-67:~/hw/hw5/solution
yidarl@andromeda-67 19:10:45 ~/hw/hw5/solution
$ make
make: `mips' is up to date.
yidarl@andromeda-67 19:10:47 ~/hw/hw5/solution
$ make
g++ -std=c++11 main.cpp -o mips -g
yidarl@andromeda-67 19:11:14 ~/hw/hw5/solution
$ ./mips assembly.txt 1 1
answer is : 10,21,93,88,67,0,44,89
2,4,6,88,67,45,44,89
after init
0
add $0,$1,$2
10,4,6,88,67,45,44,89
1
sub $1,$3,$4
10,21,6,88,67,45,44,89
2
addi $2,$3,5
10,21,93,88,67,45,44,89
3
b label1
10,21,93,88,67,45,44,89
4
label1 div $5,$5,$6
10,21,93,88,67,1,44,89
5
beq $3,$1,label2
10,21,93,88,67,1,44,89
6
div $5,$5,$6
10,21,93,88,67,0,44,89
7
bnq $3,$1,label2
10,21,93,88,67,0,44,89
8
label2 addi $2,$3,5
10,21,93,88,67,0,44,89
9
end
your answer is :
10,21,93,88,67,0,44,89
yidarl@andromeda-67 19:11:31 ~/hw/hw5/solution
$
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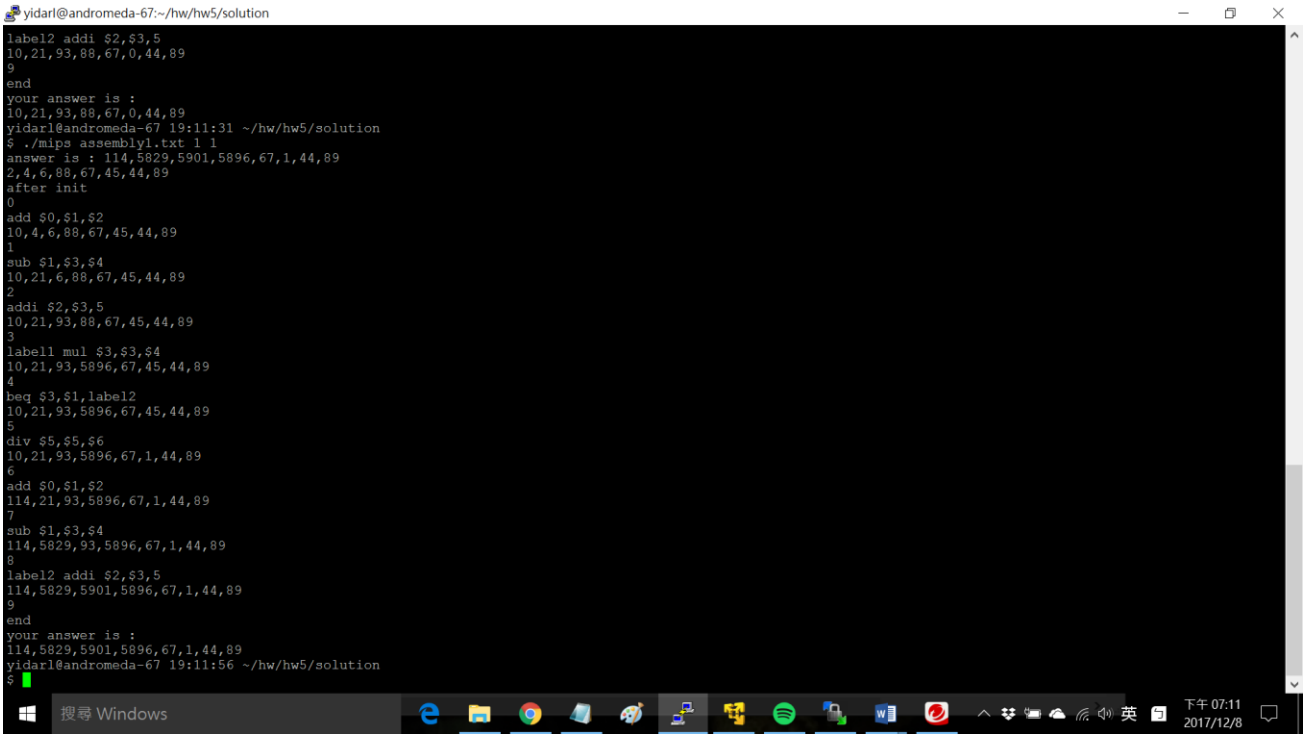
assembly1.txt

```
answer is : 114,5829,5901,5896,67,1,44,89
2,4,6,88,67,45,44,89
after init
0
add $0,$1,$2
10,4,6,88,67,45,44,89
1
sub $1,$3,$4
10,21,6,88,67,45,44,89
2
addi $2,$3,5
10,21,93,88,67,45,44,89
3
label1 mul $3,$3,$4
10,21,93,5896,67,45,44,89
4
beq $3,$1,label2
10,21,93,5896,67,45,44,89
5
div $5,$5,$6
10,21,93,5896,67,1,44,89
6
add $0,$1,$2
114,21,93,5896,67,1,44,89
7
sub $1,$3,$4
114,5829,93,5896,67,1,44,89
8
label2 addi $2,$3,5
114,5829,5901,5896,67,1,44,89
9
end
your answer is :
114,5829,5901,5896,67,1,44,89
```


yidarl@andromeda-67:~/hw/hw5/solution
label2 addi $2,$3,5
10,21,93,88,67,0,44,89
9
end
your answer is :
10,21,93,88,67,0,44,89
yidarl@andromeda-67 19:11:31 ~/hw/hw5/solution
$ ./mips assembly1.txt 1 1
answer is : 114,5829,5901,5896,67,1,44,89
2,4,6,88,67,45,44,89
after init
0
add $0,$1,$2
10,4,6,88,67,45,44,89
1
sub $1,$3,$4
10,21,6,88,67,45,44,89
2
addi $2,$3,5
10,21,93,88,67,45,44,89
3
label1 mul $3,$3,$4
10,21,93,5896,67,45,44,89
4
beq $3,$1,label2
10,21,93,5896,67,45,44,89
5
div $5,$5,$6
10,21,93,5896,67,1,44,89
6
add $0,$1,$2
114,21,93,5896,67,1,44,89
7
sub $1,$3,$4
114,5829,93,5896,67,1,44,89
8
label2 addi $2,$3,5
114,5829,5901,5896,67,1,44,89
9
end
your answer is :
114,5829,5901,5896,67,1,44,89
yidarl@andromeda-67 19:11:56 ~/hw/hw5/solution
$
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Part 2: MIPS simulator with 3-stage Pipelining and Data Forwarding

assembly.txt

```
answer is : 10,21,93,88,67,0,44,89
2,4,6,88,67,45,44,89
after init

clock cycle: 0
Fetch: add $0,$1,$2

clock cycle: 1
Fetch: sub $1,$3,$4
Execute: add $0,$1,$2

clock cycle: 2
Fetch: addi $2,$3,5
Execute: sub $1,$3,$4
Write_back: add $0,$1,$2
10,4,6,88,67,45,44,89

clock cycle: 3
Fetch: b label1
Execute: addi $2,$3,5
Write_back: sub $1,$3,$4
10,21,6,88,67,45,44,89

clock cycle: 4
Execute: b label1
Write_back: addi $2,$3,5
10,21,93,88,67,45,44,89

clock cycle: 5
Fetch: label1 div $5,$5,$6

clock cycle: 6
Fetch: beq $3,$1,label2
Execute: label1 div $5,$5,$6

clock cycle: 7
Execute: beq $3,$1,label2
Write_back: label1 div $5,$5,$6
10,21,93,88,67,1,44,89

clock cycle: 8
Fetch: div $5,$5,$6

clock cycle: 9
Fetch: bnq $3,$1,label2
Execute: div $5,$5,$6

clock cycle: 10
Execute: bnq $3,$1,label2
```

Write_back: div $5,$5,$6
10,21,93,88,67,0,44,89

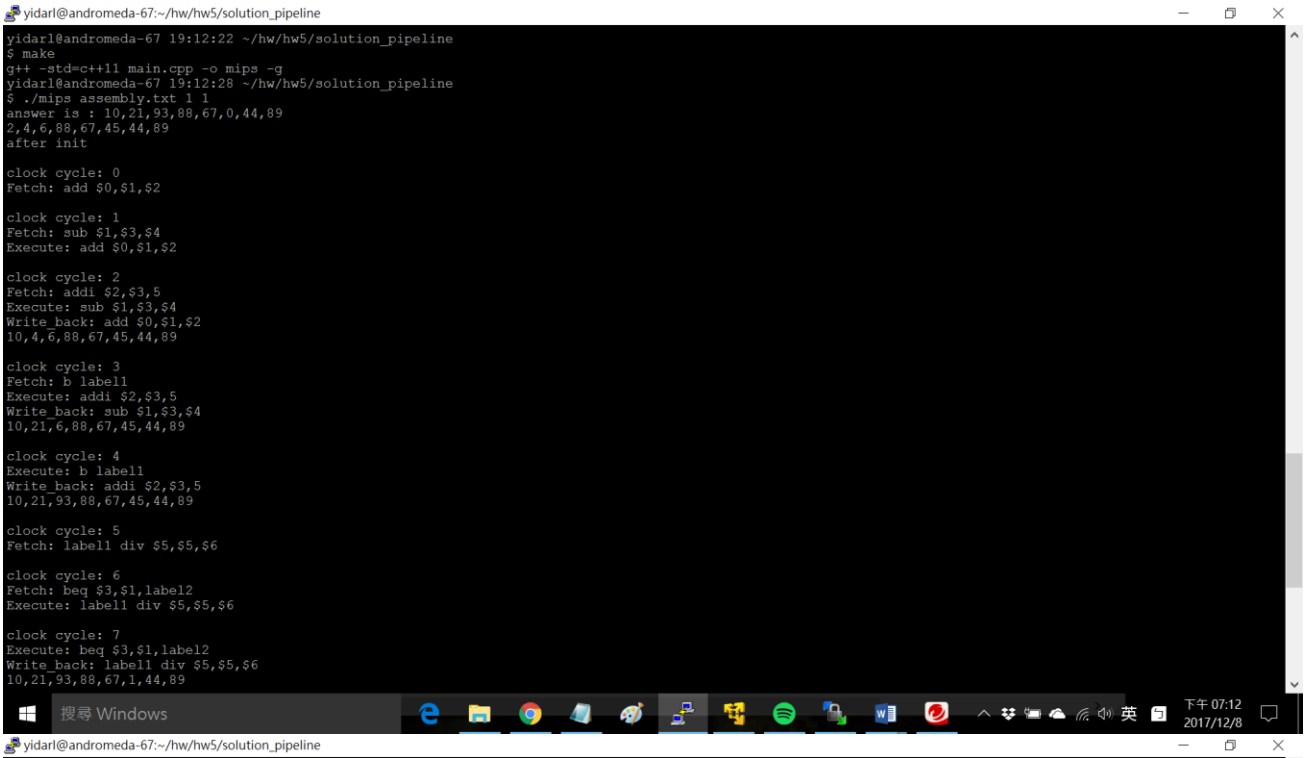
clock cycle: 11
Fetch: label2 addi $2,$3,5

clock cycle: 12
Execute: label2 addi $2,$3,5

clock cycle: 13
Write_back: label2 addi $2,$3,5
10,21,93,88,67,0,44,89

clock cycle: 14

your answer is :
10,21,93,88,67,0,44,89


yidarl@andromeda-67:~/hw/hw5/solution_pipeline
yidarl@andromeda-67 19:12:22 ~/hw/hw5/solution_pipeline
$ make
g++ -std=c++11 main.cpp -o mips -g
yidarl@andromeda-67 19:12:28 ~/hw/hw5/solution_pipeline
$ ./mips assembly.txt 1 1
answer is : 10,21,93,88,67,0,44,89
2,4,6,88,67,45,44,89
after init
clock cycle: 0
Fetch: add $0,$1,$2
clock cycle: 1
Fetch: sub $1,$3,$4
Execute: add $0,$1,$2
clock cycle: 2
Fetch: addi $2,$3,5
Execute: sub $1,$3,$4
Write_back: add $0,$1,$2
10,4,6,88,67,45,44,89
clock cycle: 3
Fetch: b label1
Execute: addi $2,$3,5
Write_back: sub $1,$3,$4
10,21,6,88,67,45,44,89
clock cycle: 4
Execute: b label1
Write_back: addi $2,$3,5
10,21,93,88,67,45,44,89
clock cycle: 5
Fetch: label1 div $5,$5,$6
clock cycle: 6
Fetch: beq $3,$1,label2
Execute: label1 div $5,$5,$6
clock cycle: 7
Execute: beq $3,$1,label2
Write_back: label1 div $5,$5,$6
10,21,93,88,67,1,44,89
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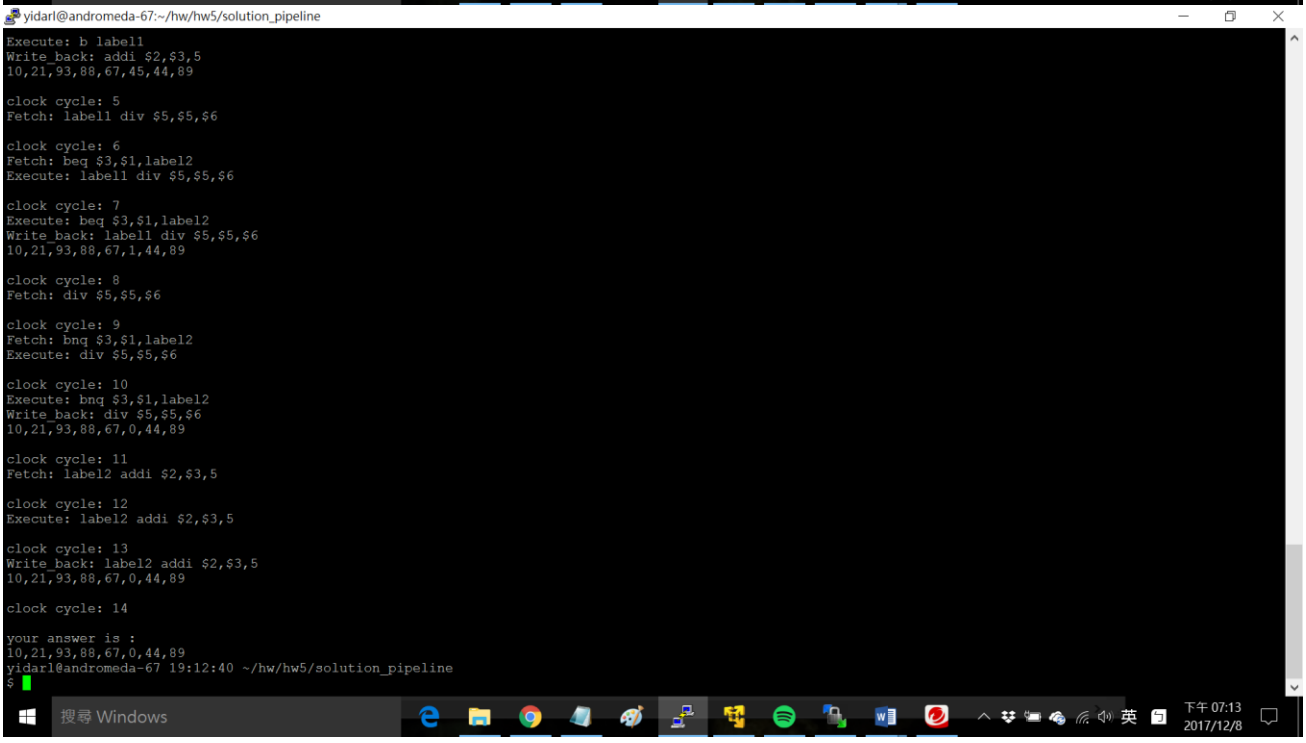
yidarl@andromeda-67:~/hw/hw5/solution_pipeline
Execute: b label1
Write_back: addi $2,$3,5
10,21,93,88,67,45,44,89
clock cycle: 5
Fetch: label1 div $5,$5,$6
clock cycle: 6
Fetch: beq $3,$1,label2
Execute: label1 div $5,$5,$6
clock cycle: 7
Execute: beq $3,$1,label2
Write_back: label1 div $5,$5,$6
10,21,93,88,67,1,44,89
clock cycle: 8
Fetch: div $5,$5,$6
clock cycle: 9
Fetch: bnq $3,$1,label2
Execute: div $5,$5,$6
clock cycle: 10
Execute: bnq $3,$1,label2
Write_back: div $5,$5,$6
10,21,93,88,67,0,44,89
clock cycle: 11
Fetch: label2 addi $2,$3,5
clock cycle: 12
Execute: label2 addi $2,$3,5
clock cycle: 13
Write_back: label2 addi $2,$3,5
10,21,93,88,67,0,44,89
clock cycle: 14
your answer is :
10,21,93,88,67,0,44,89
yidarl@andromeda-67 19:12:40 ~/hw/hw5/solution_pipeline
$
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assembly1.txt

```
answer is : 114,5829,5901,5896,67,1,44,89
2,4,6,88,67,45,44,89
after init

clock cycle: 0
Fetch: add $0,$1,$2

clock cycle: 1
Fetch: sub $1,$3,$4
Execute: add $0,$1,$2

clock cycle: 2
Fetch: addi $2,$3,5
Execute: sub $1,$3,$4
Write_back: add $0,$1,$2
10,4,6,88,67,45,44,89

clock cycle: 3
Fetch: label1 mul $3,$3,$4
Execute: addi $2,$3,5
Write_back: sub $1,$3,$4
10,21,6,88,67,45,44,89

clock cycle: 4
Fetch: beq $3,$1,label2
Execute: label1 mul $3,$3,$4
Write_back: addi $2,$3,5
10,21,93,88,67,45,44,89

clock cycle: 5
Execute: beq $3,$1,label2
Write_back: label1 mul $3,$3,$4
10,21,93,5896,67,45,44,89

clock cycle: 6
Fetch: div $5,$5,$6

clock cycle: 7
Fetch: add $0,$1,$2
Execute: div $5,$5,$6

clock cycle: 8
Fetch: sub $1,$3,$4
Execute: add $0,$1,$2
Write_back: div $5,$5,$6
10,21,93,5896,67,1,44,89

clock cycle: 9
Fetch: label2 addi $2,$3,5
Execute: sub $1,$3,$4
```

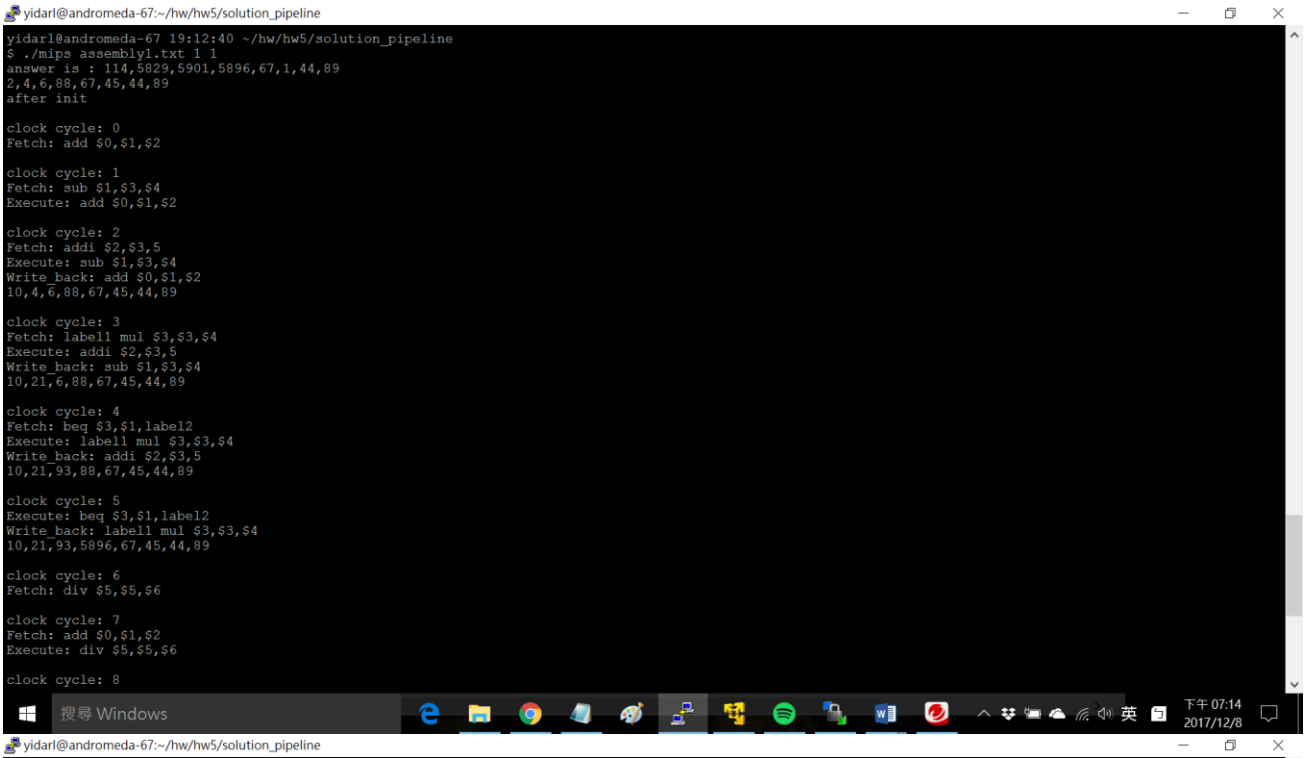
Write_back: add $0,$1,$2
114,21,93,5896,67,1,44,89

clock cycle: 10
Execute: label2 addi $2,$3,5
Write_back: sub $1,$3,$4
114,5829,93,5896,67,1,44,89

clock cycle: 11
Write_back: label2 addi $2,$3,5
114,5829,5901,5896,67,1,44,89

clock cycle: 12

your answer is :
114,5829,5901,5896,67,1,44,89


yidarl@andromeda-67:~/hw/hw5/solution_pipeline
yidarl@andromeda-67 19:12:40 ~/hw/hw5/solution_pipeline
$ ./mips assembly1.txt 1 1
answer is : 114,5829,5901,5896,67,1,44,89
2,4,6,88,67,45,44,89
after init
clock cycle: 0
Fetch: add $0,$1,$2
clock cycle: 1
Fetch: sub $1,$3,$4
Execute: add $0,$1,$2
clock cycle: 2
Fetch: addi $2,$3,5
Execute: sub $1,$3,$4
Write_back: add $0,$1,$2
10,4,6,88,67,45,44,89
clock cycle: 3
Fetch: label1 mul $3,$3,$4
Execute: addi $2,$3,5
Write_back: sub $1,$3,$4
10,21,6,88,67,45,44,89
clock cycle: 4
Fetch: beq $3,$1,label2
Execute: label1 mul $3,$3,$4
Write_back: addi $2,$3,5
10,21,93,88,67,45,44,89
clock cycle: 5
Execute: beq $3,$1,label2
Write_back: label1 mul $3,$3,$4
10,21,93,5896,67,45,44,89
clock cycle: 6
Fetch: div $5,$5,$6
clock cycle: 7
Fetch: add $0,$1,$2
Execute: div $5,$5,$6
clock cycle: 8
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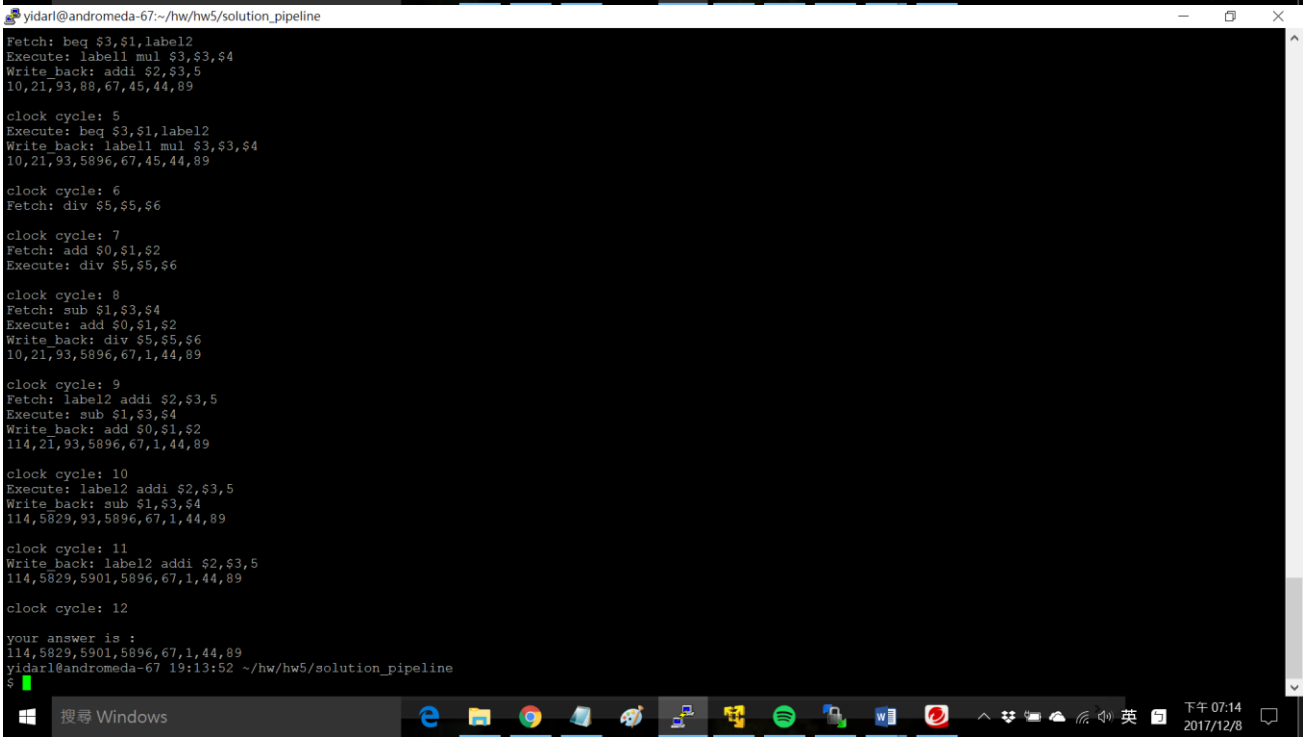
yidarl@andromeda-67:~/hw/hw5/solution_pipeline
Fetch: beq $3,$1,label2
Execute: label1 mul $3,$3,$4
Write_back: addi $2,$3,5
10,21,93,88,67,45,44,89
clock cycle: 5
Execute: beq $3,$1,label2
Write_back: label1 mul $3,$3,$4
10,21,93,5896,67,45,44,89
clock cycle: 6
Fetch: div $5,$5,$6
clock cycle: 7
Fetch: add $0,$1,$2
Execute: div $5,$5,$6
clock cycle: 8
Fetch: sub $1,$3,$4
Execute: add $0,$1,$2
Write_back: div $5,$5,$6
10,21,93,5896,67,1,44,89
clock cycle: 9
Fetch: label2 addi $2,$3,5
Execute: sub $1,$3,$4
Write_back: add $0,$1,$2
114,21,93,5896,67,1,44,89
clock cycle: 10
Execute: label2 addi $2,$3,5
Write_back: sub $1,$3,$4
114,5829,93,5896,67,1,44,89
clock cycle: 11
Write_back: label2 addi $2,$3,5
114,5829,5901,5896,67,1,44,89
clock cycle: 12
your answer is :
114,5829,5901,5896,67,1,44,89
yidarl@andromeda-67 19:13:52 ~/hw/hw5/solution_pipeline
$
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