

IT Security

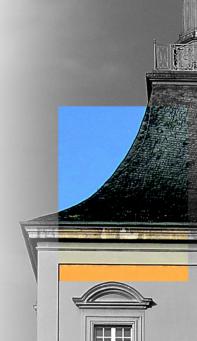
Side Channels: Attacks and Defense

Dr. Jernej Tonejc

Bundesamt für Sicherheit in der Informationstechnik Abteilung V - Verschlusssachensicherheit und Kryptographie

SCA | Universität Bonn | WS 2024/25

Gitversion: Unbekannt Filename: ITSec-lecture-SCA





Lecture overview

- Definition of a side channel
- Types of side channels/attacks
- Countermeasures
- Examples
- Examples
- Examples

- PhD in Mathematics, USA
- Working with cryptography & IT-Security since 1998
- Cyber security @ Fraunhofer FKIE, 2014-2016
- At BSI¹ since 2016
 Information Assurance Technology and IT Management Division,
 Section KM 25 IT Solution Systems for Classified I

¹Bundesamt für Sicherheit in der Informationstechnik/Federal office for information security



BSI as an employer





















Personalgewinnung BSI

bewerbung@bsi.bund.de ☑ Tel. +49 (0) 228 99 9582 6388
Bundesamt für Sicherheit in der Informationstechnik
Referat Z 8 – Personalgewinnung
Godesberger Allee 185-189
53175 Bonn





kununu"

www.bsi.bund.de/karriere

www.bsi.bund.de/studierende 🗹



Introduction

Outside the box

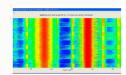
Inside the box

Watch and Listen Carefully

- What are Side Channels
- Attacks
- Countermeasures
- Turing Machine

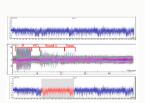


What are Side Channels



- Based on (non-intentional) physical information
- Can be inherent or induced
- Can enable new kinds of attacks









Side Channels vs. Covert Channels

Side channels ⇒ Interception/Wiretapping

The goal is to obtain the internal information about the system. The attacker is often passive.

Covert channels ⇒ Communication

The goal is to exfiltrate the information.

They require an active attacker.

A side channel can be used as a building block for a covert channel.



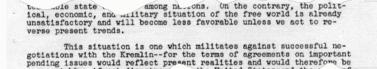
Types of Side Channels

- Timing (Kocher 1996)
- Power (KJJ 1999)
- Electromagnetic radiation (UCL &Gemplus 2001)
- Temperature (Naccache 2009)
- Light (Kuhn 2002)
- Sound (Shamir & Tromer 2004)
- Photonic emissions (TU Berlin 2012)



Some Unusual Side Channels

- Keyboard clicks can be distinguished by a cell phone's microphone [2]
- In former East Germany, a page with all possible characters was typed by each typewriter that was produced to trace them later



YOUR fingerprints



Source: Wikinedia



Source: Wikipedia



Types of Attacks

- Active vs. passive
 - Exploit abnormal behavior
 - Insertion of signals/glitches
 - Normal operation
 - Reading hidden signals
- Invasive vs. non-invasive
- Side-channel attacks are usually passive and non-invasive



Leakage is exploitable due to

- dependency on sequences of instructions executed
- dependency on data being processed
- other physical effects
- ability to work on one small part at a time



Levels of Analysis

- Simple: just one measurement
- Differential: multiple measurements, correlate
- Higher order: different samples
- Combining several side-channels
- Combining with theoretical cryptanalysis



- Digital Storage Oscilloscope (DSO ☑)
- EMF sensors and probes
- ChipWhisperer ✓

ChipWhisperer Nano, ∼50 EUR



ChipWhisperer Lite, \sim 250 EUR





Countermeasures

- TEMPEST¹
 - NSA specification & NATO certification
 - Methods of shielding against spying
 - Zone model
 - Filtering
 - Specifics are classified
- Masking, hiding
- Time/execution randomization
- Noise generation

NATO SDIP-27 Level A,B,C

Zone 0, Zone 1, Zone 2, Zone 3

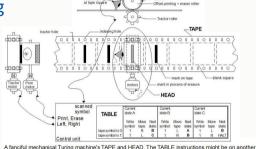
 $^{^{} extstyle 1}$ Telecommunications Electronics Materials Protected from Emanating Spurious Transmissions



Turing Machine

A mathematical model of computing

- A tape with cells
- A head for reading & writing
- A state register
- Table of instructions
- In practice: need to read, write and move around



A fanciful mechanical Turing machine's TAPE and HEAD. The TABLE instructions might be on another "read only" tape, or perhaps on punch-cards. Usually a "finite state machine" is the model for the TABLE Source: Wikinedia CC BY-SA 3.0

Church-Turing thesis

A function on natural numbers is computable by a human following an algorithm, if and only if it is computable by a Turing machine.



Introduction

Outside the box

Inside the box

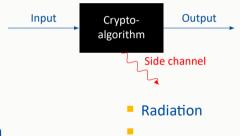
Watch and Listen Carefully

- What's the Time
- Can't Resist the Current
- The Error Was X



Side Channels on the Outside

Treat the system as a closed box



- - Time
 - Power consumption

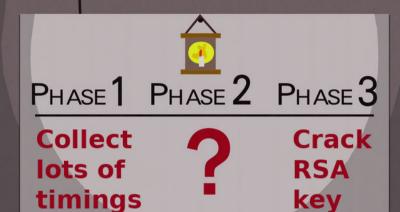
We can observe:

Passive attack



Measuring Timing Variations

- The duration depends on secret data
- Conditions:
 - Can correlate correct guesses with observed timings
 - Can work one bit/one byte at a time
- Averaging over several measurements to reduce the noise





- Public key (n, e), secret key (p, q, d)
- $\blacksquare n = p \cdot q, e \cdot d \equiv 1 \pmod{(p-1)(q-1)}, n \text{ has } k+1 \text{ bits}$
- To sign a message *m*, compute

$$m^d \mod n$$
,

using e.g. Square-and-Multiply (simplified):

```
Set y \leftarrow 1, s \leftarrow m

For bits d_0, d_1, \dots, d_k of d:

If d_i = 1:

y \leftarrow y \cdot s \mod n

s \leftarrow s^2 \mod n

Return y
```

```
Set y \leftarrow 1
For bits d_k, d_{k-1}, \dots, d_0 of d:
y \leftarrow y^2 \mod n
If d_i = 1:
y \leftarrow y \cdot m \mod n
Return y
```

- Public key (n, e), secret key (p, q, d)
- $\blacksquare n = p \cdot q, e \cdot d \equiv 1 \pmod{(p-1)(q-1)}, n \text{ has } k+1 \text{ bits}$
- To sign a message *m*, compute

$$m^d \mod n$$
,

using e.g. Square-and-Multiply (simplified):

```
Set y \leftarrow 1, s \leftarrow m

For bits d_0, d_1, \dots, d_k of d:

If d_i = 1:

y \leftarrow y \cdot s \mod n

s \leftarrow s^2 \mod n

Return y
```

Set
$$y \leftarrow 1$$

For bits d_k, d_{k-1}, \dots, d_0 of d :
 $y \leftarrow y^2 \mod n$
If $d_i = 1$:
 $y \leftarrow y \cdot m \mod n$
Return y

Data-dependent execution!



UNIVERSITÄT BONN Timing Attack

- Each signature takes time $T = e + \sum_{i=0}^{k} t_i$
- Guess the first b bits of d
- Predict the time given the guess and subtract from T
- Compute variance of the difference over all samples:
 - We obtain Var(e) + (k b) Var(t) for correct guess
 - We obtain Var(e) + (k + b 2c) Var(t) if only first c < b bits correct
- Correct guesses decrease the variance
- Similar attacks on other public-key schemes



Square-and-Multiply (simplified)

Execution-time independent implementation

```
Set y \leftarrow 1

For bits d_k, d_{k-1}, \dots, d_0 of d:

y \leftarrow y^2 \mod n, z \leftarrow y

If d_i = 1:

y \leftarrow y \cdot m \mod n

Else:

z \leftarrow z \cdot m \mod n

Return y
```

Is this safe?



Square-and-Multiply (simplified)

Execution-time independent implementation

```
Set y \leftarrow 1

For bits d_k, d_{k-1}, \dots, d_0 of d:

y \leftarrow y^2 \mod n, z \leftarrow y

If d_i = 1:

y \leftarrow y \cdot m \mod n

Else:

z \leftarrow z \cdot m \mod n

Return y
```

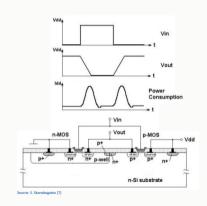
Caution: Compiler optimization may remove z!

Is this safe? Seems to be...



Power Consumption of Circuits

- CMOS¹ circuits use current when switching
- More switching ⇒ more current
- Operations correlate with current
- Measuring current reveals the operations



¹Complementary Metal Oxide Semiconductor





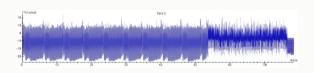
Types of Power Analysis

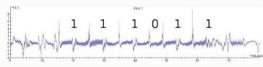
- Simple/Differential/Correlation Power Analysis (SPA/DPA/CPA)
- Template Attacks
- Stochastic Models
- Linear Regression Analysis
- Principal Component Analysis (PCA)
- **.** . . .



Simple Power Analysis

- One or few measurements
- Search for repetitive patterns
- Data-independent but instruction-dependent
- See number of rounds, memory access, key



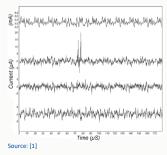




Differential Power Analysis

- Several thousand measurements
- Selection function: split the traces based on the predicted value of one cyphertext bit given the (sub)key guess
- Compare the difference of the averages of the two sets
- Correct (sub)key guess has higher difference

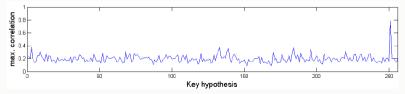
Try it yourself: https://dpacontest.telecom-paris.fr/home/





Correlation Power Analysis

- Again several thousand measurements
- Model of the side channel vs. the real side channel
- Correlation based on key hypothesis
- Correct hypothesis has highest correlation



Padding Oracle Attacks

CBC-mode¹ with PKCS7 padding:

$$P_i = D_K(C_i) \oplus C_{i-1}, C_0 = IV$$
 (decryption)

PKCS7-padding: last block has last *n* bytes equal to *n*

- Server reacts differently to different errors: bad padding vs. bad decryption
- First published in 2002 by Vaudenay
- Lucky Thirteen (2013), POODLE² (2014)

¹Cipher-Block-Chaining

² Padding Oracle On Downgraded Legacy Encryption



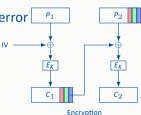
Example

• We encrypt two blocks, P_1 , P_2 , with 2 bytes of padding:

$$C_1 = E_K(P_1 \oplus IV), C_2 = E_K(P_2 \oplus C_1)$$

where P_2 ends in 0×02 , 0×02

- Modifying C_1 affects decryption of P_2 : $P_2 = D_K(C_2) \oplus C_1$
- Change the last byte b_{-1} of C_1 as $b_{-1} \leftarrow b_{-1} \oplus z_{-1} \oplus 0x01$:
 - If the last byte of the original P_2 is z_{-1} , there is no padding error
 - Otherwise, there is a padding error
 - Try with all 256 possible values for z_{-1}
- Proceed by setting $b_{-1} \leftarrow b_{-1} \oplus z_{-1} \oplus 0x02$, $b_{-2} \leftarrow b_{-2} \oplus z_{-2} \oplus 0x02$ and guessing z_{-2}





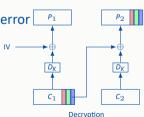
Example

• We encrypt two blocks, P_1 , P_2 , with 2 bytes of padding:

$$C_1 = E_K(P_1 \oplus IV), C_2 = E_K(P_2 \oplus C_1)$$

where P_2 ends in 0×02 , 0×02

- Modifying C_1 affects decryption of P_2 : $P_2 = D_K(C_2) \oplus C_1$
- Change the last byte b_{-1} of C_1 as $b_{-1} \leftarrow b_{-1} \oplus z_{-1} \oplus 0x01$:
 - If the last byte of the original P_2 is z_{-1} , there is no padding error
 - Otherwise, there is a padding error
 - Try with all 256 possible values for z_{-1}
- Proceed by setting $b_{-1} \leftarrow b_{-1} \oplus z_{-1} \oplus 0x02$, $b_{-2} \leftarrow b_{-2} \oplus z_{-2} \oplus 0x02$ and guessing z_{-2}





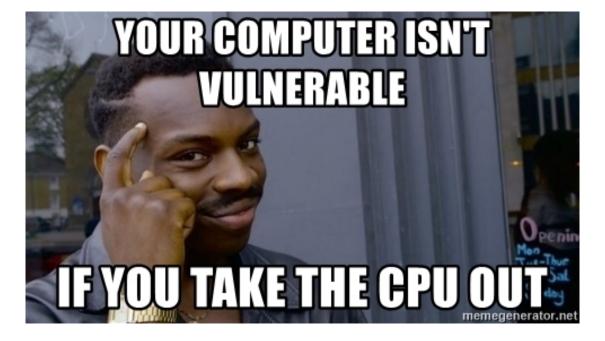
Introduction

Outside the box

Inside the box

Watch and Listen Carefully

- Rowhammer
- Flush and Reload
- Spectre and Meltdown





Actively Creating Side Channels

- Sometimes the channels are not there
- By manipulating the system, we create them
- We use the knowledge of
 - hardware
 - algorithm
 - implementation



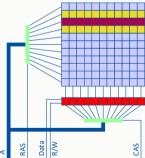
Cells in DRAM need periodic refresh

When reading, the original content is destroyed and must be copied

back

• Due to high density, rapid access causes side effects:

- Bits in adjacent rows can flip
- Depends on the module
- Unpredictable, but repeatable





- Flipping the superuser or NX-bit in a pagetable:
 - Access to kernel pages from userspace
 - Memory pages can be made executable
 - Remove write protection
- Flipping a bit in ssh public key:
 - In .ssh/authorized_keys
 - New modulus can likely be factored
 - Compute the new private key and log in



- Flipping the superuser or NX-bit impagetable:
 - Access to kernel pages from serspace
 - Memory pages carries made executable
 - Remove w protection
- Flipping a tit in ssh public key:
 - In .ssh/at horized keye
 - New modeus anxely be factored
 - Compute the new private key and log in



- Flipping a bit in server address:
 - In sources.list
 - Packages will update from a wrong server (ubuntu.com \rightarrow ufuntu.com)
- Flipping a bit in GPG key ring:
 - Similar to ssh key
 - Can now sign packages and install them



- Flipping a bit in server address.
 - In sources.list
 - Packages will poate from a wrong server (ubcom → ufuntu.com)
- Flipping a it in GPG key ring:
 - Similar to sh key
 - Can now son packages and install them



Caching in Modern Computers

- Several types of memory:
 - In CPU (registers)
 - In CPU (cache)
 - RAM
- Access times vary greatly
- Speed increases the closer the data is to CPU

- Flash drives
- Hard drives
- Tapes/DVDs (backup)



Caching in Modern Computers

- Several types of memory:
 - In CPU (registers)
 - In CPU (cache)

Fast & Volatile

- Flash drives
- Hard drives

Tapes/DVDs (backup)

Slow & Non-volatile

- RAM
- Access times vary greatly
- Speed increases the closer the data is to CPU



Intel Cache Architecture

- Several levels: L0, L1, L2, LLC¹
- Several types: TLB, LFB, BPU, BTB² ...
- LLC is shared across cores
- Can flush (evict) LLC from userspace (clflush)

Location in cache is related to the physical location in RAM



latency (cycles)

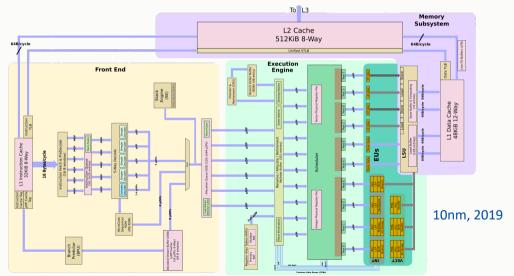
RAM

¹Last-Level-Cache

² Translation Lookaside Buffer, Line Fill Buffer, Branch Prediction Unit, Branch Target Buffer



Intel Sunny Cove Block Diagram





Cache Timing Side Channel

- Computation speed depends on the location of the data
- In cache: fast. Not in cache: slow
- Two common techniques of measuring:
 - Flush+Reload: Evict relevant data and check for reload, or
 - Prime&Probe: Check if own data got evicted due to cache collision



Attacking with Flush+Reload

- Assumption: data-dependent code lies in different cache lines
- Focus on the library code
- Flush, wait and reload
- Shorter time indicates the victim loaded it already
- This is our side channel!



Flush+Reload attack on RSA

Assume the If and Else branches lie in different cache lines:

```
Set y \leftarrow 1

For bits d_k, d_{k-1}1, \dots, d_0 of d:

y \leftarrow y^2 \mod n, z \leftarrow y

If d_i = 1:

y \leftarrow y \cdot m \mod n

Else:

z \leftarrow z \cdot m \mod n

Return y
```

Alignment determined by compiler and location in memory

• Depending on the bit value d_i , different cache lines get used



Speculative Execution

- Modern CPUs are superscalar: several execution units, long pipelines
- Conditional branches present an issue:
 branch target is unclear before the condition gets resolved
 - To increase speed, processor chooses the most likely branch instead of waiting
 - Correct choice speeds up the computation
 - Wrong choice causes a roll-back, but no loss otherwise: the processor would have to wait for the correct target anyway
- Similar problem with permissions check
- Problem: roll-back leaves cache polluted



A Library Example: Setup

- One central library
- Requests can also be made through the department's secretary
- The books arrive at the secretary's office the next day
- The secretary validates the request before giving out the book
- The books can be returned directly or to the secretary
- If a book is already at the secretary, no request is made to the library



A Library Example: Goal

- We want to find out the grade of the student John Doe
- Grades are integers between 1 and 5
- The secretary has access to all the grades
- The secretary will only give out the requester's grade
- We get no answer if we ask directly



IT Department

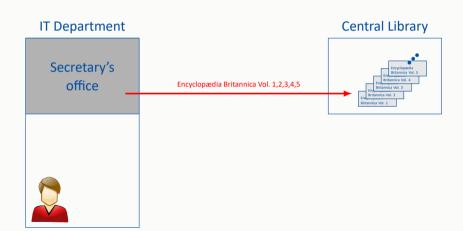


Central Library

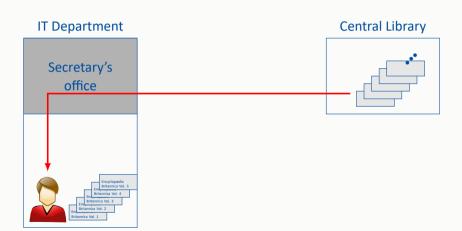


1. "I want Encyclopædia Britannica Vol. 1, 2, 3, 4, 5"

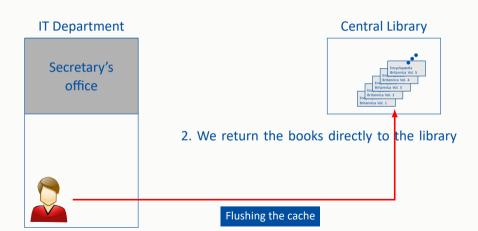










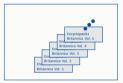




IT Department

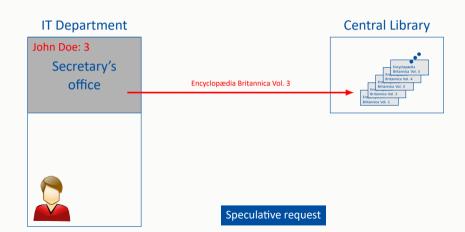


Central Library

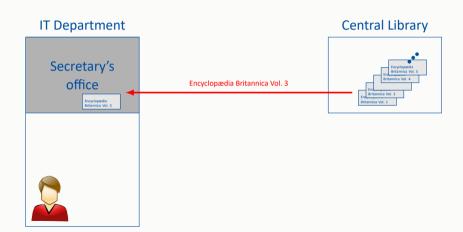


3. "I want Encyclopædia Britannica Vol. X, where X is John Doe's grade"











IT Department



Central Library



Permission check



IT Department



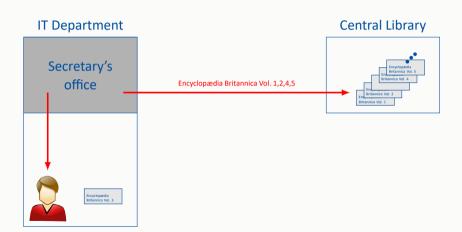
Central Library



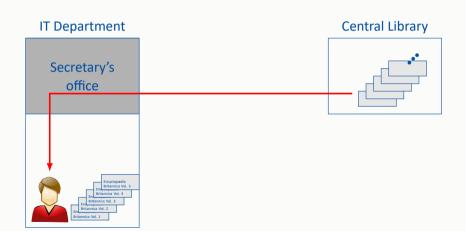
4. "I want Encyclopædia Britannica Vol. 1, 2, 3, 4, 5"









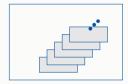




IT Department



Central Library



The book that arrived first indicates the most likely grade



Introduction

Outside the box

Inside the box

Watch and Listen Carefully

- Talking Behind Your Back
- LED it Go
- RAM Radio & AirHopper
- Twinkle, Twinkle Little Transistor



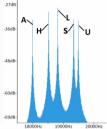
Exfiltrating Data, Linking Devices

- Main goal of these attacks is getting data out
- Use of unexpected communication channels
- Mostly uses standard equipment



Cross-Device Tracking

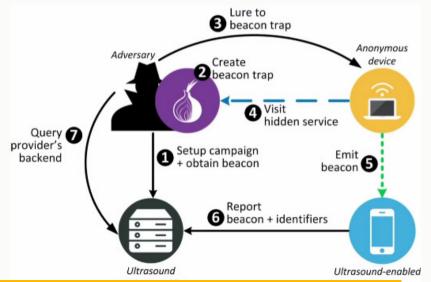
- SilverPush founded in 2012
- Embed inaudible sound in TV ads (ultrasound beacons)
- Apps on phones pick this up⇒ Cross-device user tracking
- Privacy issues voiced in 2015







Deanonymizing Tor Users





Escaping the Air-Gapped Machines

- Air-gapped: no direct connection to the world
- Need to bridge the gap to leak the data
- Infiltration doable¹, exfiltration a challenge
- Is it enough to see the machine?



Blinking HD-LED

- Disk activity makes LED blink:
 - Duration corresponds to amount read
 - E.g. <4kB \sim 0.18 ms, 5MB \sim 32ms
- Low-privilege process can read data
- Simple camera can record 60 frames/sec
- Bitrates from 60 4000 bits/sec²
- Need to control the noise



Source: [6]



(Un)expected Sources of Signals

- Data lanes within PC emit EMR³
- Need to find useful frequencies
- Example 1: DDR-RAM
- Example 2: Videocards

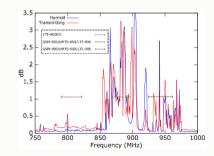


RAM Radio

- DDR-RAM
- LTE uses 800MHz carrier frequency
- Modified phone firmware⁴ can decode signals
- Use MOVNTDQ⁵ for RAM access
- Bitrates 2-100 bits/s

Standard Name	I/O bus clock (f_c)	EMR Range
DDR3-1600	800MHz	600MHz-1100MHz
DDR3-1866	933MHz	750MHz-1150MHz
DDR4-2133	1066MHz	750MHz-943MHz (fragmented) 1.04GHz-1.066GHz
Courses II		1.04GHz-1.066GHZ

Source: [8]



⁴Using e.g. OsmocomBB

⁵ Move Double Quadword Non-Temporal; avoids cache



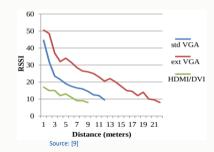
AirHopper

Video cables cary signals

$$(H_{pixel} + H_{sync}) * (V_{pixel} + V_{sync}) * RR = PC^6$$

E.g. for 1440x900 we get 106.5 MHz

- Control signals even when monitor off
- Smartphones have FM receivers
- Patch code to ignore headphones
- Use modulation (A-FSK or DTMF⁷)
- Effective range \sim 7m, 80 bits/s



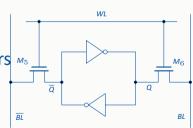
⁶Utility like cvt can be used to compute the pixel clock (PC)

⁷Audio Frequency-Shift Keying, Dual-Tone Multiple Frequency



Photonic Emission Analysis

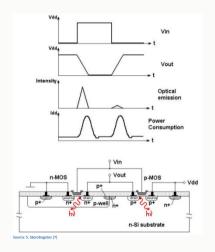
- Microprocessors are built out of lots of transistors
- Low-power embedded devices at μ m scale
- Internal memory uses SRAM cells
 - Cell consists of 6 MOSFETs⁸
 - 4 are within two cross-coupled inverters M5
 - Access through WL, value in BL, BL





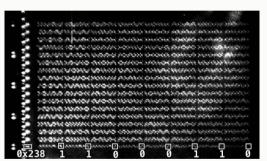
Transistor Operation

- Hot-carrier luminescence:
 Transistors emit photons when switching
- Can detect SRAM memory access
- How?
 - Picosecond imaging circuit analysis (PICA, expensive, 1,000,000+ EUR!)
 - Optical microscope + CCD (cheaper)
 - Issue: temporal vs. spatial resolution





Practical Example







Optical emission of AES S-Box, stored in SRAM of ATMega328P. 256 Bytes are stored in 32 cells of 8 bytes each. The emissions of the row drivers (left) are clearly visible.

Summary





- What is a side channel
- What types of side channels exist
- Countermeasures
- Lots of examples

Take-away

Secure software development is not enough.



UNIVERSITÄT BONN Lightning Survey





References

- 1 P. Kocher et al. Differential Power Analysis.
- 2 S. Yang. Researchers recover typed text using audio recording of keystrokes. http://www.berkeley.edu/news/me-dia/releases/2005/09/14_key.shtml
- 3 B. Gras et al. Memory Deduplication: The Curse that Keeps on Giving. 33C3
- 4 Y. Yarom. FLUSH+RELOAD: a High Resolution, Low Noise, L3 Cache Side-Channel Attack.
- 5 V. Mavroudis, F. Maggi. Talking Behind Your Back. 33C3.
- 6 M. Guri et al. LED-it-GO: Leaking (A Lot of) Data from Air-Gapped Computers via the (Small) Hard Drive LED, DIMVA 2017.
- 7 S. Skorobogatov. Using Optical Emission Analysis for Estimating Contribution to Power Analysis.
- 8 M. Guri et al. GSMem: Data Exfiltration from Air-Gapped Computers over GSM Frequencies. USENIX 2015.
- 9 M. Guri et al. AirHopper: Bridging the Air-Gap between Isolated Networks and Mobile Phones using Radio Frequencies. MALCON 2014.
- 10 M. Lipp et al. Meltdown. ArXiV e-print 1801.01207
- 11 P. Kocher et al. Spectre Attacks: Exploiting Speculative Execution. ArXiV e-print 1801.01203
- 12 B. Nassi et al. Video-Based Cryptanalysis: Extracting Cryptographic Keys from Video Footage of a Device's Power LED. IACR e-print 2023.923.