CS151B/EE116C – Solutions to Homework #3

The delay Calculation: The delay = the gate delay + the max delay among inputs

Assumption:
The sum in 1 bit full adder is implemented by 2 input-XOR gates: Sum= (a xor b) xor C

1. G0 = A0 * B0 = 2T (the delay of 2input –AND gate) + max (0T, 0T) = 2T
2. P0 = A0 xor B0 = 2T + max(0T, 0T) = 2T
-> All Gi and Pi are 2T

3. Gα = (G0*P1*P2*P3) + (G1*P2*P3) + (G2*P3) + (G3)
= 5T (the delay of 4input-OR gate) + max(5T+2T, 3T+2T, 2T+2T, 2T) = 5T + 7T = 12T
4. Pα = P0*P1*P2*P3 = 5T + max(2T, 2T, 2T, 2T) = 7T
-> All Gi and Pi of the 2-level CLG in the 16bit-HCLA are 12T and 7T respectively.

5. C12 = Gy + G_β*Py + Gα*P_β*Py+ C0*Pα*P_β*Py
= 5T (4 input-OR gate) + max (12T, 2T+max(12T, 7T), 3T+max(12T, 7T, 7T) + 5T+max(0T, 7T, 7T, 7T)
= 5T + 15T = 20T

6. C15 corresponds to the C3 in the third 4bit-CLA (CLAy) in the 16bit-HCLA
C15 = G2+G1*P2+G0*P1*P2+**C12***P0*P1*P2 since C12 is the Cin(C0) in this CLA.
= 5T (4 input-OR) + max(2T, 2T+2T, 3T+2T, 5T+**20T**) = 5T + 25T = 30T

7. C16 = G_δ+ Gy*P_δ + G_β*P_δ*Py + Gα*P_δ*P_β*Py+ C0 * P_δ*P_β*Py*Pα
= 7T + max (12T, 2T+max(12T, 7T), 3T+max(12T, 7T, 7T), 5T+max(12T, 7T, 7T, 7T) + 7T + max(0T, 7T, 7T, 7T, 7T)
= 7T + max(12T, 14T, 15T, 17T, 14T) = 7T + 17T = 24T

8. S15 corresponds to the S3 in the bottom 4bit-CLA in 16bit-HCLA
S15 = (a xor b) xor C15 = 2T + max(2T+2T, 30T) = 32T

9. C20 corresponds to the carry out (C4) of top 4bit-CLA in the 16bit-CSA.
So, C20 (C4) = G3+G2*P3+G1*P3*P2+G0*P3*P2*P1+**C16***P3*P2*P1*P0, but C16's delay is 0T in the CSA
= 7T + max(2T, 2T+2T, 3T+2T, 5T+2T, 7T+2T) = 7T+9T = 16T

10. S19 corresponds to the S3 of the top 4bit-CLA in the 16bit-CSA.
To calculate the delay of S19, the delay of C19 is required.
C19 also corresponds to the C3 of the top 4bit-CLA in the 16bit-CSA.
So, C19 (C3) = G2 + G1*P2 + G0*P2*P1 + **C16***P2*P1*P0, but C16's delay is 0T in the CSA
= 5T + max(2T, 2T+2T, 3T+2T, 5T+2T) = 5T+7T = 12T
S19 = (a xor b) xor C19 = 2T + max(2T+2T, 12T) = 14T

11. C24 corresponds to the carry out (C4) of 2nd top 4bit-CLA in the 16bit-CSA.
So, C24(C4) = G3+G2*P3+G1*P3*P2+G0*P3*P2*P1+C0*P3*P2*P1*P0
= G3+G2*P3+G1*P3*P2+G0*P3*P2*P1+**C20***P3*P2*P1*P0 since C20 is C0 in this CLA

= 7T + max(2T, 2T+2T, 3T+2T, 5T+2T, 7T+**16T**) = 7T+23T = 30T

12. C31 corresponds to the C3 in the bottom 4bit-CLA in the 16bit-CSA
    To calculate the delay of C31, the delay of C28 (Cin) is required.
    C28 corresponds to the carry out (C4) of third 4bit-CLA in the 16bit-CSA.
    C28 = G3+G2*P3+G1*P3*P2+G0*P3*P2*P1+C0*P3*P2*P1*P0
        = G3+G2*P3+G1*P3*P2+G0*P3*P2*P1+**C24***P3*P2*P1*P0, since the Cin of this CLA is C24
        = 7T + max(2T, 2T+2T, 3T+2T, 5T+2T, 7T+**30T**) = 7T+37T = 44T
    C31(C3) = G2 + G1*P2 + G0*P2*P1 + C0*P2*P1*P0 = G2 + G1*P2 + G0*P2*P1 + **C28***P2*P1*P0
        = 5T+max(2T, 2T+2T, 3T+2T, 5T+**44T**) = 5T+49T = 54T

13. C32(after MUX) = 4T (the delay of MUX) + max (C32s, selection bit(C16))
    C32 corresponds to the carry out of the bottom 4bit-CLA in the 16bit-CSA.
    C32 = G3+G2*P3+G1*P3*P2+G0*P3*P2*P1+C0*P3*P2*P1*P0
        = G3+G2*P3+G1*P3*P2+G0*P3*P2*P1+**C28***P3*P2*P1*P0
        = 7T + max(2T, 2T+2T, 3T+2T, 5T+2T, 7T+**44T**) = 7T+51T = 58T, C28 is 44T from the solution 12.
    Since C16 is 24T from the solution 7.
    C32(after MUX) = 4T + max(58T, 58T, 22T) = 62T

14. S31(after MUX) = 4T (the delay of MUX) + max(S31s, C16)
    S31 = (a xor b) xor C31 = 2T + max(2T, 54T) = 56T
    S31(after MUX) = 4T+max(56T, 56T, 24T)= 60T