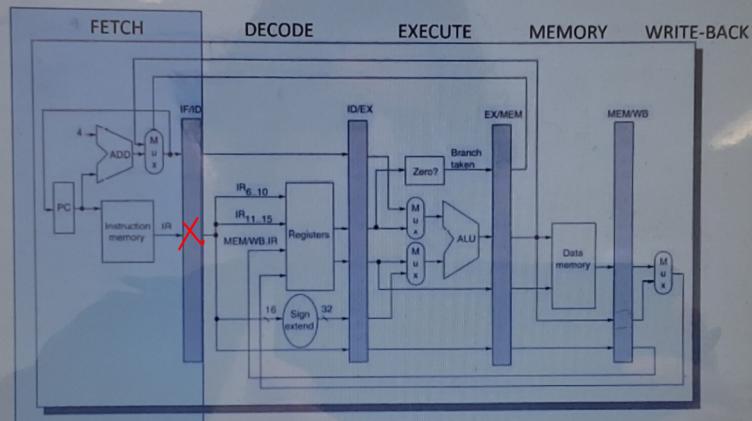


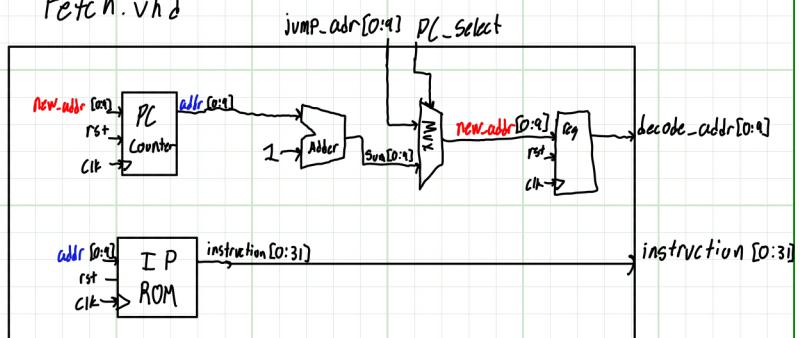
# DLX Pipeline Architecture



X: don't implement (ROM has accounted for it) still need Mux Reg

- components:
- ✓ instruction memory (ROM)
  - ✓ program counter (10 bit register, since instructions are 1024 deep with a rst function)
  - ✓ Adder (does not need to be speedy also adds 1 not 4) [should be a Ripple carry Adder]
  - ✓ 2-to-1 mux (hand made module)
  - ✓ Register for mux

Fetch.vhd



PC-Counter - inputs: data\_in [0:9]      outputs: data\_out [0:9]  
rst  
clk

IP-ROM - inputs: data\_in [0:9]      outputs: data\_out [0:31]  
rst  
clk

Adder - inputs: input1 [0:9]      outputs: sum [0:9]

Mux - inputs: input A [0:9]  
              input B [0:9]      outputs: output [0:9]

MUX-register - instantiate PC-Counter register (same inputs & outputs)