DE-10 Lite
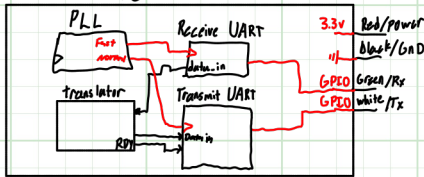

PLL: receives Clk then
slows down PClk

To-do: determine clk speed
determine 1 or 2 PLL's for Rx & Tx

Translator: Receives data from
Rx UART and determines what to
send back

inputs: 8 bit vector (data_in)
        Clk
Outputs: 8 bit vector (data_out)

Receive UART: Receives 8 data bits,
One start bit, One end bit (10 bits).
must be oversampled by 8

inputs: 1 bit Rx gpio (Rx)
        PClk
Outputs: 8 bit vector (data_in)

Transmit UART: receives translated data
and sends it back to computer

inputs: 8 bit vector (data_out)
        PClk
        1 bit start bit (start)
output: 1 bit Tx gpio (Tx)