Lab 1 -- UART

20 Points Possible

1/11/2026

Attempt 1

In Progress

NEXT UP: Submit Assignment

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Unlimited Attempts Allowed

1/12/2026

Details

Goals:

1. Review concepts of digital design, including Finite State Machines, FIFOs, PLLs, serial communication, ASCII, VHDL, etc.
2. Learn how to use the Intel Pin Planner.

Using the DE10-Lite Development Board, the Adafruit 954 USB-to-Serial Device, and a laptop or desktop running a serial terminal (e.g. PuTTy), implement a serial communication stream. Meet the following requirements:

1. Implement a UART on the FPGA, using VHDL, that operates with 8 data bits, 1 stop bit, no parity, no flow control, and 19,200 Baud. The UART receiver should over-sample by 8.
2. Configure a serial terminal session on the computer to communicate with the same parameters.
3. Uppercase characters typed in to the terminal should be converted to lowercase by the FPGA and sent back to the computer.
4. Lowercase characters typed in to the terminal should be converted to uppercase by the FPGA and sent back to the computer.
5. Any non-alphabetic characters received by the FPGA should result in a response of 'E', meaning "error".
6. Use the pin-planner utility to configure the TX and RX pins on the FPGA appropriately.

View Rubric

6930 Lab Report

Criteria	Ratings	Pts
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