Chapter 14 – VGA

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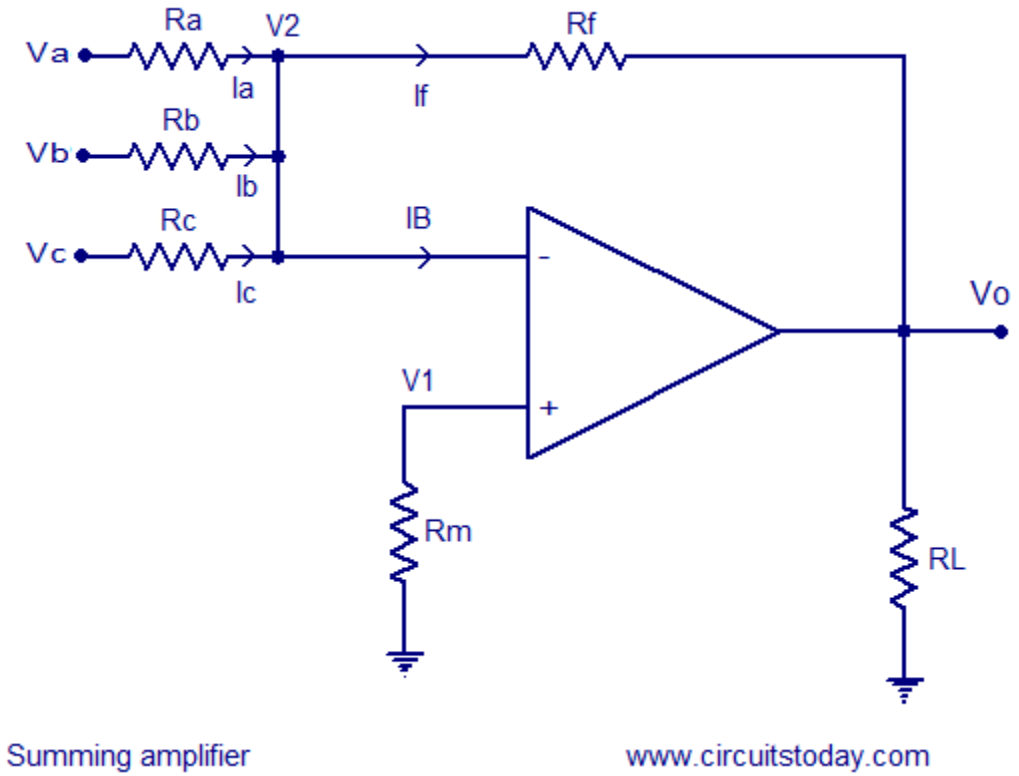
ECE 5/6930 – Reconfigurable Computing
Slides adapted from Design Recipes for FPGAs Using Verilog and VHDL

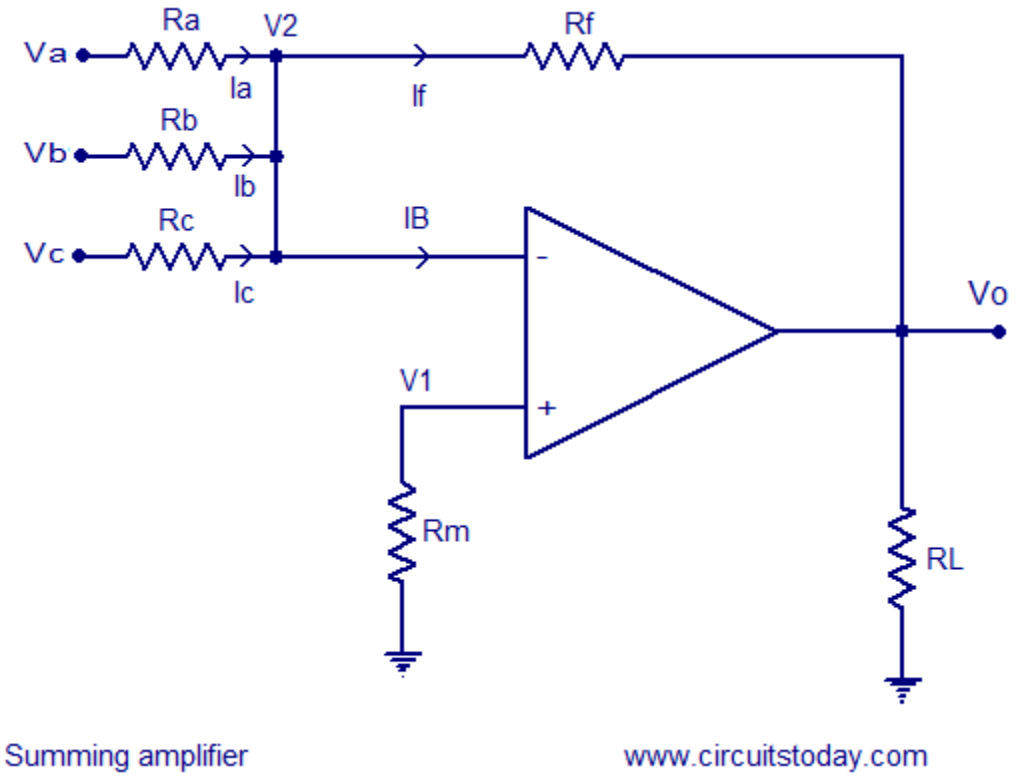
Introduction

- VGA (Video Graphics Array) is a graphics standard for video display controllers
- VGA is an analog interface
- Standard resolutions include
  - 640 x 480 – Most common and the standard we will use for labs
  - 640 x 350
  - 320 x 200
- Entire screen must be repainted at the refresh rate

What does this circuit do?



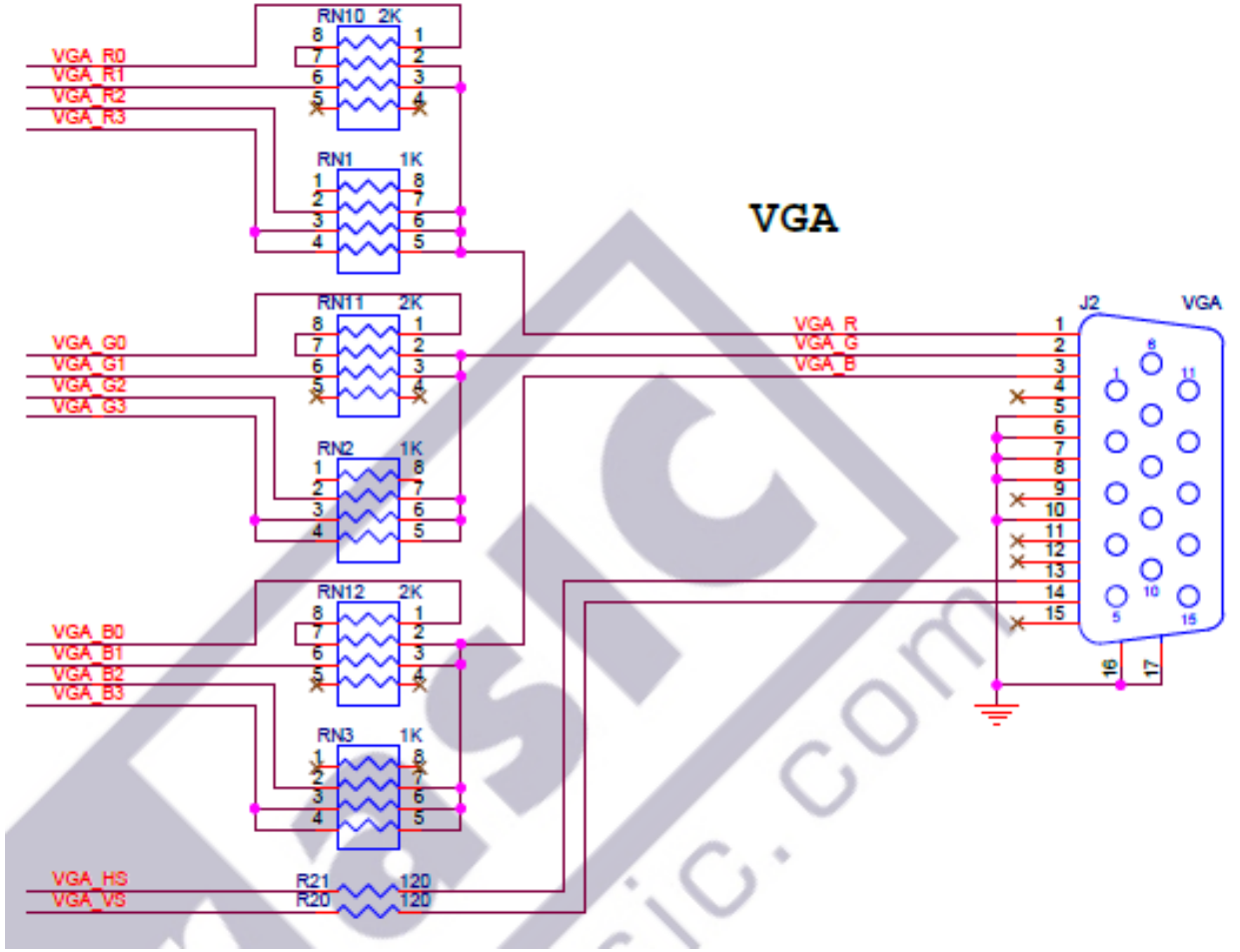
What does this circuit do?



- (Va/Ra) + (Vb/Rb)+ (Vc/Rc) = (V2-Vo)/Rf

DE10-Lite VGA Circuit

- VGA_R
- VGA_G
- VGA_B
- VGA_HS
- VGA_VS



VGA Color Scheme

- VGA is an RGB (Red / Green / Blue) protocol
- Different colors and intensities are created by varying the amount of red, green, and blue
- Each color is represented as a 4-bit value in the FPGA
- Each color is translated into an analog voltage using the weighted resistor array

Example 4-bit RGB Colors

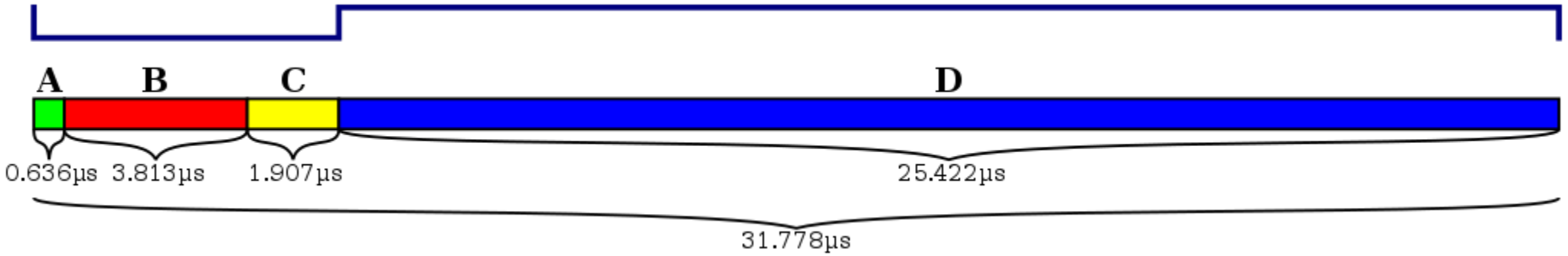
Red	Green	Blue	Output Color
1111	1111	1111	White
1111	0000	0000	Red
1000	0000	0000	Red (less intense)
0000	0000	0000	Black
1111	1111	0000	Yellow
1111	1010	0000	Orange

Specification Standards

- 640 x 480 pixels (480 lines with 640 pixels per line)
- Image display is controlled by two signals
  - Horizontal sync – marks the start and end of each line with a negative pulse
  - Vertical sync – separates each frame with a negative pulse

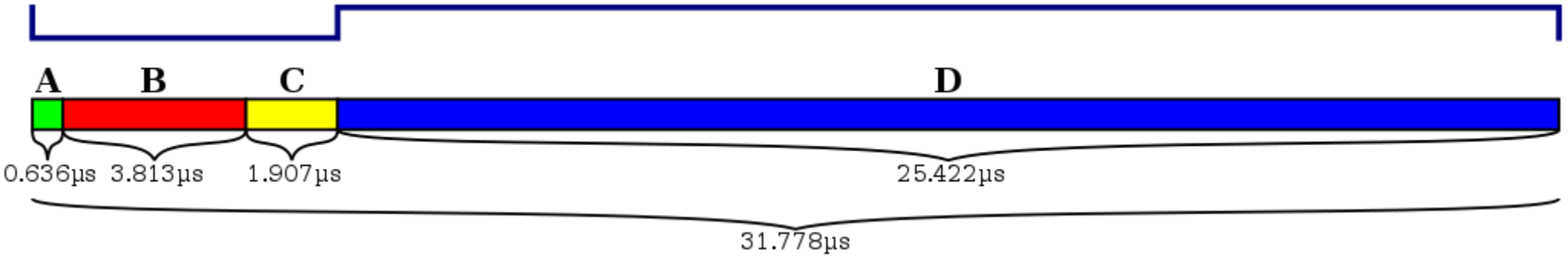
Line Rate Specifications

- Line rate is 31.468 kHz (31.778 µs)
  - i.e. 31.778 µs between horizontal sync pulses
- Actual image data is sent in a 25.422 µs window at the end of the 31.778 µs window
- 640 pixels in 25.422 µs yields 39.722 ns per pixel (i.e. 25.174966 MHz)



Line Rate Specifications

- A = 636 ns (Front Porch) – 16 pixel widths
- B = 3.813 µs (Horizontal Sync Pulse) – 96 pixel widths
- C = 1.907 µs (Back Porch) – 48 pixel widths
- D = 25.422 µs (Pixel Data) – 640 pixel widths



Frame Rate Specifications

- Frame rate is 59.94 Hz (16.683 ms)
  - i.e. 16.683 ms between vertical sync pulses
- Actual frame data is sent in a 15.253 ms window at the end of the 16.683 ms window
- 480 lines in 15.253 ms yields 31.778 µs per line
- There are similar vertical front porch, sync pulse, and back porch timings with durations of 317.78 µs, 63.556 µs, and 1.048 ms, respectively
- 317.78 µs + 63.556 µs + 1.048 ms = 1.43 ms
- 1.43 ms + (31.778 µs * 480) = 16.683 ms per frame
- 16.683 ms / 39.722 ns = 420,000 clock ticks (or pixel widths) per frame

Important Note

- Horizontal lines, including the Line Front Porch, Horizontal Sync, and Back Porch, still occur during the Frame Front Porch, Vertical Sync, and Back Porch. The pixel data during this time must be zeroes.

How to generate a 39.722 ns (25.174966 MHz) Clock

- PLL?

How to generate a 39.722 ns clock

- PLL?
  - Not easy with our 10 MHz and 50 MHz input clocks
  - VGA protocol has some tolerance built in. 25 MHz (40 ns) may be close enough.