**Digital Electronic System**

**EXERCISE : FLIP-FLOP**

**PART A**

1. Explain ONE (1) advantage for flip-flop JK compared to other flip-flop
2. State the function of PRESET, CLEAR and ENABLE inputs for a flip-flop
3. Draw the Circuit and Truth Table for SR flip flop active high
4. For diagram in Figure Q3 below, the flip-flop T is operated in positive trigger. Get the output for Q if Qinitial = 0.



1. Draw the symbol, logic circuit and truth table for flip-flop below:
2. FF SR active low
3. FF SR active high
4. FF SR Clock
5. FF JK Clock
6. Give TWO (2) differences between SR active low and SR active high.
7. Give TWO (2) advantages of FF JK compared to FF SR.
8. Draw symbol FF D using i) FF SR and ii) FF JK.
9. Draw symbol FF T using FF JK.
10. Sketch the output for following diagram

i) Find Q and for timing diagram for FF SR active low below. Assumed Qearly= 0

S

R

Q

ii) Find Q and for timing diagram for FF SR active high below. Assumed Qearly= 0

S

R

Q

iii) Find Q and for timing diagram for FF SR clock below. Assumed Qearly= 0

CLK

S

R

Q

iv) Find Q and for timing diagram for FF JK clock below. Assumed Qearly= 0

CLK

J

K

Q

1. Find Q and for timing diagram for FF D and FF T clock below. Assumed Qearly= 0

CLK

M

Q

**PART B**

1 Define flop-flop and list out 3 of its usage.

2 Sketch SR flip-flop using *NAND* and *NOR* gate. Provide truth table for each circuit

3 State two differences between both flip-flop in question 2.

4 Sketch the output waveform if given the input as the following figure:

Anssume Qinitial = ‘1’.

S

R

Q

Figure (a)

S

R

**Q?**

5 Draw symbol and circuit for clocked SR flip-flop of positive triggered.

6 Define `synchronous input'.

7 State the advantage of clocked SR flip-flop compared to ordinary SR flip-flop.

8 Show differences between positive triggered edge and negative triggered edge using timing diagram from clocked SR flip-flop.

9 Draw symbol and circuit of JK flip-flop.

10 How to do connection so you can build the JK flip-flop if given a clocked SR flip-flop.

11 Sketch output signal of Q from the following timing diagram:-

Clk

J

K

12 Sketch logic symbol of JK flip-flop and completely label the input J, K, preset, clear, clock and output Q dan Q .

13 Using JK flip-flop of positive edge and active low input of preset and clear, sketch the output Q waveform from the given timing diagram below:

Clk

J

K

PRE

CLR

14 Sketch the symbol of D flip-flop and T flip-flop.

15 Explain how JK flip-flop cam be modified into D flip-flop dan T flip-flop.

16 Base on the clock and D input of the following waveform, find the output waveform of Q by assuming the initial condition is SET.

clock

D input

17 Draw the output of the following flip-flop base on given clock and input from figure below:

a) If clock and input given to D flip-flip is positive edge.

b) If clock and input given to D flip-flip is negative edge.

Clock Input