Assignment 10
Priority Encoder

Embedded Logic Design

October 16, 2015

1 Description

Since you successfully installed Xilinx ISE® WebPACK™ Design Software, it is time to test it: Write Verilog HDL code to realize a 3 input priority encoder.

Hint: The priority encoder determines the MSB that is set to 1, from its input ports and ignores any further occurrences of set bits. Therefore the output of the inputs of e.g. 101 and 100 is the same, since the LSB is ignored. If all inputs are cleared, the output of the priority encoder is 0. If the LSB (001) is set, the output is 1.

1. Create a truth table for all possible inputs of your priority encoder.
2. Write your priority encoder using the gate-level model of Verilog.
3. Write your priority encoder using the data-flow model of Verilog.
4. Write your priority encoder using the behavioral model of Verilog.
5. Write one test bench for all 3 implementations and examine/compare the waveforms. Cover useful test cases. Which test cases are useful and why?
6. Implement an 8 input priority encoder on the FPGA using one of the models or a mix of them. As input use the switches, output the LEDs. What are the resource requirements of LUTs, IOBs?

Document your solutions including screenshots containing the waveforms of the priority encoder and resource requirements in terms of LUTs, IOBs and slices using target device Spartan-3E XC3S250E-4CP132 which is the FPGA integrated on your Basys2 board. What do these 3 terms (LUT, IOB and slices) mean? Please note that all outputs of your priority encoder must have a known state.

2 Deliverables

All files must be submitted to `nanu.iiitd.edu.in` via `git` or `subversion`. Late submissions are not evaluated nor will be submissions through `https://www.usebackpack.com` or mail. Your repository has to contain:

- Verilog code of all 3 parts (2, 3, 4)
- Verilog code for the test bench (5)
- The Verilog code that you designed for the FPGA (6)
- Truth table (1)

2.1 Remarks

If you encounter a problem, ask Google, DuckDuckGo, Bing, etc. first. The TAs will not type the question that you have, into the mask in the search engine for you. Required resources, textbooks, etc. are available on the ELD course website of `https://www.usebackpack.com` or in the Internet (datasheets, AVR library documentation, etc.)