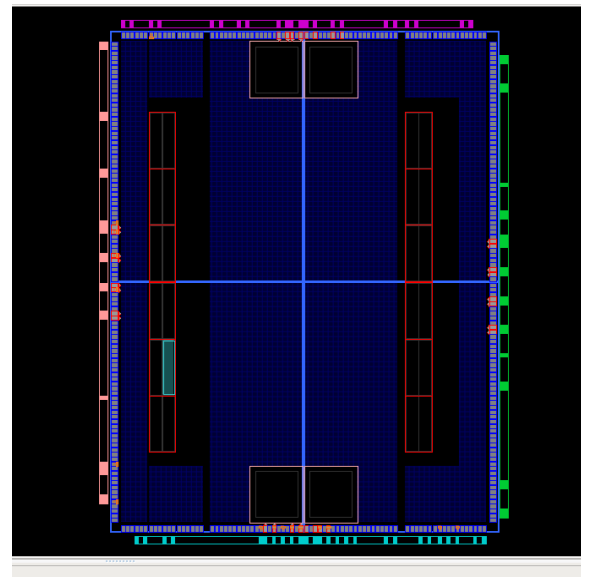
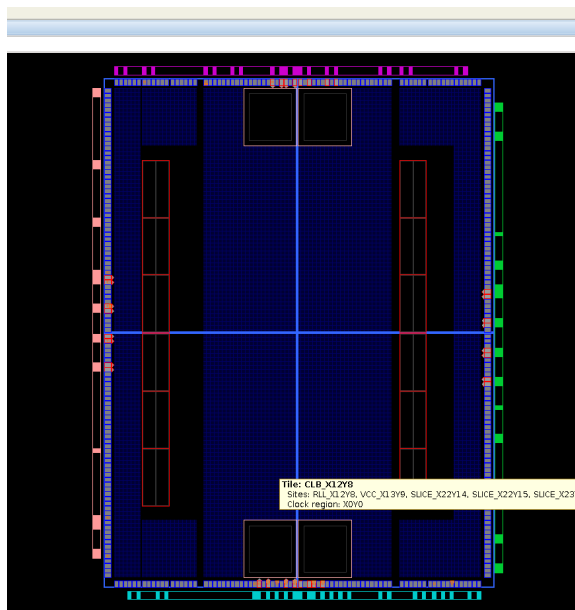


ELD Assignment
Booth Multiplier
Group08

1. How many dedicated multipliers does the FPGA have ?
There are 12 dedicated multipliers in Spartan 3E-250 CP132..
2. Where are they located physically?
They are located along with the RAM Blocks in FPGA.
3. Which one does your design use ?



DESIGN SUMMARIES:

ISE Project Navigator (P20131013) - /home/gursimran/Documents/Xilinx Projects/NEW1/NEW1.xise - [Design Summary (Programming File Generated)]

Booth_Multiplier_1 Project Status (11/06/2015 - 22:28:29)

Project File:	NEW1.xise	Parser Errors:	No Errors
Module Name:	Booth_Multiplier_1	Implementation State:	Programming File Generated
Target Device:	xc3s250e-Scp132	Errors:	No Errors
Product Version:	ISE 14.7	Warnings:	33 Warnings (32 new)
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	
Number of bonded IOBs	19	92	20%	
Average Fanout of Non-Clock Nets	0.00			

Performance Summary

Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:			

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Fri Nov 6 22:28:03 2015	0	1 Warning (0 new)	5 Infos (0 new)
Translation Report	Current	Fri Nov 6 22:28:08 2015	0	0	0
Map Report	Current	Fri Nov 6 22:28:13 2015	0	10 Warnings (10 new)	4 Infos (2 new)
Place and Route Report	Current	Fri Nov 6 22:28:20 2015	0	12 Warnings (12 new)	1 Info (0 new)
Power Report					
Post-PA Static Timing Report	Current	Fri Nov 6 22:28:22 2015	0	0	6 Infos (0 new)

Console

WARNING: PhysisDesignRules:367 - The signal <multiplier<3>_IBUF> is incomplete. The signal does not drive any load pins in the design.

Process "Generate Programming File" completed successfully

ISE Project Navigator (P20131013) - /home/gursimran/Documents/Xilinx Projects/NEW2/NEW2.xise - [Design Summary (Programming File Generated)]

Booth_Multiplier_II Project Status (11/06/2015 - 22:40:02)

Project File:	NEW2.xise	Parser Errors:	No Errors
Module Name:	Booth_Multiplier_II	Implementation State:	Programming File Generated
Target Device:	xc3s250e-Scp132	Errors:	No Errors
Product Version:	ISE 14.7	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	
Number of bonded IOBs	16	92	17%	
Number of MULT18X18SIOs	1	12	8%	
Average Fanout of Non-Clock Nets	2.75			

Performance Summary

Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:			

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Fri Nov 6 22:39:09 2015	0	0	0
Translation Report	Current	Fri Nov 6 22:39:40 2015	0	0	0
Map Report	Current	Fri Nov 6 22:39:46 2015	0	0	2 Infos (0 new)
Place and Route Report	Current	Fri Nov 6 22:39:52 2015	0	0	1 Info (0 new)
Power Report					

Console

Running bitgen...
Command Line: bitgen -intstyle ise -f Booth_Multiplier_II.ut Booth_Multiplier_II.ncd

Process "Generate Programming File" completed successfully

SIMULATIONS:

