

Josh's VNA

Components and Pin Connections:

- Synth:** MAX2871_MOSI, MAX2871_MISO, MAX2871_CLK, MAX2871_LE, MAX2871_CHIP_EN, MAX2871_RFOUT_EN, RF_OUT_PD, RF_OUT_ND, LDD, MAX2871_LD, R1 470R, D1 LED, GND.
- Filter Bank:** RF_IN, RF_OUTD, 3V3, 3V3A, Filter_CTRL1, Filter_CTRL2, filterBank.sch, Insertion Loss: -2 to -3 dB.
- Source Leveling:** RF_IN, RF_OUTD, 100mA, 5V0, 10mA, 3V3A, ATTN_DATA, ATTN_CLK, ATTN_LE, PA_PWRDN, AD8319_RF, RF_PWR_IN, RF_PWR_LEVEL, sourceLevel.sch, Gain: -23 to 10 dB.
- Directional Couplers:** RF_IN, RF_OUTD, Insertion Loss: -1.5 to -3 dB, Reverse_CPLD, Forward_CPLD, couplers.sch.
- Gain Phase Detection:** 3V3A, RF_FWD_CPL, RF_REV_CPL, RF_THROUGH, FRONT_E_CTRL_1, FRONT_E_CTRL_2, gainPhaseDetect.sch.
- Microcontroller:** 3V3, 3V3A, USB_DP, USB_DM, USB_D+, USB_D-, MAX2871_SPL_SCKD, MAX2871_SPL_MOSI, MAX2871_SPL_MISO, MAX2871_LED, MAX2871_CED, MAX2871_RF_END, MAX2871_LD, Filter_CTRL1, Filter_CTRL2, ATTN_DATA, ATTN_CLK, ATTN_LE, PA_PWRDN, INPUT_SW_1D, INPUT_SW_2D, FRONT_E_CTRL_1, FRONT_E_CTRL_2, SDA, SCL, MAX2871_CLK, MAX2871_MOSI, MAX2871_MISO, MAX2871_LE, MAX2871_CHIP_EN, MAX2871_RFOUT_EN, MAX2871_LD, SDADC_AIN4P, SDADC_AIN5P, SDADC_AIN6P, SDADC_AIN7P, SDADC_AIN8P, AD8302_VPHASE, AD8302_VMAG, AD8302_VREF, SWD_IO, SWD_CLK, SWD_nRST, nRST, SDA, SCL, MAX2871_CLK, MAX2871_MOSI, MAX2871_MISO, MAX2871_LED, MAX2871_CED, MAX2871_RF_END, MAX2871_LD, Filter_CTRL1, Filter_CTRL2, ATTN_DATA, ATTN_CLK, ATTN_LE, PA_PWRDN, INPUT_SW_1D, INPUT_SW_2D, FRONT_E_CTRL_1, FRONT_E_CTRL_2, SDA, SCL, MAX2871_CLK, MAX2871_MOSI, MAX2871_MISO, MAX2871_LED, MAX2871_CHIP_EN, MAX2871_RFOUT_EN, MAX2871_LD, SDADC_AIN4P, SDADC_AIN5P, SDADC_AIN6P, SDADC_AIN7P, SDADC_AIN8P, AD8302_VPHASE, AD8302_VMAG, AD8302_VREF, SWD_IO, SWD_CLK, SWD_nRST, nRST.
- Power:** VBUS, 5V0, 3V3, 3V3A, 1V8, power.sch, 5V: 100mA, 3V3A: 200mA, 3V3: 100mA.

Power In / Data

E-Cal / Power Out

SWD Header

Port 1

Port 2

Bill of Materials:

Ref	Value	Part	Quantity
1	100n	C1	1
2	1n	C2	1
3	1n	C3	1
4	100n	C4	1
5	1n	C5	1
6	1n	C6	1
7	470R	R1	1
8	499R	R2	1
9	16R6	R3	1
10	16R6	R4	1
11	16R6	R5	1
12	16R6	R6	1
13	16R6	R7	1
14	16R6	R8	1
15	16R6	R9	1
16	16R6	R10	1
17	16R6	R11	1
18	16R6	R12	1
19	16R6	R13	1
20	16R6	R14	1
21	16R6	R15	1
22	16R6	R16	1
23	16R6	R17	1
24	16R6	R18	1
25	16R6	R19	1
26	16R6	R20	1
27	16R6	R21	1
28	16R6	R22	1
29	16R6	R23	1
30	16R6	R24	1
31	16R6	R25	1
32	16R6	R26	1
33	16R6	R27	1
34	16R6	R28	1
35	16R6	R29	1
36	16R6	R30	1
37	16R6	R31	1
38	16R6	R32	1
39	16R6	R33	1
40	16R6	R34	1
41	16R6	R35	1
42	16R6	R36	1
43	16R6	R37	1
44	16R6	R38	1
45	16R6	R39	1
46	16R6	R40	1
47	16R6	R41	1
48	16R6	R42	1
49	16R6	R43	1
50	16R6	R44	1
51	16R6	R45	1
52	16R6	R46	1
53	16R6	R47	1
54	16R6	R48	1
55	16R6	R49	1
56	16R6	R50	1
57	16R6	R51	1
58	16R6	R52	1
59	16R6	R53	1
60	16R6	R54	1
61	16R6	R55	1
62	16R6	R56	1
63	16R6	R57	1
64	16R6	R58	1
65	16R6	R59	1
66	16R6	R60	1
67	16R6	R61	1
68	16R6	R62	1
69	16R6	R63	1
70	16R6	R64	1
71	1		

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MAX2871 23.5 – 6000 MHz PLL

Clock Ref

RF OUT (single ended)

U3 MAX2871

PLL Loop Filter

RF_OUT_P

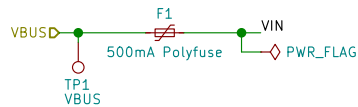
RF_OUT_N

Rev: 0

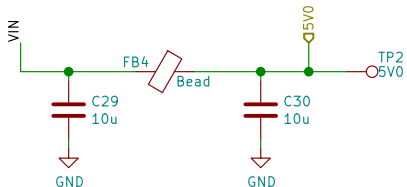
Id: 2/8

Id: 2/8

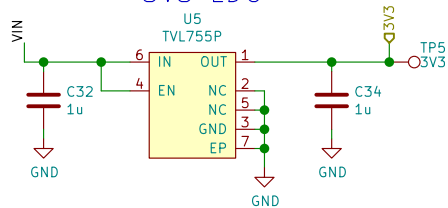
Input Protection



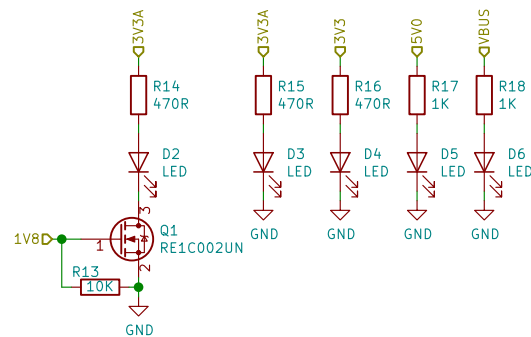
5V (Filtered)



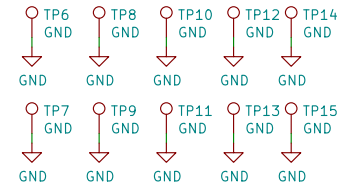
3V3 LDO



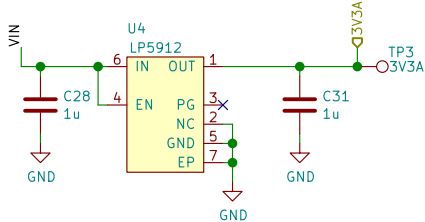
Voltage Rail LEDs



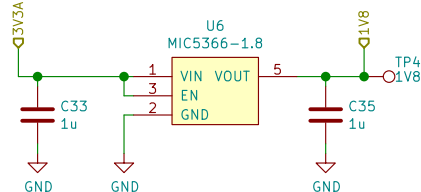
Ground Test Points



3V3A LDO



1V8 LDO



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Sheet: /Power/
File: power.sch

Title: Power

Size: A4 Date: 2019-04-06

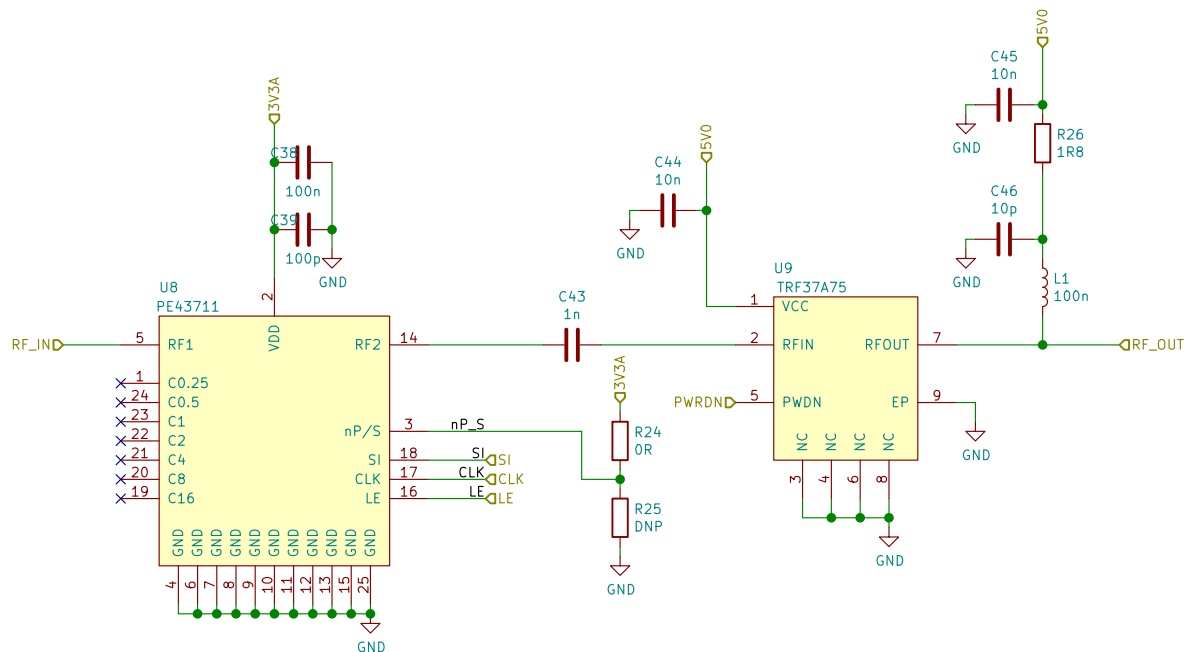
KiCad E.D.A. kicad (5.1.0)-1

Rev: 0

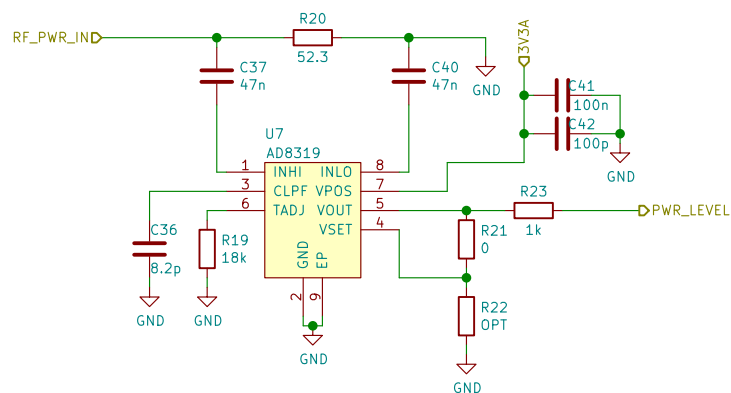
Id: 3/8

Programmable Attenuator

Amplifier
(Gain = 12dB P1dB = +18dBm IP3 = +32.5dBm)



Power Detector



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Sheet: /Source Leveling/

File: sourceLevel.sch

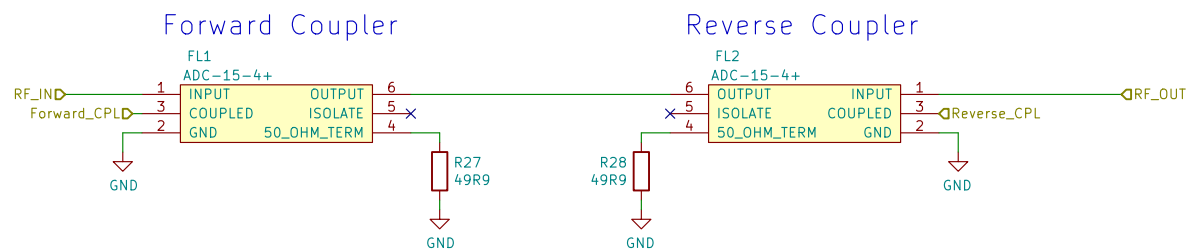
Title: Source Leveling

Size: A4 Date: 2019-04-06

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Rev: 0

Id: 4/8



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Sheet: /Directional Couplers/
File: couplers.sch

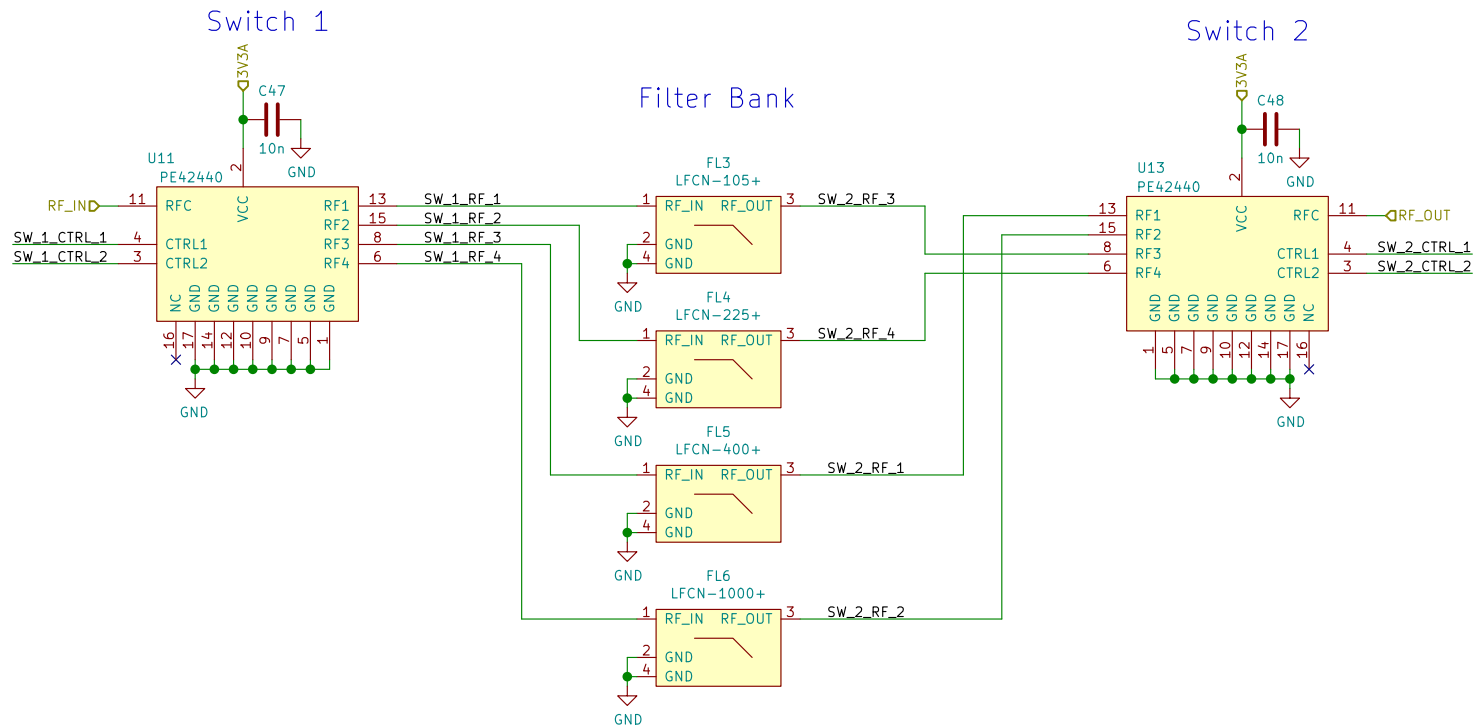
Title: Directional Couplers

Size: A4 Date: 2019-04-06

KiCad E.D.A. kicad (5.1.0)-1

Rev: 0

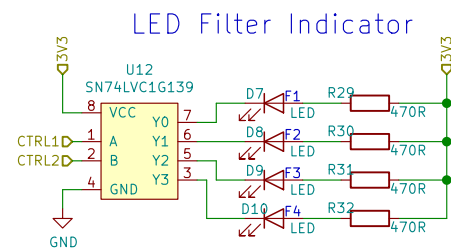
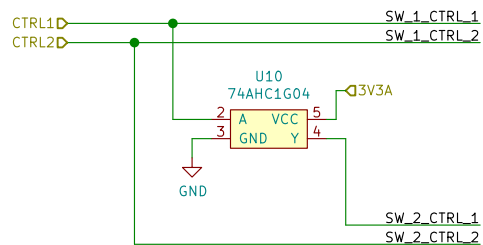
Id: 5/8



Switch Configuration

74AHC1G04 is a not gate, used to allow the below truth tables to be correct with only two control lines following the values in the first table

SW_1	CTRL_1	CTRL_2	SW_2	CTRL_1	CTRL_2
1	0	0	3	1	0
2	0	1	4	1	1
3	1	0	1	0	0
4	1	1	2	0	1



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Sheet: /Filter Bank/
File: filterBank.sch

Title: Filter Bank

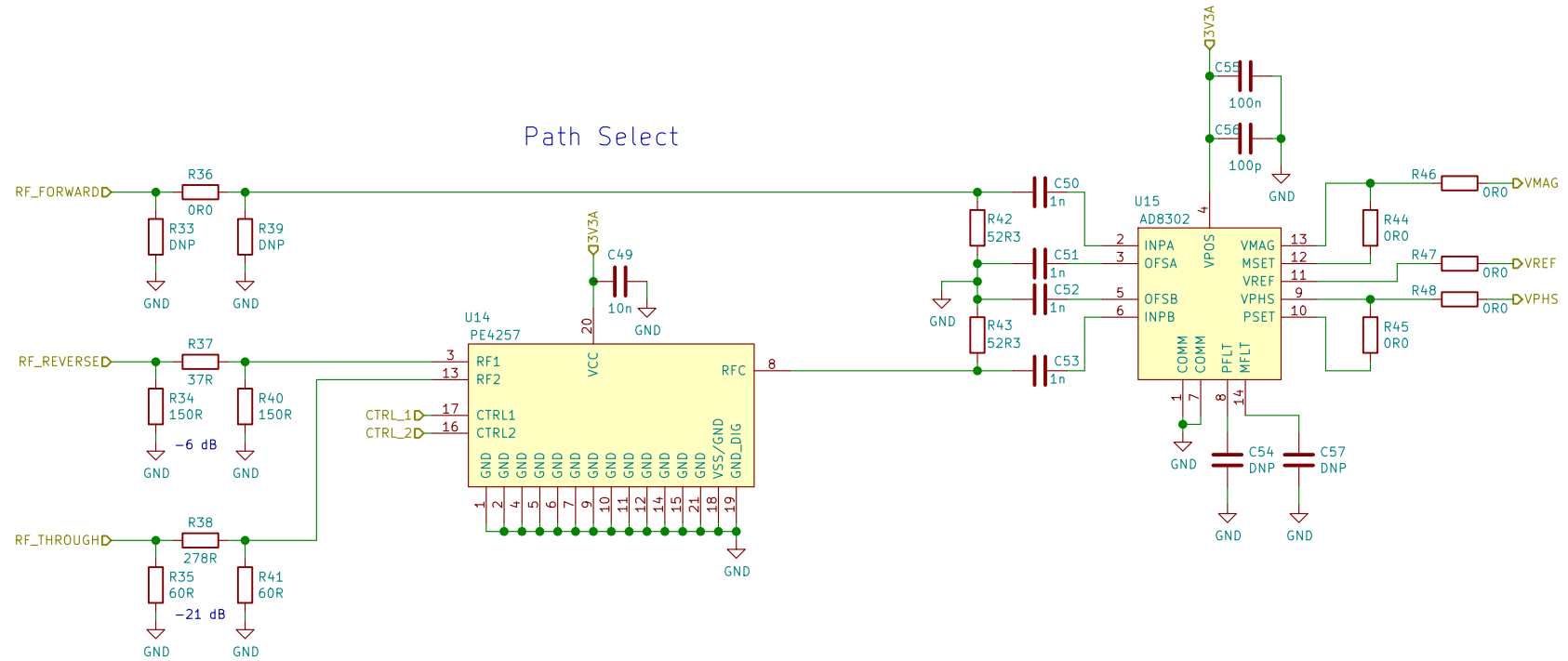
Size: A4 Date: 2019-04-06

KiCad E.D.A. kicad (5.1.0)-1

Rev: 0

Id: 6/8

AD8302 Gain Phase Detector



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Sheet: /Gain Phase Detection/
File: gainPhaseDetect.sch

Title: Gain Phase Detector

Size: A4 Date: 2019-04-06

KiCad E.D.A. kicad (5.1.0)-1

Rev: 0

Id: 7/8

