On-Chip Temperature Sensor with High Tolerance for Process and Temperature Variation

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Abstract — **A reliable temperature sensor circuit that is robust against wafer or chip process and sensing temperature variation is introduced. The circuit includes a reference voltage generator and a constant current bias voltage generator in order to compensate for process and sensing temperature variations. This method eliminates post-production adjustments by circuits such as fuses or non-volatile memory devices. It reduces adjustment test costs and silicon area for these devices, their test control circuits and the interface circuits. Temperature measurement variation of less than 0.6 ˚C by the proposed circuit with a simple low-power structure was verified. The circuit is implemented for a refresh cycle control in 1.5 times of the PAD space on a low-power pseudo-SRAM type DRAM product with a 0.175-µm CMOS bulk process.**

I. INTRODUCTION

Controlling the circuit operations according to with temperature is used in many applications. It is one of the most effective methods to meet severe performance requirement such as low-power dissipation or high-speed operation, because the I-V characteristics of semiconductor devices vary greatly with temperature. When replacing SRAM with DRAM (pseudo-SRAM) for higher density and lower SER (Soft Error Rate), the hidden self-refresh requirement is essential for products. Because the required refresh cycle for DRAM cells strongly depends on the temperature, controlling the DRAM self-refresh cycle is one of the most common uses of temperature sensors (TS) [1], [2], [3], [4]. To detect the chip temperature, an on-chip TS is used. In these examples, tuning or calibration is required to achieve sensing temperature error of less than 2 or 3 ˚C because they use resistors that have large dependencies on process variations. Alternately, there are methods to implement a TS with special devices [5], [6]. However their process costs have been too expensive. With ordinary CMOS process, there are several approaches to implement an on-chip TS. Increasing the temperature gain is one of the commonly used methods to improve the sensitivity of a TS [1], [5], [7], [8]. However these methods require post-production adjustments because the sensing point can be greatly affected by the wafer and chip process variations. Some of other methods use a diode connected MOSFET to implement a TS [9], [10]. However, it is difficult to implement a current source and a resistor that are independent of the process variation with simple circuits. The main goal of this new TS design is to achieve maximum temperature gain with minimum process sensitivity. In addition, the temperature gain of the TS should be independent of the sensing temperature to get a constant response for any sensing temperature. The third goal of the new TS is to achieve above performance with some simple and low-power circuits because the TS is targeted at low-power applications. This paper proposes a new TS with almost no process sensitivity without any adjustments. It also has a large and constant temperature gain for any sensing temperature by compensating for variations of the reference voltage against temperature using the V_{BE} characteristic of a bipolar transistor. A simple and compact low-power implementation is presented along with its evaluation data. Section II describes the proposed TS in comparison with a conventional one. Section III shows the evaluation results for the proposed TS. Section IV concludes the paper.

II. TEMPERATURE SENSOR CIRCUIT

There are several methods to implement a TS on a semiconductor wafer. For low-power applications, the TS

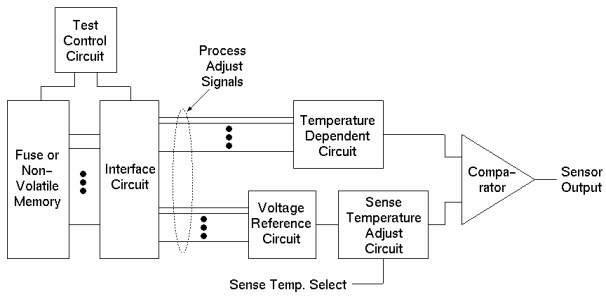

Figure 1. Conventional TS.

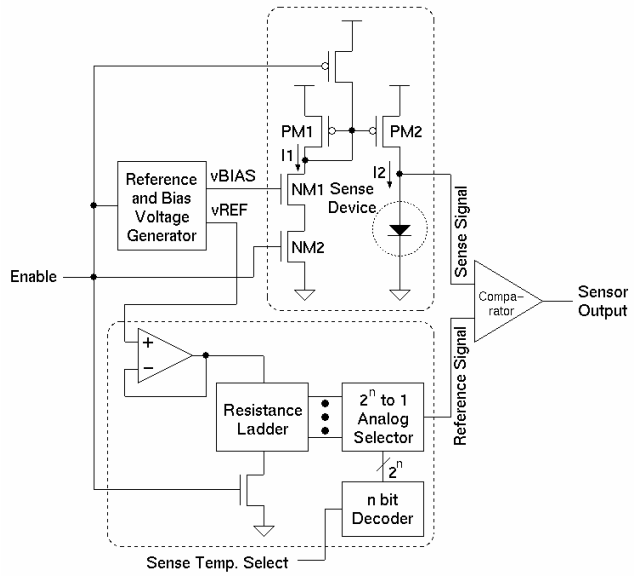

Figure 2. Proposed TS.

should be implemented with a simple scheme such as comparison of reference and sense output. Figure 1 shows one of the conventional TS circuits [11]. This TS includes a voltage reference circuit, a temperature dependent circuit and comparator. The voltage reference circuit and temperature dependent circuit require some process adjustment signals to compensate for process and temperature variations. To set signals, the TS needs an adjustment test and a fuse or memory setting using the three circuit blocks on the left side of the figure. These are fairly large blocks of circuitry, which is a drawback for mass production. Figure 2 shows the proposed TS circuit. In this circuit, the vREF is a reference voltage that is independent of temperature. The vBIAS is the gate bias voltage which generates the temperature-independent drain-source current I1 at the MOSFET NM1. Thus the current I2 is also independent of the

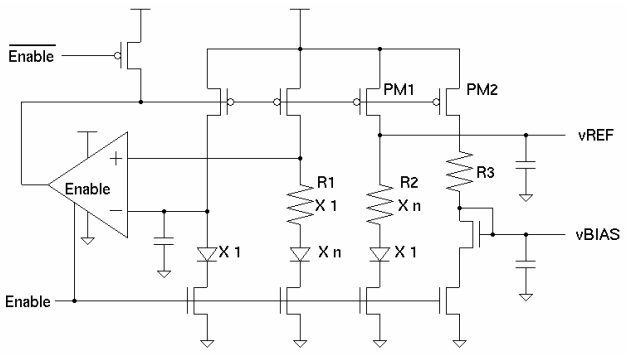

Figure 3. Reference and bias voltage generator.

temperature because current I1 is mirrored to current I2with the large current mirror circuit consisting of PM1 and PM2. The sensing device of p-n junction diode is implemented with a PNP bipolar transistor with its base and collector nodes are connected to GND. Its emitter node named Sense Signal is connected to the drain of PM2. The Reference Signal is generated by dividing the vREF signal with resistance ladder block. This circuit does not require accuracy for the absolute resistance values because it uses only the ratio of the resistances. The Sensor Output is given by comparing the Sense Signal and the Reference Signal using the comparator. The Sense Temp. Select input sets the target sensing temperature. Both the signals of vBIAS and vREF are generated in the reference and bias voltage generator. These signals are generated in the same circuit so that they can be equally affected by process and temperature variations. Figure 3 shows the reference and bias voltage generator. A bandgap voltage reference for the low voltage power supply was adopted to generate the vREF signal. Since this voltage reference is used for many other purposes, the TS requires only a small additional part, just one current path. The additional current path through PM2 and resistance R3 is implemented to generate the vBIAS signal. The vBIAS provides the nMOSFET gate bias voltage for a constant current. Since the same differential amplifier controls the gates of PM1 and PM2, vBIAS tracks the vREF variation quite well. In addition, the circuits in Figure 2 and Figure 3 are not affected by variations of the power supply voltage because the current in all paths is determined by the nMOSFETs. The Enable signals in Figures 2 and 3 are used to enable or to disable the TS operation for low-power operation.

III. EVALUATION

Table I shows simulation results. In this table, the voltage levels of vREF, vBIAS, Sense Signal, Reference Signal and the difference between Sense Signal and Reference Signal for typical and extreme process corners are listed. The left character in the Process column shows the speed of nMOSFET while the right one shows that of pMOSFET. The characters T, S and F indicate typical, slow and fast, respectively. In this evaluation, the temperature to be sensed was set to 45 °C. These results show how the levels of vREF and Reference Signal vary depending on both process and temperature. However, the level of vBIAS compensates for these variations because vBIAS and vREF are generated in the same reference and bias voltage generator circuit. As a result, the level of Sense Signal generated by vBIAS has same value with that of Reference Signal between 40 and 50 °C.

TABLE I. TS PERFORMANCE

VDD = 1.65 (V) Process : nMOSFET pMOSFET, T: typical, S: Slow, F: Fast

Process	Temp.	vREF (V)	vBIAS (V)	Sen. Signal (V)	Ref. Signal (V)	Diff (mV)	Error (deg C)
TT	−10	1.1626	0.9904	0.77259	0.68570	86.89	−0.2256152
	40	1.1495	1.0102	0.68612	0.67798	8.14	
	50	1.1466	1.0143	0.66735	0.67626	−8.91	
	70	1.1407	1.0227	0.63241	0.67278	−40.37	
	85	1.1365	1.0292	0.60562	0.67031	−64.69	
SS	−10	1.1632	1.0730	0.77224	0.68606	86.18	−0.6034224
	40	1.1498	1.0956	0.68516	0.67815	7.01	
	50	1.1469	1.1003	0.66751	0.67644	−8.93	
	70	1.1410	1.1099	0.63200	0.67296	−40.96	
	85	1.1367	1.1172	0.60518	0.67043	−65.25	
FF	−10	1.1624	0.9075	0.77293	0.68558	87.35	0.0803976
	40	1.1493	0.9244	0.68595	0.67786	8.09	
	50	1.1464	0.9279	0.66831	0.67615	−7.84	
	70	1.1405	0.9351	0.63284	0.67267	−39.83	
	85	1.1363	0.9407	0.60606	0.67019	−64.13	
SF	−10	1.1624	1.0620	0.77254	0.68558	86.96	−0.2227826
	40	1.1493	1.0824	0.68550	0.67786	7.64	
	50	1.1465	1.0866	0.66785	0.67621	−8.36	
	70	1.1406	1.0953	0.63235	0.67273	−40.38	
	85	1.1363	1.1020	0.60555	0.67019	−64.64	
FS	−10	1.1631	0.9194	0.77264	0.68600	86.64	−0.274866
	40	1.1497	0.9387	0.68562	0.67809	7.53	
	50	1.1468	0.9426	0.66798	0.67638	−8.40	
	70	1.1409	0.9508	0.63248	0.67290	−40.42	
	85	1.1367	0.9570	0.60569	0.67043	−64.74	

The Diff column shows the differences between Sen. Signal and Ref. Signal. The levels of Diff at 40 ˚C and 50 ˚C are from 7 mV to 9 mV for all process cases. The final column, Error shows the temperature error between the temperature when this TS flips and the target temperature of 45 (C. From this result, the maximum temperature error is about 0.6 (C for all process cases. Figure 4 shows the relationship between temperature and the Diff value. The graphs for all process cases are on almost the same straight line. This shows the sensitivity of this TS is constant and independent of the target temperature regardless of the process variations. These results show the proposed TS is able to sense temperature without any adjustment for process or sensing temperature variations. The TS was implemented in the temperature-dependent

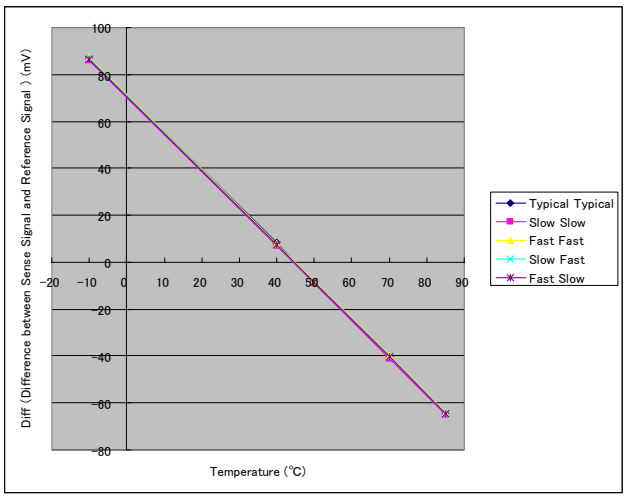

Figure 4. Difference between sense signal and reference signal vs temperarure.

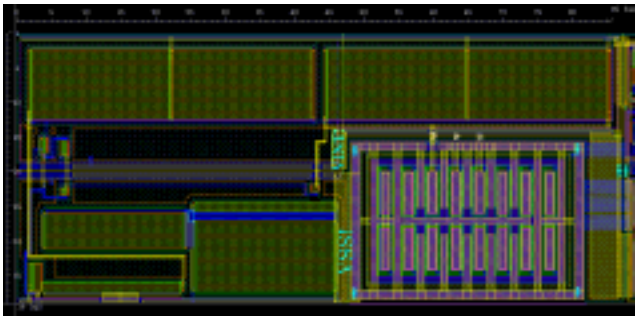

Figure 5. Layout of the proposed TS circuit except comparator.

refresh timer of a low-power DRAM product. Figure 5 shows the layout of the proposed TS circuit of Figure 2 except the comparator. The p-n diode sense device consisting of a PNP bipolar transistor is placed in the right lower corner. Only the central device surrounded by dummy transistors is used to minimize the effect of process variation. To avoid process variation effects, large devices on the top row and lower middle portions are placed for NM1, NM2, PM1 and PM2. Figure 6 shows the layout of the comparator in the proposed TS. This is a differential amplifier with the devices placed symmetrically. This circuit is placed far away from the noisy blocks to avoid malfunction. Figure 7 shows the layout of the reference and bias voltage generator of Figure 3, which includes the additional current path. As ordinary reference voltage generator is used in the DRAM circuit, so the proposed TS requires only the "Additional Circuit for vBIAS Generation" block surrounded by the white outline. The p-n diode devices with the same shapes are implemented in the upper middle area on this figure, and are used in the TS circuit in Figure 5 to realize better process matching between these two circuits. The total space for the proposed TS is about 4,580 μm^2 , which is only about 1.5 times of a PAD area. Figure 8 shows a microphoto of the TS on the DRAM chip. The measured results match the simulations quite well. The total DC current for this TS is less than 1 μA.

IV. CONCLUSION

We have described a structurally simple temperature sensor with high tolerance for process and sensing temperature variation. The circuit compensates for these variations by generating reference and bias voltages in the same circuit. It can achieve less than 0.6 ˚C temperature error without any post-production adjustment. As a result, it eliminates additional circuits and test for post-production adjustments. It was

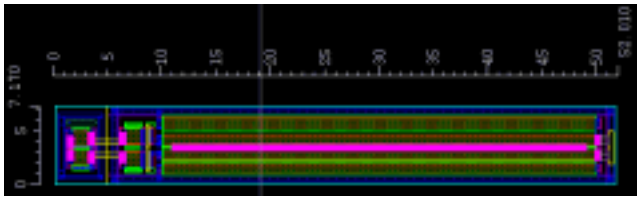

Figure 6. Layout of the comparator in the proposed TS circuit.

implemented for a refresh timer cycle control in a small area on a low-power DRAM chip. The refresh timer was controlled successfully depend on the temperature. Implementing multiple TSs with different target sensing temperatures enable more complicated temperature control. The total DC current is less than 1 μA. This method can be applied to various low-power and low-cost applications.

ACKNOWLEDGMENT

The author wishes to thank T. Sunaga and K. Hosokawa for their useful suggestions. He also thanks all of the members of low-power DRAM project in which this temperature sensor circuit was implemented.

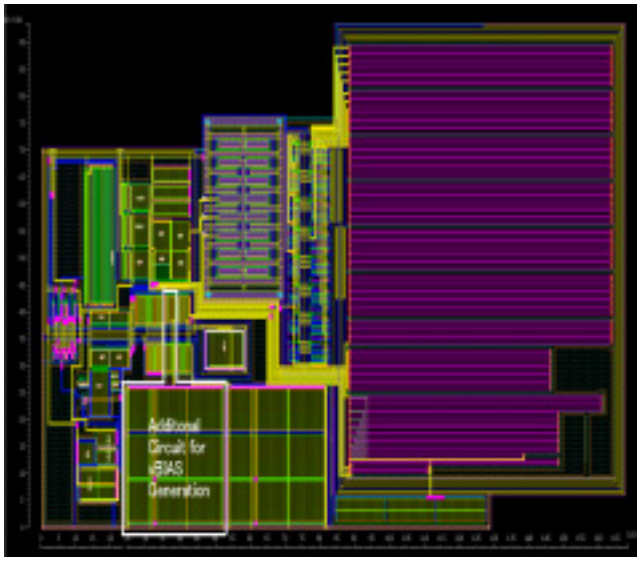

Figure 7. Layout of the reference and bias voltage generator and additional circuit for vBIAS generation.

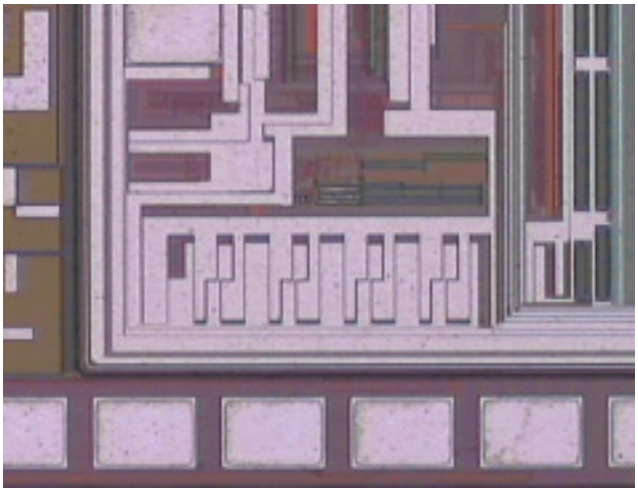

Figure 8. TS microphoto.

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