Reliability Implications of Bias-Temperature Instability in Digital ICs

Sang Phill Park
Purdue University

Kaushik Roy
Purdue University

Kunhyuk Kang
Intel

Editor's note:
Bias temperature instability (BTI) is one of the major reliability challenges in nanoscale CMOS technology. This article investigates the severity of such degradation in logic and memory circuits. The simulation results reveal that BTI poses severe constraints on reliable memory design, especially in the presence of random process variations.

—Yu Cao, Arizona State University

Successful design of digital ICs has often relied on complicated optimization among various design specifications such as silicon area, speed, testability, design effort, and power dissipation. Such traditional design approaches inherently assume that transistors' electrical and physical properties are deterministic, and hence predictable over the device's lifetime. However, with silicon technology shrinking below 100 nm, transistors no longer act deterministically over time. One of the most important phenomena causing such a change is the temporal reliability degradation in MOSFETs due to bias-temperature instability.[1]

Negative bias-temperature instability (NBTI) is a PMOS-specific transistor-aging effect that increases a device's threshold voltage V_{TH} and reduces the carrier mobility μ as a function of time and stress condition. Experimental analysis has shown that NBTI can result from continuous trap generation in a transistor's Si-SiO_2 interface.[1-4] These traps usually originate from Si-H bonds generated after the hydrogen passivation process to remove dangling silicon atoms at the Si-SiO_2 interface. However, under stressed operating conditions (that is, the *on* state, with negative gate bias under elevated temperatures for PMOS), these bonds can easily break with time and generate positive interfacial traps (a donor-like state), which increase V_{TH}. The device reliability community has been aware of the NBTI process for decades; however, NBTI has recently gained more attention, largely because of the wide use of ultrathin oxide devices. Specifically, the *International Technology Road Map for Semiconductors* (*ITRS*) projects oxide thicknesses of less than 10 angstroms for technology nodes below 32 nm. These thin oxides will substantially increase the vertical oxide field (E_{ox}) to the range of a few megavolts per centimeter, which in turn can result in more severe NBTI degradations and a corresponding V_{TH} increase.[1] Heavily nitrided oxides (mainly employed to alleviate gate leakages) can further expedite the degradation process.[2]

Aggressive scaling of transistor dimensions can also lead to statistical variation of NBTI-induced degradation. Similar to the well-known random dopant fluctuation (RDF) effect, very-short-channel devices have relatively few Si-H bonds, ranging from tens to hundreds of pairs, depending on the specific technology. Because of the finite number of Si-H bonds, breaking and repassivation of Si-H bonds can experience a significant statistical fluctuation during the degradation process.[5] Such statistical variation of the NBTI process results in an additional random variation of V_{TH} on top of the nominal degradation (that is, static NBTI) and must be considered during the performance analysis of digital circuits. Unlike the random variations

0740-7475/09/$26.00 © 2009 IEEE Copublished by the IEEE CS and the IEEE CASS

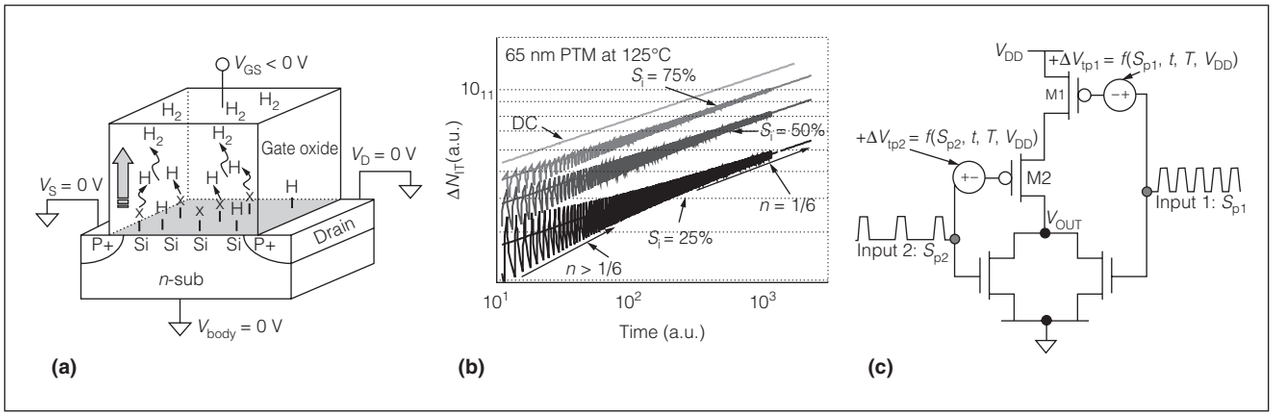

Figure 1. Negative bias-temperature instability (NBTI) degradation process in a PMOS transistor based on the reaction diffusion (RD) model (a), NBTI degradation under DC and AC stress with various signal probabilities (b), and circuit simulation model for NBTI degradation in a two-input NOR gate (c). (a.u.: arbitrary unit.)

due to RDF, NBTI-induced V_{TH} variations depend on the operating temperature and the effective stress period that a particular transistor experiences. Hence, an effective compact circuit-level V_{TH} model that considers such NBTI variation is necessary.

In this article, we examine NBTI-induced performance degradation in two major circuit applications: random logic and memory arrays. We also extensively analyze the impact of statistical variation of NBTI in advanced-technology nodes. Our study provides a comprehensive understanding of NBTI degradation in circuits and draws a general design guideline for NBTI-tolerant logic and memory design. We introduce an analytical NBTI model based on the reaction diffusion (RD) framework to determine performance degradation in a single transistor.[3,4] We show how to adapt this single-device-level model to a higher-level simulation model for circuit-level estimation. We then apply this model to evaluate the impact of NBTI degradation on both logic and memory circuits.

Simulation results obtained from several ISCAS 1985 benchmark circuits designed in a 65-nm predictive technology model (PTM) (http://www.eas.asu.edu/~ptm) show that NBTI's impact in random-logic circuits is minimal compared to single-device-level degradation. Moreover, considering the relative magnitude of degradation in random logic, we show that simple delay guard-banding at the initial design phase can easily undermine the effectiveness of complex reliability-aware design techniques such as gate sizing and logic synthesis.[6,7] However, for memory arrays, mismatches among transistors are the critical source of stability problems. Hence, the effect of NBTI is more detrimental. As a result, memory arrays require more sophisticated circuit design techniques to minimize the impact of NBTI over their lifetime. Finally, using a statistical V_{TH} model, we show that the impact of random NBTI variations on top of nominal degradation can reduce a circuit's lifetime, so this should be considered during the initial design phase in advanced-technology nodes.

Compact circuit simulation models

Here, we review the temporal V_{TH} model under NBTI degradation using the RD framework.[3,4] Then we show how Spice-level simulations adopt the basic V_{TH} models.

Temporal RD-framework-based V_{TH} model

NBTI causes a temporal increase in V_{TH} because of the generation of traps at the Si-SiO_2 interface. In the past few decades, numerous experiments have empirically shown that the increase in V_{TH} due to NBTI under constant DC stress closely follows a power law with respect to time t, with a fixed exponent n (that is, $V_{TH} \sim t^n$).[1-4] Time exponent n represents the experimental dependency of the degradation process. On-the-fly measurement has indicated a value of n close to 1/6,[2] whereas $n \sim 1/4$ for measurements with delay.[3,4]

One of the most promising physical models to explain this phenomena is the RD framework (there are also models based on hole-trapping dynamics). The RD-based model interprets the degradation process as a consequence of the interaction of inversion layer holes with hydrogen-passivated silicon atoms, as Figure 1a shows. Under negative gate bias, cold

holes from the inversion layer can break the Si-H bonds, creating interface traps (in a donor-like state) and neutral H atoms. The latter can form H_2 molecules, which can diffuse away from the interface (through the oxide) or can anneal existing traps. Generated interface traps increase the device V_{TH} as follows:

$$\Delta V_{TH}(t) \simeq \frac{qN_{IT}(t)}{C_{ox}} \simeq f_{AC}(S_p)K_{DC}t^n \quad (1)$$

where N_{IT} is the density of the interfacial trap, C_{ox} is the oxide capacitance, and q is the charge of an electron. K_{DC} is a technology-dependent constant that depends on the temperature, V_{DD}, the device geometry, the oxide nitrogen concentration, and other factors.[2-4] Function f_{AC} represents the AC dependency of the process.

In reality, transistors are seldom applied with a constant DC stress. Rather, they experience a series of AC stresses with varying signal probabilities, S_p. Here, S_p is the fraction of time when the PMOS is negatively biased. During negative bias, PMOS experiences a constant degradation process. However, when the stress is removed (the *off* condition), a reverse annealing process occurs and recovers the device toward the original V_{TH}. Experiments have shown that NBTI degradation under AC stresses are independent or weakly dependent on operating frequency.[2-4] Various groups have also shown that AC degradation has a similar time exponent ($n \sim 1/6$) as DC degradation. However, the absolute magnitude of degradation is scaled down by a constant factor, which Equation 1 represents by a signal-probability-dependent function, f_{AC}. We can compute this AC dependency function using the same RD framework. Kumar, Kim, and Sapatnekar proposed an example of a circuit-simulation-compatible AC NBTI model.[8] Figure 1b depicts NBTI degradation for AC stress with different signal probabilities. Owing to the recovery process, AC degradation is significantly lower than DC degradation.

NBTI circuit simulation model

Various circuit-compatible simulations have adopted RD-based V_{TH} models.[6,8] Most of these models are based on a compact form of Equation 1 for circuit-level simulations. Figure 1c shows a simple example of a two-input NOR gate. For the given bias condition V_{DD}, operating time t, stress temperature T, and signal probability S_p, V_{TH} degradation in each PMOS transistor is calibrated (using Equation 1) and applied to the gate input as a voltage source. (Given this setup, we could apply any type of circuit simulation to obtain worst-case frequency and power dissipation).

This simple approach can be applied to any existing CAD tools (Spice, static timing analysis, and so on) with minimum effort while ensuring sufficient accuracy.[6-8] However, this approach also has some limitations. Because V_{TH} degradation depends on the signal probability (see Figure 1b), the latter can largely affect the overall accuracy. In reality, an accurate estimation of signal probability is a difficult problem, so a certain amount of guard-banding is necessary to ensure correct functionality using this approach.

NBTI in random-logic circuits

Using the RD-based compact NBTI model just proposed, we estimate performance degradation in random-logic circuits under NBTI. We then discuss the effectiveness of present reliability-aware design techniques and compare them with a simple delay guard-banding approach.

Performance degradation

The impact of NBTI on random-logic circuits is most evident in its delay degradation. Increased V_{TH} reduces the drive current and thus increases individual-gate delays. To estimate the delay degradation in logic circuits, we first characterize a standard cell library considering NBTI degradation. We then represent each cell's delay in terms of input signal probability, temperature T, and operation time t as follows:

$$\text{Delay} = f_D(S_{pi}, \ldots, S_{pn}, t, T) \quad (2)$$

where S_{pi} represents the signal probability at the ith input.

Once we obtain the cell library, we can compute the delay degradation in circuits using standard static timing analysis (STA) tools. Figure 2a shows the simulation results obtained using STA and an NBTI-aware standard cell library. We performed simulations at three different temperature stresses—25°C, 75°C, and 125°C—on a set of ISCAS 1985 benchmark circuits synthesized using a 65-nm PTM. We assumed that the signal probability at the primary input was 0.5 and that it was properly propagated to every node inside the circuit. For each simulation, we compared the average percentage degradation in maximum operating frequency (f_{max}) of the nine different benchmark

circuits to its initial value (at $t = 0$) from 1 second to three years ($\sim 10^8$ seconds). As Figure 2 shows, depending on the stress temperature, NBTI can result in f_{max} degradation of up to 8.8% in three years (at 125°C). However, as the operating temperature decreases to 25°C, the degradation process significantly slows down and results in only a 3.3% reduction of f_{max}. This result suggests that for a realistic estimation of long-term degradation, it's essential to consider the expected temperature profile for the entire lifetime of the device. Simply applying a constant high temperature might be too pessimistic in most cases.

The simulation results also show that, compared to single-device-level degradation, overall performance degradation in large circuits is relatively small, for the following reasons:

- NBTI mainly affects the rising transition of CMOS gates. Hence, in normal timing paths, where rising and falling transitions occur consecutively, the impact of NBTI decreases by almost half.
- Different gates have different sensitivities with respect to NBTI. NOR-type gates with stacked PMOS networks experience more degradation, because multiple transistors in the stack simultaneously affect the transition.
- Because of a wide variation of signal probability at different nodes, the overall effect of NBTI is minimal, considering a realistic AC input pattern.

Figure 2a also shows that the degradation of f_{max} retains a power relation with respect to time (with a fixed exponent of 1/6), which is identical to the single-device degradation indicated in Equation 1. This power relation is unique to NBTI-induced performance degradation, and it has been analytically shown and experimentally validated.[6]

Reliability-aware circuit design

Because NBTI can slow down a circuit throughout its lifetime and possibly result in a timing failure, various design techniques have been proposed to handle this problem.[6,7] To compare the effectiveness of these design techniques, we implemented both our sizing technique[6] and the synthesis method proposed by Kumar, Kim, and Sapatnekar[7] for ISCAS benchmark circuits in a 65-nm PTM node. We targeted a lifetime of three years at 125°C and 75°C, with random AC stress ($S_p = 0.5$) applied at the primary inputs. Table 1 summarizes the simulation results. We

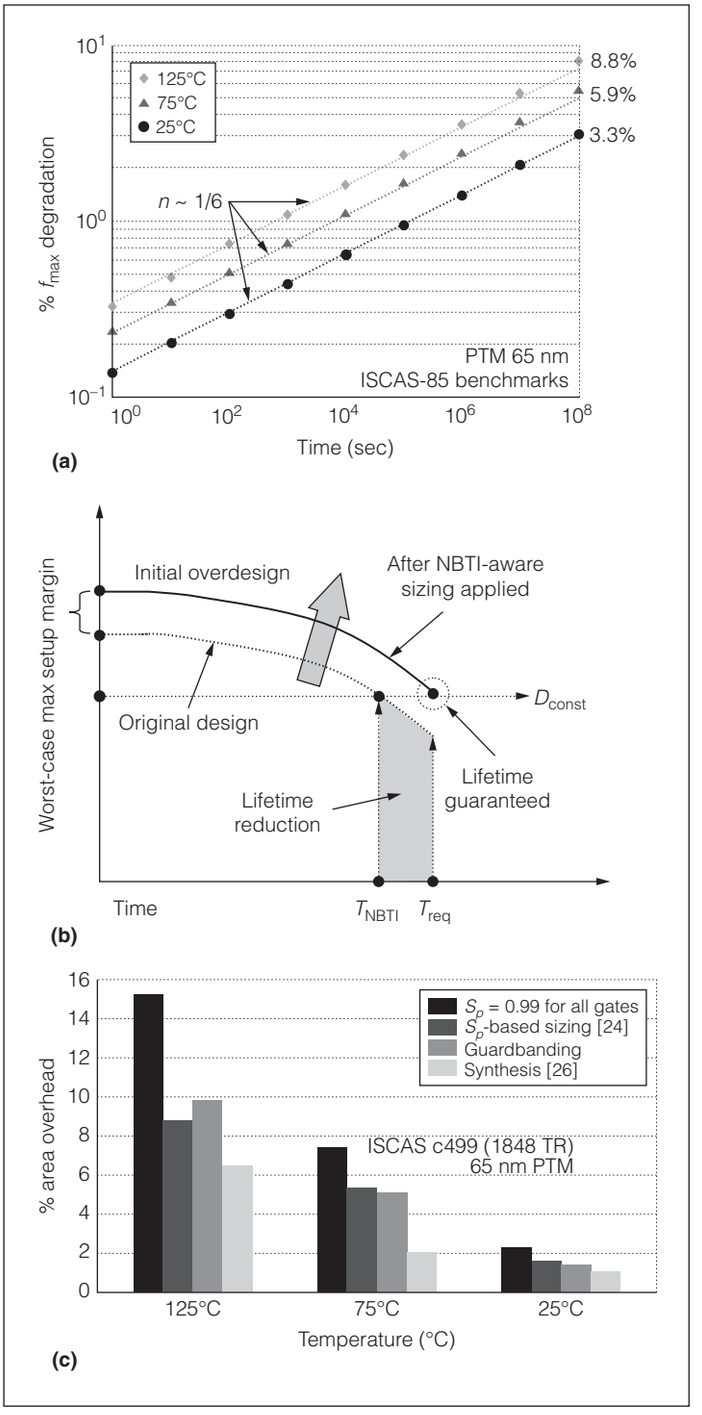

Figure 2. Average maximum operating frequency (f_{max}) degradation in ISCAS 1985 benchmark circuits at different temperatures (a), reliability-aware gate sizing to guarantee the duration of time the circuit is required to operate (T_{req}) for the entire lifetime of the circuit (b), and comparison between different reliability-aware design techniques and simple guardbanding (c). (D_{const}: delay constraint.)

Table 1. Area overhead of reliability-aware sizing, synthesis, and guard-banding.

Circuit	No. of gates	Nominal design (μm)	Area overhead (%) at 125°C				Area overhead (%) at 75°C			
			WC sizing	Opt sizing	Guard-banding	Synthesis	WC sizing	Opt sizing	Guard-banding	Synthesis
c432	184	225.7	8.59	6.13	7.98	4.25	5.35	4.03	4.57	1.14
c1908	466	537.2	13.79	9.17	10.21	10.38	7.62	5.72	5.70	4.40
c499	534	567.7	15.25	8.75	9.81	6.45	7.39	5.34	5.04	2.02
c2670	686	801.5	7.16	5.33	5.55	5.01	5.07	2.26	2.45	2.54
c3540	1,134	1,392.7	6.36	3.41	4.27	0.40	2.85	1.98	1.92	0.20
Average			10.23	6.56	7.56	5.30	5.66	3.87	3.94	2.06

* Opt: optimal; WC: worst case.

implemented the sizing algorithm in two different versions. The WC-sizing method represents the worst-case sizing results, assuming all nodes in the circuits degrade on the basis of signal probabilities of 0.01. For optimal (Opt) sizing, we obtained a realistic estimate of signal probability at each node from Monte-Carlo simulations and applied them during sizing. As Table 1 shows, the Opt-sizing approach reduces area overhead considerably.

To better understand the effectiveness of the sizing and synthesis techniques, we also designed circuits using a simple guard-banding method. During initial sizing, we tightened the delay constraints with a fixed amount of delay guard-banding. We selected the guardband as the average delay degradations in these circuits for three years. The simulations discussed earlier predicted these values to be 8.8% and 5.9% at 125°C and 75°C, respectively (Figure 2a). Table 1 shows sizing results using guard-banding. Figure 2c shows typical results obtained from example circuit c499. Interestingly, these results do not show much of a difference compared to optimal sizing (1% at 125°C) or the synthesis method (2.06% at 125°C). Possible reasons for this negligible difference include the following:

- Although guard-banding ignores the sensitivity of individual gates with respect to NBTI, delay degradation weakly depends on how the circuits were originally designed. With a well-selected delay constraint, guard-banding indeed produced comparable results.
- The synthesis method shows slightly better results, mainly because the NBTI-aware synthesis algorithm uses logic gates that are less sensitive to NBTI degradations.
- For many noncritical paths, even after the worst-case NBTI degradation, the path still maintains a sufficient margin. Such paths do not affect sizing. Even at the minimum size, these paths have enough timing margins to avoid failures after NBTI degradation.

Also, as the operating temperature drops to 75°C, the difference between guard-banding and the other methods becomes less noticeable.

These results show that simple guard-banding can be as effective as other existing computationally complex techniques to alleviate NBTI issues in random-logic circuits. Nevertheless, there are still extreme situations, such as a very high operating temperature, very high signal probability, and many near-critical paths, that require a more aggressive design.

Reliability analysis of 6T SRAMs

Here, we explore the impact of NBTI on six-transistor (6T) SRAM-type memory arrays. Figure 3a shows the schematic of a basic 6T SRAM cell. In contrast to the logic circuits, parametric failures in memory arrays due to local mismatches among six transistors in a cell can lead to failures. As a result, NBTI degradation, which affects only PMOS transistors [PL and PR (left and right pull-up PMOS transistors) in Figure 3a], can significantly impact SRAM parametric failures. For example, Kang et al. reported that NBTI-induced V_{TH} degradation can severely damage an SRAM cell's read stability (although write properties slightly improved).[6] Simulation results obtained for a constant AC stress at high temperatures (110°C and 125°C) show that the static noise margin (SNM) of an SRAM cell can decrease by more than 9% in three years. Figure 3b summarizes the results. Although these

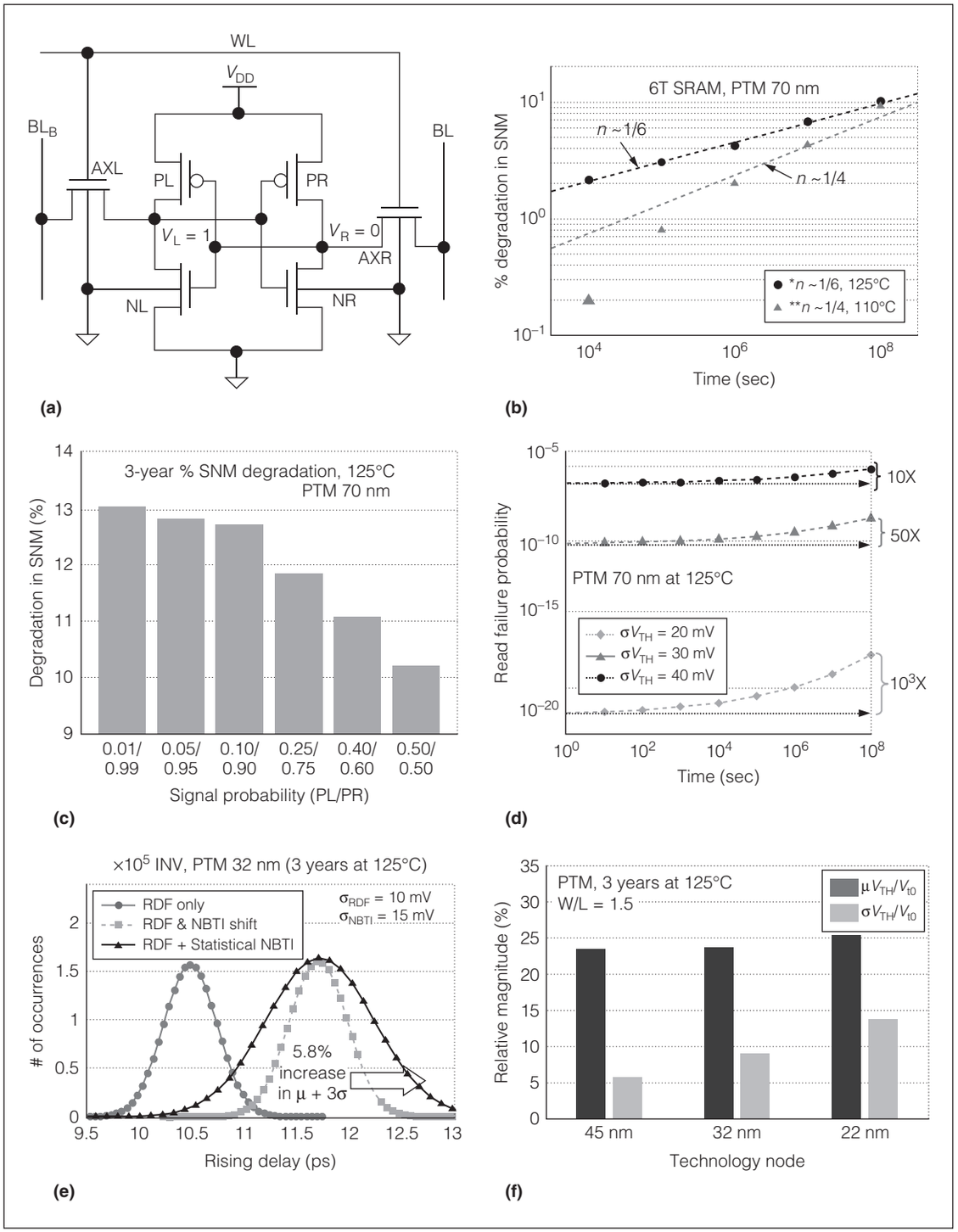

Figure 3. Six-transistor (6T) SRAM cell schematic (a), degradation in SRAM read stability under NBTI (b), degradation in SRAM static noise margin (SNM) under unmatched signal probabilities between PMOS transistors PL and PR (c), read failure probability of an SRAM cell under various V_{TH} standard-deviation values (d), variation of inverter gate delay (rising transition) under NBTI degradation (e), and NBTI variation at various technology nodes (f).

results are based on a V_{TH} model with different time exponents (n in Equation 1 is 1/4 in the work of Krishnan et al.[3] and Alam,[4] and 1/6 in the work of Varghese et al.[2]), they commonly show a significant degradation in SNM over time.

We obtained the results in Figure 3b from an identical stress condition applied to PL and PR. In certain cases, signal probabilities at PL and PR can differ from each other. A typical example is a bit cell storing constant data for a long period of time. Considering the dependency of degradation with respect to signal probability (see Figure 1b), in such cases one PMOS transistor can experience more degradation than the other, further increasing the mismatch. We conducted simulations using the framework proposed by Kang et al. to determine the impact of unmatched signal probability between PL and PR. As Figure 3c shows, SNM degradation severely increases with unmatched signal probabilities. We observed an increase in SNM reduction of nearly 30% when signal probabilities at PL and PR were 0.99 and 0.01, respectively.

In reality, most transistor mismatches originate from random intradie variations—for example, random dopant fluctuation (RDF)—in each transistor's V_{TH}. Several statistical-analysis techniques have shown the significance of RDF-induced parametric failures in SRAM arrays.[9] Under such circumstances, it's more meaningful to observe the impact of NBTI combined with random process variation. The simulation methodology proposed by Kang et al. is one of the earliest works that emphasized the combined effect of NBTI and process variation in SRAM cells.[6] They modeled the transistor's V_{TH} as a temporal random variable:

$$V_{TH} = V_{TH0}(t_{op}) + \Delta V_{TH} \Rightarrow \mu_{VTH} = V_{TH0}(t_{op}), \quad \sigma_{VTH} = \sigma_{\Delta VTH} = \sigma_{NBTI} \tag{3}$$

where μ_{VTH} and μ_{VTH} represent the mean and standard deviation of V_{TH}. Equation 3 shows that μ_{VTH} depends on operation time t_{op}, whereas σ_{VTH} is fixed with respect to time and is only affected by the RDF. We applied this temporal V_{TH} model to the statistical framework to compute the read failure probability of an SRAM cell, as Figure 3d shows. NBTI-induced temporal degradation severely increases the chance of read failures in an SRAM cell. For example, when the initial σ_{VTH} is 20 mV (due to RDF), the three-year NBTI degradation at 125°C can increase the read failure probability by more than 1,000×. Such an increase in read failure probability can drastically reduce the parametric yield of the memory arrays. This result indicates that NBTI in SRAM arrays should be analyzed in combination with the impact of random process variation. These results also show that NBTI has a far greater impact on memory arrays than on random-logic circuits.

Statistical variation in NBTI

Thus far, we've neglected one of the key features of the NBTI mechanism in scaled technologies: the statistical variation of the degradation process. With aggressive scaling of device dimensions, breaking and repassivation of the small number of Si-H bonds in the channel (which are randomly placed and varying in number) experience stochastic fluctuations. This phenomenon is similar to the random V_{TH} variation induced by the number and placement of dopant atoms in the channel, known as the RDF effect. To analyze this problem, Rosa et al. developed a compact statistical NBTI model that considers the random nature of the Si-H bonds breaking in scaled transistors.[5] Using this model, we explore the impact of NBTI variation on lifetime circuit performance. From a circuit-level perspective, NBTI variation closely resembles RDF-induced V_{TH} variation in that it's completely random, even among transistors closely placed on the same chip. Hence, we consider simultaneous RDF- and NBTI-induced V_{TH} variation (σ_{RDF} and σ_{NBTI}) as follows:

$$\sigma_{VTH} = \sqrt{\sigma_{RDF}^2 + \sigma_{NBTI}^2(t)} \tag{4}$$

where σ_{VTH} represents the total V_{TH} variation after time t. This equation neglects the possible correlation between RDF and NBTI. For example, if V_{TH} is skewed by RDF variation, the oxide field and doping concentration also changes, which could have a nonnegligible effect on the scale factor K_{DC} of the temporal V_{TH} model. For simplicity, we don't consider the impact of this correlation in our analysis. However, to establish a more accurate NBTI model, we hope to incorporate this correlation in our future work.

Impact on random-logic circuits

Figure 3e represents the histogram of a simple inverter delay with and without the impact of NBTI variation, assuming three-year stress. We applied Monte-Carlo-based HSpice simulations to obtain the results using a 32-nm PTM file. Because PMOS transistors are mainly affected by NBTI, we measured the gate's rising delay. As the two curves on the right of

Table 2. Rising-delay degradation due to NBTI variation.

		32-nm node						22-nm node					
		Rising delay (ps)				Degradation (%)		Rising delay (ps)				Degradation (%)	
Circuit	Line no.	μ_{init}	μ_{life}	σ_{RDF}	σ_{all}	σ	$\mu + 3\sigma_{life}$	μ_{init}	μ_{life}	σ_{RDF}	σ_{all}	σ	$\mu + 3\sigma_{life}$
INV	1	10.27	11.50	0.20	0.41	100.67	16.98	6.12	7.46	0.25	0.60	140.41	34.91
NAND	2	14.39	15.92	0.25	0.53	108.89	15.56	9.93	11.49	0.27	0.66	143.38	25.38
NOR	2	15.40	17.73	0.52	0.74	42.38	17.63	9.85	12.59	0.23	0.51	119.61	33.88
NOR	3	11.92	13.66	0.13	0.26	95.53	17.25	6.99	8.93	0.22	0.44	97.16	33.78
NAND	4	17.00	18.63	0.25	0.53	108.89	13.80	11.85	13.47	0.30	0.73	140.48	22.73
invch5	1	53.51	57.78	0.84	1.47	74.95	11.00	36.60	40.25	0.82	1.72	111.01	16.32
invch9	1	96.91	104.15	1.59	2.61	64.07	10.13	66.90	72.91	1.52	2.95	93.91	14.41

* Invch: a nominal size inverter chain; μ_{init}: mean delay at time 0; μ_{life}: mean delay after three years of NBTI stress at 150°C; σ_{RDF}: standard deviation of the delay considering only random dopant fluctuation (RDF); σ_{all}: standard deviation of the delay considering both RDF and statistical NBTI variation simultaneously; $\mu + 3\ \sigma_{life}$: overall delay push-out in a 99% cumulative distribution function (CDF) point after three years of stress due to statistical NBTI variation.

Figure 3e show, the added impact of NBTI can significantly increase the variability of gate delay. For this specific example, a 99% cumulative distribution function (CDF) point of the rising delay has been pushed out by 5.8%. Table 2 summarizes the simulation results, showing the impact of NBTI variations on different circuits designed at 22-nm and 32-nm technology nodes. As the table shows, the standard deviation of delay can change significantly, because of the impact of NBTI variation. Compared to the standard gate-level results, circuit-level results (for example, invch5 and invch9) indicate only minimal change in delay variation. This is due to the variation-canceling effect between different gates on the same timing path, and is quite significant in circuits with large logic depth. Comparing 32-nm and 22-nm node results shows that NBTI variations have a greater impact on scaled technology (Figure 3f).

Impact on 6T SRAM cells

If the statistical read failure event is defined as a cell having a read SNM value less than a predefined limit, SNM_{fail},[9] we can define an SRAM cell's read failure probability as

$$P_{RF}(t) = \int_{-\infty}^{SNM_{fail}} f_{SNM(t)}(x)dx = \Phi\left(\frac{SNM_{fail} - \mu_{SNM}(t)}{\sigma_{SNM}(t)}\right) \quad (5)$$

where $f_{SNM}(t)$ represents the probability density function (PDF) of SNM at time t and can be approximated as a Gaussian random variable, $\mu_{SNM}(t)$ and $\sigma_{SNM}(t)$ are the mean and standard deviation of SNM at time t and can be extracted from the HSpice Monte-Carlo simulation, and Φ is the standard Gaussian CDF.

Figure 4a shows the read failure probability computed using Equation 5 for three-year NBTI stress with different SNM_{fail} values. We assumed equal signal probabilities of 0.5 for nodes VL and VR (left value and right value). We obtained the results for three different conditions:

- RDF only,
- static NBTI shift and RDF, and
- statistical NBTI variation combined with RDF (Equation 4).

Comparing the last two conditions shows that the impact of NBTI variation can significantly increase an SRAM cell's read failure probability. Hence, NBTI variation should be considered for temporal SNM analysis.

The impact of NBTI variation also applies for different signal probabilities. Figure 4b plots the 99% CDF point of SNM distribution for various signal probability pairs. As Kang et al. and Chang et al. explain,[6,9] the SNM distribution has the largest value when the signal probabilities at PL and PR are equal. Moreover, the impact of NBTI variation can reduce the SNM values.

TRANSISTOR RELIABILITY COULD be an even more severe problem in future technology nodes. For instance, the time exponent of NBTI degradation can

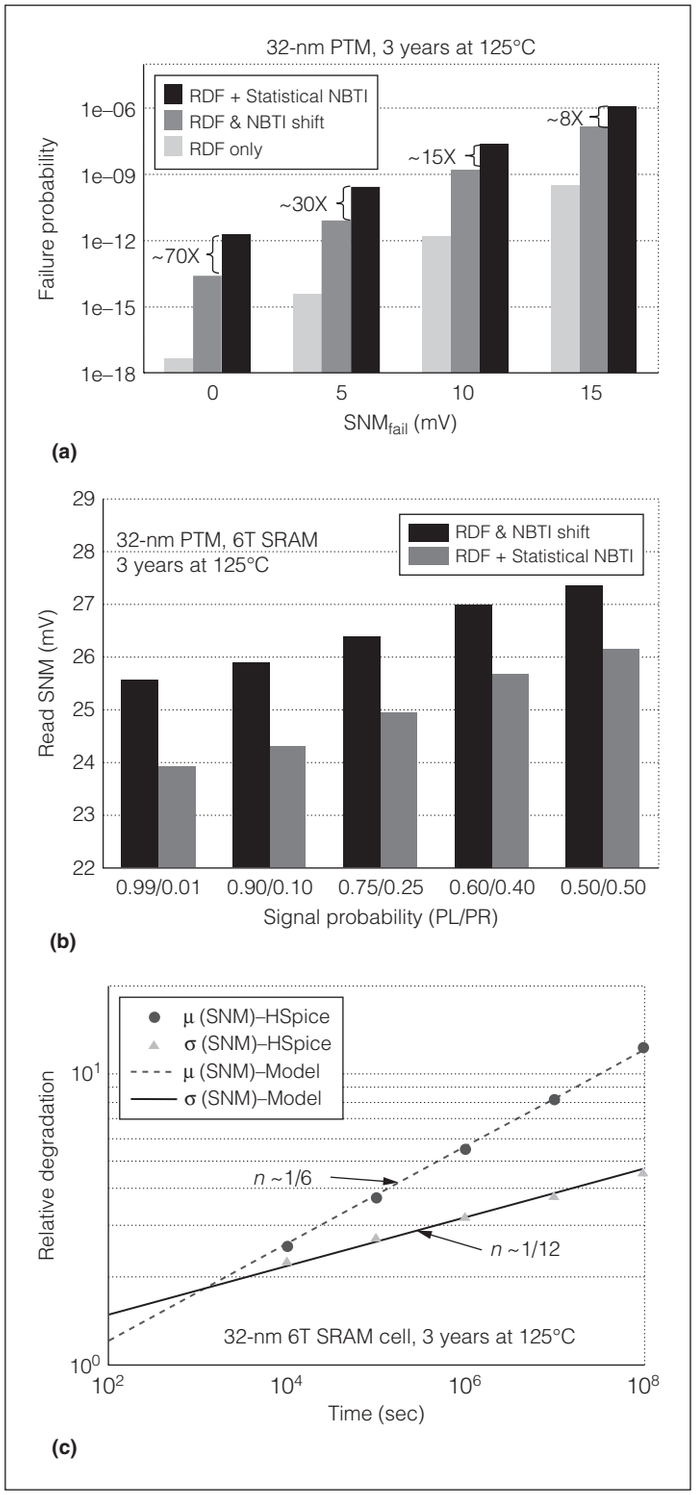

Figure 4. SRAM read failure probability after three-year NBTI stress (a), 99% CDF point of SNM distribution for different signal probability pairs (b), temporal SNM degradation: degradation in μ and σ of SNM under NBTI matched with the model (c).[3]

be larger in device structures such as FinFETs and carbon nanotube FETs than in conventional bulk MOSFETs.[10] As a result, the predicted device lifetimes might be shorter in those devices. Similar phenomena have recently been observed for metal-gate high-*k* dielectric transistors because of bias-temperature instability and charge trapping.[11] Other reliability mechanisms such as hot-carrier injection, time-dependent dielectric breakdown, electromigration, and radiation-induced damages can also impact scaled technology and further reduce device lifetime. Hence, reliability-aware design of digital circuits and memories is essential for future nanotechnologies to ensure robust and stable products. ■

References

1. D.K. Schroder and J.A. Babcock, "Negative Bias Temperature Instability: Road to Cross in Deep Submicron Silicon Semiconductor Manufacturing," *J. Applied Physics,* vol. 94, no. 1, 2003, pp. 1-18.
2. D. Varghese et al., "On the Dispersive versus Arrhenius Temperature Activation of NBTI Time Evolution in Plasma Nitrided Gate Oxides: Measurements, Theory, and Implications," *Proc. IEEE Int'l Electronic Devices Meeting* (IEDM 05), IEEE Press, 2005, pp. 684-687.
3. A.T. Krishnan et al., "Material Dependence of Hydrogen Diffusion: Implications for NBTI Degradation," *Proc. IEEE Int'l Electronic Devices Meeting* (IEDM 05), IEEE Press, 2005, pp. 688-691.
4. M.A. Alam, "A Critical Examination of the Mechanics of Dynamic NBTI for PMOSFETs," *Proc. IEEE Int'l Electronic Devices Meeting* (IEDM 03), IEEE Press, 2003, pp. 14.4.1-14.4.4.
5. G. La Rosa et al., "Impact of NBTI Induced Statistical Variation to SRAM Cell Stability," *Proc. 44th Ann. IEEE Int'l Reliability Physics Symp.* (IRPS 06), IEEE Press, 2006, pp. 274-282.
6. K. Kang et al., "NBTI Induced Performance Degradation in Logic and Memory Circuits: How Effectively Can We Approach a Reliability Solution?" *Proc. Asia and South Pacific Design Automation Conf.* (ASPDAC 07), IEEE CS Press, 2007, pp. 726-731.
7. S.V. Kumar, C.H. Kim, and S.S. Sapatnekar, "NBTI-Aware Synthesis of Digital Circuits," *Proc. 44th Design Automation Conf.* (DAC 07), ACM Press, 2007, pp. 370-375.
8. S.V. Kumar, C.H. Kim, and S.S. Sapatnekar, "An Analytical Model for Negative Bias Temperature Instability," *Proc. IEEE/ACM Int'l Conf. Computer-Aided Design* (ICCAD 06), ACM Press, 2006, pp. 493-496.

9. I.J. Chang et al., "Fast and Accurate Estimation of Nano-scaled SRAM Read Failure Probability Using Critical Point Sampling," *Proc. IEEE Custom Integrated Circuits Conf.* (CICC 05), IEEE Press, 2005, pp. 439-442.
10. H. Kufluoglu and M.A. Alam, "Theory of Interface-Trap-Induced NBTI Degradation for Reduced Cross Section MOSFETs," *IEEE Trans. Electron Devices,* vol. 53, no. 5, 2006, pp. 1120-1130.
11. A.S. Oates, "Reliability Issues for High-k Gate Dielectrics," *Proc. IEEE Int'l Electron Devices Meeting* (IEDM 03), IEEE Press, 2003, pp. 38.2.1-38.2.4.

Sang Phill Park is pursuing a PhD in electrical engineering at Purdue University. His research interests include variation-resilient ultralow-power circuit design, and failure- and fault-tolerant design methodologies. He has a BS in computer engineering from the University of Arizona, Tucson. He is a student member of the IEEE.

Kunhyuk Kang is a senior CAD engineer in the Design Technology and Solutions Division at Intel in Hillsboro, Oregon. His research interests include design for manufacturability, design for reliability, modeling and design methodology for failure and fault tolerance, and statistical CAD algorithms under process variation. He has a PhD in electrical and computer engineering from Purdue University.

Kaushik Roy holds the Roscoe H. George Chair of Electrical and Computer Engineering at Purdue University, where he is a professor. His research interests include VLSI design and CAD for nanoscale silicon and nonsilicon technologies, low-power electronics for portable computing and wireless communications, VLSI testing and verification, and reconfigurable computing. He has a PhD in electrical and computer engineering from the University of Illinois at Urbana-Champaign. He is a Fellow of the IEEE and is a member of the editorial board of *IEEE Design and Test*.

■ Direct questions and comments about this article to Sang Phill Park, School of Electrical and Computer Engineering, Purdue University, 465 Northwestern Ave., West Lafayette, IN 47906; sppark@purdue.edu.