Design Methods for Misaligned and Mispositioned Carbon-Nanotube Immune Circuits

Nishant Patil, Jie Deng, Albert Lin, H.-S. Philip Wong, *Fellow, IEEE*, and Subhasish Mitra

***Abstract*—Carbon-nanotube (CNT) field-effect transistors (CNFETs) are promising extensions to silicon CMOS. Simulations show that CNFET inverters fabricated with a perfect CNFET technology have 13 times better energy delay product compared with 32-nm silicon CMOS inverters. The following two fundamental challenges prevent the fabrication of CNFET circuits with the aforementioned advantages: 1) misaligned and mispositioned CNTs and 2) metallic CNTs. Misaligned and mispositioned CNTs can cause incorrect functionality. This paper presents a technique for designing arbitrary logic functions using CNFET circuits that are guaranteed to implement correct functions even in the presence of a large number of misaligned and mispositioned CNTs. Experimental demonstration of misaligned and mispositioned CNT-immune logic structures is also presented.**

***Index Terms*—Carbon-nanotube (CNT) field-effect transistors (CNFETs), misaligned and mispositioned CNT-immune circuits.**

I. Introduction

CARBON-NANOTUBE (CNT) field-effect transistors (CNFETs) are promising candidates as extensions to silicon CMOS due to fine pitch and excellent device characteristics [35]. Fig. 1 shows the side view of a CNFET. Parallel semiconducting CNTs[1] are grown on or transferred to a substrate. The regions of the CNTs under the gate are undoped. The conductivity of these undoped regions is controlled by the gate. The source and drain regions of the CNTs are heavily doped. The gate, source, and drain contacts and interconnects are defined by conventional lithography. With this structure, a large portion of the existing design and manufacturing infrastructure for FET-based large-scale electronics systems can be utilized.

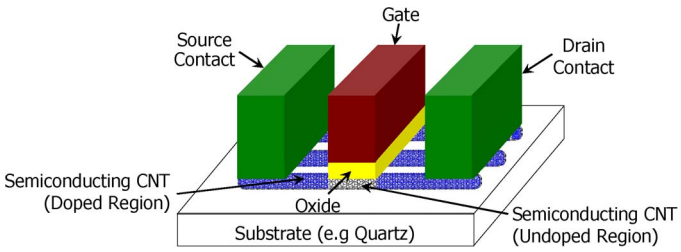

Fig. 1. CNFET.

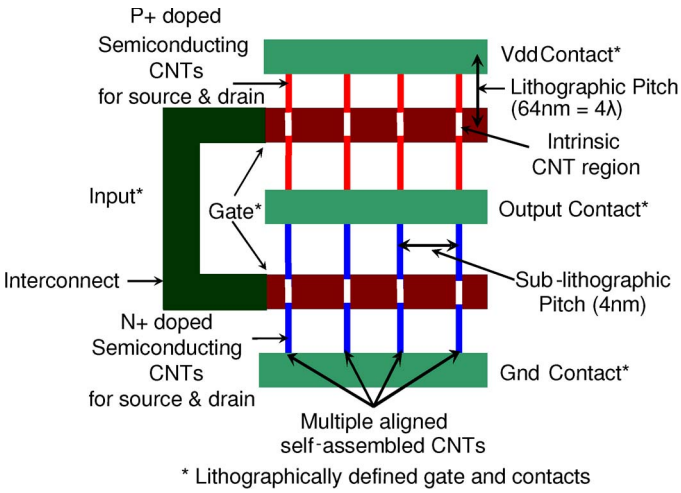

Fig. 2. CNFET inverter.

Fig. 2 shows the schematic of a CNFET inverter in the 32-nm-technology node. The inverter consists of contacts, p+-doped source and drain regions of semiconducting CNTs for the pull-up PFET network, n+-doped source and drain regions of semiconducting CNTs for the pull-down NFET network, two gates for the pull-up and pull-down networks, undoped or intrinsic regions of CNTs under the gates, and local interconnects connecting the gates. The conductivity of the semiconducting regions of the CNTs is controlled by the corresponding gate [16], [17]. The distance between the gates and the contacts is limited by the lithographic feature size (lithographic pitch in Fig. 2). The inter-CNT distance (sublithographic pitch in Fig. 2) is not limited by lithography because the CNTs are grown through self-assembly.

Fig. 3 shows a brief overview of the process of manufacturing CNFET circuits. Semiconducting CNTs are grown on or transferred to a substrate. The regions of logic cells

Manuscript received February 28, 2008; revised May 9, 2008. Current version published September 19, 2008. Part of this paper was presented at the Design Automation Conference (DAC) 2007, N. Patil, J. Deng, H.-S. P. Wong, and S. Mitra, "Automated Design of Misaligned-Carbon-Nanotube-Immune Circuits," DAC 2007, and at the VLSI Technology Symposium 2008, N. Patil, A. Lin, E. R. Myers, H.-S. P. Wong and S. Mitra, "Integrated Wafer-scale Growth and Transfer of Directional Carbon Nanotubes and Misaligned-Carbon-Nanotube-Immune Logic Structures." This work was supported in part by the Focus Center Research Program (FCRP, GSRC, C2S2, FENA), by the National Science Foundation, and by a Stanford Graduate Fellowship. This paper was recommended by Associate Editor K. Chakrabarty.

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Digital Object Identifier 10.1109/TCAD.2008.2003278

[1]In this paper, all CNTs are single-walled CNTs.

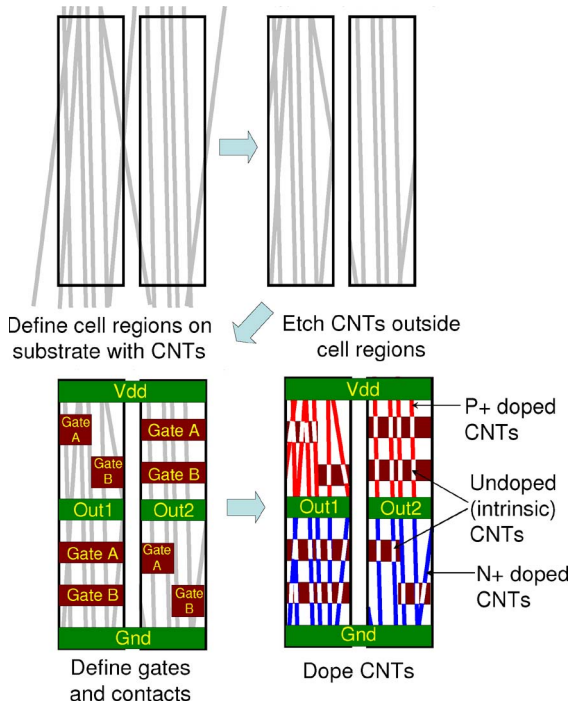

Fig. 3. CNFET circuit fabrication process.

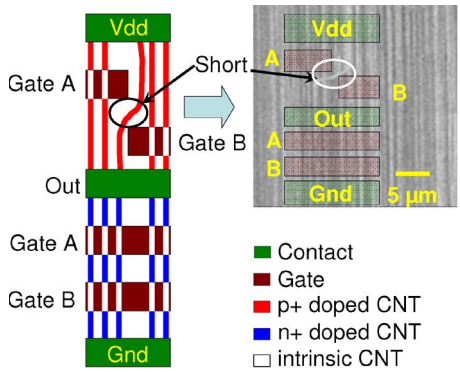

Fig. 4. Misaligned CNT causing short in NAND logic gate.

are defined using lithography, and CNTs outside these cell regions are etched away. Then, the gate and contact regions are defined using lithography. Next, the CNT regions corresponding to PFET transistors are doped p-type (the NFET regions are lithographically masked during this step), and the CNT regions corresponding to NFET transistors are doped n-type (the PFET regions are lithographically masked during this step). The CNT regions under the gates remain undoped because they are masked during the doping steps in this self-aligned process. Finally, interconnects are defined using lithography.

Simulation results show that a CNFET inverter fabricated using a perfect CNFET technology has 5.1 times faster FO4 delay and 2.6 times lower energy per cycle compared with a 32-nm silicon CMOS inverter [9]. However, there are two major challenges that must be overcome before the large-scale integration of CNFETs becomes feasible.

1) Misaligned and Mispositioned CNTs: A major challenge in CNT manufacturing is the accurate positioning and placement of CNTs to make CNFETs [13], [18], [19]. Fig. 4 shows SEM images of CNTs on quartz that we have grown in our laboratory. Although a large fraction (∼99%) of the CNTs grown aligned to the crystal orientation of the single crystal quartz substrate (Fig. 4), a nonnegligible (∼1%) fraction of CNTs are *misaligned* [18]. Even if all the CNTs were aligned, the CNTs may be *mispositioned* and lie outside the gate region. It is nearly impossible to guarantee perfect alignment and positioning of all CNTs at VLSI scale. This can result in incorrect logic behaviors of fabricated logic structures (Fig. 5). Fig. 4 shows a possible CNFET NAND cell layout overlaid on a SEM image of directional CNTs grown on quartz. The misaligned CNT in Figs. 4 and 5(a) causes a Vdd to Output short in this NAND cell. This is because the portion of this CNT between Vdd and Output is entirely p-doped. Fig. 5(b) shows a complex logic circuit in which misaligned and mispositioned CNTs cause incorrect logic functionality.

2) Metallic CNTs: Metallic CNTs cannot be used to make CNFETs because their conductivity cannot be controlled by the gate, thereby creating shorts in the transistors. For a random distribution of CNTs, about 1/3 of the CNTs are metallic [30]. Current CNT synthesis techniques yield between 10% and 70% metallic CNTs [21]. There are no known CNT synthesis techniques that grow exclusively semiconducting CNTs. There has been work on metallic CNT removal after CNT growth by electrical burning [5] or selective etching [36]. However, such metallic CNT removal techniques are imperfect, since they do not remove all metallic CNTs and remove some semiconducting CNTs. Hence, cooptimization between the design and processing is required to design circuits that function correctly in the presence of metallic CNTs [38].

Both misaligned and mispositioned CNTs, and metallic CNTs are major challenges for CNFET circuits. This paper focuses on the first challenge of misaligned and mispositioned CNTs and provides a design solution to address the problem. Discarding defective chips with misaligned and mispositioned CNTs or reconfiguring around defective cells after testing may be very expensive for future gigascale systems. Traditional fault-tolerance techniques, such as triple modular redundancy, are also very expensive in terms of area, power, and speed. The misaligned and mispositioned CNT-immune design technique described in this paper can be applied to any logic function and is compatible with VLSI processing. This technique has a minimal impact on existing VLSI manufacturing flows since it does not require die-specific customization. Also, this technique has minimal impact on existing VLSI design flows because imperfection-immune CNFET library cells can be designed using this technique.

The major contributions of this paper are the following.

1) A technique for designing CNFET logic circuits that are guaranteed to implement correct logic functions even in the presence of a large number of misaligned and mispositioned CNTs. We refer to these circuits as *misaligned and mispositioned CNT-immune circuits*.
2) An automated algorithm to determine whether a given CNFET layout is vulnerable to misaligned and mispositioned CNTs.

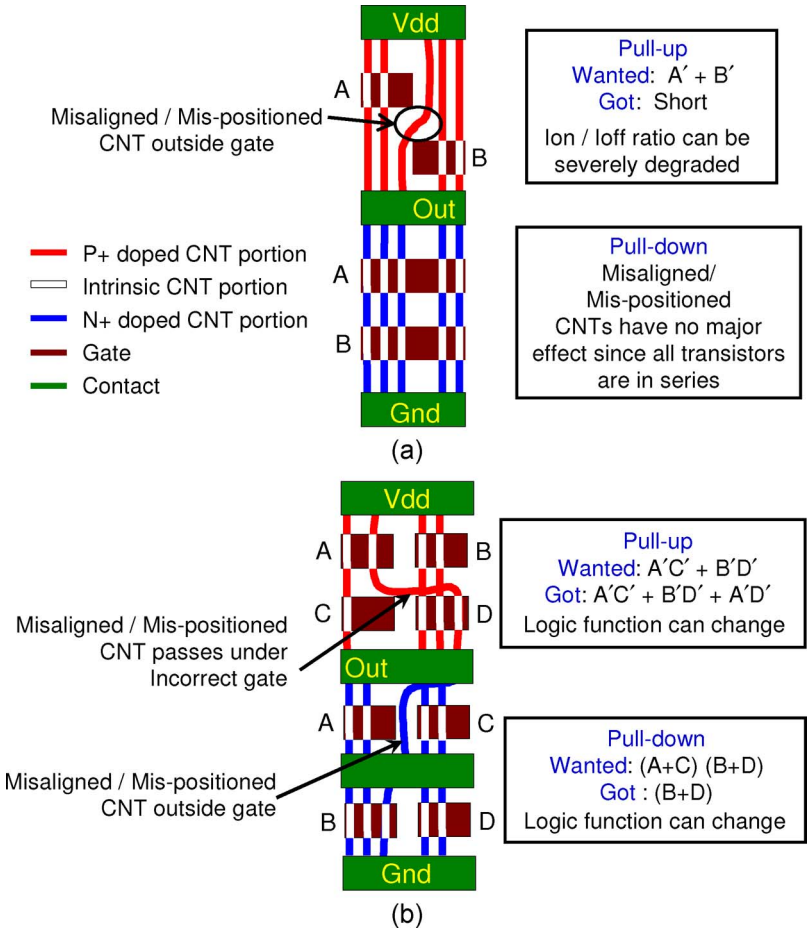

Fig. 5. Incorrect logic functionality caused by misaligned and mispositioned CNTs.

3) A technique for automatically generating CNFET-based logic circuit designs that are misaligned and mispositioned CNT-immune.
4) Simulation results to compare energy, delay, and area of misaligned and mispositioned CNT-immune circuit designs compared with designs that are not guaranteed to be misaligned and mispositioned CNT-immune. The worst-case energy, delay, and area penalties of misaligned and mispositioned CNT-immune standard logic cells are 18%, 13%, and 21%, respectively (details in Section IV), compared with designs that are not misaligned and mispositioned CNT immune. These penalties are significantly lower than traditional defect- and fault-tolerance techniques. These penalties decrease with larger CNFET logic gate sizes.
5) Experimental demonstration of misaligned and mispositioned CNT-immune logic structures.

Section II describes the algorithm for determining whether a given CNFET layout design is misaligned and mispositioned CNT immune. In Section III, we present an automated technique for generating misaligned and mispositioned CNT-immune logic circuit designs. Section IV presents simulation results. The experimental demonstration of misaligned and mispositioned CNT-immune logic structures is presented in Section V. Related work is described in Section VI, followed by conclusions in Section VII.

II. Determining Misaligned and Mispositioned-CNT Vulnerability

Given the layout of a CNFET-based circuit implementing a logic function, we need to determine whether one or more misaligned or mispositioned CNTs can result in incorrect logic function implementation. We will use a graph abstraction of the layout for this purpose. Fig. 6 shows three possible structures for a NAND circuit (the interconnect between the PFET and the NFET inputs is not shown for clarity). These structures will be used to illustrate our technique. The two gates in the pull-up network shown in Fig. 6(a) (corresponding to inputs A and B) are not at the same horizontal level to create a compact layout in the horizontal direction. This also reduces the gate capacitance for the gates in the pull-down network. In Fig. 6(b) and (c), the two gates in the pull-up network are at the same horizontal level separated by an undoped region [Fig. 6(b)] or an etched region [Fig. 6(c)]. As discussed earlier in Section I, the regions outside the cell boundaries are devoid of CNTs (removed by the etching of CNTs). In the ideal case, all CNTs should grow on the substrate in one direction from one contact to another, only passing under the gates. However, in reality, not all CNTs will be perfectly aligned and positioned (as discussed in Section I). Consider the misaligned CNT shown in Fig. 6(a), which is completely doped, similar to the case shown in Fig. 4. This CNT will cause a short between the Vdd and Output nodes. On the other hand, any misaligned or mispositioned CNT in

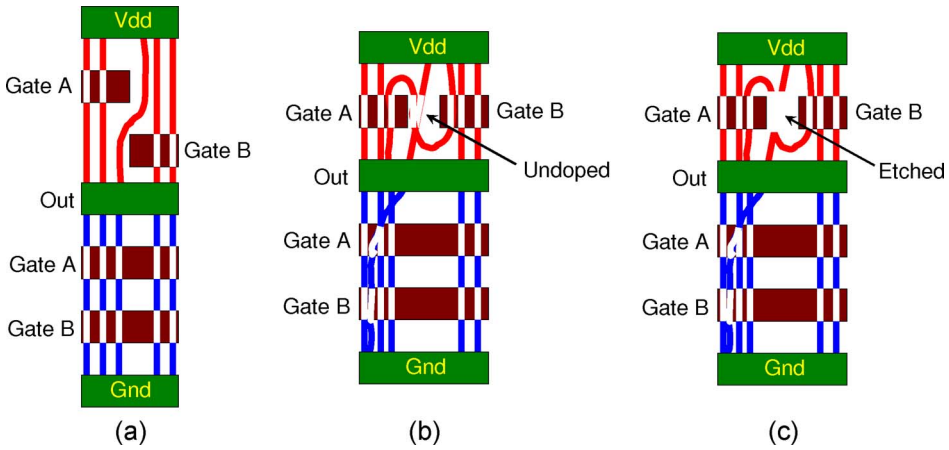

Fig. 6. (a) Misaligned and mispositioned CNT-vulnerable NAND cell. (b) Misaligned and mispositioned CNT-immune NAND cell with undoped region. (c). Misaligned and mispositioned CNT-immune NAND cell with etched region.

TABLE I
LABELS ASSOCIATED WITH NODES IN THE GRAPH

Node type	Node Label	Boolean Function
Gate with input variable A	G_A	A
Gate with input variable A′	$G_{A'}$	A′
Doped Region	D	1
Undoped Region	UD	0
Etched Region	E	0
Vdd contact	C_V	1
Gnd contact	C_G	1
Output contact	C_O	1
Any intermediate contact	C	1

Fig. 6(b) or (c) will not cause a malfunction. This is because any CNT in the pull-up network of Fig. 6(b) and (c) either passes under the gates corresponding to inputs A or B or passes through the undoped or etched region between the two gates, in which case it will not conduct [given a sufficient CNT density ($>$100 CNTs/μm),[2] the chance that no CNT passes through a given gate (e.g., Gate A or B) is very remote].

The first step in our automated analysis is to divide the cell into pull-up and pull-down regions. We will analyze each of these regions separately. Each region is decomposed into a finely divided *square grid.* The dimension of each side of a square in this grid is equal to the smallest lithography feature size. Each square in this grid has a *label* — contact (C), doped (D), undoped (UD), etched (E) or gate (G). For a gate, we also include the input variable associated with that gate (e.g, G_A in Fig. 7). For a contact, we label a Vdd contact as C_V, ground contact as C_G, output contact as C_O, and any other intermediate contact as C. Fig. 7 shows the grid decomposition of the NAND cell layouts in Fig. 6.

We create a graph, where each square in the grid is a node in the graph. The label associated with a node is the same as that associated with the corresponding square as described in Table I. There is an edge between two nodes in the graph if and only if the corresponding squares in the grid are adjacent, i.e., the squares corresponding to those two nodes have a boundary

[2]CNT density of $>$100CNTs/μm is needed for CNFETs to be competitive with silicon CMOS transistors [9].

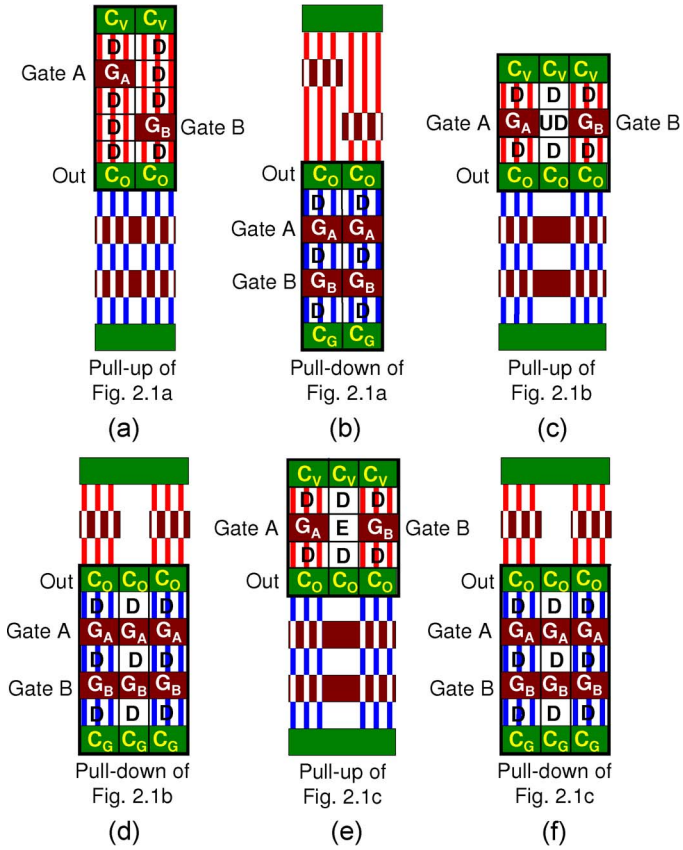

Fig. 7. Grid decomposition of NAND cell layouts in Fig. 6. (a) Pull-up of Fig. 6(a). (b) Pull-down of Fig. 6(a). (c) Pull-up of Fig. 6(b). (d) Pull-down of Fig. 6(b). (e) Pull-up of Fig. 6(c). (f) Pull-down of Fig. 6(c).

or a vertex in common. Two nodes with an edge between them are referred to as *neighboring nodes*.

Any CNT can be represented by a path from a contact node, e.g., C_V for the pull-up and C_O for the pull-down, to another contact node, e.g., C_O for the pull-up and C_G for the pull-down, in the graph extracted from the layout. A CNT in a given square in the grid decomposition of the layout can grow into any of its adjacent squares in the grid. Any CNT can be represented by a path in this graph, considering that the edges in the graph account for all possible growth directions of CNTs.

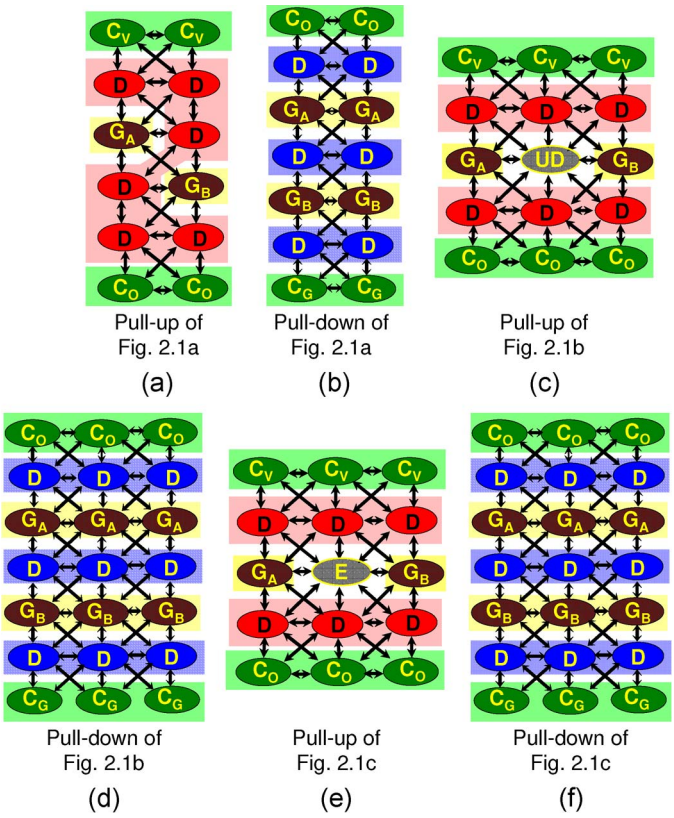

Fig. 8. Graph representations of NAND cell layouts in Fig. 7. (a) Pull-up of Fig. 6(a). (b) Pull-down of Fig. 6(a). (c) Pull-up of Fig. 6(b). (d) Pull-down of Fig. 6(b). (e) Pull-up of Fig. 6(c). (f) Pull-down of Fig. 6(c).

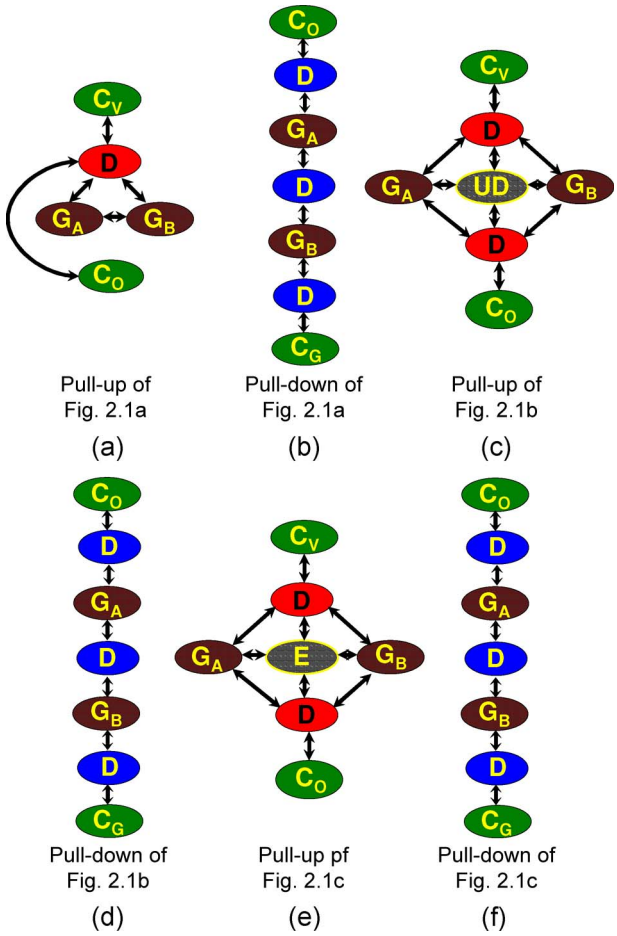

Fig. 9. Reduced graphs for NAND cell layouts in Fig. 7. (a) Pull-up of Fig. 6(a). (b) Pull-down of Fig. 6(a). (c) Pull-up of Fig. 6(b). (d) Pull-down of Fig. 6(b). (e) Pull-up of Fig. 6(c). (f) Pull-down of Fig. 6(c).

Fig. 8 shows the graphs corresponding to the layouts in Fig. 7. To reduce the number of nodes and edges in the graph, we can recursively combine neighboring nodes with the same labels as in Fig. 8 into a single node. The set of neighbors of this new combined node comprises the union of the neighbors of its constituent nodes. Fig. 9 shows the reduced versions of the graphs in Fig. 8. Considering that we preserve the neighbor list of the graph nodes, we can work on the reduced graph to determine whether a given layout is immune to misaligned and mispositioned CNTs.

Each node in the graph has an associated Boolean function as defined in Table I. For example, the gate node G_A has the associated function A since the CNTs under that gate conduct when Gate A is turned on (for the PFET pull-up, CNTs under the gate conduct when A is low, whereas for the NFET pull-down, CNTs under the gate conduct when A is high). For a node with label D, the associated function is one because the doped region of the CNT always conducts. For an undoped region, the corresponding Boolean function is zero because an undoped region of the CNT does not conduct. For an etched region, the corresponding Boolean function is zero because the CNT portion in the etched region is removed and does not conduct.

To determine whether the pull-up (pull-down) network implements the correct function in the presence of misaligned and mispositioned CNTs, we need to traverse all possible paths between the Vdd contact (Gnd contact) node and the output contact in the corresponding graph. For the pull-down network, we compare against the complement of the function implemented by the standard logic cell. In the case of the pull-up network, we apply De-Morgan's law and then complement the variables. The above step simplifies the analysis (Fig. 10).

Let us first consider paths with no loops. The *Boolean function associated with each path* is obtained by AND-ing the Boolean functions associated with the nodes along the path. This Boolean function of a path represents the switch-level function implemented by a CNT traversing that path. For example, in Fig. 9(c), the path $C_V-D-G_A-D-C_O$ has the Boolean function A and the path $C_V-D-UD-D-C_O$ has the Boolean function zero. In Fig. 9(a), the path C_V-D-C_O has the Boolean function one. For paths with loops, we traverse the loops only once, considering that the Boolean expression associated with the path will not change with multiple traversals of the same loops [6].

The OR of the Boolean functions associated with all paths must be identical to the intended function (function without misaligned or mispositioned CNTs) for the circuit to be immune to misaligned and mispositioned CNTs. This is because the paths represent all possible CNT misalignment and mispositioning scenarios. In our implementation, we used standard equivalence checking techniques for this purpose [3].

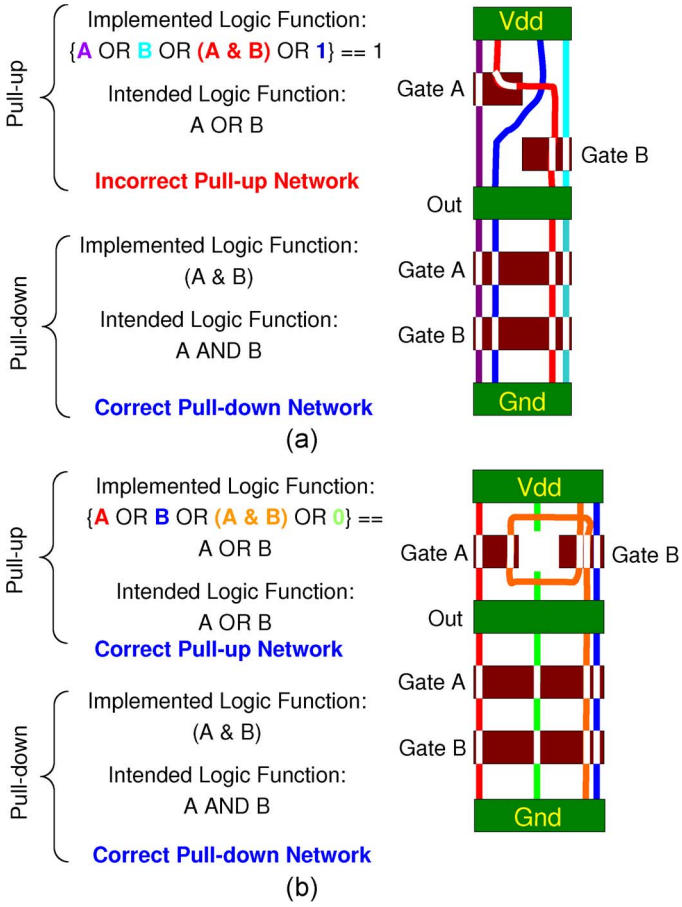

Fig. 10. Traversal of NAND cell graphs in Fig. 9.

Multiple CNT paths can interact in two ways, either through conduction between CNTs or through electrostatic shielding between CNTs. The effect of interactions between CNT paths is discussed in the Appendix.

We show a few examples of this graph traversal in Fig. 10. Note that the pull-down network is compared with (A and B), which is the complement of the NAND function, whereas the pull-up network is compared with (A OR B), which is a function obtained by applying De-Morgan's law and then complementing the inputs. The functionality of the pull-down networks in both misaligned and mispositioned CNT-vulnerable and CNT-immune NAND cell designs is not affected by misaligned and mispositioned CNTs. The reader can verify that the OR of the Boolean functions of all paths in the graphs of Fig. 9(b) and (d) are identical to the intended function implemented by the pull-down network of a NAND cell. These graphs have special properties, and we refer to them as *straight-line graphs*. A misaligned or mispositioned CNT in the pull-up network of the misaligned and mispositioned CNT-vulnerable cell may create a short between the Vdd and Output because the Boolean function of the path $C_V - D - C_O$ in Fig. 9(a) is one (which includes all possible minterms). However, the pull-up network of the misaligned and mispositioned CNT-immune NAND is immune to both misaligned and mispositioned CNTs because the Boolean function of any path cannot include minterms that are not present in the original function.

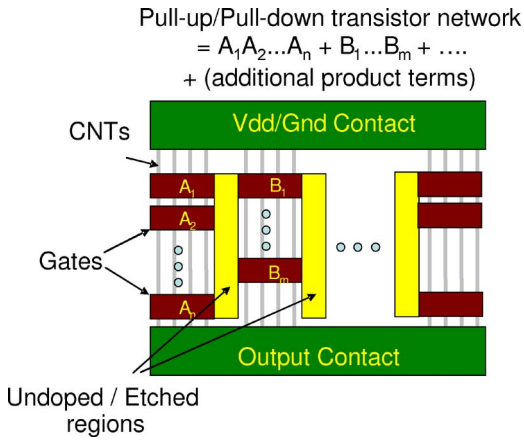

Fig. 11. Misaligned and mispositioned CNT-immune layout for a network specified in SOP Form.

In summary, the algorithm to determine the misaligned and mispositioned CNT immunity for a given layout comprises of the following steps:

1) perform grid decomposition of cell layout;
2) extract graph representation of layout;
3) perform graph reduction to obtain reduced graph;
4) traverse all paths in graph and OR Boolean functions corresponding to paths;
5) determine whether the OR-ed Boolean functions of all paths equal the intended function;
6) Layout is misaligned and mispositioned CNT immune if and only if the OR of the Boolean functions of all paths in graph is equal to the intended function.

III. Sufficient Condition for Misaligned and Mispositioned CNT-Immune Design

We will now describe an algorithm that can be used to implement misaligned and mispositioned CNT-immune layouts of the pull-up and pull-down networks for a standard logic cell. The inputs to our algorithm are the pull-up and pull-down networks represented as a combination of series and parallel transistor networks. We first discuss the case where the pull-up and pull-down networks are expressed in sum of products (SOP) or product of sums (POS) form.

For a network specified in SOP form, the misaligned and mispositioned CNT-immune layout implementation is shown in Fig. 11. Any path in the corresponding graph between the Vdd/Gnd contact and the Output contact must pass through all the gates corresponding to a product term or through an undoped or etched region. Hence, the Boolean function corresponding to that path cannot include minterms that are not present in the SOP representation of the network. Hence, the overall layout in Fig. 11 is immune to misaligned and mispositioned CNTs.

The undoped regions in Fig. 11 can be defined using the same process described in Section I, with an additional processing step. Prior to the doping step, an extended gate region, which includes the actual gate regions as well as the undoped region, is defined; the regions to be doped must not be included. For example, in Fig. 11, a structure that includes only the undoped regions and the Gates A_i's, B_i's . . . is defined. During doping,

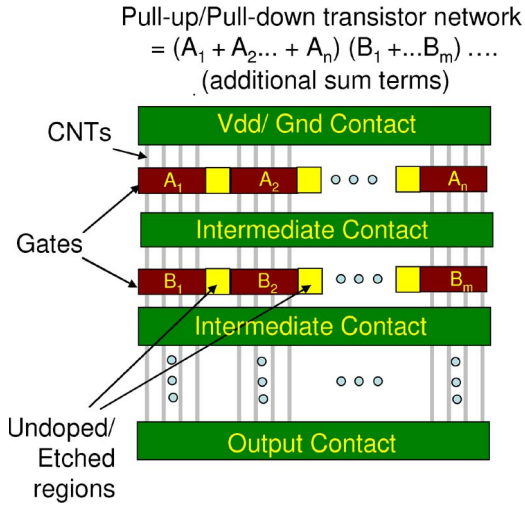

Fig. 12. Misaligned and mispositioned CNT-immune layout for a network specified in POS form.

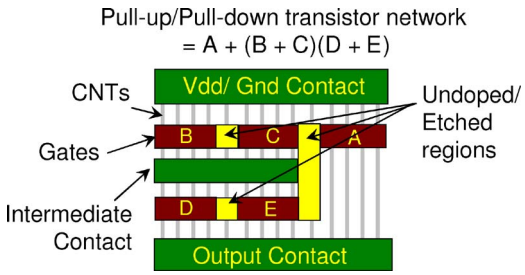

Fig. 13. Misaligned and mispositioned CNT-immune layout for network represented by the function $A + (B + C)(D + E)$.

the regions of the CNTs under this extended gate region are masked and remain undoped. After the doping step, the regions of the extended gate over the undoped regions are etched away to define individual gates. Alternately, the CNTs can be removed from the lithographically defined etched regions using oxygen plasma (discussed further in Section VI).

For a network specified in POS form, the misaligned and mispositioned CNT-immune layout implementation is shown in Fig. 12. This structure is immune to misaligned and mispositioned CNTs since each sum term is immune to misaligned and mispositioned CNTs (by the same argument as in the SOP case). Any CNT that spans multiple sum terms must pass through a contact, and this does not change the function implemented by the cell.

An arbitrary representation of the network may not be in either SOP or POS form. In that case, each sum term is implemented with parallel CNFETs with gates at the same horizontal level and undoped/etched regions between the gates (similar to Figs. 11 and 12). Each product term is implemented as a series network of CNFETs. For example, consider the network represented by the expression $A + (B + C)(D + E)$. We first implement the term $(B + C)(D + E)$ similar to Fig. 12. Next, we implement A in parallel with this structure and separated by an undoped region or an etched region similar to Fig. 11. Figs. 14 and 15 show the fabrication steps to fabricate the transistor network in Fig. 13. We use additional metal layers to route the inputs to the logic function, as done in CMOS standard cells.

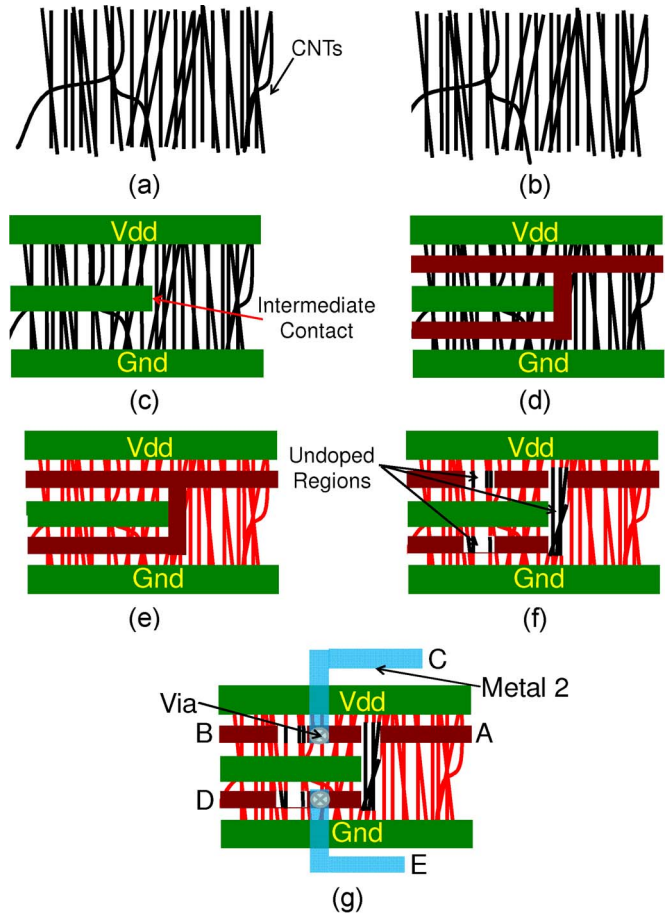

Fig. 14. Steps to create misaligned and mispositioned CNT-immune layout of Fig. 13 with undoped regions. (a) CNTs on substrate. (b) Etch CNTs outside cell. (c) Define contacts. (d) Define extended gates. (e) Dope CNTs (CNTs under gate remain undoped). (e) Etch to create isolated gates. (f) Add subsequent metal layers (along with interlayer dielectric) to interface with other cells.

The misaligned and mispositioned CNT-immune design technique works for any arbitrary function with any number of inputs as shown in Figs. 13–15. The inputs can be routed in the standard cell using multiple metal layers after the etched and the undoped regions are created. The use of multiple metal layers for routing in standard cells is a common practice in CMOS. Other nanoscale standard cell design techniques described in [1] also use metal 1, gate, and metal 2 wiring within standard cells.

To make an arbitrary CMOS layout misaligned and mispositioned CNT immune, we need to have undoped/etched regions in the CNFET layout outside the corresponding CMOS diffusion and active regions of the transistors to render the CNTs in those regions nonconductive. This represents a sufficient, but not necessary, condition for misaligned and mispositioned CNT-immune design. This technique is compatible with existing VLSI design flows and does not require die-specific customization.

IV. Simulation Results

A misaligned and mispositioned CNT-immune layout may impose energy, delay, or area penalties because of additional undoped or etched regions between gates. In this section, we

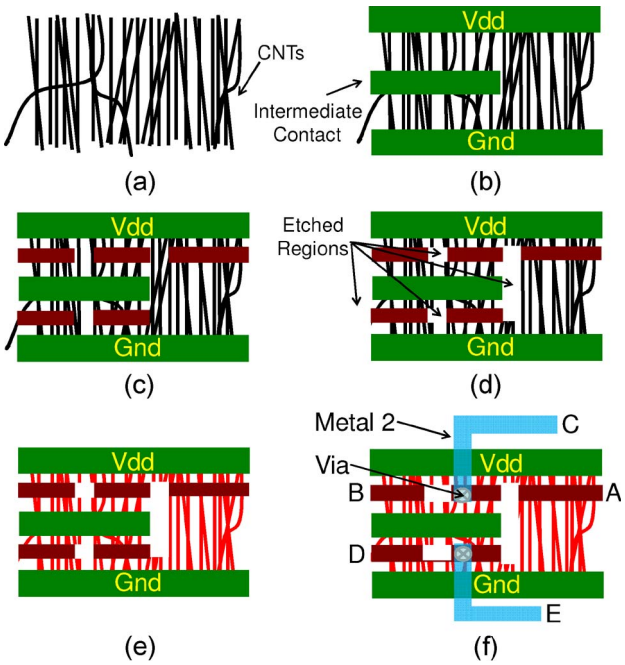

Fig. 15. Steps to create misaligned and mispositioned CNT-immune layout of Fig. 13 with etched regions. (a) CNTs on substrate. (b) Define contacts. (c) Define gates. (d) Etch CNTs between gates and outside cell. (e) Dope CNTs (CNTs under gate remain undoped). (f) Add subsequent metal layers (along with interlayer dielectric) to interface with other cells.

present simulation results to quantify these penalties for standard logic library cells. For circuit simulations, we use a CNFET HSPICE model that is implemented with practical device nonidealities and calibrated to 90% accuracy using experimental CNT data [8]. For each standard cell, we simulated a five-stage fan-out-of-four (FO4) chain of that cell, and measured the delay through and the switching energy consumed by the third stage. We used a 0.9-V power supply for CNFET circuits at the 32-nm-technology node [15]. Fig. 16 shows the circuit layouts of misaligned/mispositioned CNT-vulnerable NAND3 and AOI21 standard cells. Fig. 17 shows the layouts of misaligned and mispositioned CNT-immune NAND3 and AOI21 standard cells. The presence of undoped or etched regions increases the width of the gates, resulting in increased area and energy. Table II shows the area, delay, and energy improvements of a minimum-sized CNFET logic cell over a minimum-sized logic cell in 32-nm Si CMOS. The silicon CMOS standard cells were simulated using the BSIM4 predictive technology models [39]. Table III shows the penalties for misaligned and mispositioned CNT-immune cells compared with misaligned and mispositioned CNT-vulnerable cells. Area penalties were calculated directly from the cell layouts. These area penalties decrease in the case of nonminimum-sized standard cells because the fraction of the cell area occupied by the etched or undoped region is reduced.

V. Experimental Demonstration

We present experimental demonstration of misaligned and mispositioned CNT-immune logic structures. These logic structures correspond to pull-ups of NAND, NOR, AND–OR–INVERT, and OR–AND–INVERT functions. Directional CNTs were

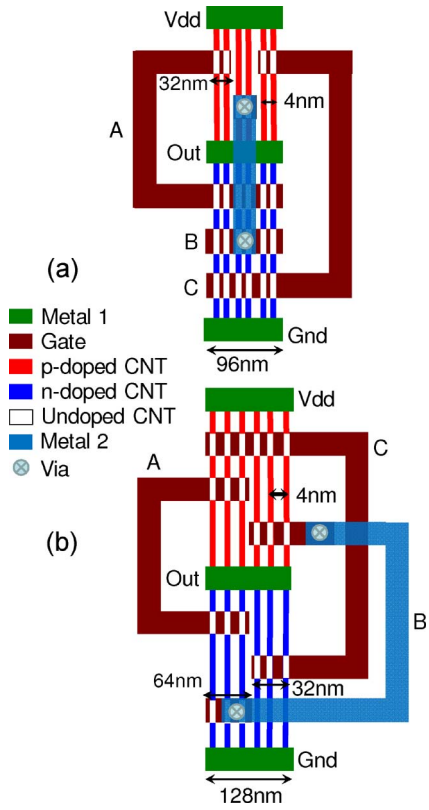

Fig. 16. Misaligned and mispositioned CNT-vulnerable (a) NAND3 and (b) AOI21.

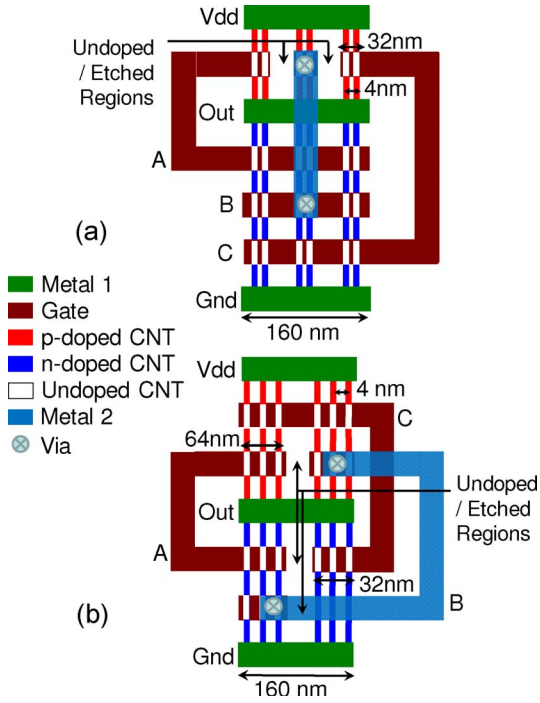

Fig. 17. Misaligned and mispositioned CNT-immune (a) NAND3 and (b) AOI21 cells.

grown on single-crystal quartz using ferritin or iron as catalyst [20]. After growth, the contact metal (palladium), gate oxide (hafnium oxide), and gate metal (platinum) were defined using conventional photolithography. The CNTs were etched from lithographically defined regions for misaligned and

TABLE II
AREA, ENERGY, AND DELAY IMPROVEMENTS OF MINIMUM-SIZED CNFET STANDARD CELLS COMPARED TO CORRESPONDING MINIMUM-SIZED STANDARD CELLS IN 32-nm CMOS

	Misaligned / Mis-positioned CNT vulnerable layout			Misaligned-and-mis-positioned CNT immune layout		
	Area	Energy	Delay	Area	Energy	Delay
nand2	3.41x	1.15x	5.83x	3.45x	1.12x	6.28x
nand3	3.73x	1.31x	6.28x	3.35x	1.15x	5.72x
nand4	3.73x	1.44x	6.95x	3.08x	1.22x	6.16x
nor2	3.18x	1.28x	7.21x	3.22x	1.22x	7.14x
nor3	4.00x	1.23x	7.87x	3.59x	1.07x	7.15x
nor4	3.75x	1.23x	7.56x	3.09x	1.09x	8.00x
aoi21 ~(ab+c)	3.40x	1.69x	7.30x	3.49x	1.68x	7.24x
oai21 ~((a+b)c)	3.20x	1.41x	7.64x	3.28x	1.40x	7.58x

TABLE III
PENALTIES FOR MISALIGNED AND MISPOSITIONED CNT-IMMUNE DESIGN

Cell Type	Penalties		
	Area*	Energy*	Delay [max {rise, fall}]*
nand2	-1%	3%	-7%
nand3	11%	15%	10%
nand4	21%	18%	13%
nor2	-1%	5%	1%
nor3	11%	16%	10%
nor4	21%	12%	-5%
aoi21 [f = ~(ab+c)]	-2%	1%	1%
oai21 [f = ~((a+b)c)]	-2%	1%	1%
Full Adder	12%	10%	7%

* Negative penalties imply improvements

mispositioned CNT-immune logic structures [Fig. 18(d)]. Metallic CNTs were removed using electrical breakdown [5] after the fabrication of misaligned and mispositioned CNT-immune logic structures to improve the on–off ratio of the CNFETs. Fig. 19 shows SEM images of misaligned and mispositioned CNT-immune logic structures with the etched CNT regions. Details of the fabrication process are found in [25].

Consider the NAND pull-up [Figs. 19(a) and 20(a)]. When both gates are off, the drive current (I_{drive}) is very small. When both gates are on, I_{drive} is at maximum, and when only one of the gates is on, I_{drive} is approximately halfway between the minimum and maximum values. For the NOR pull-up [Figs. 19(b) and 20(b)], the drive current is large only when both gates are on; when either of the gates is off, the drive current is very small.

VI. RELATED WORK

Several earlier publications addressed the problem of high defect rates in nanoscale circuits manufactured using self-

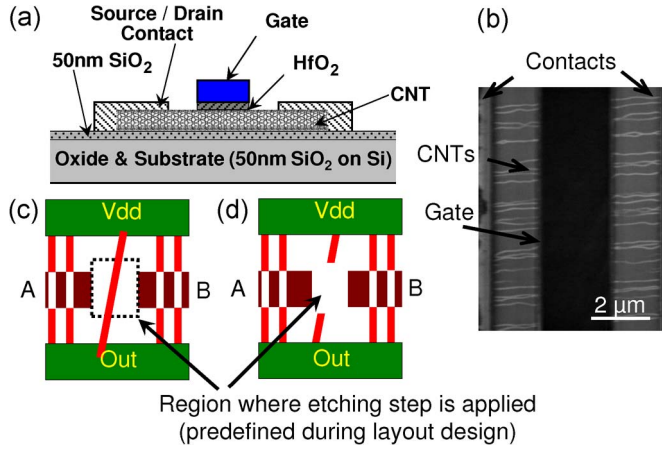

Fig. 18. Misaligned and mispositioned CNT-immune CNFET circuits. (a) Cross section of CNFET. (b) SEM of fabricated CNFET. (c) Misaligned and mispositioned CNT-immune NAND pull-up before etching. (d) Misaligned and mispositioned CNT-immune NAND pull-up after etching.

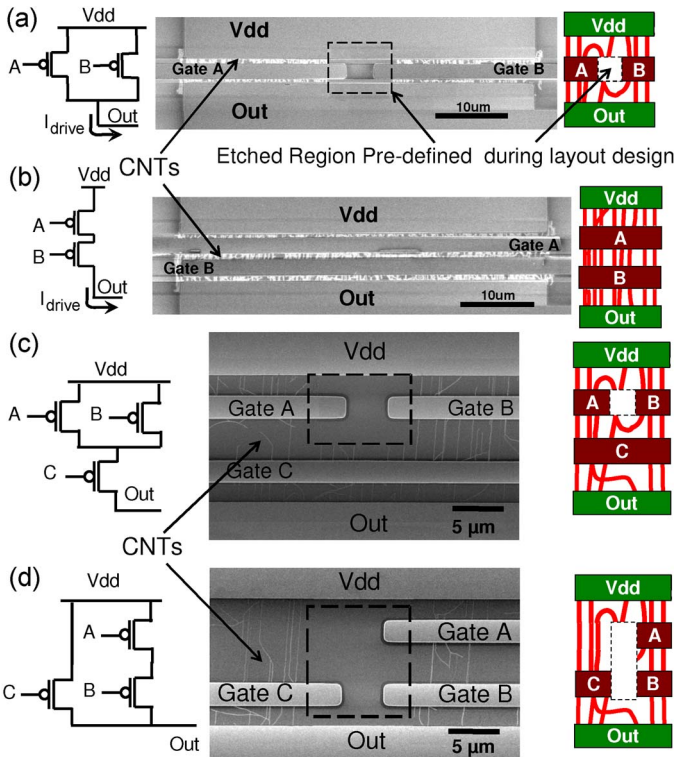

Fig. 19. Experimental demonstration of misaligned and mispositioned CNT-immune logic structures. SEM images of logic structures corresponding to (a) NAND, (b) NOR, (c) AND–OR–INVERT, and (d) OR–AND–INVERT pull-ups.

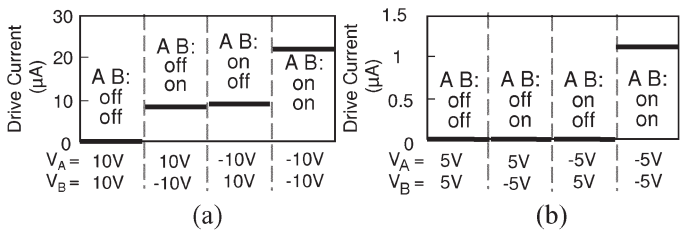

Fig. 20. Experimental demonstration of correct logic behavior of misaligned and mispositioned CNT-immune (a) NAND and (b) NOR pull-up logic structures.

assembly. They also stressed the need for design techniques to overcome these problems. For example, it was observed in [4] that the defect rates of nanotechnology will be large and conventional fault-tolerance techniques may not be sufficient. Several publications discuss the use of test, reconfiguration, and fault-tolerance techniques for such purposes [7], [12], [23], [26]–[28], [31]–[34]. The design technique in this paper addresses the misaligned and mispositioned CNT problem at a much lower level of abstraction at the layout itself. It is demonstrated that the misaligned and mispositioned CNT problem can be successfully solved at this level of abstraction, reducing the burden on higher level techniques. This technique is compatible with existing VLSI design flows and does not require die-specific customization. As a result, synthesis techniques for tolerating high defect rates, e.g., [14] and [37], can incorporate suitable cost tradeoffs using the misaligned and mispositioned CNT-immune standard cells. CNT modeling techniques described in [24] and [29] can be integrated to quantify the performance of logic circuits designed using our technique in the presence of misaligned and mispositioned CNTs.

The use of CNTs for future interconnects has been studied in [2] and is complementary to this paper. It will be interesting to investigate if our presented technique can be extended for the design of self-assembled CNFETs using DNA [10] or graphene nanoribbon field-effect transistors [22].

VII. Conclusion

Misaligned and mispositioned CNTs impose a major barrier to practical implementations of CNFET-based logic circuits. This paper shows that it is possible to overcome this barrier by designing CNFET-based logic circuits that are inherently immune to misaligned and mispositioned CNTs. The energy, delay, and area costs associated with such a design technique are significantly lower than traditional fault-tolerance techniques. Moreover, this design technique can be easily automated and is compatible with existing VLSI design flows, as demonstrated in this paper. We have also demonstrated actual hardware prototypes of misaligned CNT-immune logic structures. Major areas of future research include the following: 1) automated techniques for synthesizing misaligned and mispositioned CNT-immune circuit layouts together with global energy, delay, and area optimization (this is in contrast to the sufficient condition we use in this paper for generating misaligned and mispositioned CNT-immune layouts); 2) collection of CNT misalignment statistics to further reduce costs associated with misaligned and mispositioned CNT-immune designs; and 3) techniques for designing CNFET-based logic circuits immune to metallic CNTs. An interesting open question is the applicability of the presented design methods for other nanodevices, such as semiconductor nanowire or graphene nanoribbon field-effect transistors.

Appendix

CNTs can interact among themselves in two ways.

1) Conduction between CNTs [11]. This can occur when CNTs contact each other, either in the doped source and drain or in the channel region. Conduction between CNTs creates additional paths for current to flow between contacts. Considering that the algorithm described in Section II accounts for all such conduction paths, if such a path causes incorrect logic functionality, it will be reported by the algorithm. Further, the misaligned and mispositioned CNT-immune design technique described in Section III will prevent incorrect logic functionality in this case.
2) Electrostatic shielding between CNTs. If CNT misalignment occurs under the gate region, the upper CNT partially shields the gate from the lower CNT (Fig. 21). Hence, the conductivity of the lower and upper CNTs are controlled by the gate, and the on current through the lower CNT decreases. We use a 3-D field solver to calculate the four electrostatic coupling capacitances shown in Fig. 21 and then exported these values to the CNFET HSPICE model [8]. In the worst case (when two CNTs overlap along the entire gate region), the on current of the bottom CNT degrades by 11%. Here, the small diameter ($<2-3$ nm) of the CNTs has a very important role, as the gate control for CNTs is through fringing electric fields and the top CNT does not completely shield the bottom CNT from the gate. Thus, the current through CNTs is, to the first order, independent of the effects of electrostatic shielding.

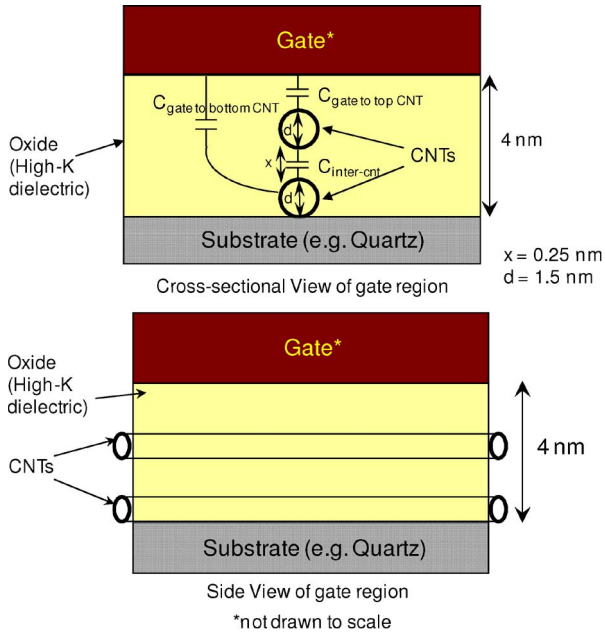

Fig. 21. CNT interactions under the gate.

Acknowledgment

The authors would like to thank D. Akinwande, A. Badmaev, Prof. H. Dai, Dr. J. McVittie, Prof. Y. Nishi, K. Ryu, H. Wei, J. Zhang, and Prof. C. Zhou for fruitful collaborations. The fabrication was done in the Stanford Nanofabrication Facility of the National Nanotechnology Infrastructure Network.

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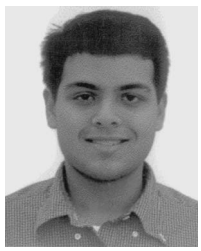

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