Digital Circuit Design Trends

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I. Introduction

THE past 20 years have seen enormous growth in the capability and ubiquity of digital integrated circuits. Today, it sometimes seems difficult to buy any product without them—even greeting cards have chips in them. In a short review paper like this, it is unfortunately impossible to mention (let alone describe) all of the great work that was done and published in the VLSI Circuits Symposium during this period. So, rather than attempting this task, this paper uses papers from the conference to illustrate some of the major trends in the design of digital circuits during the past 20 years. Adopting this approach means that many interesting papers are not included, and we apologize in advance if your favorite is one of these.

At the time of the first VLSI Circuits Symposium in 1987, many of the dominant digital technology trends had already emerged. The first microprocessors were developed in the 1970s and were already starting to drive computing in the mid 1980s. Due to power issues with both nMOS and bipolar technology, by the mid 1980s, the industry had also mostly transitioned to CMOS technology for high-performance digital design. However, in the late 1980s, both microprocessors and CMOS appeared to be vulnerable to competing alternatives. Significant effort was expended in trying either to improve CMOS circuit performance or to find alternative technology/approaches for high-performance designs. BiCMOS was quite popular in the late 1980s and early 1990s, and many different CMOS circuit forms were also presented during this time.

Indeed, looking over the papers dealing with low-level circuit design issues (as we will do in Section II) makes it apparent that technology's path was not as clear then as it seems now in hindsight. However, over time, the industry settled on a relatively small set of circuit styles, and circuit innovation moved toward dealing with the new problems that arose due to the increases in complexity enabled by scaling. For example, many papers dealing with issues such as signal integrity, power supply quality, and the distribution of precise timing references were presented during the 1990s, and many of these issues continue to be explored today.

Since much of the work in digital circuits was driven by processor design, and since these new system problems were most acute for processors, Section III examines the evolution of both application specific and general purpose processors. During the mid to late 1990s, the growing computational power enabled by the improvements in processor design and increases in complexity created two additional "new" problems that needed to be addressed. The first was the need for increased communication bandwidth required to sustain the drastic improvements in on-chip computation, and thus Section IV describes how I/O systems evolved to satisfy this need. The second issue brought on by complexity and performance scaling was the reemergence of a power dissipation problem even in CMOS. This issue was initially thought only to be critical for systems with limited battery sizes and thermal envelopes (like cellphones and personal digital assistants), but over time it has become clear that power dissipation is critical in all digital circuits, including high-end processors. This trend is discussed in Section V.

II. Technology and Circuit Design Trends

As clearly evidenced by the papers presented in the conference, the primary concerns of the digital designer have changed significantly over these past two decades. In the early years, there were many more publications focused on new circuit forms or on circuits for technologies other than CMOS. The early conference papers might even give the impression that bipolar/BiCMOS was the technology of the future. In 1987, there were a number of BiCMOS papers including an invited paper by Kubo on BiCMOS technology trends [1]. Three years later, George Wilson from BIT gave a keynote on the bipolar microprocessors that SUN and MIPS were developing [2], and that year (which was clearly the peak for bipolar digital circuits) the digital logic session had only one CMOS paper. The other papers were on BiCMOS circuits, including complementary BiCMOS [3] and a new nonthreshold bipolar logic [4].

While 1991 still saw a number of BiCMOS papers, there was also a rump session [5] that discussed the problematic future of BiCMOS in the face of continued voltage scaling. Although there was further work on getting bipolar circuits to work at lower voltages by Razavi [6] and others, the number of digital bipolar papers dropped off considerably. The early years of the conference also saw digital circuit papers in other unusual technologies, including superconducting Josephson circuits [7] in 1989 and a CCD processor in 1992 [8]. However, by the mid 1990s, it was clear that plain voltage-scaled CMOS technology was going to win, and since that time there have been few papers about novel digital technologies.

Like papers describing bipolar and BiCMOS circuits, papers describing novel CMOS logic families were much more common in the first decade of the conference than in the second decade. A good example is a multivalued logic technique proposed by Kawahito [9]. Representing a sign/digit number on one wire greatly reduced the hardware needed in a multiplier. Also, in the late 1980s and early 1990s, creating new pass transistor logic families was common—especially for adders. Examples include Yoshida's ALU design using double-path transistor

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logic (DPL) [10] and Cheng's current-sensed complementary pass transistor logic [11]. Other circuit ideas that were tried include using a high-speed memory technique—self-resetting gates—to create high-performance registers and incrementers, presented by Haring [12], and making tradeoffs between speed and noise margin by precharging and/or predischarging internal nodes of dynamic logic [13].

As the complexity of chips grew during the 1990s, the digital circuit designer's focus moved to address system-level issues that had now become critical: supply distribution, clock distribution and latch design, and noise robustness. Power supply distribution grew to be a huge issue as the rising complexity and performance of digital systems coupled with decreasing supply voltages led to large increases in supply current. Lower voltage and higher current required that the supply impedance decrease even more rapidly. Early work in this area included Loinaz measuring and modeling noise coupling through the common substrate in 1992 [14] and Kitchin evaluating electro-migration in an Alpha microprocessor in 1995 [15]. By early 2000, power supply design was a major conference topic. In 2002, Rahal-Arabi presented the design and validation of the supply network in a couple of Intel processors [16]. A circuit to detect supply noise was presented in 2003 [17], and by 2004 there was an entire session devoted to power supply design, analysis, and measurement. More recent work has focused on trying to mitigate the effect of supply noise on performance [18].

As designers tried to improve performance by reducing the number of gates between flops in order to increase clock frequency, clock distribution and latch design also became a challenge during the mid 1990s. In the early 1990s, Digital Equipment Corporation introduced the first "short tick" processor which spurred interest in this area. Yuan presented new true single phase clocking flops in 1996 [19], and Klass presented his pulsed dynamic flop in 1998 [20] with reduced timing overhead. The conference in 1998 also included Restle's talk on how to distribute a high-quality clock [21]. Clocking has continued to grow in importance, with an entire session devoted to this topic at the 2003 conference.

More recently, designers have become concerned that noise events such as cosmic rays and the increasing device variability that comes with scaling will affect circuit robustness. Karnik in 2001 analyzed the effect of soft errors in latches [22], and in 2007 Mathew presented a paper on how to build fault-tolerant processor execution units [23].

As we have already seen, one of the major drivers for these circuits papers were microprocessor designs. Thus, Section III takes a step up from low-level circuits to look at how processors have evolved during the past 20 years.

III. Processor Design

The advance in processors during the past 20 years has been breathtaking. In the late 1980s, the debate over instruction set complexity (RISC versus CISC) was in full swing, new ISAs were being developed, and processors ran at 10–30 MHz. A good example of this early processor was the TRON TX1 presented by Tokumaru in 1988 [24]. In 1989, Katz correctly predicted a number of the challenges and trends for microprocessors, including the need for more pin bandwidth (which is discussed in Section IV), scaling clock frequency, and the importance of instruction set compatibility [25]. Overcoming these challenges has allowed us to create the multi-GHz multicore processors we see today [27].[1]

This increase in processor performance came from two main factors: exploiting instruction-level parallelism and higher clock rates. In 1990, Uvieghara presented HPSm [28], the first integrated processor to execute instructions out of program order. This ability to rearrange instructions dynamically was the key technology that allowed processors to exploit instruction-level parallelism and execute more instructions each cycle. The other factor driving performance was scaling clock frequency. Part of the increase in clock frequency came from technology scaling providing faster gates, but the rest came from reducing the number of levels of logic between flops. Initially these fast cycle-time machines used the simpler in-order issue model, but in 1997 Farrell described how to build an out-of-order processor that ran at 600 MHz [29]. By the late 1990s there was a speed race to see who could build the shortest clock cycle machine. The result in 2000 was a 1 GHz processor produced in a 0.18 μm technology by IBM Research [30], [31]. Processor frequency continued to scale, with Intel reaching 3 GHz in 2002 [32].

The push for higher clock speeds was not without a large cost, and 2004's rump session, titled "Limitations of low FO4 designs" [33], signaled that designers had begun to recognize that this path would hit significant barriers. The principal issue facing these machines was that their power consumption rose to around 100 W, which is right at the limit of cost-effective cooling solutions. Power constraints thus greatly slowed the scaling of clock frequencies, and, in fact, most of today's processors run at lower clock frequencies than those of the processors from the early 2000s. By 2006, power was clearly at the forefront of digital design, and that year Naffziger described the changes in processor design required to cope with the new power constraint [34]; these methods will be described in Section V.

Before moving on, it is interesting to look at some of the specialized processors that were presented at the conference in order to gain insight into which application areas were critical enough to warrant chip development. In the late 1980s, fax transmission was growing, and being able to compress and decompress images efficiently was critical. This led to specialized image compression chips, like the one presented by Kowashi in 1989 [35]. Many facets of image processing were of growing importance; the discrete cosine transform chip from 1991 [36] is one example of a more general image compression device developed during this time. This interest in image processing broadened to the more general area of multimedia in the early 1990s, and in 1993 Ackland outlined the opportunities for VLSI in this area [37]. Media processing became a large growth area during the rest of the 1990s, leading to chips optimized for different applications. By 1996, Chromatic Research had built a more general multimedia processor that was flexible enough to handle all

[1]Interestingly, in 1990 Katz and his student proposed building caches from DRAM [26], a topic that has recently become popular as Mbytes of cache memory are integrated on processors.

of the multimedia needs (e.g, video, sound, and graphics) of a PC [38].

During the internet boom in the late 1990s, many processor designs were optimized for operation in networking hardware. Since network switches had very high computational load and many parallel tasks, these designs contained some of the first chip-level multiprocessors [39]. The bursting of the Internet bubble and rapid growth of the consumer market has caused recent processor designers to focus more on visual/video processing. For example, talks in this year's conference described processors for mobile graphics [40], mobile multimedia [41], and H.264 encode/decode [42].

High-performance processors—whether for visual/video processing or for general computation—require huge memory bandwidth to supply the data they consume. Satisfying this requirement created an active area of circuit research on high-speed I/O design, which is the topic of Section IV.

IV. High-Speed Links

Communication between devices was not a major issue at the early VLSI Circuit Symposiums. The TRON processor presented in 1988 had a clock speed of 25 MHz, and I/O was not even mentioned in the paper [24]. Higher speed devices, such as the SRAM from Schuster, typically had ECL interfaces [43] because compatibility with existing systems and standards was paramount. Designers used considerable ingenuity to make CMOS compatible with the older bipolar ECL/TTL families, concentrating on meeting all aspects of the standard without requiring external components[44], [45].

It soon became apparent that requiring backward compatibility was not always necessary or desirable. Ishibe's 1991 paper paid close attention to characteristics of the communication channel and impedence matching, achieving 1 Gb/s in a purely CMOS topology [46]. In 1992, Kushiyama described a multi-drop system with 500 Mb/s/pin performance that used many of the techniques which became mainstream, including PLL-synchronized data reception/transmission and source synchronous clocking [47].

Larger industry trends accelerated the movement to higher speed interfaces. As Rent had noted in the 1960s, increases in component count lead to higher interconnect bandwidth requirements, and technology scaling brought both more gates and higher clock frequencies. Diverging technology roadmaps made communication between logic and memory a particular problem. By 1994, the symposium had an entire session dedicated to inter-chip communication. Designers struggled to find the best PLL and DLL architectures, interconnect topologies, and termination schemes. Lee's serial link paper exemplifies many of these trends and was notable both for its use of bidirectional signaling and of a digital PLL [48].

Increasing use of digital techniques was a feature throughout the 1990s. Older analog circuit structures became difficult to reuse as power supplies decreased, and link proliferation drove topologies that could be more easily ported between processes. For example, Yang's 4 Gb/s oversampling receiver showed that both high link speed and good jitter tolerance could be achieved in a semi-digital design [49], and Sidiropoulos showed that delay lines and voltage-controlled oscillators (VCOs) composed of inverters running from a regulated supply could have good power supply rejection in addition to well-controlled loop dynamics [50].

As process speeds improved and designers gained experience with circuit topologies, the primary system limitation in terms of I/O shifted from the devices themselves to the interconnect. The 4-PAM signaling and pre-emphasis adopted in Farjad-Rad's 1998 paper [51] are good examples of the types of techniques used to compensate for channel characteristics. Classic techniques from communications systems were reapplied to inter-chip communication, as with Sohn's decision feedback equalizer (DFE) for SSTL DRAM interfaces [52].

In the 21st century, link design entered the power-limited regime. Higher frequencies and more elaborate equalization schemes now had to be balanced against the energy per bit transferred, and the new figure of merit became milliwatts per gigabit per second. Lee's 2001 transceiver achieved 20 mW/Gb/s [53], which was surpassed in the 2003 conference by Wong's 7.5 mW/Gb/s design [54].

V. Low-Power Circuits

While high-performance processors and links just recently became power-limited, reducing power was a critical issue much earlier for many digital systems. Soon after the switch to CMOS in the mid 1980s, designers realized that low power and increasing integration would enable new high-functionality portable devices powered by batteries. For these applications, very low operating power would be needed, and the power of standard CMOS was simply too high to meet this requirement. Broderson's invited 1991 paper [55] outlined many of the approaches that designers would use to reduce power consumption: technology scaling, logic family selection, and architectural and algorithm selection. He also described the favorable power tradeoff available by adopting lower frequency and more parallel designs, a lesson that the processor community is just now applying.

Many initial approaches concentrated on reduction of dynamic (CV^2f) power. Nakagome's 1992 paper is a good example of this: reduced bus swings gave lower power consumption, with low threshold devices used to maintain speed [56]. Gutnik's 1996 paper took this idea to its logical conclusion: scaling the supply voltage dynamically based on the device's workload [57]. However, on-die variability can stress the robustness of this type of tracking power supply system. Das's paper in 2005 presented one solution to this issue for a processor—build a flop which can detect when data arrives late and then lower the supply until some errors start to appear [58]. The paper proposed using the standard processor retry mechanism to recover from the few errors that are detected, which allowed the processor to run at a lower voltage and power than any other approach.

By 1994, low-power design efforts were in full swing, with a dedicated session at the Symposium. In addition to reduced swing, some authors experimented with adiabatic techniques, which minimize power consumption by keeping the voltage drop across conducting devices small. Kramer's 2N-2ND logic family was a good example of this [59]. In addition to minimizing voltage drops, it also presented a constant load to the

clock used to power the circuits, raising the possibility of using an inductively tuned driver. Adiabatic circuits initially looked attractive with the high-supply voltages of the time, but had difficulty competing with voltage-scaled CMOS technology. Interestingly, the technique reappeared in Lal's paper on a low-power LCD driver [60], an application which needed a "large" fixed output swing.

The primary low-power approach remained technology and voltage scaling, which required scaling of threshold voltages. Portable applications with low standby power requirements were the first to experience leakage problems from reduced thresholds. To achieve nano-ampere level standby currents, Shigematsu adopted a multithreshold CMOS scheme, where regular threshold transistors were used during operation but powered down in standby mode. A parallel set of always-on high-threshold circuits maintained the system state [61].

As continued technology scaling made leakage a problem even during active operation, designers adopted more elaborate multithreshold schemes. For the Pentium 4, Delganes used low-threshold gates for critical paths and normal-threshold gates elsewhere for reduced leakage [32]. Mizuno adjusted transistor thresholds dynamically by varying the body voltage, choosing a threshold just low enough to run at the selected speed [62]. Ye managed to reduce leakage without additional process overhead by ensuring that more than one device in a stack is turned off when a block is inactive [63], a technique that works well for gates but not inverters.

Power remains one of the critical challenges for future VLSI systems. We will need innovation at all levels to continue performance scaling while maintaining power dissipation within acceptable levels. This is especially true since leakage currents have made it hard to continue to scale the supply voltage. The net result is that even high-end processors are being forced to reduce clock rates and use parallel cores to control power dissipation.

VI. Conclusion

Digital designs have gone through dramatic changes over the past two decades—moving from chips that contained tens of thousands of devices to today's chips that may contain over a billion transistors. The job of the digital circuit designer has grown with the chips, moving from optimizing and validating gates, to working on functional units, to now designing complete systems. While the progress in digital design has clearly been tremendous, tackling current and future system issues and power challenges will lead to significant further innovation. We look forward to seeing continued reports of these digital circuit design advances over the next two decades of the conference.

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