Ultralow-Voltage Power Gating Structure Using Low Threshold Voltage

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***Abstract*—A novel power gating (PG) structure using only low-threshold-voltage metal–oxide–semiconductor field-effect transistors (MOSFETs) is proposed to extend the PG to an ultralow-voltage region (∼0.3 V). The proposed structure deploys series-connected low-$V_{\rm th}$ footers with two virtual ground ports and selectively chooses the logic cells for connecting them to each virtual ground port according to the delay criticality. Furthermore, additional circuitry is designed to reduce not only the subthreshold leakage current but also the gate-tunneling leakage and to reduce the wake-up time and rush current compared to the conventional PG. The total PG switch size of the proposed PG structure including the additional circuits is less than the conventional one. The simulation results are compared to those of other well-known circuit schemes and show that, in the ultralow-voltage region, the other high-$V_{\rm th}$-based PG schemes cannot be used due to the impractical delay increase and long wake-up time, whereas the proposed PG structure keeps the balance among the critical PG issues. The proposed PG is evaluated using inverter chains and ISCAS85 benchmark circuits at 0.6-V supply voltage, which are designed using 45-nm complementary metal–oxide–semiconductor predictive technology model.**

***Index Terms*—Gate tunneling leakage, multimode, power gating, subthreshold leakage, ultralow voltage, wake-up bounce, wake-up rush current, wake-up time.**

I. Introduction

POWER gating (PG) is one of the most effective methods of reducing the subthreshold leakage power of portable systems in the standby mode where a header and/or footer (called sleep transistor) with a high $V_{\rm th}$ is added between the actual power/ground rail and the virtual power/ground. The subthreshold leakage power is significantly reduced by cutting off the high-threshold sleep transistor in the standby mode, while still keeping a high speed in the active mode [1], [2].

However, several critical issues should be resolved for PG structure design. The conventional PG has the disadvantage that an instantaneous charge current rushes through the sleep transistor operating in its saturation region while switching back to the active mode from the sleep mode. Due to the inductive noise problem caused by bonding/package inductance, these current surges cause voltage fluctuations in the on-chip power distribution network [3]. If the magnitude of the voltage fluctuation is greater than the noise margin of a circuit, the circuit may propagate a wrong value. On the other hand, the virtual ground rail takes some time to discharge through the sleep transistor when the PG circuit switches from the sleep mode to the active mode. The time is known as the wake-up time (or latency) for the circuit to be functional and to start working at its full operating speed. Thus, a short wake-up time is required for high-speed processing [1], [2].

As an attempt to overcome these problems, several PG structures have been suggested [3]–[7]. However, these PG structures are no longer effective in the sub-1-V region because the high $V_{\rm th}$ of the PG structures degrades the operation frequency and rapidly increases the wake-up time at the low voltage. Although super-cutoff CMOS can be used at this low supply voltage, it suffers from reduced performance and a long wake-up time [8]. To solve this issue, this brief proposes a novel PG structure in which two n-type MOS (NMOS) transistors with a low $V_{\rm th}$ are used in series with the low-$V_{\rm th}$ transistors of logic circuits to use the PG structure in the sub-1-V region and to keep the fast operating speed of the logic circuits. For the speed improvement of the series-connected footer structure, the drain node of the each footer is used as a virtual ground port, where the upper virtual ground port is connected to the logic circuits on the noncritical paths, and the lower virtual ground port is connected to the logic circuits on the critical paths. For a low rush current and a fast wake-up time, sleep signals having different switching times are deployed. This technique can also be applied to the conventional PG, as shown in [3].

In addition, although PG effectively reduces the subthreshold leakage, the gate tunneling leakage (hereafter called gate leakage) is not well controlled by the PG. The gate leakage grows very fast with CMOS technology scaling, even faster than subthreshold leakage due to the scaling down of the gate oxide thickness [9]. Furthermore, a sleep transistor with a low $V_{\rm th}$ and a thin oxide suffers from the gate leakage much more seriously than a sleep transistor with a high $V_{\rm th}$ and a thick oxide as a result of exponential dependence on the oxide thickness. To reduce the gate leakage of the sleep transistor, a circuit-level technique using the conventional silicon dioxide is introduced, where it is assumed that all the MOSFETs use the conventional silicon dioxide because the use of high-k materials for reducing the gate leakage may lead to mobility and stability issues in the low-voltage region.

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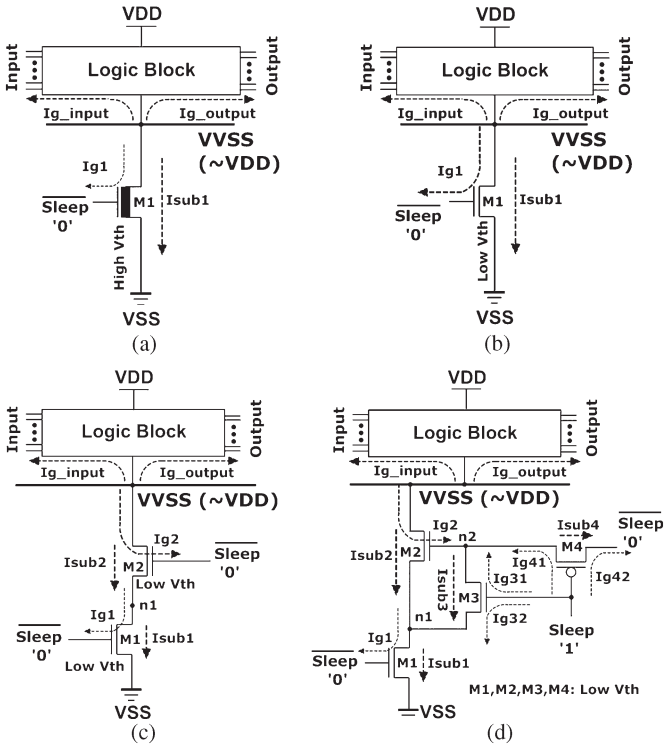

Fig. 1. PG structures. (a) Conventional PG. (b) Single footer with a low $V_{\rm th}$. (c) Two series-connected footers with a low $V_{\rm th}$. (d) New footer with a low $V_{\rm th}$.

II. Design of the PG Structure and the Power Network

A. Single Low-$V_{\rm th}$ PG

In this section, a new PG structure is proposed to reduce the subthreshold and gate leakage current of the PG structure at the sub-1-V supply voltage range. As shown in Fig. 1(a), three gate leakage currents ($I_{\rm g\_input}$, $I_{\rm g\_output}$, and $I_{\rm g1}$) are generated in the conventional PG structure. In [9], the authors present that the impact of the input gate leakage is determined by the primary input vectors and propose an input control circuit to reduce the input gate leakage. However, they did not show how to decrease the gate leakage of the footer. Although $I_{\rm g\_input}$ and $I_{\rm g\_output}$ are dominant, $I_{\rm g1}$, in the case of a big footer, should not be negligible because the gate leakage is a current flowing (tunneling) into the gate of the transistor, and with an increase in the gate area, the tunneling also increases.

Moreover, the conventional PG is no longer effective at sub 1 V for nanoscale CMOS circuits since the conventional PG uses a high $V_{\rm th}$ to reduce the subthreshold leakage. To overcome the technology scaling issue with a high-$V_{\rm th}$ footer and to make it effective at sub 1 V, a single footer with a low-$V_{\rm th}$ instead of a high-$V_{\rm th}$ footer can be used, as shown in Fig. 1(b), at the cost of subthreshold and gate leakage: $I_{\rm g1}$ and $I_{\rm sub1}$ are much greater than those of the conventional PG. Fig. 1(c) shows two series-connected footers for suppressing the subthreshold leakage of the low-$V_{\rm th}$ footer by the effect of the low drain-to-source voltage (stack effect). Even though the stack decreases the subthreshold leakage, the gate leakage still exists. For gate leakage reduction in the PG structure using the low-$V_{\rm th}$ footer, a new PG structure is proposed, as shown in Fig. 1(d). The dominant gate leakage component in Fig. 1(d) is $I_{\rm g2}$ because the voltage difference between the virtual ground and the gate node of M2 is close to $V_{\rm DD}$. In Fig. 1(d), M3 connects the gate node of M2 to the n1 node during the sleep mode, where the gate-to-source voltage of M2 is almost 0 V (the gate voltage of M2 is the same as the n2 voltage), and M2 is turned off. Therefore, the voltage difference between the virtual ground and the gate node of M2 is decreased from $V_{\rm DD}$ to $V_{\rm DD} - {\rm n1}$ voltage, which makes $I_{\rm g2}$ decrease. Although the reduced gate leakage still flows through M3 to the n2 node, as shown in Fig. 1(d), the gate leakage is suppressed by M1 because $I_{\rm sub1}$ is much smaller than that of a one-footer PG structure: less than 0.25 times. On the other hand, in the active mode, M3 is turned off, and M4 is turned on. Therefore, the sleep signal is asserted to M2 in the same way as that of the conventional PG. In the proposed PG, M1 and M2 are strong transistors used as the main sleep transistors, whereas M3 and M4 are minimum-sized (weak) transistors used as the control transistors.

TABLE I
$I_{\rm sub}$ AND $I_{\rm gate}$ OF PG STRUCTURES

VDD = 0.6V	Isub (A)	Igate (A)	Vvss (V)	n1 (V)	n2 (V)
Single Footer (high-Vth)	3.70e-09	6.73 e-12	0.579	N/A	N/A
Single Footer (low-Vth)	6.58 e-08	5.68 e-10	0.422		
Two Footers (low-Vth)	4.06 e-09	6.82 e-10	0.530	0.04	
Proposed PG	4.88 e-09	3.19 e-12	0.530	0.08	0.08

Table I shows the simulation result of 30 inverter chains at 0.6-V supply voltage, with each chain having 20 inverters using a 45-nm predictive technology model in which the footer size is 10% of the total NMOS width in the inverter chains. As shown in Table I, the new PG structure decreases the gate leakage by 31% for the inverter chain compared to the high-$V_{\rm th}$ single footer, although the subthreshold leakage is increased due to the weak stack effect: the gate-to-source voltage of M2 in Fig. 1(d) is not negative but is of zero voltage. Therefore, it is expected that the total leakage can be reduced much more as the technology scales down and the gate leakage increases.

B. Ultralow-Voltage PG Based on Dual Virtual Ground

In spite of using low-$V_{\rm th}$ footers, the series-connected low-$V_{\rm th}$ footer scheme reduces leakage power due to the stack effect and smaller footer size, as presented in the previous section. However, it suffers from increased delay, wake-up time, and wake-up fluctuation due to increased resistance. To compensate for the reduced performance, the proposed scheme uses two virtual lines, as shown in Fig. 2, in which M1 and M2 are strong transistors (main footers) and the other weak transistors are deployed for gate leakage reduction, wake-up time reduction, and wake-up fluctuation reduction.

The first virtual ground $V_{\rm VSS1}$ is connected to the gates on the noncritical paths: this connection reduces the leakage current of the gates on the noncritical paths during the sleep mode, although they increase the gate delay during the active mode. On the other hand, the second virtual ground $V_{\rm VSS2}$ is connected to the gates on the critical paths: this connection reduces the gate delay of the critical paths during the active mode, although it increases a certain amount of leakage current of the gates during the sleep mode. The total size of the proposed PG consisting of n-type MOSFETs is smaller than one footer size of the conventional PG because the reduced width of the footer is compensated with a low $V_{\rm th}$ and thin oxide thickness;

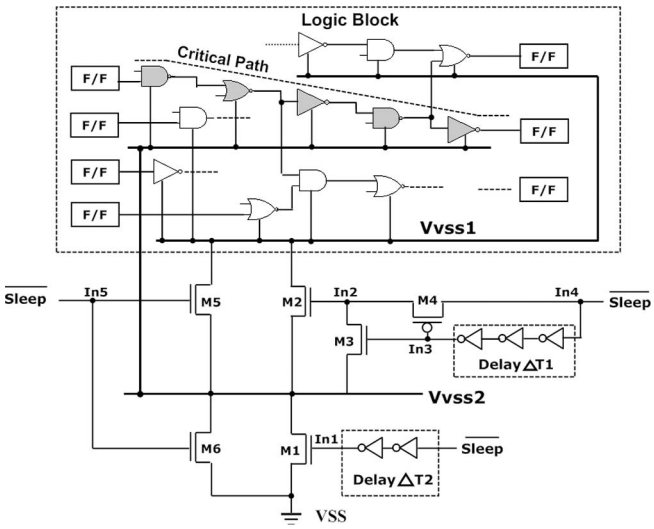

Fig. 2. Block diagram of the proposed PG structure.

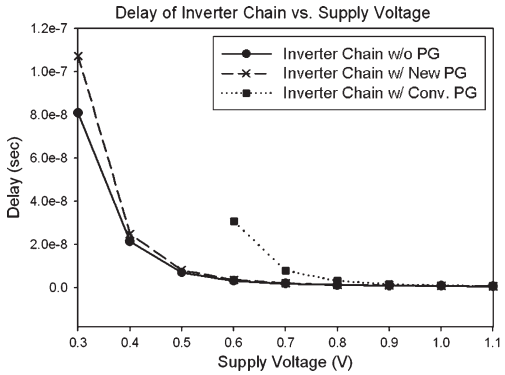

Fig. 3. Delay dependence of the PG structure on the power supply voltage.

the reason is that in the active mode, the footer operates in the linear region, and the footer current is given by

$$I_{\text{footer}} \approx \mu \left(\frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}}\right)\left(\frac{W}{L}\right)(V_{\text{GS}} - V_{\text{th}})V_{\text{VSS}} \qquad (1)$$

where ε_{ox} is the permittivity of SiO_2, t_{ox} is the oxide thickness, μ is the mobility, and V_{VSS} is the virtual ground voltage.

Furthermore, the new structure extends the PG to an ultralow-voltage region while keeping a high speed in the active mode. Fig. 3 presents a simulation result showing the delay dependence of the proposed PG on V_{DD} for 20 inverter chains, and the simulation result is compared with that of the conventional PG and logic block without PG. The inverter chains consist of 16 chains having 30 inverters each and four chains having 40 inverters each using 45-nm CMOS technology. The area overhead of each PG is 10% of the total NMOS width in the inverter chain. For the proposed PG, the 16 chains having 30 inverters are connected to V_{VSS1}, and the four chains having 40 inverters are connected to V_{VSS2}. As V_{DD} decreases below 0.8 V in the active mode, the inverter chain using the proposed PG becomes more than two times faster than the chain using the conventional PG, and its delay decreases by 88.24% compared to the chain using the conventional PG at 0.6 V. Moreover, the delay of the conventional high-V_{th} PG is exponentially increased at a V_{DD} below 0.6 V.

The leakage current during the sleep mode and the wake-up time during mode transition depend on the potential of each

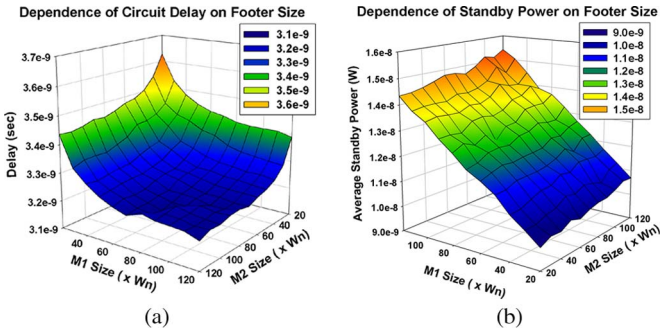

Fig. 4. Dependence of the delay and the standby power on the M1 and M2 sizes for the ISCAS85 C432 circuit. (a) Delay. (b) Average standby power.

virtual ground in the proposed PG. Under the assumption that the logic circuit is two simple inverters and that the footers are biased in the weak inversion region, the steady potential of each virtual ground is obtained by matching the leakage currents of the inverters with the leakage currents of the footers as follows:

$$V_{\text{VSS1}} = \frac{-V_{\text{th}} + 4\eta V_{\text{DD}} - S\log_{10}\left(\frac{W_{\text{M1}}^2 W_{\text{M2}}}{W_{\text{NC}}^3 W_{\text{C}}}\right)}{5\eta} \qquad (2)$$

$$V_{\text{VSS2}} = \frac{-2V_{\text{th}} + 3\eta V_{\text{DD}} - S\log_{10}\left(\frac{W_{\text{M2}}^2}{W_{\text{M1}} W_{\text{NC}} W_{\text{C}}^2}\right)}{5\eta} \qquad (3)$$

where η is the DIBL coefficient, S is the subthreshold slope, W_{M1} and W_{M2} are the width of M1 and M2, respectively, and W_{C} and W_{NC} are the total width of the circuits on the critical paths and noncritical paths, respectively.

From (2) and (3), V_{VSS2} is changed depending on each footer size, which is determined by the performance, and a low V_{VSS2} reduces the leakage current and wake-up time of the gates on the critical paths. Fig. 4 shows the dependence of the delay and standby power on the M1 and M2 sizes for the C432 benchmark circuit using a 45-nm predictive technology model in which the supply voltage is 0.6 V and the total footer size is 130 $\times$ W_n (minimum size), which is 10% of the total NMOS width in C432 circuit. In Fig. 4, as the total size increases, the delay decreases and is saturated to a value of around 40 $\times$ W_n of each M1 and M2 size, and the standby power significantly increases. The circuit delay and the standby power are more dependent on the M1 size than on the M2 size, and the increase rate of the standby power is larger than that of the delay. Therefore, each footer size has to be reduced as much as possible within the delay requirement to effectively decrease the standby power.

C. Wake-Up Rush Current and Wake-Up Time

The proposed PG structure also reduces the magnitude of the rush current through the virtual ground rail, as well as the minimum time (known as the wake-up time) required to stabilize ground rails. If the sleep mode is long enough, the virtual ground will be charged close to V_{DD}. When the footer is fully turned on during the mode transition by a sharp control signal, the virtual ground will sharply be discharged, causing a large transient current. This large current leads to a great fluctuation in the power/ground grid due to the parasite inductance and capacitance in the power and ground pins. In Fig. 2, M5 and M6 suppress the rush current generated at sleep-to-active transition time. The key idea to reduce the rush current during

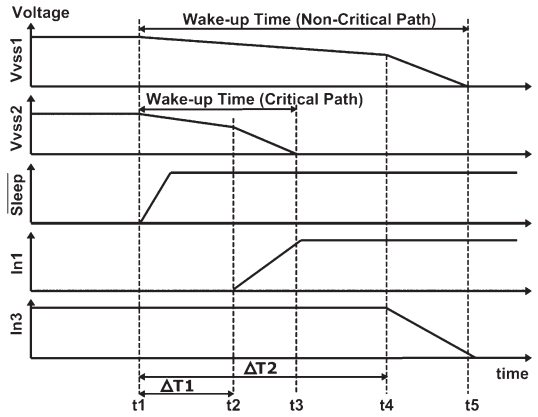

Fig. 5. Virtual ground at sleep-to-active transition time.

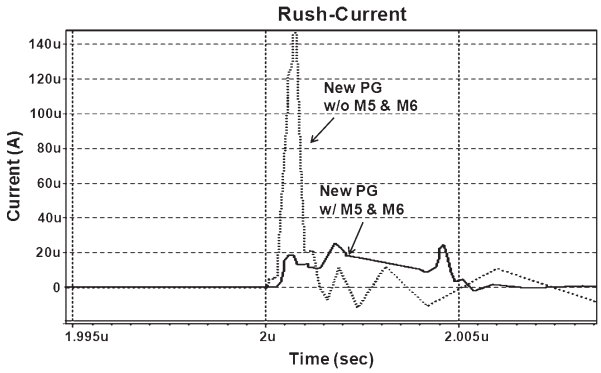

Fig. 6. Rush current of the new PG structure for the 20-inverter chains.

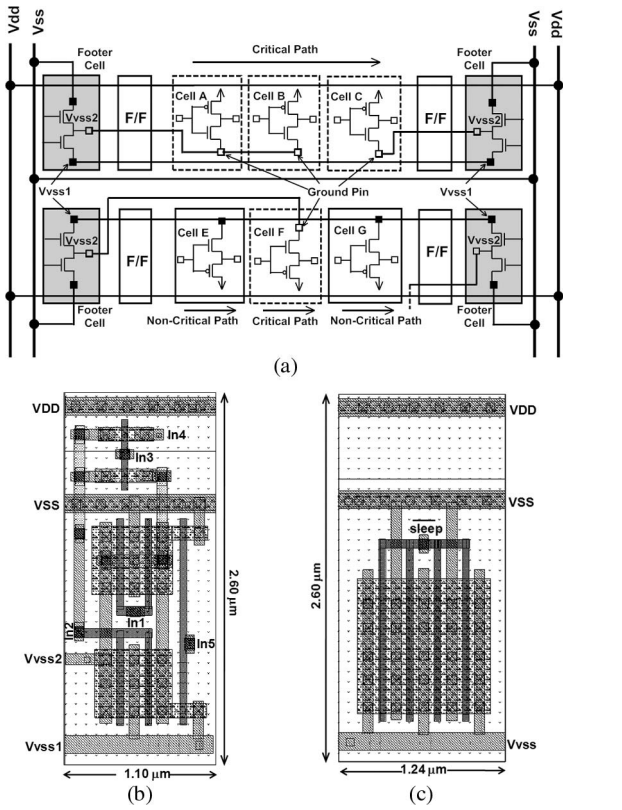

Fig. 7. Conceptual power network for the new PG structure. (a) Power network. (b) Layout of the proposed PG cell for the C432 circuit. (c) Layout of the conventional PG cell for the C432 circuit.

mode transition is to gradually decrease $V_{\rm VSS1}$ and $V_{\rm VSS2}$ with multiple voltage steps. Fig. 5 shows the waveforms of each footer input and the virtual grounds. Initially, the PG structure is partially turned on using M5 and M6 at time t1 (sleep-to-active transition time), then $V_{\rm VSS1}$ and $V_{\rm VSS2}$ begin to drop off. After ΔT1 is induced by a delay line, M1 is turned on, and V_{VSS2} is completely discharged to 0 V at t3 (the wake-up time of the circuits on the critical paths), whereas $V_{\rm VSS1}$ is not fully discharged. After ΔT2 is induced by another delay line, M3 is turned off, and M4 is turned on. Finally, $V_{\rm VSS1}$ is completely discharged at t5 (the wake-up time of the circuits on the noncritical paths). This gradual discharging approach considerably reduces the rush current during mode transition. The rush current has to be reduced as much as possible since the noise margin of circuits is small in the ultralow-voltage region. Fig. 6 presents the large reduction in the rush current when M5, M6, and delay lines are inserted to the series-connected PG.

On the other hand, the wake-up time increases as the rush current decreases. Therefore, the tradeoff between the rush current and the wake-up time has to be considered under the condition that the wake-up time is less than two or three clock cycles. In this approach, ΔT1 is smaller than ΔT2, which means that the circuits on the critical path wake up earlier than those on the noncritical path. This also means that this approach decreases the effective wake-up time maintaining the low rush current.

D. Power Network Design

For the simple cell-based physical design of the new PG, the new PG cell can be placed in the same placement strategy as that of the conventional cell-based PG, except $V_{\rm VSS2}$: $V_{\rm VSS1}$ is connected to the local ground rail in the same way as the virtual ground of the conventional PG, whereas $V_{\rm VSS2}$ is used as a pin to connect the ground pins of the modified logic cells on the critical paths. The lines between $V_{\rm VSS2}$ and the logic cells on the critical paths are routed as intercell wires. Fig. 7(a) and (b) shows the conceptual power network for the new PG structure and the layout of the proposed PG cell for the C432 circuit, respectively. The layout of the conventional PG cell is shown in Fig. 7(c) to compare it with that of the proposed PG cell.

III. Experimental Results

The proposed PG structure using a 45-nm predictive technology model has been implemented and evaluated using inverter chains designed in the same technology in which $V_{\rm DD}$ is 0.6 V, the low $V_{\rm th}$ and the high $V_{\rm th}$ are 0.165 and 0.524 V for NMOS, respectively (-0.165 and -0.524 V for PMOS), and the $t_{\rm ox}$ of the low-$V_{\rm th}$ MOS and that of high-$V_{\rm th}$ MOS are 1.1 and 1.9 nm, respectively. In this experiment, the power network model is used to get more accurate results: L (the bonding/package inductance) is 2 nH, R (the supply network resistance) is 0.05 Ω, and C (the supply network capacitance) is 0.05 pF. The footer size of the conventional PG schemes used in this experiment is 10% of the total NMOS width in each original logic block, whereas the size of the proposed PG is smaller than 10% of the total NMOS width, and the upper footer size is equal to the lower footer size. All the simulation results have been measured using random input test vectors. To show the good balance of the proposed methodology among the wake-up time, the delay, the wake-up

TABLE II
SIMULATION RESULTS FOR THE INVERTER CHAINS

Power Gating Scheme (Vdd=0.6)	Normalized by Low-Vth Designed Logic Block			Normalized by Conventional PG		
	Leakage Power	**Delay**	Area	Wake-up Power	**Wake-up Time**	Wake-up Noise
Low-Vth logic w/o PG	1.000	1.000	1.000	N/A	N/A	N/A
High-Vth logic w/o PG	0.004	143.3	1.000			
Dual-Vth logic w/o PG	0.252	0.993	1.000			
Conventional PG	0.042	7.925	1.100	1.000	1.000	1.000
Multi-mode PG	0.043	7.928	1.103	1.016	1.010	0.895
Two-pass PG	0.041	7.647	1.103	0.958	0.958	0.568
Zigzag PG	0.094	Fail	1.150	0.178	0.309	0.126
Selective PG	0.013	6.968	1.025	0.254	0.998	0.054
New PG	0.082	**1.079**	1.064	0.520	**0.020**	0.014

Note : For ultra-low voltage circuits such as below 0.6 V, previous PG schemes (Conventional PG[1], Multi-mode PG[4], Two-pass PG[5], Zigzag PG[6], and Selective PG[7]) cannot be used due to the impractical delay increase and long wake-up time.

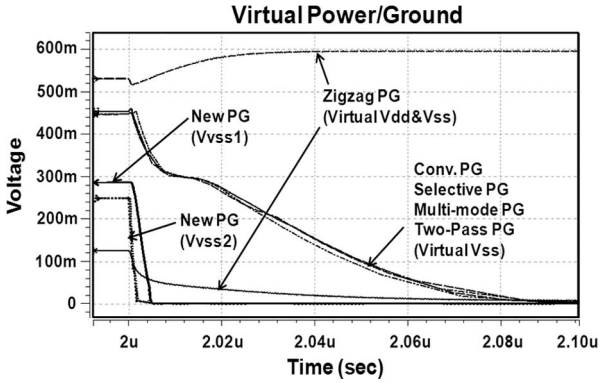

Fig. 8. Wake-up time of the new PG structure.

power, the wake-up fluctuation, and the leakage power of the PG structure, the 20 inverter chains used in Section II-B are simulated for nine circuit schemes at two temperature conditions (25 °C for the sleep mode and 125 °C for the active mode) and compared, as shown in Table II. As expected, the results present that the new PG provides good balance among all the critical issues, and previous high-$V_{\rm th}$-based PG schemes cannot be used for ultralow-voltage circuits due to the impractical delay increase and long wake-up time. Fig. 8 shows the virtual ground voltage of previous PG structures and the proposed PG structure during the sleep-to-active mode transition.

To show the efficiency of the new PG at 0.6-V supply voltage, the ISCAS85 benchmark circuits are also simulated for a low-$V_{\rm th}$ logic block, the conventional PG, and the proposed PG in the same conditions as those for the inverter chains, except that the total footer size of the proposed PG is almost 5% of the total NMOS width to get a 5% delay penalty. For this simulation, the longest paths of each ISCAS85 circuit are extracted using a static timing analysis tool and the conventional algorithm of dual-$V_{\rm th}$ CMOS circuits [10], and all the cells on the critical paths are modified from virtual ground pins ($V_{\rm VSS2}$ is assigned to 20% of the transistors on the critical paths on the average). As shown in Table III, the proposed PG structure reduces the gate leakage by 71.07%, the delay by 35.66%, the wake-up power by 6.87, the wake-up time by 98.02%, and the area by 47.63 on the average for the ISCAS circuits compared to the conventional PG structure where the wake-up fluctuation items for the both structures are left out because it can be negligible (less than 0.002 V),

TABLE III
SIMULATION RESULTS FOR ISCAS85 BENCHMARK CIRCUITS

Logic	Normalized by Logic Block		Normalized by Conventional PG					
	Leak. Power	Delay	Leak. Power	Gate Leak. Power	Delay	Wake-up Power	Wake-up Time	Area
C432	0.128	1.026	1.088	0.182	0.793	0.963	0.025	0.423
C880	0.155	1.095	1.143	0.407	0.351	0.933	0.022	0.485
C1355	0.114	1.034	0.869	0.403	0.648	1.017	0.026	0.458
C1908	0.083	1.057	0.849	0.102	0.674	1.002	0.018	0.460
C2670	0.110	1.096	1.395	0.573	0.444	0.954	0.018	0.497
C5315	0.018	1.046	0.976	0.340	0.885	0.962	0.017	0.500
C6288	0.090	1.043	1.348	0.134	0.490	0.979	0.014	0.500
C7552	0.012	1.008	1.142	0.417	0.934	0.380	0.018	0.487
Avg. Rate	90.03 (%)	-5.16 (%)	-11.8 (%)	**71.07** (%)	**35.66** (%)	6.87 (%)	**98.02** (%)	**47.63** (%)

and the total leakage is slightly increased by 11.08% on the average under the influence of the subthreshold leakage, but it is expected that the total leakage can be reduced much more as the technology scales down and the gate leakage increases.

IV. CONCLUSION

This brief has proposed a novel PG structure using a single low-threshold voltage in ultralow-voltage nanoscale circuits. To extend the PG structure to the sub-1-V region, series-connected footers with a single low $V_{\rm th}$ have been used. For the subthreshold and gate leakage reduction of the low-$V_{\rm th}$ footers, a new approach has been proposed. Finally, to solve rush current and wake-up time issues, the virtual ground has gradually been decreased with multiple voltage steps. The results have shown that the proposed PG structure is a practicable solution for high-energy reduction in the ultralow-voltage nanoscale CMOS circuits.

REFERENCES

[1] K. Shi and D. Howard, "Challenges in sleep transistor design and implementation in low-power designs," in *Proc. IEEE Des. Autom. Conf.*, Jul. 2006, pp. 113–116.
[2] M. Anis, S. Areibi, and M. Elmasry, "Design and optimization of multi-threshold CMOS (MTCMOS) circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 22, no. 10, pp. 1324–1342, Oct. 2003.
[3] S. Kim, C. J. Choi, D.-K. Jeong, S. V. Kosonocky, and S. B. Park, "Reducing ground-bounce noise and stabilizing the data-retention voltage of power-gating structures," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 197–205, Jan. 2008.
[4] S. Kim, S. V. Kosonocky, D. R. Knebel, K. Stawiasz, and M. C. Papaefthymiou, "A multi-mode power gating structure for low-voltage deep-submicron CMOS ICs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 7, pp. 586–590, Jul. 2007.
[5] P. Royannez, H. Mair, F. Dahan, M. Wagner, M. Streeter, L. Bouetel, J. Blasquez, H. Clasen, G. Semino, J. Dong, D. Scott, B. Pitts, C. Raibaut, and U. Ko, "90 nm low leakage SoC design techniques for wireless applications," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2005, pp. 138–139.
[6] Y. Shin, S. Paik, and H.-O. Kim, "Semicustom design of zigzag power-gated circuits in standard cell elements," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 28, no. 3, pp. 327–339, Mar. 2009.
[7] K. Usami, N. Kawabe, and M. Koizumi, "Automated selective multi-threshold design for ultra-low standby applications," in *Proc. IEEE Int. Low Power Electron. Des.*, Aug. 2002, pp. 202–206.
[8] H. Kawaguchi and T. Sakurai, "A super cut-off-CMOS (SCCMOS) scheme for 0.5-V supply voltage with pico-ampere stand-by current," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1498–1501, Oct. 2000.
[9] Y. Shin, S. Heo, H. Kim, and J. Choi, "Simultaneous control of subthreshold and gate leakage current in nanometer-scale CMOS circuits," in *Proc. IEEE Des. Autom. Conf.*, Jan. 2007, pp. 654–659.
[10] L. Wei, Z. Chen, K. Roy, M. C. Johnson, Y. Ye, and V. K. De, "Design and optimization of dual-threshold circuits for low-voltage low-power applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 7, no. 1, pp. 16–24, Mar. 1999.