INVITED PAPER

Carbon Nanotubes for VLSI: Interconnect and Transistor Applications

Use of nanotubes to fabricate MOSFETs, interconnects, and vias is discussed in this paper; a technique is proposed to use fixed charges to control carrier polarity.

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ABSTRACT | Carbon nanotubes (CNTs) offer unique properties such as the highest current density, ballistic transport, ultrahigh thermal conductivity, and extremely high mechanical strength. Because of these remarkable properties, they have been expected for use as wiring materials and as alternate channel materials for extending complementary metal–oxide–semiconductor (CMOS) performance in future very large scale integration (VLSI) technologies. In this paper, we report the present status of CNT growth technologies and the applications for via interconnects (vertical wiring) and field-effect transistors (FETs). We fabricated CNT via and evaluated its robustness over a high-density current. In our technology, multiwalled carbon nanotubes (MWNTs) were successfully grown at temperatures as low as 365 °C using Co catalyst nanoparticles, which were formed and deposited by a custom-designed particle generation and deposition system. The density of MWNTs grown at 450 °C reaches more than 1×10^{12} /cm^2. MWNTs were grown in via holes with a diameter as small as 40 nm. The resistance of CNT vias with a diameter of 160 nm was found to be of the same order as that of tungsten plugs. The CNT via was able to sustain a current density as high as 5.0×10^6 A/cm^2 at 105 °C for 100 h without any deterioration in its properties. We propose a Si-process compatible technique to control carrier polarity of CNFETs by utilizing fixed charges introduced by the gate oxide. High-performance *p*- and *n*-type CNFETs and CMOS inverters with stability in air have been realized.

KEYWORDS | Carbon; field-effect transistors (FETs); high-speed electronics; interconnections; nanotechnology; wiring

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I. INTRODUCTION

A carbon nanotube (CNT), which is made by rolling up a sheet of graphite or graphene (a monolayer of sp2 bonded carbon in a honeycomb lattice) into a cylinder [1], exhibits not only unique atomic arrangements (Fig. 1) but also interesting physical properties [2], including current carrying ability [3], long ballistic transport length [4], high thermal conductivity [5], and mechanical strength [6], [7]. These remarkable properties make CNTs one of the most important emerging research materials (ERM) for not only the front-end devices [8] but also back-end devices [9]–[11] for LSIs for the next decade. The number of published CNT-related papers increases monotonously and reached

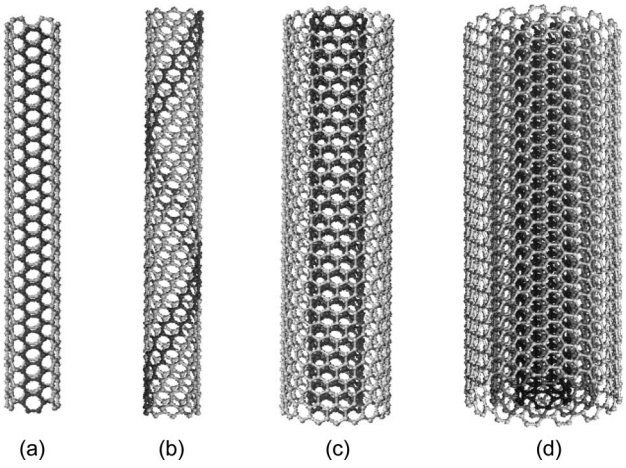

Fig. 1. *Structures of single-walled [(a) arm-chair-type, (b) zigzag-type], (c) double-walled, and (d) multiwalled nanotubes.*

more than 8000 per year in 2009. At the 2008 public conference of the International Technology Roadmap for Semiconductors (ITRS), ERM and emerging research device (ERD) working groups recommended carbon-based nanoelectronics as promising ERD technologies with targeting of commercial demonstration in the 5–10-year horizon [12]. Their advantages are not only that they can provide a technology platform enabling a new "beyond complementary metal–oxide–semiconductor (CMOS)" information processing paradigm, such as spintronics, but also they potentially can have an impact on scaled CMOS device and circuits by providing an alternate field-effect transistor (FET) channel and an alternate metal wiring. Both multiwalled CNTs (MWNTs) and single-walled CNTs (SWNTs) are potentially viable candidates for LSI interconnects, while both SWNTs and double-walled CNTs (DWNTs) are potentially viable candidates for channels. We already reported selective synthesis of SWNTs, DWNTs, and MWNTs from size-controlled catalytic nanoparticles by adjusting the dilution ratio of source gas for low-temperature chemical vapor deposition (CVD) [13]. CNTs are also expected as management candidates for assembly and package applications in 3–5 years to enable reliable electrical and thermal interconnects [14]–[16]. The time frame of assembly and package applications seems to be earlier than those of interconnects and FETs. Even if there is a target application of a new material in semiconductor LSIs, the introduction of the new material would not have to start with such a target application. Once the new material has been employed in some part of LSI, it would be expected that the knowledge and application of the material will gradually expand. Needless to say, materials that have compatibility with the conventional Si LSI technology are more likely to be employed. In this paper, we discuss CNT technologies for future LSIs, in particular, CNT via interconnects and CNT-FETs.

II. CNT VIA INTERCONNECTS: FABRICATION AND ELECTRICAL PROPERTIES

A. Introduction

Advanced very large scale integrations (VLSIs) employ copper (Cu) as an interconnect material because of its low resistivity. A continuing shrinkage in the dimensions of LSIs, however, is causing increase in the current density in the Cu interconnect [17], and this makes the Cu interconnect unreliable due to electromigration problems, as shown in Fig. 2. CNTs are one of the promising candidates to replace Cu as an interconnect material due to their excellent electrical properties. These include abilities to sustain a current density as high as 10^9 A/cm^2 [3], which is two to three orders of magnitudes higher than that for Cu, and to exhibit a ballistic transport along the tube, which may be the solution to the high-resistance problem in scaled-down vias [4]. Also, conventional copper vias need a barrier layer, which results in an increase in resistance and in process complexity. CNT vias do not need sidewall barrier layers. In fact, there have been several reports on the use of MWNTs for LSI via interconnects (Fig. 3) [18]–[21]. In order to construct CNT vias, however, there are several issues to be addressed. One of them is the need to lower the electric resistance of the CNT via. Apparently, the more CNTs that are in a via hole, the lower the resistance is. Although close-packed-grown CNTs are desirable, it is not easy to obtain such CNTs. We previously grew MWNTs in via holes using sputtered Co film as a catalyst and the site density of the MWNTs was around 5×10^{10} cm^{-2}, which accounted for only a few percent of the space in the via hole [22]. In that case, it is believed that the Co film became particles by heating and that MWNTs grew from such particles. In order to increase the CNT density further, the number of particles in the via hole should somehow be controlled. Another issue

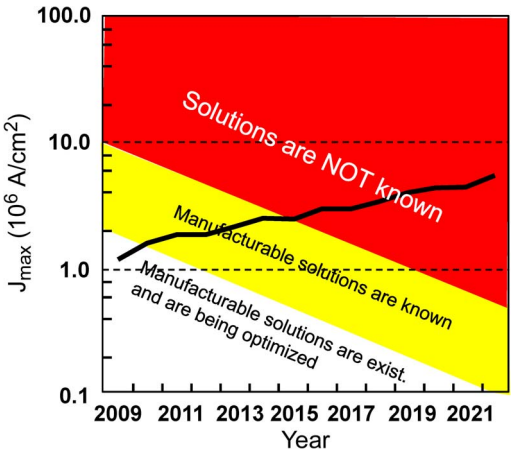

Fig. 2. *Maximum current density requirement for local interconnects (ITRS public conference 2009).*

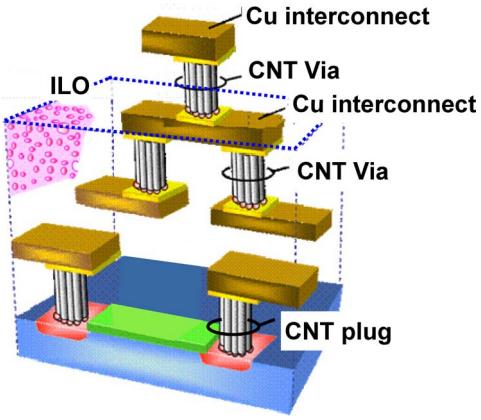

Fig. 3. *Schematic view of CNT via interconnects.*

is to lower the growth temperature of CNTs. A growth temperature of 450 °C or lower is at least required to avoid any damage to LSIs. In our former studies above, the growth temperature ranged from 540 °C to 450 °C [18], [19], [22]. Although studies regarding the low-temperature CNT growth have been reported [23]–[25], there are few studies showing the electrical properties, especially for a maximum current density, of CNTs grown at low temperatures down to 400 °C. One of the other important issues for realizing CNT vias is to develop a fabrication process that is compatible with the standard LSI processes. Especially, planarization of a substrate with CNT vias is essential. In this section, we introduce our recent progress in developing the CNT via technologies [26]–[29]. We first describe a novel process to fabricate CNT vias. This process includes the deposition of size-controlled catalyst nanoparticles using a custom-designed particle deposition system [26], low-temperature growth of MWNTs (510 °C–365 °C) using such catalyst particles [27], [28], and planarization of a substrate with CNT vias by chemical mechanical polishing (CMP) [29]. We then show the electrical properties of vias made of bundles of MWNTs, including their electrical resistance and robustness over a high current density [27], [28].

B. CNT via Process

A typical fabrication process of a CNT via is schematically shown in Fig. 4. We proposed CNT damascene process to integrate scaled-down CNT vias with Cu interconnects [27]. The processes were mostly compatible with conventional Cu interconnects. A substrate with a Cu interconnect covered by a dielectric layer was first prepared. The dielectric layer was SiOC with a dielectric constant (k) of 3.0 or 2.6. Via holes with a diameter of 160 nm were made using conventional photolithography followed by dry etching. A TaN/Ta barrier layer and a TiN contact layer were deposited by physical vapor deposition (PVD). Size-controlled Co particles with a mean diameter of about 4 nm were then deposited using a custom-designed particle generation and deposition system, which is explained in Section II-C. MWNTs were grown by thermal CVD with C_2H_2 diluted by Ar as the source gas. The pressure of the source gaswas 1 kPa. The substrate temperature ranged from 365 °C to 510 °C. The substrate with MWNTs was then coated with spin-on glass (SOG) and planarized by CMP. The CMP condition was similar to the one used for polishing a silicon dioxide layer. Actually, the substrate was

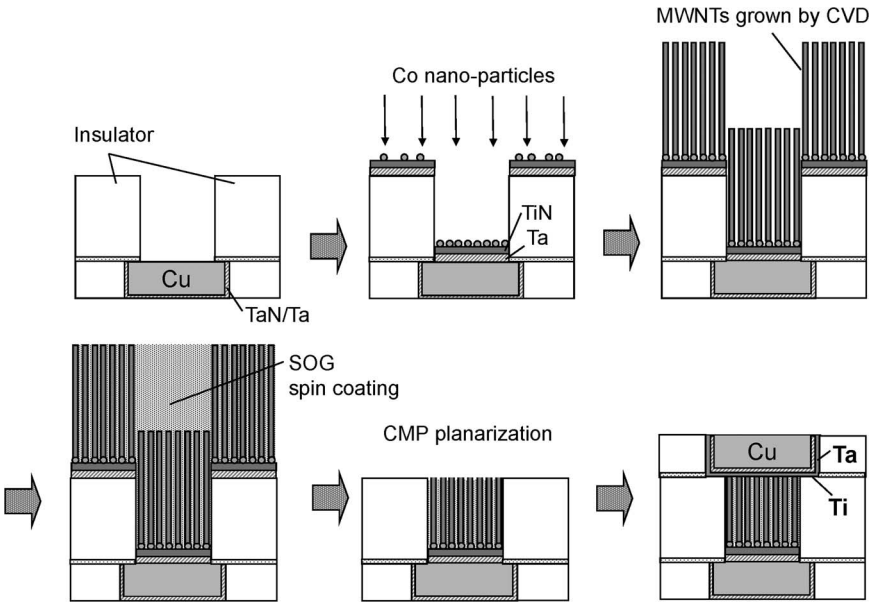

Fig. 4. *Typical fabrication process of a CNT via.*

polished with conventional IC1000 pad and silica slurry under pressures of 2 psi (13.8 kPa) for 150 s. Finally, a Ti top contact layer, a Ta barrier layer, and a Cu wire were connected to the CNT vias by PVD. Although CNT vias with a diameter of 160 nm were mainly used for evaluating the electrical properties, we also prepared CNT vias with different diameters, ranging from 2800 to 40 nm.

C. Preparation and Deposition of Catalyst Nanoparticles

In this section, the particle generation and deposition system used in this study is described. This new system was briefly described in our previous paper [30], but more detailed descriptions are given here. The system is schematically illustrated in Fig. 5. Cobalt catalyst particles were generated by laser ablation of a Co target in a low-pressure He environment (~1 kPa) [31], [32]. A pulsed Nd:YAG laser (wavelength: 532 nm; power: 2 W; repetition frequency: 20 Hz) was employed for this purpose. The particles were then brought to a size classifier consisting of an impactor with a 1–2 slpm (standard liter per minute) of He carrier gas. An impactor is a piece of apparatus often used in the aerosol field in order to collect ambient particles using their inertia [33]. Here we designed an impactor for the purpose of classifying particles smaller than 5 nm, which is something that had probably not been attempted before. Briefly, an impactor consists of a nozzle and a downstream impaction plate. Particles are accelerated with a carrier gas in a nozzle and directed to the impaction plate. If the inertia of the particles is large enough, they collide with the plate and are collected. As a result, those particles with a smaller inertia (i.e., particles of smaller sizes) are brought downstream with the carrier gas. The size of particles penetrating with a 50% probability (cut size) can be controlled by parameters such as the gas flow rate, gas pressure, and nozzle diameter [33]. Although the impactor removes only larger particles, nanometer-size particles usually have a smaller size limit due to particle growth by condensation and coagulation. Therefore, particles with a relatively narrow size distribution can be obtained just by using the impactor. In our experiments, the experimental conditions were optimized to obtain particles with a mean diameter of ~4 nm. The size-classified particles were then led to a high-vacuum deposition chamber (~10^{-3} Pa) via differential pumping to form a directed particle beam. The directed particles beam enables us to deposit particles at the bottom of tiny via hole patterns. The movable substrate stage enabled particle deposition all over the substrate. The current system can handle a substrate up to 200 mm in diameter. The typical deposition rate was 10^{13}–10^{14} min^{-1}, which was about 1000 times higher than the previous system using the differential mobility analyzer (DMA) [31], [32]. We expect that the deposition rate will be increased furtherby scaling up the system.

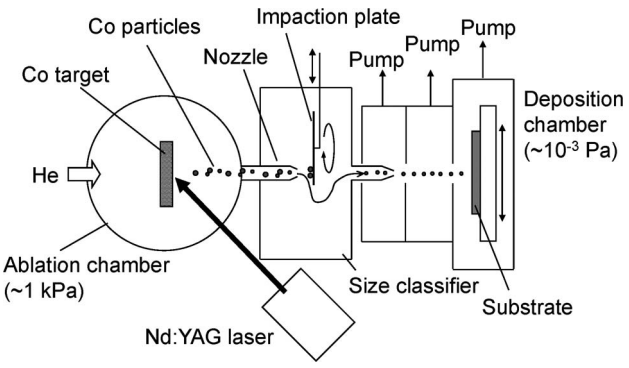

Fig. 5. ***Particle generation and deposition system.***

D. Size-Classified Catalytic Nanoparticles for CNT Diameter Control

A scanning electron microscope (SEM) image of Co particles classified with the impactor is shown in Fig. 6(a). A transmission electron microscope (TEM) image along with an electron diffraction pattern is also shown [Fig. 6(b) and (c)]. In this case, the Stokes number, which is a dimensionless parameter to control particle deposition in an impactor [33], was 0.5 for particles with a diameter of 4.2 nm. The size distribution of particles is shown in Fig. 6(d). The geometric mean diameter and geometric standard deviation obtained from the TEM images were 3.8 nm and 1.21, respectively. Fig. 7(a) shows cross-sectional SEM images of test via holes with a lateral size of ~100 nm after particle deposition. Particles at the bottom of a via hole can be clearly seen, while there are few particles found on the sidewall. The particles were also deposited at the bottom of a 40-nm diameter hole [Fig. 7(b)]. In our deposition system, the directionality of particles can be controlled according to the choice of orifices used in the differential pumping unit. Therefore, in principle, our system can deposit catalyst particles at the bottom of via holes with an even smaller diameter and a high aspect ratio.

E. CNTs Grown in via Holes

Fig. 8(a) and (b) are the cross-sectional SEM images of MWNTs grown in via holes with a diameter of 160 nm at growth temperatures of 450 °C and 400 °C. We can see in the images that MWNTs grown at 400 °C are a little less straight than those grown at 450 °C, suggesting that MWNTs at 400 °C are a little more defective. To elucidate the quality of MWNTs, we performed TEM analyses, and the results are shown in Fig. 9(a) and (b). The TEM images indicate that MWNTs grown at either temperature are of high quality, although, again, MWNTs at 400 °C might be a little more defective. Incidentally, it is considered that the low-temperature growth we have achieved is partly due to the existence of the TiN layer under Co particles. In fact, we could not grow CNTs under the same growth conditions

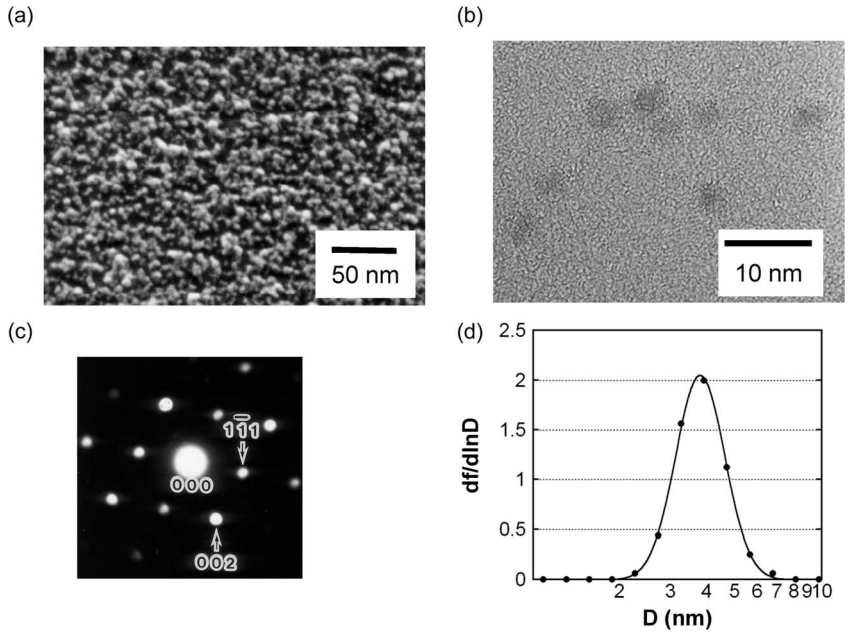

Fig. 6. *Cobalt particles obtained by the particle generation and deposition system: (a) SEM image; (b) TEM image; (c) electron diffraction pattern from a Co particle; and (d) size distribution obtained from TEM images. The vertical axis shows a number fraction divided by the logarithmic range width. The curves were obtained by fitting a log-normal distribution to the distribution data.*

without the TiN layer. This result is similar to our former experimental results showing that alloy particles consisting of Co and Ti are more effective as a catalyst for CNT growth than pure Co particles [32]. The average site density of MWNTs in the 160-nm via holes was 3×10^{11} cm^{-2}. Fig. 8(c) shows MWNTs grown in a via hole with a diameter of 40 nm (growth temperature: 510 °C). In this case, the MWNT density was 9×10^{11} cm^{-2}. The site densities of MWNTs were higher than those in the former studies in which a catalyst film had been used for CNT growth [18], [19], [22]. However, the particle site density was actually about 5×10^{12} cm^{-2}, so we have not yet succeeded in growing MWNTs from all the particles available. Incidentally, Figs. 8(d) and 9(c) show SEM and TEM micrographs, respectively, of MWNTs grown at 365 °C. Surprisingly the product still has a tubular structure. We are planning to fabricate vias made of MWNTs grown at this low temperature in the near future. By optimizing catalyst and thermal CVD conditions, we

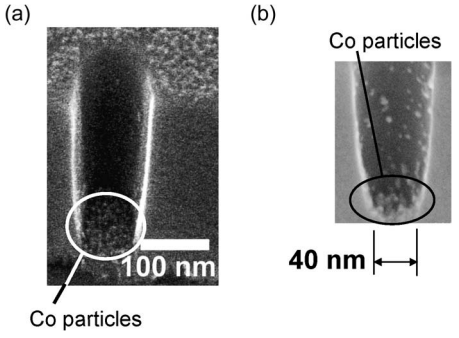

Fig. 7. *Cobalt particles deposited in via holes with a (a) lateral size of 100 nm, and a (b) diameter of 40 nm.*

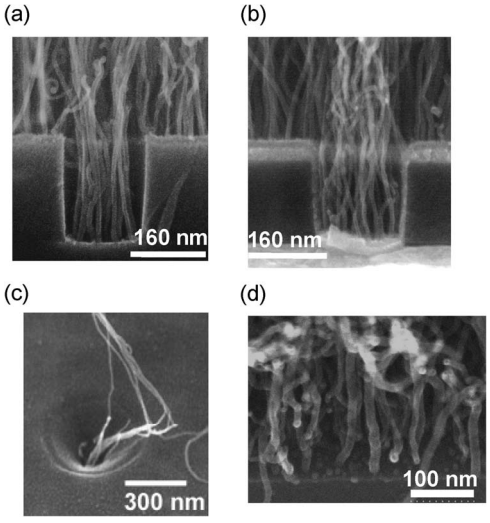

Fig. 8. *Cross-sectional SEM images of MWNTs grown in a viahole at (a) 450 °C, and (b) 400 °C. (c) SEM images of MWNTs grown in a via hole with a diameter of40 nm at 510 °C. (d) SEM image of MWNTs grown at 365 °C.*

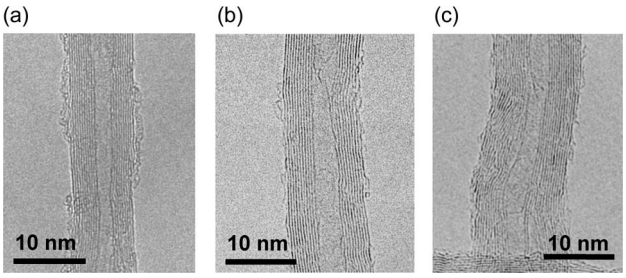

Fig. 9. *TEM images of MWNTs grown at (a) 450 °C, (b) 400 °C, and (c) 365 °C.*

successfully obtained a higher site density of 1.4×10^{12} cm^{-2} at 450 °C, as shown in Fig. 10(a) [34], [91]. High-density CNT growth can also be obtained by a plasma-based CVD. For this purpose, we developed a new growth procedure, a multistep growth [35]. This method consists of three steps: an extremely high-density catalytic nanoparticle formation, CNT nucleation process, and CNT growth, where these are performed by an optimized plasma condition individually. It is noteworthy that nanoparticles covered with graphene shells obtained in second step are effective not only for inhibiting aggregation completely but also for increasing the yield of CNT growth. Fig. 10(b) shows a high-density CNT forest grown at 450 °C by the plasma CVD method [25], [35]. The CNT packing density was estimated to be also 1×10^{12} cm^{-2}. We confirmed that the plasma method is applicable to an ultrafine via [36].

F. Electrical Properties of CNT Vias

The resistances of 160-nm CNT vias were measured with a four-point probe using Kelvin patterns. The current-voltage characteristics are shown in Fig. 11(a). It was found that the resistance depended on the growth temperature. The via resistance was 34 Ω for a growth temperature of 450 °C, and 64 Ω for 400 °C [28]. As shown in Figs. 8 and 9, there is little difference between these two growth temperature in CNT density (3×10^{11}/cm^3), shell number, and diameter of the CNTs. It is considered that the difference in resistance may have been caused by the difference in CNT quality. The resistance obtained at 450 °C is of the same order as that of W plugs and one order of magnitude higher than that of Cu [37]. Recently, a resistance of 450Ω at low voltage for a CNT via with a width of 300 nm was reported by another research group [38], which is, however, not as good as our resistance values above. Fig. 11(b) shows the temperature dependence of the via resistance of 2.8-um-diameter CNT vias grown at 450 °C [27]. The resistance of the via of 520-nm height decrease by decreasing the temperature, which is typical Ohmic-type temperature dependence, which has been attributed to phonon scatterings. On the other hand, the resistance of 60-nm-height vias is independent of temperatures up to about 400 K. This suggests that the carrier transport in this shorter via might be ballistic. In order to confirm the another evidence for ballistic transport, we estimated the via resistance from the number of nanotubes and the shell numbers of a nanotube in the via, which were measured by SEM and TEMs. If we assume the ballistic transport, we can estimate the via resistance of about 0.05 Ω, which agrees well with the experimentally obtained value for the 60-nm via height. This result also suggests that the carrier transport must be ballistic for the 60-nm via height [27]. Fig. 11(c) shows via resistance as a function of the via height, and all the data are normalized to a diameter of 2.8 um. The dashed lines indicate the via resistance obtained by assuming various ballistic lengths for CNTs based on the theoretical model [39]. As can be seen in the figure, the data points for 450 °C fall on the line for a ballistic length of 80 nm. On the other hand, the resistance for 400 °C falls on the line for a ballistic length of 40 nm, which suggests the quality of CNTs grown at 400 °C is not as high as those grown at 450 °C, as can also be imagined from the TEM results. The ballistic length of 80 nm at the 450 °C is about the same as the via height for LSIs of the hp32-nm technology node.

The stability of the via resistance under an electric current of a density of 5.0×10^6 A/cm^2 is shown with a cross-sectional TEM image in Fig. 12 [28]. The via diameter and growth temperature were 160 nm and 400 °C, respectively. The dielectric layer was made of SiOC with $k = 2.6$ (referred to as "ULK"). The measurement was performed at 105 °C in a vacuum. The resistance remained stable even after running the electric current for 100 h. This indicates that the CNT via is robust over a high-density current as we expect. The robustness of CNT vias demonstrated here, however, is still similar to that of Cu. This is mainly because the MWNTs filled only part of the space in the via hole. We expect that CNT vias with a higher CNT density will be much more robust than Cu vias. N. Srivastava *et al.* [10] demonstrated from their simulations that the CNT vias integrated with Cu interconnects can greatly reduce the interconnect temperature rise, which is due to the CNT's high thermal conductivity, and consequently improve the Cu interconnect lifetime by two orders of magnitude. The CNT density

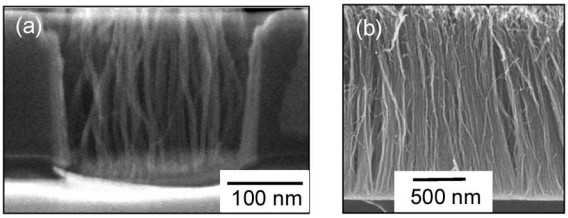

Fig. 10. *A SEM images of high-density MWNTs (> 1×10^{12} /cm^2) grown at 450 °C by (a) thermal CVD [34], [91] and (b) plasma CVD [35].*

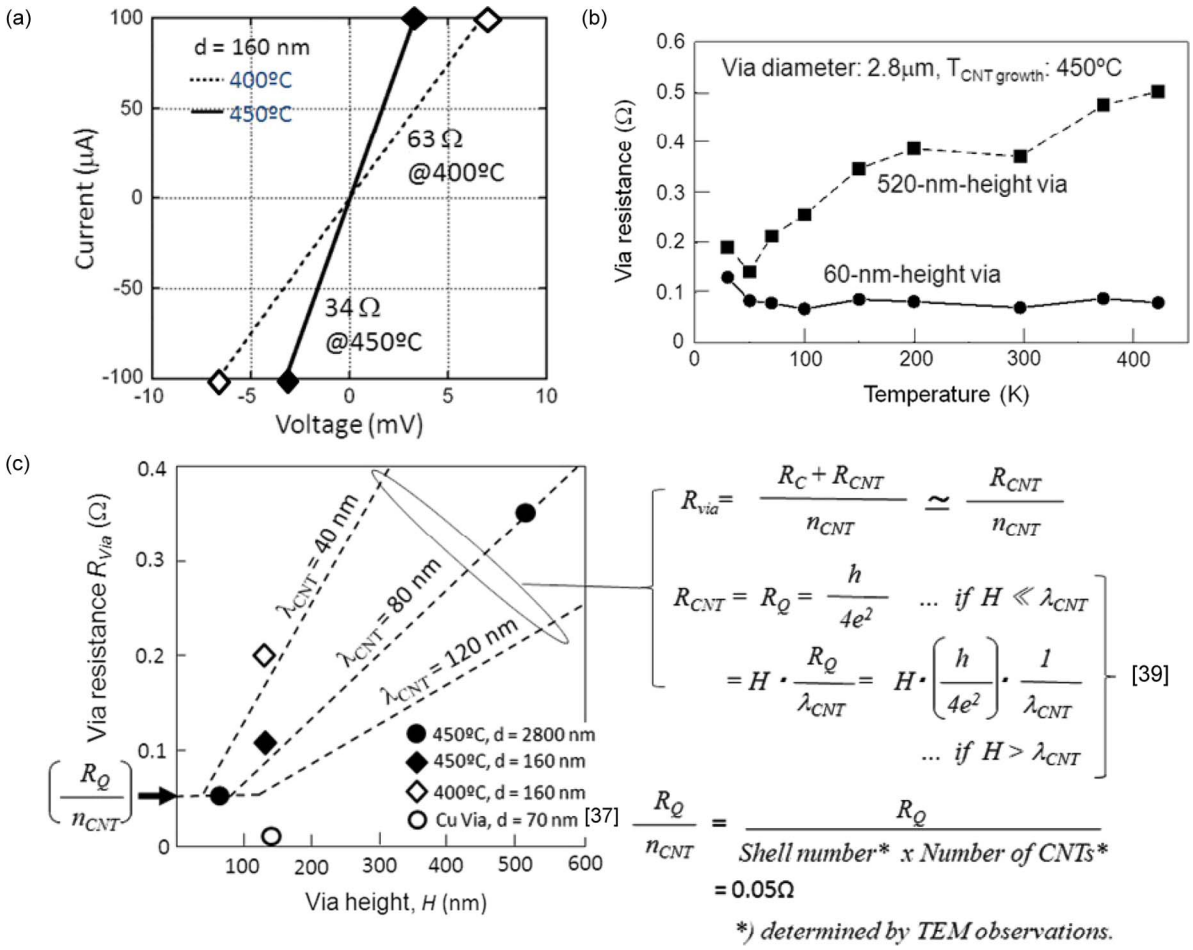

Fig. 11. *(a) Current-voltage characteristics of 160-nm CNT vias. (b) Temperature dependent of via resistance and (c) via resistance as a function of the via height. The data are normalized to a via diameter d of 2800 nm. The dash lines indicate the via resistance obtained by assuming various ballistic lengths for CNTs λ [39].*

of 3×10^{11} cm^{-2}, which we applied, seems to be not high enough to realize such a thermal advantage. Incidentally, the via shape looks deformed in the TEM image, but this was actually caused by high-energy electrons during the TEM observation. Although the ULK is vulnerable to heat, we found that it was not damaged during CNT growth thanks to our low growth temperature.

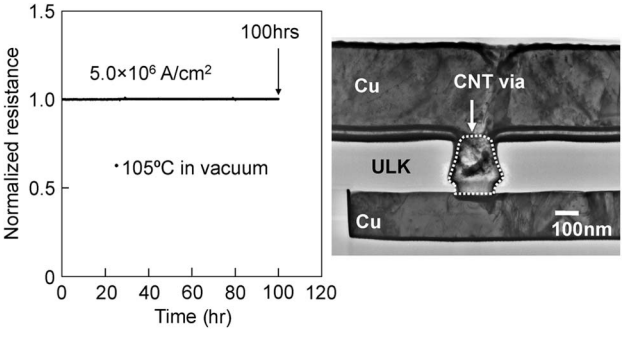

Fig. 12. *Stability of the via resistance under an electric current of a density of 5.0 $\times$ 10^6 A/cm^2. A cross-sectional TEM image of the CNT via is also shown.*

In this paper, we are mainly focusing on via interconnects, however, high-density CNT growth technology mentioned above can be applied for horizontal wiring by using contact blocks with the catalytic metal on the side surfaces [40]. A circuit level demonstrations of CNT horizontal wirings using a CNT transfer technology (not a direct CVD growth technology on the substrate) has been reported [41]. There are several excellent papers on the theoretical predictions of electrical performance of CNT horizontal wirings [9]–[11] and multilayered graphene nanoribbon (GNR) horizontal wirings [42]. GNRs are a very promising candidate because of their patternability using conventional lithography and etching techniques, however, there are still several issues to be addressed, including growth temperature as low as 400 °C [43].

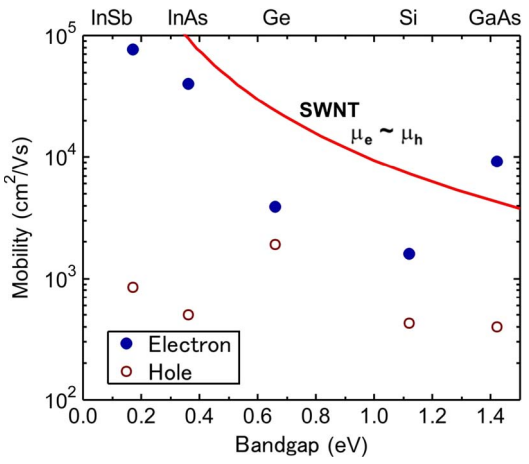

Fig. 13. *Carrier mobilities of s-SWNTs and conventional semiconductors versus bandgap.*

III. CNT FIELD-EFFECT TRANSISTORS FOR FUTURE CMOS CIRCUITS: FABRICATION AND CONTROL OF CONDUCTION PROPERTY

A. Introduction: Advantages of SWNTs as a Channel Material of CMOS Devices

The s-SWNTs are promising candidate for the channel material of CMOS devices because of their two advantages over the other semiconductor materials: the high carrier mobility (μ) and 1-D thin body. Fig. 13 shows μ of s-SWNTs [44] and representative semiconductor materials [45], versus bandgap energy (E_g). For s-SWNTs, μ depends on E_g, which is inversely proportional to the diameter $\sim 0.9/d$ (eV) [2]. Here, d is the diameter of an s-SWNT in unit of nanometer. The high μ of s-SWNTs originate from anomalously long carrier mean free path which exceeds several hundred nanometers even at room temperature [46]. Thus, carriers run through SWNTs without scattering by lattice vibration in short channel FETs, and so-called ballistic transport occurs.

The performance of CMOS devices depends on both electron mobility (μ_e) and hole mobility (μ_h). In conventional semiconductor materials, since effective mass of a hole is heavier than that of an electron, μ_h is generally lower than μ_e, and thus limits CMOS performance. Therefore, a combination of InGaAs for NMOS and Ge for *p*-channel MOS (PMOS) has been proposed as a candidate for channel replacement of CMOS devices. However, the fabrication process would be complicated. In contrast, because of the symmetric structure of conduction and valence bands near those edges [2], the high μ are obtained for both electrons and holes in s-SWNTs.

The second advantage of s-SWNTs is the ultrathin 1-D structure, which can suppress the short channel effect (SCE) in ultrashort channel devices in terms of electrostatics. In conventional MOSFETs, with shrinking the channel length (L_{ch}), the potential of the channel becomes dependent on drain field as well as gate field. As a result, with increasing drain-source voltage (V_{DS}), the drain current (I_D) no longer saturates but increases, and off current also increases. To suppress SCE, doping concentration in the channel is required to increase. However, the higher doping density is, the lower μ becomes, and thus there is a tradeoff between the suppression of SCE and μ. Alternative method to suppress SCE is to decrease the thickness of the channel to improve the electrostatic profile. For example, silicon-on-insulator (SOI) structure has already been introduced in current ultra-large scale integration (ULSI), and in near future, Fin FETs with a double or triple gate structure, and nanowire FETs with gate-all-around (GAA) structure will be developed as shown in Fig. 14. The s-SWNTs have self-organized, ultimately thin, and 1-D body, which is supposed to be an ideal structure to suppress SCE.

B. Device Structure, Fabrication, and Operation

The basic structure of a CNFET is illustrated in Fig. 15(a). A common CNFET is three- or four-terminal

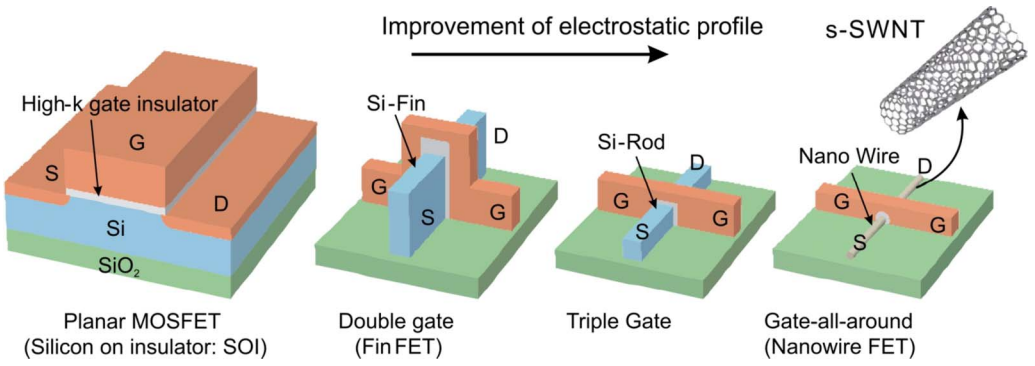

Fig. 14. *Schematics of future progress of transistor structure to suppress short channel effect, SOI MOSFET, Fin FET with double and triple gates, nanowire FETs, and CNFETs.*

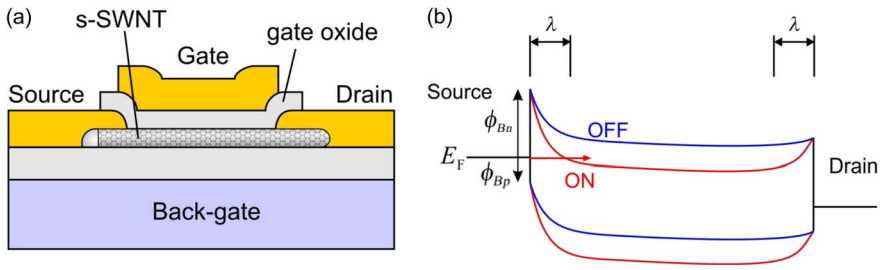

Fig. 15. ***Schematic structure of CNFET, and energy band diagrams at ON and OFF states.***

device that consists of an SWNT on which two metal electrodes, the source and drain, are formed. The contact material is one of key parameters to determine the device property as described later. A heavily doped Si substrate with a thermally oxidized SiO_2 layer is often used for a back gate. For a top gate device, the high-k gate dielectric such as Al_2O_3, ZrO_2, and HfO_2 is formed by the atomic-layer deposition (ALD) technique, which can deposit the insulator without damaging the SWNT [47]. The adsorption of ALD precursors on the surface of SWNTs is difficult due to its inertness. Because of this nucleation problem, uniform coating of high-k on SWNTs, which is an essential requirement for high-performance devices, is difficult. In order to achieve thin uniform coating of an SNWT with a dielectric by ALD, it is necessary to modify the SWNT surface by introducing a functional layer such as DNA [48], NO_2 [49], diazonium compounds [50], and so on.

Since the source and drain contacts of a CNFET consist of metal–semiconductor junctions, a Schottky barrier (SB) is usually formed at the contacts. In the case when SB height is higher than a few kT, the CNFET can be considered as a type of SB FETs. The schematic energy band diagram across the source-drain contacts is shown in Fig. 15(b). The SB heights, ϕ_{Bn} for electrons and ϕ_{Bp} for holes, are determined by the work functions of the metal and the s-SWNT and E_G of the SWNT in an ideal case. When the gate-source voltage (V_{GS}) is applied with a positive V_{DS} so that the conduction band edge (E_C) of the channel comes below the Fermi energy (E_F) of the source, electrons are injected from the source to the channel by thermal-assisted tunneling process. The tunneling probability, hence I_D, depends on the thickness of SB which is modified by V_{GS}.

Similarly, hole current can flow when the valence band edge (E_V) of the channel comes above E_F of the drain at negative V_{GS}. Therefore, ambipolar characteristics, in which both electron and hole currents flow depending on V_{GS}, are often observed in the case when E_g of the SWNT is small [51] and E_F of the source is positioned in the middle of E_g [52]. To suppress the ambipolar characteristics and control the polarity of conduction carriers in CNFETs, the energy band profile near the source and drain contacts is needed to be modified to increase the Schottky barrier for minority carrier, for example, by selecting metal work function [53] or by doping technique such as the electrostatic doping using a dual-gate structure [54] and the chemical doping [55], and so on.

The profile of SB is determined by the electrostatic profile near the contact as well as by the work function of the contact metal. The gate field is screened by the potential of the source and drain metal near the contacts [56]. The screening length (λ) is approximately given by $\lambda = \sqrt{(\varepsilon_{\mathrm{SWNT}}/\varepsilon_{\mathrm{ox}})d_{\mathrm{SWNT}}t_{\mathrm{ox}}}$ for a planar device configuration [57]. Here, $\varepsilon_{\mathrm{SWNT}}$ and $\varepsilon_{\mathrm{ox}}$ are dielectric constants of the s-SWNT and gate oxide, respectively, d_{SWNT} is the diameter of the s-SWNT, and t_{ox} is the thickness of the gate oxide. λ decreases with decreasing t_{ox} and increasing $\varepsilon_{\mathrm{ox}}$. To reduce contact resistance of an SB FET, λ should be reduced. For example, the lower contact resistance is obtained for the thinner gate oxide [56]. Since chemical doping [58] and interface charges [59] can modify SB in the screened range near contacts, they can reduce contact resistance, and even change the polarity of conduction carriers as described in Section III-C.

λ is also important for scaling of a CNFET. As L_{ch} of a CNFET decreases so that λ is comparable to L_{ch}, drain-induced barrier lowering and punch-through between the drain and source will eventually occur. It has been suggested that the actual L_{ch} should be about three times larger than the screening length [60]. Further improvement in electrostatics near the contact can be expected in GAA structure, where $\lambda = \sqrt{(\varepsilon_{\mathrm{SWNT}}/8\varepsilon_{\mathrm{ox}})d_{\mathrm{SWNT}}^2 \ln(1+(2t_{\mathrm{ox}}/d_{\mathrm{SWNT}}))}$ [61], [62]. GAA CNFETs have been realized by depositing Al_2O_3 by ALD technique on a NO_2-functionalized SWNT [62]. For more detailed discussions on scaling of CNFETs, including the influence of quantum capacitance, see [60].

C. Control of Conduction Property of CNFETs for CMOS Applications

For CMOS application, the control of the conduction property of CNFETs is required. Development of technologies to control the polarity of conduction carriers is still an important issue, especially, regarding stability in air, device performance, and process compatibility to Si

process. The *p*-type conduction is usually obtained in back-gate devices in air due to the effect of ambient oxygen. When oxygen molecules adsorb on the surface of contact metal, a dipole is formed so to increase the work function of the contact metal [56], and then holes are dominantly injected into the s-SWNT. Even though the effect of oxygen disappears when the SWNT is covered with a passivation film or a gate insulator in top-gate CNFETs, hole current can be injected by using metals with the large work function such as Pd and Au [64], [65]. Such metals with a large work function are chemically inert and stable in air.

On the other hand, to realize *n*-type devices, chemical doping with K [66], [67], annealing in a vacuum [68], contact with low work function such as Ca [53], and Sc [69] have been suggested, so far. However, so-obtained *n*-type devices are unstable in air. Moreover, it is well known that the ions of alkaline and alkaline earth metals such as K, Ca, and Sc are contamination species for VLSI. The ions of such metals are mobile in a gate insulator, which can cause hysteresis and threshold voltage shift depending on the sequence of voltage application [45]. At present, making an *n*-type CNFET is more difficult compared to a *p*-type device because of aforementioned reasons. The polarity control technique which is chemically stable and compatible to Si VLSI process is required.

Recently, CMOS inverters and five-stage ring oscillators have been demonstrated, in which ambipolar CNFETs play roles of NMOS or PMOS depending on the work function of the gate metals [70]. This technique could have an excellent controllability of the threshold voltage of CNFETs in addition to the chemical stability and Si-process compatibility. However, ambipolar devices generally have large OFF current, which seriously increases power consumption of VLSI.

Here, we introduce recent challenge to control the polarity of carriers, utilizing interface charges introduced at the interface between the gate insulator and substrate [59]. Fig. 16(a) shows I_D–V_{GS} characteristics of a back-gate CNFET with Au contact electrodes and L_{ch} of 0.7 μm. When a HfO_2 layer was deposited on top of the device by ALD, the transfer characteristics changed from those of a *p*-type device (red curve) to an *n*-type device (blue curve). The conductance for *n*-type conduction is 11% of the quantum conductance $(4e^2/h)$. The contact resistance has been evaluated to be ~14 kΩ for *n*-type current. The *n*-type conduction has been maintained for more than 150 days in air.

We attributed the cause of change in carrier polarity to positive charges introduced at the interface of HfO_2 layer and SiO_2/Si substrate. The capacitance-voltage characteristics of metal–insulator–semiconductor diodes confirmed the existence of the positive fixed charges at the HfO_2/SiO_2 interface. The interface charge density (N_{it}) was estimated to be $\sim 2 \times 10^{13}$ cm^{-2}. It can be expected that when positive fixed charges are introduced around the source contact, electric force lines diverging from the positive charges are terminated at the source contact, inducing negative charges on the surface of the metal, as shown in Fig. 16(b). The electric force lines cause an abrupt band bending in SB, resulting in a reduction in SB thickness for electrons.

Since the charge density and polarity of interface fixed charges are dependent on the material of the insulator and conditions of ALD and the postannealing process [71], the carrier type of CNFETs can be controlled by choosing these conditions. In our experiments, when an Al_2O_3 layer was deposited instead of an HfO_2 layer, *p*-type CNFETs were obtained after postdeposition annealing process. The condition of the postdeposition annealing was 400 °C for 30 min in N_2 atmosphere. In this case, N_{it} was estimated to be $\sim 2 \times 10^{11}$ cm^{-2} with positive polarity, and then the device polarity was determined by the large work function of Au contacts.

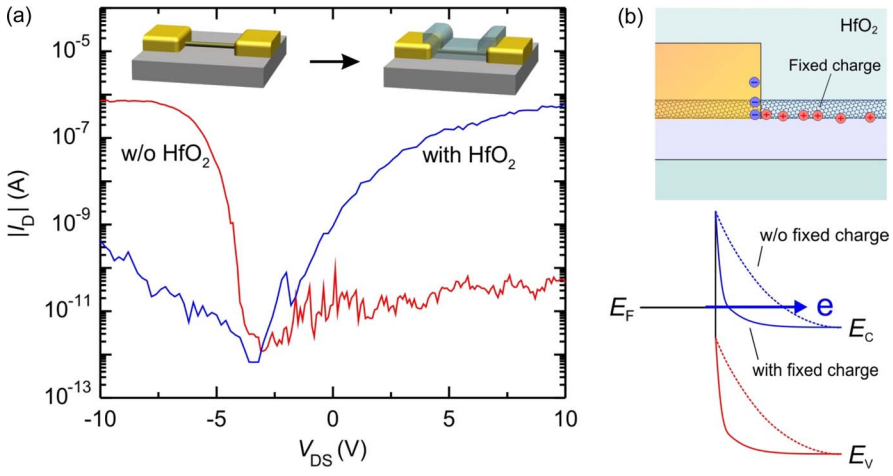

Fig. 16. *(a) Change in carrier type observed in back-gate CNFET by deposition of HfO_2 by ALD and (b) its mechanism explained by abrupt energy band bending near source contact caused by positive fixed charges introduced at interface between HfO_2 and SiO_2.*

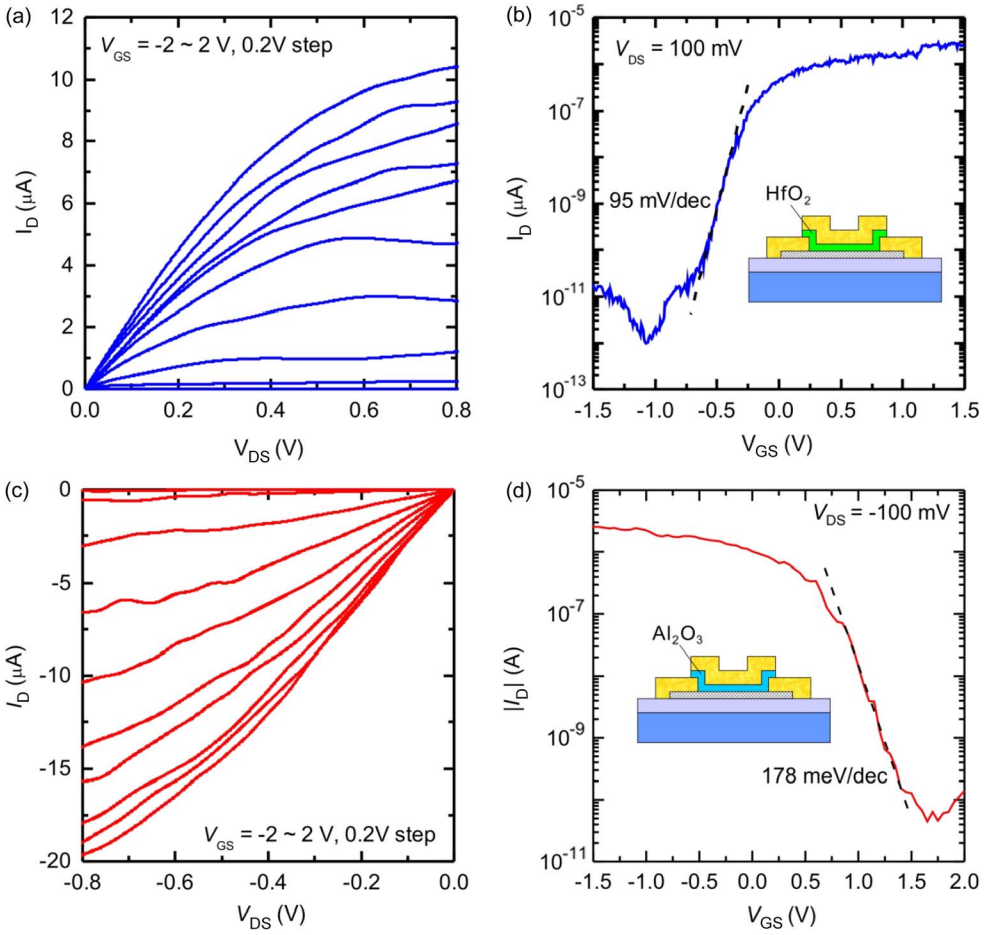

Fig. 17. ***(a)*** I_D–V_{DS} ***and (b)*** I_D–V_{GS} ***characteristics of*** *n*-***type top-gate CNFET with*** HfO_2 ***gate insulator. (c)*** I_D–V_{DS} ***and (d)*** I_D–V_{GS} ***characteristics of*** *p*-***type top-gate CNFET with*** Al_2O_3 ***gate insulator. For*** I_D–V_{GS} ***characteristics,*** $|V_{DS}| = 100$ ***mV.***

D. High-Performance Top-Gate CNFETs Based on Interface-Charge Control and Their Operation Mechanism

The top-gate devices with L_{ch} of 100 nm and Au contacts were fabricated on individual SWNTs directly grown on a SiO_2/Si substrate. A gate insulator layer HfO_2 or Al_2O_3, with a thickness of 12 nm, was deposited by ALD technique. The device fabrication was completed by forming a top-gate electrode of Ti/Au. All measurements were carried out in air at room temperature. Fig. 17 shows the electrical characteristics of fabricated top-gate CNFETs: I_D–V_{DS} [Fig. 17(a)] and I_D–V_{GS} [Fig. 17(b)] characteristics of a HfO_2-gate CNFET, and I_D–V_{DS} [Fig. 17(c)] and I_D–V_{GS} [Fig. 17(d)] characteristics of an Al_2O_3-gate CNFET. The conduction types were *n*-type for the HfO_2-gate CNFET and *p*-type for the Al_2O_3-gate CNFET. This suggests again that the carrier type of CNFETs can be controlled by selecting the material for the gate insulator. The device performances are quite high, especially, for *n*-type CNFETs stable in ambient air as summarized in Table 1.

The potential of the top-gate CNFET changes drastically in the presence of interface charges. Fig. 18(a) and (b) shows the model for potential calculations, and calculated potential distributions of top-gate CNFET structure (without a SWNT channel) near the source contact at $V_{GS} = 2$ V (ON state for *n*-type) [Fig. 18(c) and (d)] and $V_{GS} = -3$ V (OFF state for *n*-type) [Fig. 18(e) and (f)], for $N_{it} = 2 \times 10^{11}$ cm^{-2} [Fig. 18(c) and (e)] and

Table 1 Performance Indices of Top-Gate CNFETs

	HfO_2 gate	Al_2O_3 gate
Carrier type	*n*	*p*
L_{ch} (nm)	100	100
I_{ON} (μA)	11	22
g_m (μS)	14	14
I_{ON}/I_{OFF}	~10^6	~10^5
s-factor (mV/dec.)	95	200

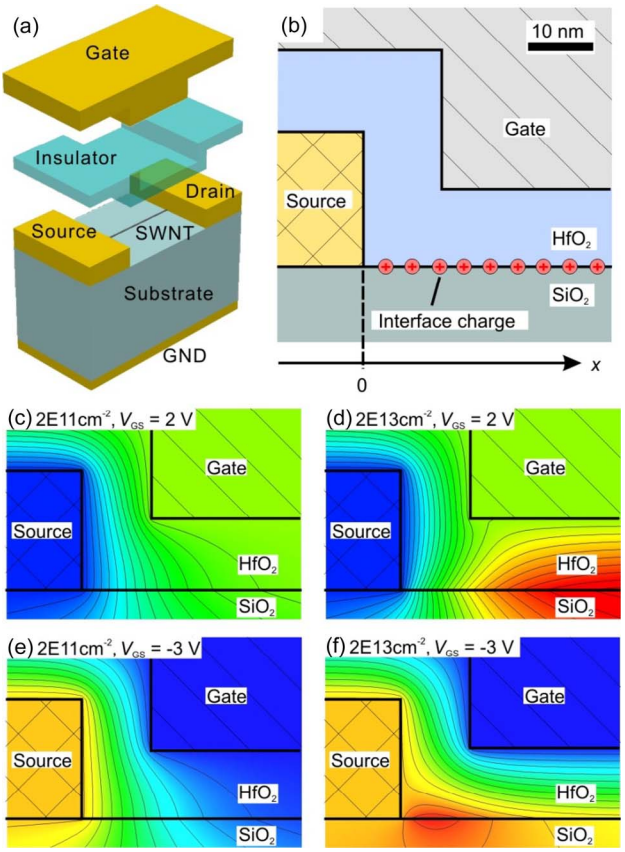

Fig. 18. ***(a) Device model of the top-gate CNFET for simulation. (b) Cross-sectional view near the source contact of the device model. Calculated potential distribution near the source electrode of top-gate CNFET structure, without an SWNT channel, at (c)–(d) $V_{GS} = 2$ V (ON state for n-type) and (e)–(f) $V_{GS} = -3$ V (OFF state for n-type). interface charge densities are (c)–(e) 2×10^{11} cm^{-2} and (d)–(f) 2×10^{13} cm^{-2}.***

$N_{it} = 2 \times 10^{13}$ cm^{-2} [Fig. 18(d) and (f)]. Here, $V_{DS} = 0$ V. In the case of $N_{it} = 2 \times 10^{11}$ cm^{-2}, no significant effect of the interface charges was observed in either the ON or OFF state. In contrast, in the case of $N_{it} = 2 \times 10^{13}$ cm^{-2}, the potential at the HfO_2/SiO_2 interface, where a SWNT channel will be placed, becomes higher than that of the gate electrode as shown in Fig. 18(d). A part of the electric force lines diverging from the interface charges terminate at the source electrode. As a result, a strong field develops between the channel region and source. This implies that the SB at the source contact is strongly bent by the field and electrons can be injected through the SB. In the OFF state, a high-potential region was observed near the source contact, as shown in Fig. 18(f). In this region, the electrostatic field of the gate electrode is screened by the source electrode, and hence, positive interface charges build up the potential.

The operation mechanism in CNFETs is expected to change in the presence of interface charges. Fig. 19 shows energy band profiles of the SWNT channel placed in the CNFET structure at various V_{GS} between ON and OFF states for $N_{it} = 2 \times 10^{11}$ cm^{-2} [Fig. 19(a)] and $N_{it} = 2 \times 10^{13}$ cm^{-2} [Fig. 19(b)]. In the case of $N_{it} = 2 \times 10^{11}$ cm^{-2}, both the channel potential and SB thickness are modulated by V_{GS}. This is the operation of SB FETs, where the drain current is modulated by the SB thickness, depending on V_{GS}. The SB thickness does not decrease at V_{GS} higher than 0.6 V owing to the screening of the gate field near the source contact, which results in the large contact resistance of SB FETs. In the case of $N_{it} = 2 \times 10^{13}$ cm^{-2}, on the other hand, the SB thickness is much thinner than that for $N_{it} = 2 \times 10^{11}$ cm^{-2}, and is hardly modulated by V_{GS} as shown in Fig. 19(b). The mechanism of the drain current modulation can no longer be described by the SB modulation model. Nevertheless, the drain current could be modulated by V_{GS} since the potential of the region underneath the gate electrode depends on the gate field. These simulation results suggest that the mechanism of the current modulation changes from the SB modulation model to the channel modulation model in the presence of the interface fixed charges.

Furthermore, the high-potential region that formed near the source contact could suppress the minority carrier injection from the drain electrode in the OFF state, which is often observed as ambipolar conduction in SB FETs [52]. When the device is biased in the deep-OFF state in *n*-type SB CNFETs, hole current would be injected from the drain electrode through the SB thinned by the gate field as shown in Fig. 20(a). On the other hand, in the presence of interface fixed charges, the hole injection could be blocked by the high-potential region that formed near the drain electrode as shown in Fig. 20(b).

E. Integration of *p*-CNFET and *n*-CNFET on a Single SWNT for CMOS Devices

Finally, we fabricated CMOS inverters by integrating a HfO_2-gate CNFET for NMOS and an Al_2O_3-gate CNFET for PMOS. Fig. 21(a) is the schematic of fabricated CMOS inverters. Both NMOS and PMOS were integrated on a single SWNT. After the growth of the SWNT, contact electrodes (Ti/Au) were formed by using electron beam lithography. An Al_2O_3 gate insulator for PMOS was deposited by ALD at 150 °C. Here, we used electron beam lithography and liftoff process to pattern the gate insulator [72]. After the annealing process at 400 °C for 30 min in N_2 atmosphere, the gate electrode (Ti/Au) for PMOS was deposited on top of the Al_2O_3 gate insulator. Then, a HfO_2 gate insulator for NMOS was deposited on the whole surface of the sample. The device fabrication was completed by forming the gate electrode (Ti/Au) for NMOS after opening the contact holes on the HfO_2 layer by reactive ions etching. Fig. 21(b) shows the SEM image of a fabricated CMOS inverter. The channel length was 500 nm.

Fig. 21(c) shows the voltage transfer curve of a fabricated CMOS inverter (red curve) measured in air at room temperature. A clear inverter operation with a maximum

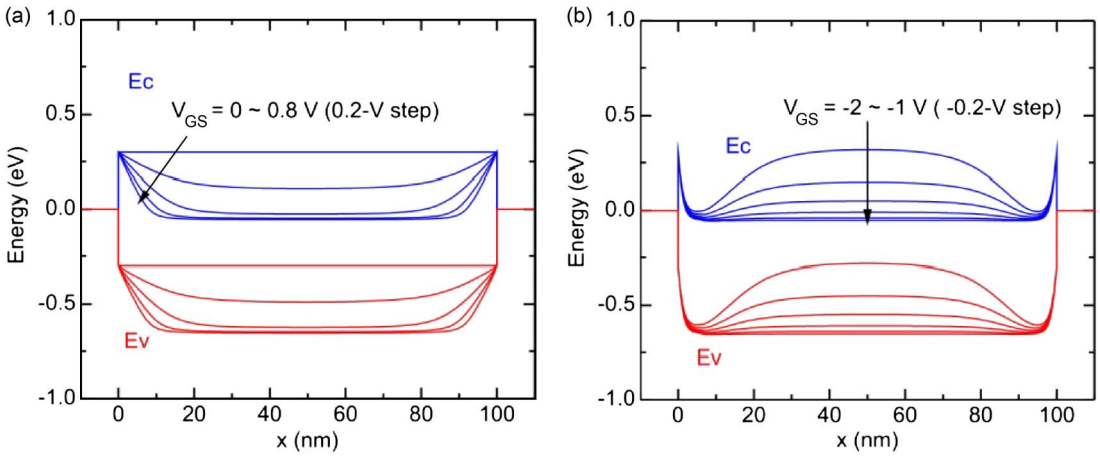

Fig. 19. *Calculated energy bands for various V_{GS} ranging between ON and OFF states for (a) $N_{it} = 2 \times 10^{11}$ and (b) $N_{it} = 2 \times 10^{13}$ cm^{-2}.*

voltage gain of 26 was obtained. The logic threshold voltage was able to be adjusted by applying the substrate bias. Then, the matching between input voltage and output voltage was obtained, which is required for CMOS logic circuits to transfer the logic output to the input of the next stage sequentially. The noise margin, which expresses the robustness of logic operation, is schematically represented by the area of eyes in the folded voltage transfer curve (blue curve). The noise margin defined by the unity-gain points and stable logic points was about 70% of $V_{dd}/2$. The CNT CMOS inverter with air stability and high performance was realized by Si-process compatible technique utilizing interface charges.

F. Future Issues

Even though CNFETs show promising performances, there are still many issues to be addressed for their VLSI applications as follows.

1) For an individual device level, precise control of device characteristics such as threshold voltage is required. The channel region under the gate electrode should be lightly doped to control the threshold voltage. The areas near the source and drain contact, on the other hand, should be doped with a high concentration to determine the polarity of carriers and to reduce the contact resistance. For this purpose, a precisely controllable doping technique such as ion implantation conventionally used in Si VLSI process is necessary. Similar to the interface fixed charges as described in previous section, ions or fixed changes need to be implanted not into the SWNT channel, but into gate oxide around the SWNT channel.
2) A process to fabricate very short channel devices is also one of important issues. A technique to deposit uniform ultrathin gate insulator on the

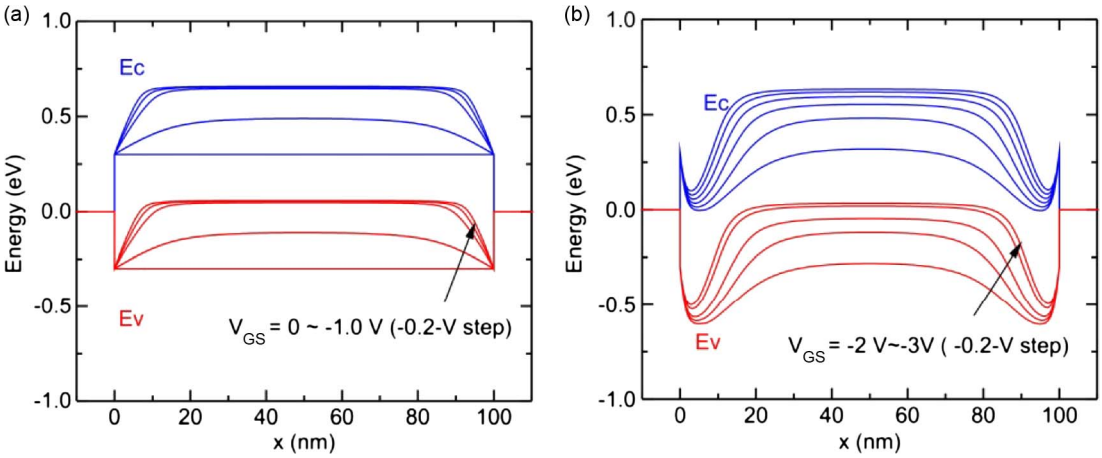

Fig. 20. *Calculated energy bands for various V_{GS} from OFF to deep-OFF states for (a) $N_{it} = 2 \times 10^{11}$ and (b) $N_{it} = 2 \times 10^{13}$ cm^{-2}.*

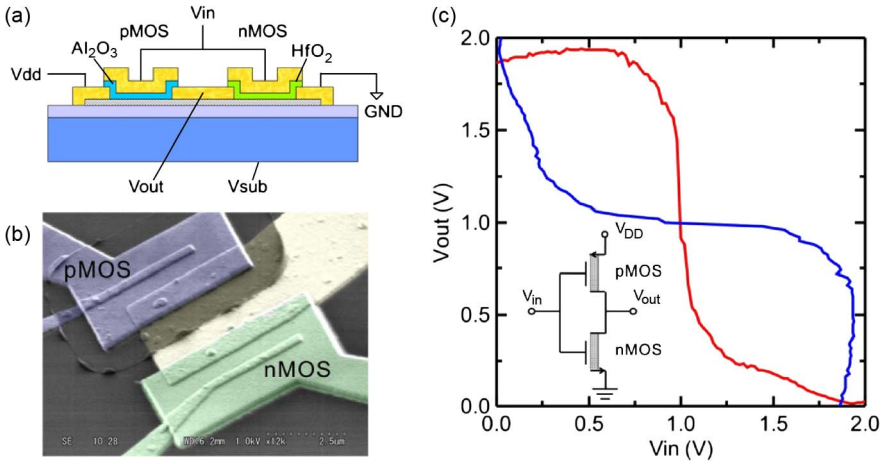

Fig. 21. *(a) Schematic device structure and (b) SEM image of a fabricated CMOS inverter. (c) Voltage transfer curve at $V_{dd} = 2.0$ V and $V_{sub} = -20$ V (red curve), and the folded voltage transfer curve (blue curve), showing the noise margin.*

SWNT channel is necessary. For this, surface functionalization technique without current degradation is required. An etching technology with a high selectivity between an SWNT and photoresist material is also necessary to shrink the device size by pattern trimming technique.

3) A demonstration of high-speed operation is also important. Although CNFETs are expected to operate at frequencies of the terahertz regime [73], [74], the record current-gain-cutoff frequency f_T of 80 GHz is two orders of magnitude lower than the expectation [75]. The f_T is dominantly degraded by parasitic gate-source and gate-drain capacitances. One approach to reduce the influence of parasitic capacitances is to use a parallel array of SWNTs, which can be grown by CVD on crystalline oxide substrates such as sapphire [76], [77] and quarts [78], [79]. At even higher densities, screening by adjacent SWNTs reduces the transconductance and gate capacitance per SWNT, and hence f_T. When the channel contains metallic SWNTs, f_T is further degraded due to the drain conductance with parasitic source and drain resistances. See [80] for detailed discussions on high-frequency operation of CNFETs. For the purpose of high-frequency operation, reduction of metallic SWNTs, and decrease in gate oxide thickness or introduction of GAA structure are beneficial as well as increase in SWNT-array density.
4) More difficult challenges are necessary for IC level demonstration. The state-of-the-art CNT CMOS-based IC demonstrated would be five-stage ring oscillator, where 12 CNFETs were integrated on a single, long s-SWNT [70]. For further development of nanotube integrated circuits (ICs), a critical step is the large scale integration of CNFETs consisting of s-SWCNTs with the same chirality.The separation of metallic and semiconducting SWNTs has been attempted by many different approaches, including dielectrophoresis [81], amine extraction [82], DNA wrapping [83], density-gradient ultracentrifugation [84], gel-based separation [85], and so on. The highest purity of metal/semiconductor separation reported so far is ~95% [86], while a standard method to evaluate purity has not been established. More recently, chirality separation has been achieved by DNA recognition of SWNTs [87] with a purity of around 90%, which is still far from VLSI grade. Those separated SWNTs can be assembled on a wafer by dielectrophoretic self-limiting deposition method [88], [89]. Even though the yield of dielectrophoretic deposition is ~90% at the present, the device array of high density as several million devices per squared centimeter has been realized, which is comparable to the current ULSI level. These solution-based technologies possibly cause contamination problems [90] such as hysteresis and threshold voltage shift in CNFETs due to the dispersant and so on. In addition to improvements of the purity of chirality separation and the yield of SWNT assembly, cleaning technologies to remove dispersants would be required. ■

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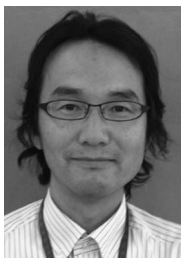

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