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Title : VEDA: Vectorless Event-Driven Approach for Optimal Switch Sizing of Power-Gating Circuits to Reduce Two Orders of Magnitude of Leakage Power

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Abstract

In this paper, an effective and feasible design methodology and fully automated software tool for MTCMOS power-gating circuits is introduced to reduce leakage by two-orders of magnitude. A new method, Vector-less Event-Driven Approach (VEDA) utilizes static timing analysis and composite current waveforms to optimize power switches in MTCMOS power-gating circuits. Using a 90nm industry library and more than 10 typical benchmark circuits, the proposed method shows that it always produces worst-case results while reducing power switch area overhead by 87.4 percent over previous approaches without compromising speed, functionality, run-time, or memory usage.

1. Introduction

It is well known that the impact of the technology scaling on leakage power continues to increase. With respect to total power consumption, leakage power has increased from an almost negligible level to nearly 20 percent in 130-nanometer (nm) designs, 40 percent in 90-nm designs, and over 50 percent in 65-nm designs. Now, managing leakage power effectively is critical to the success of mobile applications [1].

Several techniques have been proposed to reduce leakage power such as dual-Vth [4], mixed-Vth [5], off-off MOS stacking [6], input-vector control [7], multi-threshold (MT) CMOS [8], selective MTCMOS (SMT) [9], Zigzag super cut-off CMOS (ZSCCMOS) [10], optimal Zigzag CMOS (OZ) [11], body-bias control [12], transistor width sizing [13], transistor channel scaling [14], and voltage islands [15].

Among the leakage-control techniques, power gating, also known as MTCMOS, has traditionally been the most effective way to lower the leakage of a VLSI circuit in the leakage dominant era. Power-gating uses a PMOS transistor or an NMOS transistor to disconnect the circuit's supply voltage from the logic during standby mode. This technique can reduce leakage by more than two orders of magnitude with negligible speed degradation.

However, since the power-gating scheme was introduced in 1993 [16], designers have had difficulty deploying it due to the additional design complexity. One of the most difficult problems is power-switch sizing because the optimum power switch size is determined by several critical design parameters such as virtual rail voltage drop, wake-up time, rush current, area, and delay. Therefore, optimizing the power-switch size is essential for power-gating design.

Several approaches have been proposed to solve the sizing problem as shown in Table 1.

Table 1. Traditional Approaches of Switch Sizing

Technique	Method
Mutually Exclusive [Kao, 98]	- Mutually exclusive discharging pattern based
Average Current Method (ACM) [Mutoh, 99]	- Average current based
Min-Max Window Based [Anis, 03]	- Min-Max trapezoidal discharging current based
Switch-In-A-Cell [Qualcom, 04]	- Each cell based, no sharing

In this paper, to solve the sizing problem, a vectorless event-driven approach, VEDA, is proposed to calculate the currents that flow from gated logic to power switch by utilizing static timing analysis, STA, and composite current waveforms.

The paper is organized as follows: i) theoretical background, ii) power-switch operations and impact, iii) traditional approaches, iv) VEDA concept, v) experimental results, and vi) conclusions.

2. Theoretical Background

Leakage current has several different components, however the largest components in 90 nm technologies are sub-threshold related. The sub-threshold leakage current is represented as

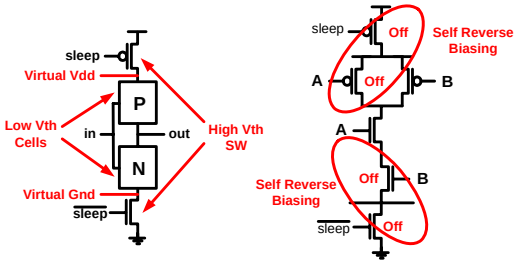
$$I_{sub-leak} = K_1 \cdot \frac{W}{L_{eff}} \cdot (V_T)^2 \cdot e^{\frac{V_{gs} - V_{th0} - \gamma V_s + \eta V_{ds}}{nV_T}} \cdot \left(1 - e^{\frac{-V_{ds}}{V_T}}\right) \quad (1)$$

where, V_{th0} is the zero bias threshold voltage, γ is the linearized body effect coefficient, V_s is the source to bulk voltage, η is the DIBL (drain induced barrier lowering) coefficient, n is the sub-threshold swing coefficient of the transistor, $V_T=KT/q$ is the thermal voltage, and K_1 is a process constant.

Most leakage reduction techniques focus on controlling one or more terms in the equation. Basically, the methods of the leakage reduction techniques are categorized as reducing W (transistor width), increasing L_{eff} (channel

length), cooling down V_T (thermal voltage), reducing or making negative V_{gs} (gate to source voltage), increasing V_{th0} (zero bias threshold voltage), increasing V_s (source to bulk voltage), and reducing V_{ds} (drain to source voltage).

Fig. 1 shows the power-gating mechanisms. In active mode, the sleep transistor is on and the circuit functions as usual. In standby state, the switch transistor is turned off, which disconnects the logic gate from power or ground. The following mechanisms are involved in reducing leakage power in power-gating techniques: i) high-Vth switch, which impacts the V_{th0} term in Eqn. (1), and ii) off-off stacking effect, which impacts DIBL, body effect, negative V_{gs}, and small signal rail (V_{ds}) in Eqn. (1).



(a) High-Vth Switch (b) Self Reverse Biasing (Off-Off Stacking)

Fig. 1. Power Gating Circuit and Mechanisms

3. Power-Switch Operations and its Sizing Impact

In power-gated circuits, the active mode performance penalty is a function of the switch "on" resistance, where the "on" resistance is determined by switch sizing, and the switch sizing is determined by discharging currents. The following equations show the relationships.

Current in linear-region:

$$I_D = \frac{\mu_{eff} \cdot C_{OX} \cdot W}{L_{eff}} \cdot \frac{1}{1+\frac{V_{DS}}{E_C \cdot L_{eff}}} \cdot \left(V_{GS} - V_{tH} - \frac{1}{2} \cdot V_{DS}\right) \cdot V_{DS} \quad (2)$$

$$V_{DS} \ll V_{GS} - V_{tH} \quad (3)$$

$$I_D \propto W \cdot \left(V_{DD} - V_{tH}\right) \cdot V_{DS} \quad (4)$$

Trade-off between current and "on" resistance:

$$\frac{1}{R_{ON}} = \frac{I_D}{V_{DS}} \propto W \cdot \left(V_{DD} - V_{tH}\right) \quad (5)$$

If the discharging current is calculated much larger than real situation, then larger size of power switch is needed to reduce "on" resistance of the power switch, resulting in far from the optimal design (over-design). Fig. 2 shows the power-switch characteristic according to its operation. In active mode, the power-switch operates in linear region, in standby mode, the power-switch operates in cut-off region, and in wake-up mode, the power-switch operates in saturation region. Fig. 3 shows the design impact of the power-switch according to its operation mode. The switch sizing will impact to the delay in the active mode, to the leakage power in the standby mode, and to the rush current in the wake-up mode.

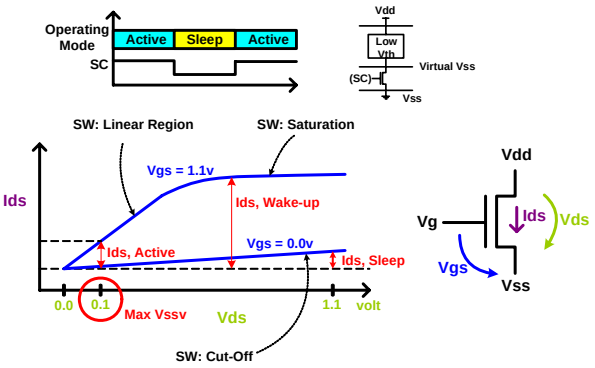


Fig. 2. Power-Switch Operations

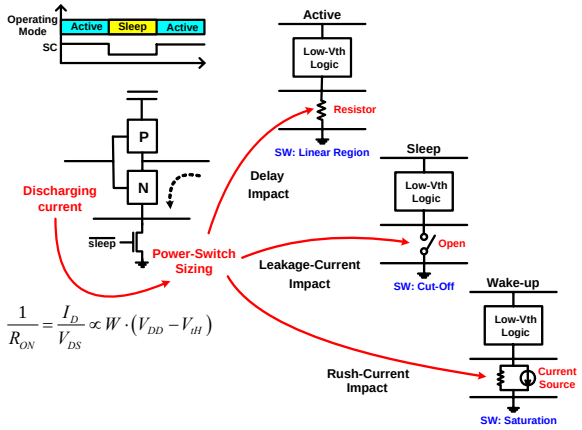


Fig. 3. Power-Switch Impact

Therefore, the discharging current calculation for the sizing is essential for MTCMOS power-gating designs. In the following two chapters, the previous approaches and the proposed VEDA scheme for calculating the discharging current in complicated circuit design structures are described.

4. Traditional Approaches

4.1. Mutually Exclusive Method [17]

In this technique, power-switch sizing is based on mutual exclusive gate discharge patterns.

If there are *n* logic gates whose output transition windows are non-overlapping, and each has a power-switch transistor whose width is *Wi*, then these sleep transistors may be replaced with a single transistor whose width is *Wmax = Max(Wi)* for *1<i<n*.

The mutual exclusion method provides an upper bound on the required size of the power-switch.

However, this scheme only utilizes structural information to find mutual exclusion, not logical information. The structural mutual exclusion does not take into account the fact that only about half of gates in a circuit switch from high to low in a given cycle. Thus, using of the mutual exclusion method produces overly conservative results.

4.2. Average Current Method [18]

This technique assumes that the current consumed in

the power-gating circuit is constant, or time invariant. The rationale of the scheme is as follows:

Let's say the delay without power-switch is

$$\tau_d \propto \frac{C_L \cdot V_{dd}}{(V_{dd} - V_{tL})^{\alpha}} \quad (6)$$

the delay with power-switch is

$$\tau_d^{sleep} \propto \frac{C_L \cdot V_{dd}}{(V_{dd} - V_X - V_{tL})^{\alpha}} \quad (7)$$

If 5% speed loss is assumed, then the delay loss with power-switch is $\frac{\tau_d}{\tau_d^{sleep}} = 95\%$ (8)

The Eqn. (6) and (7) are combined with Eqn. (8)

$$1 - \frac{V_X}{(V_{dd} - V_{tL})} = 95\% \quad (9)$$

Then, the virtual rail voltage is

$$V_X = 0.05 \cdot (V_{dd} - V_{tL}) \quad (10)$$

Current through linearly-operating power-switch is

$$I_{Average\_Current} = \mu_n \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_{sleep} \cdot \left[(V_{dd} - V_{tH}) \cdot V_X - \frac{V_X^2}{2}\right]$$

$$\approx 0.05 \cdot \mu_n \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_{sleep} \cdot (V_{dd} - V_{tL}) \cdot (V_{dd} - V_{tH}) \quad (11)$$

Therefore, the size of the power-switch is

$$\left(\frac{W}{L}\right)_{sleep} = \frac{I_{Average\_Current}}{0.05 \cdot \mu_n \cdot C_{OX} \cdot (V_{dd} - V_{tL}) \cdot (V_{dd} - V_{tH})} \quad (12)$$

While easy to implement, this approach is problematic in that peak currents can deviate substantially from simple multiples of average current due to issues such as clock skew, decoupling capacitance, and package inductance; each of these issues affects the peak current and voltage spikes but does not alter the average values. Thus the use of average currents to size virtual grounds and switches is risky as the peak value of the dynamic voltage drop may be significantly underestimated.

4.3. Min-Max-Window Clustering Method [19]

To improve upon the mutual exclusion technique, a clustering method is proposed in which a min-max-based trapezoidal current profile is used for each logic gate in the circuit.

For each gate, all input combinations are applied, the highest discharging current at the output of every gate is monitored and the probability that discharging actually occurs is calculated. Next, the discharging probability is multiplied by the corresponding discharge peak to obtain a current for use in estimating the proper power-switch size.

However, this approach has a very serious issue in that it is not a worst case calculation, and thus presents similar risks to the use of average currents – neither approach can deterministically account for worst case current flow in switching scenarios wherein multiple cells switch simultaneously.

4.4. Switch-In-A-Cell Method [20]

This scheme may be thought of as an extreme form of local power gating implementation and is distinguished by the existence of a switch transistor in each individual logic cell.

This approach has several notable advantages and disadvantages. Its primary advantages are that delay calculation is very straightforward and that it can be placed, generally without restriction, like any other standard cell.

However, its disadvantages are significant, chief among them being that the area overhead is substantial due to an additional transistor in the pulldown stack, and the need to size up the previously existing logic transistors to compensate for the additional device in the stack. And, given that each individual instance has its own switch, the aggregate input capacitance presented to the sleep signal is much larger than needed for shared switches requiring a larger than necessary amount of dynamic energy to open and close the switches. Additionally, since the size of the switch transistor is set during the design of each of the individual cells, the performance impact of the switch is also set at the time of the cell design, thus potentially limiting the applicability of the cells to either low-performance or high-performance unless of course two complete sets of logic cells are designed with each set utilizing different switch transistor sizing.

5. Proposed Vectorless Event -Driven Approach (VEDA) in CoolPower™

5.1. STA based All Events are countered

VEDA (vectorless event-driven approach) uses a vectorless static timing analysis (STA) to compute the entire set of potential switching events (as shown in Fig. 9 in the next section). This set contains all of the potential events, both rising and falling, at the particular times at which each event occurs. This set is then filtered to remove redundant and don't care events, such as those that cannot occur due to modal operation.

5.2. Composite Waveform based Current Analysis

From this set of filtered events, a set of current events (that is, a set of events that will result in current being consumed) are computed to create a composite current waveform for each instance. The composite current waveform represents the maximum current consumed, at each point in time, by that particular instance. This includes the current consumed by rising and falling output transitions, internal crowbar currents, as well as currents consumed by input only events. Thus, the composite current waveform may have numerous peaks and troughs, with each peak occurring at the time at which that cell is scheduled to switch (as shown in Fig. 10 in the next section). In this way, neither switching events nor current peaks are neglected.

5.3. Motivational Example of Discharging Current Computation in VEDA

To illustrate the VEDA current computation procedure, let's consider the 1-bit carry-lookahead adder in Fig. 4 and its STA timing windows; its falling events are shown in Fig. 5 and Fig. 6. Fig. 7 and Fig. 8 show the Min-Max Approach that was described in the Section 4.3. Fig. 9 and Fig. 10 illustrate the proposed VEDA scheme that was explained in the Section 5.1 and 5.2.

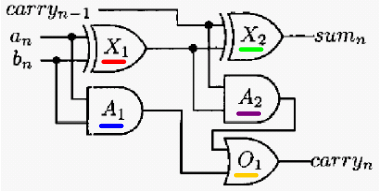


Fig. 4. 1-bit carry-lookahead adder

Gate	$rise_{min}$	$rise_{--}$	$rise_{max}$	$fall_{min}$	$fall_{--}$	$fall_{max}$
X_1	98.90	100.90	107.52	104.24	132.50	183.28
A_1	51.52	52.79	56.33	42.82	42.95	43.01
X_2	83.22	200.89	290.10	132.75	250.47	277.42
A_2	58.31	78.67	168.80	46.43	132.55	232.62
O_1	123.60	157.39	234.09	73.92	198.26	260.11

Fig. 5. Events occurred

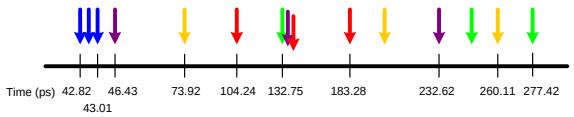


Fig. 6. Actual falling events

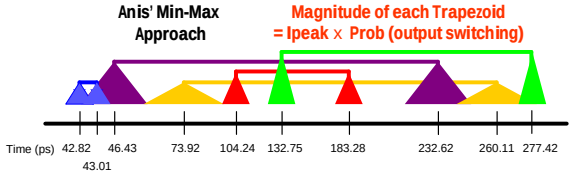


Fig. 7. Min-Max Approach

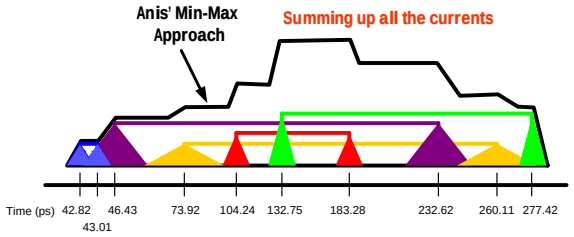


Fig. 8. Summation of all the currents in Min-Max

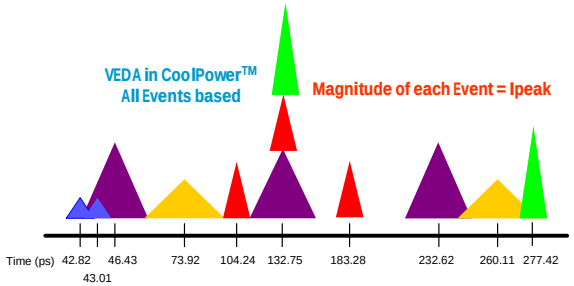


Fig. 9. All the events countered in VEDA

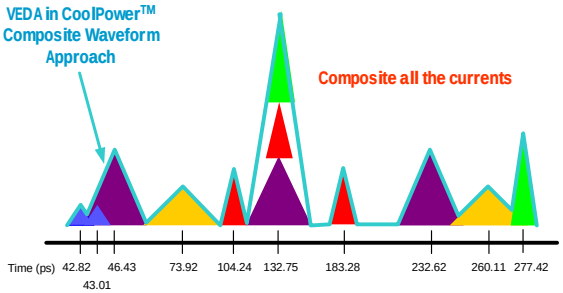
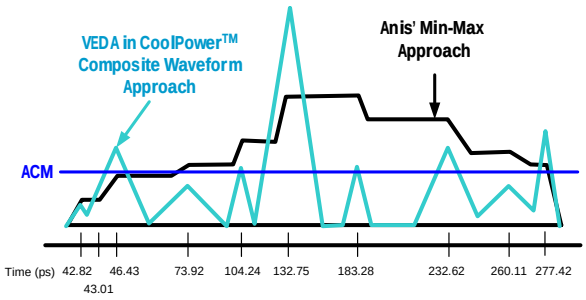


Fig. 10. Composite waveform in VEDA



***Note: VEDA in CoolPower Composite Current Waveform Approach to read Worst Case**

Fig. 11. Comparison between Min-Max, ACM, and VEDA

Fig. 11 shows that the traditional approaches such as the Min-Max approach or the average current method are problematic in that they cannot reliably address worst-case operation.

5.4. Comparisons with Previous Approaches

Table 2 shows a comparison between the traditional approaches and VEDA's enhancements.

Table 2. VEDA vs. Traditional Approaches

Technique	Current Calculation Method	Merits	Drawbacks
Mutually Exclusive [Kao, 98]	- Mutually exclusive discharging pattern based	- Provide upper bound on the switch sizing	- Over design - Routing complexity is high
Average Current Method (ACM) [Mutoh, 99]	- Average current based	- Avoid dynamic current analysis	- No worst-case sizing
Min-Max Window Based [Anis, 03]	- Min-Max trapezoidal discharging current based	- Clusters to minimize the max. simultaneous switching current	- No worst-case sizing - Pessimistic
Switch-In-A-Cell [Qualcom, 04]	- Each cell based, no sharing	- Easy to characterize	- Large area overhead - Library complexity is high
VEDA [CoolPower™, 06]	- STA driven - Composite waveform based	- 100% events covered - Worst-case sizing - Physical distance aware - EM considered	- Potential oversizing

6. Experimental Results

VEDA is embodied in a fully automated software tool, CoolPower [2][3], for power gating implementation and optimization. The switch network topology employs local power gating with a shared switch architecture, and the switches are sized according to the currents computed with VEDA. Moreover, during CoolPower optimization, the size of the switches is based not only on instance currents but also on switch placement and virtual rail metal resistance. These optimizations are performed subject to user specified constraints for maximum transient virtual ground voltage, maximum distance between switches, and electromigration limits.

Table 3 demonstrates that by using the proposed VEDA in CoolPower, an average of 87.4 percent switch-area can be saved over the mutually exclusive approach without compromising speed or functionality, with little difference in run times.

Fig. 12 and Fig. 13 show simulation results illustrating VEDA's ability for worst-case design. In this simulation, the instance currents were first calculated by using an exhaustively generated all input-vector simulation as shown in Fig. 12, after which we compared the resulting currents with the currents calculated by VEDA. Fig. 13 illustrates that our VEDA method always computes for worst-case operation even though VEDA requires no external stimulus.

Table 3. Switch-Area Reduction by using VEDA over Traditional Approach

Comparison Results

Technology : 90 nm industry lib / 13 ISCAS-89 Benchmark / Operational Vdd: 1.3 (Best), 1.1 (Worst) / Clock Speed: 10 nsec / Max. Vssv: 100 mv / Max. vg-wire-limit: 50 um

Benchmark Circuits	Total # of Instances	Total Logic Cell Area (um^2)	Total SW Cell Area (um^2)		Ratio of SW Area over Logic		Total # of SWs after PGO		Worst-Case Sizing		Time Complexity (run-time, min.)		Space Complexity (mem usage, MByte)		SW Area Reduction by VEDA over MEP (%)
			MEP	VEDA	MEP	VEDA	MEP	VEDA	MEP	VEDA	MEP	VEDA	MEP	VEDA	
s27	14	43.90	61.46	11.28	1.401	0.257	14	1	Yes	Yes	2.53	2.59	53.93	53.13	81.0
s298	154	506.77	496.11	60.83	0.979	0.120	113	6	Yes	Yes	4.47	4.35	57.03	55.32	87.8
s344	164	482.94	447.82	65.22	0.932	0.135	102	7	Yes	Yes	5.03	5.45	56.70	55.38	85.9
s382	199	613.40	719.39	99.09	1.172	0.161	163	9	Yes	Yes	3.09	4.55	59.30	55.75	86.2
s386	200	676.74	764.55	99.09	1.129	0.146	169	9	Yes	Yes	2.55	3.24	60.10	55.71	87.3
s820	458	1588.59	1704.10	162.44	1.093	0.104	383	14	Yes	Yes	2.03	2.05	64.79	52.16	90.4
s953	417	1210.49	1260.04	129.83	1.040	0.107	287	13	Yes	Yes	2.13	3.51	61.10	51.59	89.7
s1238	567	1808.84	1820.13	216.38	1.006	0.119	412	19	Yes	Yes	3.21	3.59	66.48	52.81	88.1
s1423	671	2122.448	1916.09	243.98	0.902	0.115	433	24	Yes	Yes	4.20	4.50	70.13	59.16	87.3
s1488	769	2701.97	3027.48	326.14	1.120	0.120	675	29	Yes	Yes	4.11	5.49	176.86	154.81	89.2
s9234	5878	16869.80	13399.93	1809.47	0.794	0.107	2980	163	Yes	Yes	5.44	5.59	288.25	192.26	86.4
s38417	22958	64342.95	52335.06	5435.94	0.813	0.084	11680	502	Yes	Yes	37.25	36.20	711.59	350.44	89.6
s38584	20411	63473.75	40489.02	5060.87	0.637	0.079	8965	468	Yes	Yes	85.02	79.55	444.94	217.42	87.5
Average															87.41 %

*Note: Vssv = Virtual Ground Voltage, SW = Power Switch, MEP = Mutually-Exclusive-Pattern Method, VEDA = Proposed Vectorless-Event-Driven Approach, PGO = Power Gating Optimization

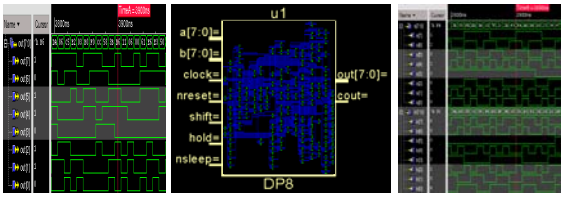


Fig. 12. DP8-testbench and input/output waveforms

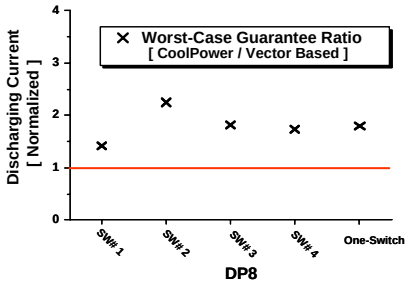


Fig. 13. Worst-case results for DP-8

7. Conclusions

In this paper we have presented an effective and feasible current calculation method to solve the problem of power-switch sizing for worst-case operation with minimal switch-area overhead and circuit speed degradation. The proposed Vector-less Event-Driven Approach shows an average of 87.4 percentage reduction of power-switch size compared to a previous approach without compromising speed, functionality or run-time using 90nm technology and 13 typical benchmark circuits.

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