Circuit Techniques for Dynamic Variation Tolerance

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Abstract

Three circuit techniques for dynamic variation tolerance are presented: (i) Sensors with adaptive voltage and frequency circuits, (ii) Tunable replica circuits for timing-error prediction with error recovery, and (iii) Embedded error-detection sequential circuits with error recovery. These circuits mitigate the clock frequency guardbands for dynamic variations, thus improving microprocessor performance and energy-efficiency. These circuits are described with a focus on the different trade-offs in guardband reduction and design overhead. Opportunities for CAD to further enhance microprocessor performance and energy efficiency are offered.

Categories & Subject Description:

B.7.1 [Integrated Circuits]: Types and design styles

General Terms: Design, performance, reliability

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1. Introduction

Dynamic variations in supply voltage (V_{CC}), temperature, transistor aging, cross-coupling capacitance, and multiple-input switching adversely impact the clock frequency (F_{CLK}) and energy efficiency of microprocessors. Conventional designs build guardbands into the operating F_{CLK} to ensure correct functionality within the presence of worst-case dynamic variations over the microprocessor lifetime. Consequently, these inflexible designs cannot exploit opportunities for higher performance by increasing F_{CLK} or lower energy by lowering V_{CC} during favorable operating conditions and lack of aging degradation. Since most systems usually operate at nominal conditions where worst-case scenarios rarely occur, these infrequent dynamic variations severely limit the performance and energy efficiency of conventional microprocessor designs.

In this paper, dynamic variation sources are reviewed and three circuit techniques are described to reduce the F_{CLK} guardbands for dynamic variations to improve microprocessor performance and energy efficiency. The variation-tolerant circuit techniques provide different trade-offs in guardband reduction and design overhead. CAD research opportunities to further enhance microprocessor performance and energy efficiency are offered.

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2. Dynamic Variation Sources

The primary sources of dynamic variations include: (i) V_{CC} droops, (ii) temperature changes, (iii) transistor drain current aging and recovery, (iv) cross-coupling capacitance changes, and (v) multiple inputs switching (MIS) in logic gates. V_{CC} droops are induced from abrupt changes in switching activity, resulting in large current transients in the power delivery system. The magnitude and duration of V_{CC} droops depend on the interaction of capacitive and inductive parasitics at the board, package, and die levels with changes in current demand [1]. V_{CC} droops contain high frequency (i.e., fast changing) and low frequency (i.e., slow changing) components and occur locally and globally across the die. Temperature variations depend on workload, environmental conditions, and the heat-removal capability of the package. Temperature changes occur at a relatively slow time scale with local hot spots on the die.

Transistor drive current degrades slowly over time as a function of gate bias and temperature conditions. As an example in Fig. 1, path delay degradation is measured across different circuit types from a 45nm test-chip at various intervals of accelerated DC stress [2]. Since the path delay reduction is similar for different circuit types, a circuit path containing simple inverter components sufficiently tracks the worst-case DC stress on critical paths.

Cross-coupling capacitance between adjacent wires can induce a data-dependent RC delay on the wire, which varies as adjacent wires switch in the same or opposite direction. MIS affects logic gate delay depending on the input transitions and arrival times. Path delay variations resulting from cross-coupling capacitance and MIS are fast-changing and local.

3. Sensors with Adaptive Voltage & F_{CLK}

As illustrated in Fig. 2 for a generic microprocessor with N pipeline stages, on-die sensors coupled with dynamic voltage and frequency (DVF) control circuits [2]-[5] can adjust F_{CLK}, V_{CC}, or

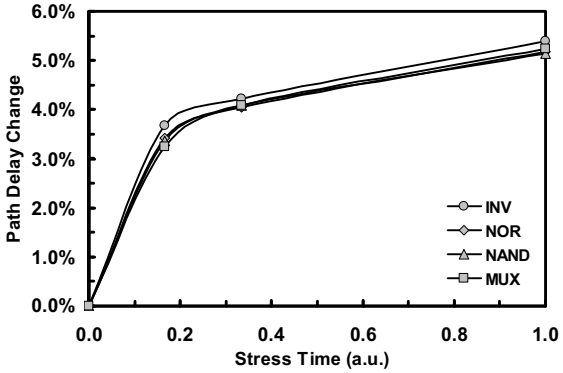

Fig. 1: Measured path delay degradation versus accelerated DC stress time for various circuit types [2].

body bias in response to dynamic variations. Thermal sensors [4] are inserted at local hot spots on the die to measure worst-case temperature. V_{CC} droop sensors [1] detect global V_{CC} fluctuations observed across the die which affect all circuit paths. Although the actual drain current change from aging and recovery depends on the local transistor activity factor and state probability, aging sensors [2], [5]-[9] can track critical path degradation from worst-case DC stress to capture the effects and aging and recovery during power up/down sequences and sleep modes [2]. Since this design requires time to detect and respond to dynamic variations to avoid actual timing violations, this circuit technique reduces the F_{CLK} guardbands for slow-changing global variations, resulting in higher average F_{CLK}. Alternatively, the average F_{CLK} benefits may be converted to lower average energy by decreasing V_{CC}.

As an example of this circuit technique, measurements from a 90nm test-chip [5] demonstrate the dynamic response to temperature changes in Fig. 3. The test-chip [5] contains thermal and V_{CC} droop sensors as well as adaptive F_{CLK} and body biasing circuits. Starting at time zero in Fig. 3, the test-chip operates at an F_{CLK} and body bias targeted for 60°C. Body bias is optimized for minimum total power at a given F_{CLK}. As temperature increases, the thermal sensor detects the temperature change and communicates this change to the adaptive control circuits. Since the test-chip performance degrades at higher temperature, the adaptive control circuits respond by lowering F_{CLK} to ensure correct operation at the higher temperature. Furthermore, the body bias is also lowered to counteract the increasing leakage current at higher temperatures. As temperature decreases, F_{CLK} and body bias are adjusted to the original values to maintain higher performance and energy efficiency.

The disadvantages of on-die sensors and adaptive circuits include the inability to respond to fast-changing variations such as high-frequency V_{CC} droops [1] or local path-level variations.

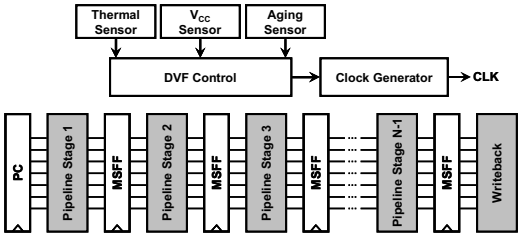

Fig. 2: Sensors with dynamic voltage and frequency (DVF) control circuits.

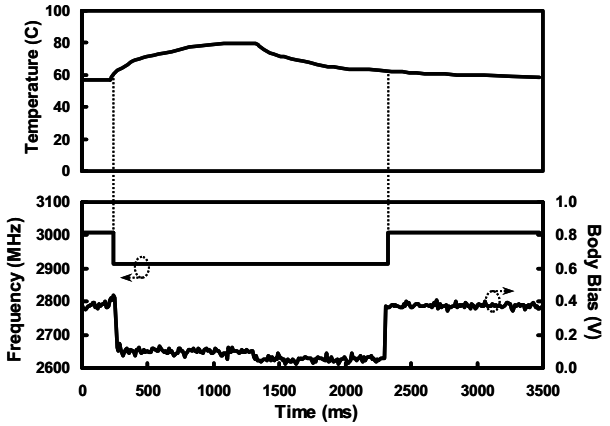

Fig. 3: Measured dynamic response in clock frequency and forward body bias to on-die temperature variations [5].

Furthermore, analog and digital sensors as well as adaptive circuits require substantial calibration time per die, leading to increased testing costs. Although sensors may be tuned during test to reduce the impact of within-die variations on sensor accuracy, an F_{CLK} guardband is still necessary to ensure coverage across a wide range of V_{CC} and temperature conditions as well as for transistor aging.

4. Tunable Replica Circuits with Recovery

In comparison to the previous circuit technique in Section 3, F_{CLK} guardbands are further reduced by combining tunable replica circuits (TRC) for timing-error prediction with error recovery [2] as illustrated in Fig. 4. This scheme removes the response time constraint imposed on the previous technique, thus eliminating the F_{CLK} guardbands for both slow and fast global dynamic variations. TRCs, which toggle each clock cycle, are inserted adjacent to each pipeline stage and calibrated to track local critical path delays. In contrast to previous TRC designs with time-to-digital converters [10], the TRCs in Fig. 4 drive an error-detection sequential (EDS) [11]-[17] to detect late timing transitions from dynamic variations. The TRC and the local pipeline stage use the same V_{CC} and clock, enabling the TRC to detect V_{CC} droops at finer granularity and to capture the clock-to-data relationship per pipeline stage.

TRCs are designed with different logic stages (e.g., inverters, NANDs, NORs, pass gates, and repeated interconnects). In Fig. 5, path delay sensitivities to V_{CC} droop and temperature are measured across various circuit types. At high V_{CC}, a combination of inverter and repeated interconnect delay components is adequate for the TRC to track critical path delay variations [10]. From Fig. 5, additional delay components (e.g., stacked gates and pass gates) or re-tuning may be required to track variations across wide ranges of V_{CC} and temperature, where delay sensitivities increase and the inverse delay dependence on temperature is observed.

When dynamic variations induce a late timing transition in the TRC, the EDS generates an error signal, which is pipelined to the writeback stage and the error control unit (ECU). Valid control logic at the writeback stage invalidates erroneous data. The ECU replays the appropriate instruction and signals the DVF control to halve F_{CLK} to ensure correct operation during the replay even if dynamic variations persist [17]. After the replayed instruction finishes, the ECU sends a reset signal to validate data at the writeback stage and signals the DVF control to resume at target F_{CLK}. By detecting and correcting timing errors, proper logic functionality is maintained. Since additional clock cycles are

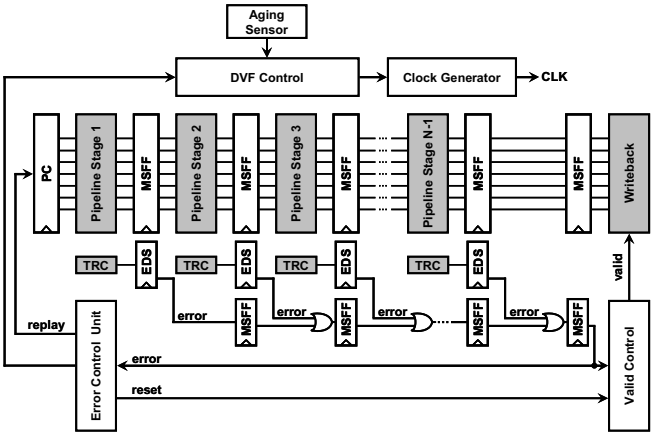

Fig. 4: Tunable replica circuits (TRCs) for error prediction with error recovery.

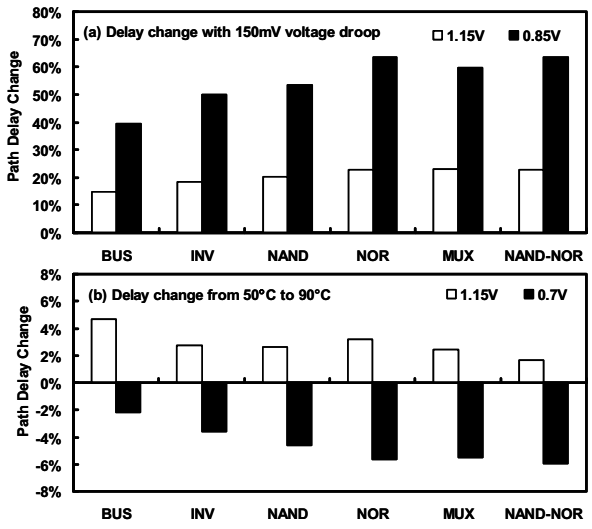

Fig. 5: Measured path delay change for various circuit types due to (a) 150mV voltage droop and (b) temperature change from 50°C to 90°C [2].

required for error recovery, instructions per cycle (IPC) reduce as errors occur. Assuming infrequent timing errors from dynamic variations, the IPC reduction is relatively small as compared to the F_{CLK} gains from removing the guardbands for slow and fast global dynamic variations, resulting in higher performance. As an alternative to performance benefits, the F_{CLK} gains may be traded-off for energy efficiency by reducing V_{CC}.

The disadvantages of the TRC with recovery include signaling errors and activating recovery when an actual error did not occur. In addition, TRCs cannot detect path-level dynamic variations and TRCs require a delay guardband to ensure that the TRC per pipeline is slower than the critical paths across wide ranges of V_{CC} and temperature. Although the digital TRCs are less complex than the analog sensors in Section 3, post-silicon tuning of TRCs impact testing costs. The recovery design requires an additional stabilization pipeline stage to accommodate the 1-cycle latency for propagating error signals in the N-1 pipeline stage [14]-[17]. This stabilization stage ensures that instructions are valid before committing the state at writeback.

5. Embedded Error Detection with Recovery

As illustrated in Fig. 6, embedding EDS circuits [11]-[17] in all critical paths eliminates the F_{CLK} guardbands for fast and slow as well as global and local dynamic variations. In contrast to the circuit techniques in Sections 3 and 4, this design does not require post-silicon tuning. Embedded EDS circuits detect late transitions in the actual critical paths. Error signals from each EDS per pipeline stage are combined via an OR tree to generate a single error signal. The recovery circuits in Fig. 4 and Fig. 6 are similar. When dynamic variations induce an actual timing error, the error is detected and corrected to maintain proper system functionality. In addition to removing the F_{CLK} guardbands for dynamic variations, further F_{CLK} benefits are possible by exploiting path-activation probabilities. If the slowest paths on the die are infrequently activated, the F_{CLK} may increase higher than the critical path operating frequency. When these critical paths are activated, the timing error is detected and corrected.

In Fig. 7, measurements from a 65nm test-chip [17] with embedded EDS and recovery circuits demonstrate the capability to

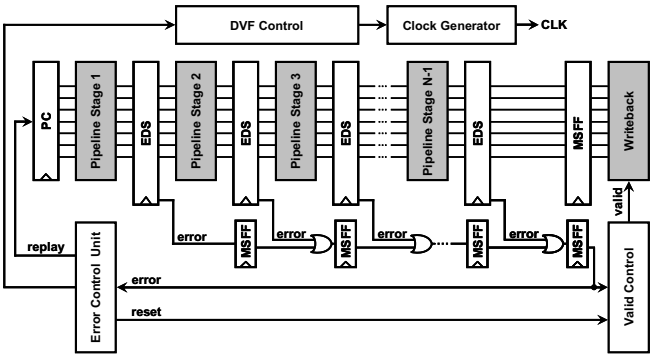

Fig. 6: Embedded error-detection sequential (EDS) circuits with error recovery.

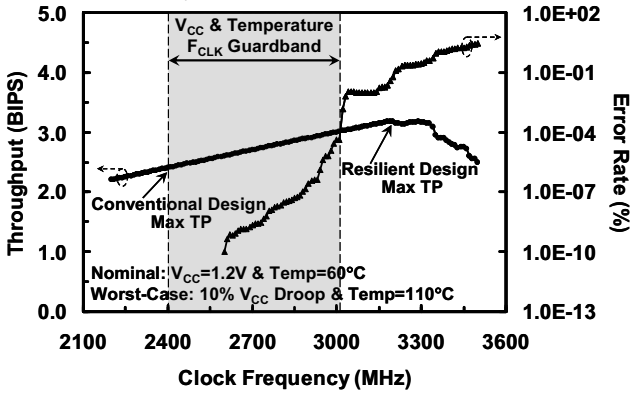

Fig. 7: Measured throughput (TP) and error rate versus clock frequency (F_{CLK}) for a 65nm resilient circuit test-chip with embedded EDS and recovery circuits [17].

eliminate the F_{CLK} guardbands for dynamic V_{CC} and temperature variations as well as to exploit path-activation probabilities for maximizing throughput. For a given F_{CLK}, error rate depends on the path histogram, as dictated by design optimization, as well as path-activation probabilities and environmental variations, as determined by workloads. In Fig. 7, throughput increases linearly as F_{CLK} increases with no errors. Once errors occur, IPC reduces as a function of error rate and recovery time. Since V_{CC} droop events are infrequent, throughput gains continue as F_{CLK} increases into the V_{CC} and temperature guardband region. When F_{CLK} reaches 3020MHz, the first path failure occurs under nominal conditions, resulting in a sharp error rate increase. Since the path-activation probability is low for slow paths in this workload, further throughput gains are achieved at higher F_{CLK}. The maximum throughput of 3.17 billion instructions per second (BIPS) corresponds to a 3200MHz F_{CLK}. Increasing F_{CLK} further leads to a larger error rate, where IPC reduction outweighs F_{CLK} gains. The maximum throughput to guarantee correct functionality within the presence of worst-case dynamic V_{CC} and temperature variations for a conventional design is 2.4BIPS, corresponding to an F_{CLK} of 2400MHz. From Fig. 7, a resilient design with embedded EDS and recovery circuits enables 25% throughput gain over a conventional design by eliminating the F_{CLK} guardband for dynamic V_{CC} and temperature variations and an additional 7% throughput increase from exploiting path-activation probabilities.

The disadvantages of embedded EDS circuits with recovery include the additional clock energy overhead for EDS circuits. Although datapath metastability has previously been the primary concern for EDS circuits, this issue has been addressed in recent EDS implementations [16]-[17]. The fundamental trade-off in

embedded EDS circuits is the maximum path delay (max-delay) constraint versus the minimum path delay (min-delay) constraint. The fraction of the cycle time in which late timing transitions can be detected in embedded EDS circuits directly penalizes the min-delay constraint. Although this trade-off may not be advantageous for microprocessors with deep pipelines (i.e., small number of logic stages between sequentials) and corresponding stringent min-delay requirements, the microarchitecture for recent microprocessors has moved towards shallow pipelines (i.e., large number of logic stages between sequentials) to improve energy efficiency [18]-[19]. Microprocessors with shallow pipelines greatly relax the min-delay requirements as compared to a deep pipeline design, enabling a more effective trade-off of max-delay improvement for min-delay penalty. Furthermore, embedded EDS circuits require duty-cycle control circuits to maintain a constant high clock phase delay (i.e., error-detection window) at low and high F_{CLK} for min-delay protection. As described for the recovery design in Section 4, an additional stabilization pipeline stage is required for recovery.

6. Opportunities for CAD

Recommendations are offered for CAD research to further enhance the performance and energy efficiency of dynamic variation-tolerant circuit techniques. First, a rigorous analysis of microprocessor path-activation probabilities is desired across a range of typical workloads. This exploration would provide insight to the potential gains of exploiting activation probabilities in critical paths through embedded EDS and recovery circuits. Second, the path-activation probabilities introduce a new variable for timing optimization. As illustrated through a conceptual example in Fig. 8(a), all paths in a conventional timing optimization must satisfy a target cycle time. For embedded EDS and recovery circuits, timing optimization is based on combining the path-delay histogram with path-activation probabilities. As described in Fig. 8(b), infrequently activated paths could have a relaxed timing constraint as compared to frequently activated paths to reduce energy. Third, less stringent assumptions for cross-coupling capacitance and MIS could be applied in timing analysis for energy savings. Pre-silicon design methodologies often apply pessimistic assumptions for cross-coupling capacitance and MIS even though these events may rarely occur, leading to an over-design for many paths, and consequently, high energy costs. Allowing embedded EDS and recovery circuits to detect and correct late transitions from infrequent cross-coupling and MIS events, the timing constraints for cross-coupling capacitance and MIS could be relaxed, resulting in lower energy. Finally, the additional circuit features for dynamic variation tolerance introduce new placement and routing complexities, warranting an investigation in floorplanning optimization.

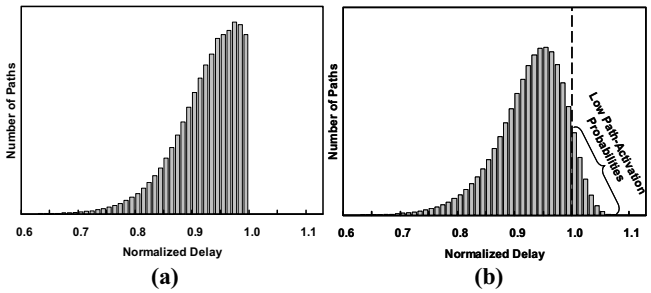

Fig. 8: Conceptual path-delay histograms optimized for (a) conventional and (b) embedded EDS with recovery circuits.

7. Conclusion

Dynamic variation sensors with adaptive voltage and frequency circuits, tunable replica circuits for timing-error prediction with error recovery, and embedded error-detection sequential (EDS) circuits with error recovery are three circuit techniques that reduce the clock frequency guardbands for dynamic variations to improve microprocessor performance and energy efficiency. These circuits provide unique trade-offs in guardband removal and overhead. CAD research opportunities to further enhance performance and energy efficiency include: (i) Explore path-activation probabilities across various workloads, (ii) Optimize timing by coupling the path-delay histogram with path-activation probabilities, (iii) Relax cross-coupling capacitance and multiple-input switching constraints in timing analysis, and (iv) Optimize floorplanning to accommodate additional circuit features.

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