

## **DLD Lab End Exam Spring - 2022**

### **Instructions**

1. Time: 9:00 Am to 11:00 Am
  2. Date: 31/03/2022
  3. Naming convention to upload the files
    - a) Roll No\_Name\_Q.No.pdf
    - b) Roll No\_Name\_Q.No.circ (logisim file)
- A2. Implement a synchronous counter using JK flip-flop for the given sequence

**0,1,3,5,7,9,11,13**

Steps to be followed

- 1.Flip-flop truth table
- 2.Excitation table
- 3.State Diagram
- 4.Circuit excitation table
- 5.K-Maps
- 6.Booleen Expressions
- 7.Logic Diagram/Circuit Diagram
- 8.Logisim file/Simulation file.