DLD, Mid semester Exam

IIITS, Chittoor

Date: 25/03/2022 Duration: 90 Mins Maximum Marks: 25M

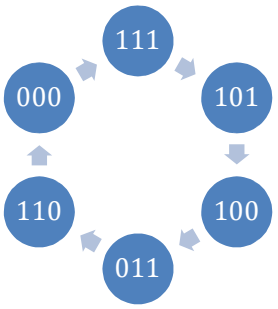
SET-Q

1. Implement the following Boolean expression using 2:4 Decoder and other external logic gates. [5M]

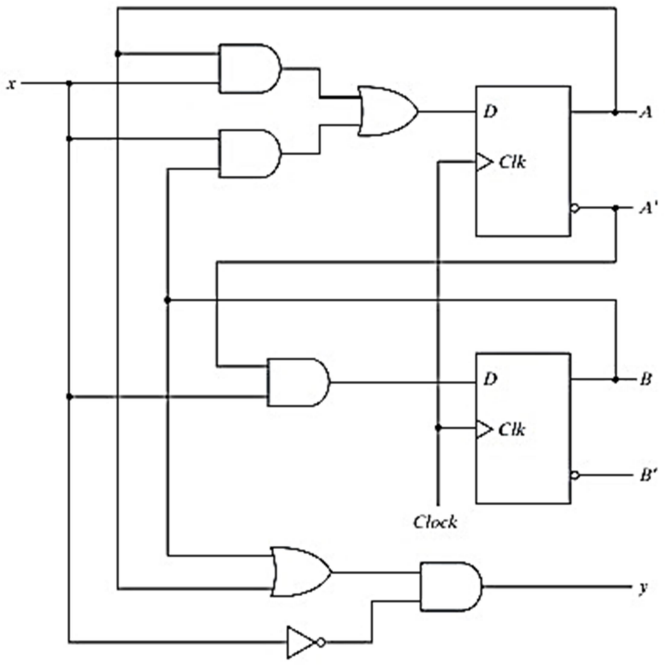
$$F(A, B, C) = AB'C + A'BC' + B'C'$$

2. Design a magnitude comparator circuit to compare the following inputs
A=110; B= 111 [5 M]

3. Design the counter using T flip-flop which the following state diagram [5 M]



4. Determine the Next State and Output value of the following circuit, when the present state of the $A(t)=1$, $B(t)=1$, and input $x(t)=0$. [5M]



5. Write a Verilog gate-level model of a circuit that will produce 2:4 decoder [5M]

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