DLD

Mid semester Exam

IIITS, Chittoor

Date: 25/03/2022 Duration: 90 Mins Maximum Marks: 25M

Instructions

a) Answer all questions
b) Do not copy from any source, if found, you will be penalized according to institute norms.
c) Write neatly in A4 sheets (White).
d) On all pages write
    a. Your name
    b. Roll number
    c. Question paper code
e) Scan properly and convert into.pdf format as a single file (Only pdf is allowed)
f) **For uploading the file in Google form, Name the file as "Rollno.pdf"**
If you don't upload the correct file or if you submit an invalid file, e-mailing faculty or uploading later is not allowed.

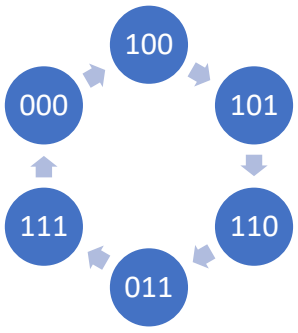
Paper Code B

1. Implement the following Boolean expression using 2:4 Decoder and other external logic gates.

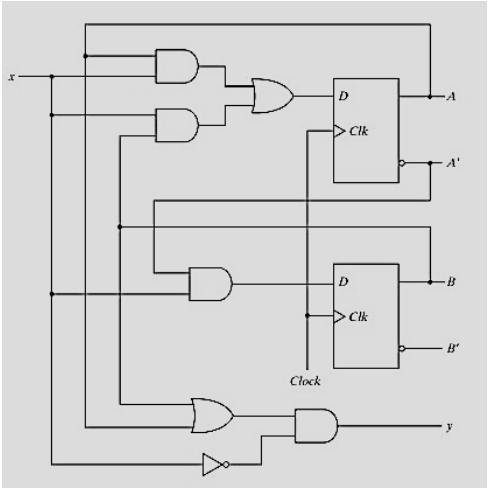
$$F(A,B,C) = AC + A'BC + B'C'$$

2. Design a magnitude comparator circuit to compare the following inputs. A= 111; B= 010

3. Design the counter using D flip-flop which the following state diagram



4. Determine the Next State and Output value of the following circuit, when the present state of the A(t)=0, B(t)=1, and input *x*(t)=1.



5. Draw a 2 x 2 RAM circuit. Write Verilog code for the following circuit.