GD54/74HC74, GD54/74HCT74 DUAL D-TYPE FLIP-FLOPS WITH PRESET & CLEAR

General Description

These devices are identical in pinout to the 54/74LS74. They consist of two D-type flip-flops with individual preset, clear, and clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \overline{Q} outputs are available from each flip-flop. The preset & clear inputs are asynchronous. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- · Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts for HCT 4.5 to 5.5 volts
- Low input current: 1µA Max.
- Low quiescent current: 40µA Max. (74HC)
- High noise immunity characteristic of CMOS
- · Diode protection on all inputs

Pin Configuration 14 Vcc 1CLR 1 13 2CLR 1D 2 1CLK 3 12 2D 1PR 4 74 11 2CLK 10 2PR 10 5 10 6 9 20 8 2ā GND 7 Suffix-Blank Plastic Dual In Line Package Suffix-J Ceramic Dual In Line Package Suffix-D Small Outline Package

Logic Diagram

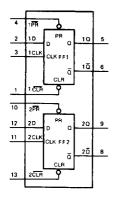


Fig. 1 Logic diagram

Function Table

| | INPL | OUTPUT | | | |
|----|------|--------|----|----|----|
| PR | CLR | CLK | nD | пQ | ηQ |
| L | Н | Х | Х | Н | L |
| Н | L | Х | Х | L | Н |
| L | L | Х | Х | Н | н |

| | INPL | JTS | OUTPUTS | | | | |
|----|------|-----|---------|------------------|----------------------|--|--|
| PR | CLR | CLK | nD | Q _{n+1} | \overline{Q}_{n+1} | | |
| н | Н | 1 | L | L | Н | | |
| Н | н | 1 | Н | н | L | | |

H = HIGH voltage level

L = LOW voltage level

X = don t care

= LOW to-HIGH CLK transition

Q_{n+1} = state after the next LOW to-HIGH CLK transition

Absolute Maximum Ratings

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX. | UNIT |
|---------------------------------|-----------------------------------|---|-----|------------|------|
| V _{cc} | DC Supply voltage | | -05 | +7 | > |
| l _{ik} l _{ok} | DC input or output diode current | for V _I <-0.5 or V _I >V _{CC} +0 5V | | 20 | mA |
| l _o | DC output source or sink current | for -0 5V <v<sub>o<v<sub>cc+0 5V</v<sub></v<sub> | | 25 | mA |
| Icc | DC V _{CC} or GND current | | | 50 | mA |
| T _{stg} | Storage temperature range | | -65 | 150 | °C |
| P _D | Power dissipation per package | above +70°C. derate linearly with 8mW/K | | 500 | mW |
| T _L | L'ead temperature | At distance 1/16±1/32 in from case for 60 sec(CERAMIC) 10 sec(PLASTIC) | | 300 260 | °C |

Recommended Operating Conditions

| | LIM | IITS | UNITS |
|---|-----|-----------------|-------|
| CHARACTERISTIC | MIN | MAX | UNITS |
| Supply-Voltage Range V _{CC} . GD54/74HC Types | 2 | 6 | ٧ |
| GD54/74HCT Types | 4 5 | 5.5 | |
| DC Input or Output Voltage V _I , V _O | 0 | V _{cc} | ٧ |
| Operating Temperature T _A : GD74 Types | -40 | +85 | °C |
| GD54 Types | -55 | +125 | 0 |
| Input Rise and Fall times t _r , t _i . GD54/74HC Types at 2V | | 1000 | |
| at 4.5V | | 500 | ns |
| at 6V | | 400 | 113 |
| GD54/74HCT Types at 4 5V | | 500 | |

Logic diagram

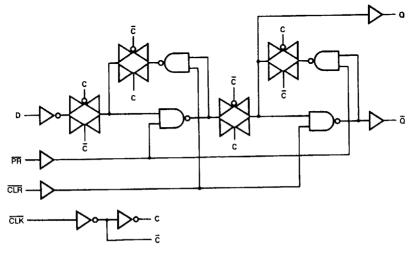


Fig. 2 Logic diagram (one flip-flop)

DC Electrical Characteristics for HC

| SYMBOL | PARAMETER | TEST | CONDITION | v _{cc} | Т | 25°(| 0 | GD74HC 74 | | GD54HC74 | | UNIT |
|--------------------|-----------------------------------|---|--|-------------------|--------------------|-------------------|-------------------|--------------------|-------------------|--------------------|-------------------|------|
| | | | | (V) | MIN. | TYP | MAX. | MIN | MAX | MIN. | MAX | |
| V ^{IH} | HIGH level input | | | 2.0 4.5 6.0 | 1 5 3 15 4 2 | | | 1 5 3 15 4.2 | | 1 5 3 15 4 2 | | v |
| V _{IL} | LOW level input voltage | | | 2.0 4.5 6.0 | | | 0.3 0 9 1 2 | | 03 09 12 | | 03 09 12 | V |
| HIGH leve | HIGH level | V _{IN} =V _{IH} | I _{OH} = ~ 20μA | 2 0 4.5 6.0 | 1 9 4 4 5 9 | 2.0 4.5 6.0 | | 1.9 4 4 5 9 | | 1 9 4 4 5 9 | | v |
| | output voltage or V _{IL} | | I _{OH} =-4mA I _{OH} =-5.2mA | 4 5 6 0 | 3 98 5 48 | 4.3 5 2 | | 3 84 5 34 | | 3 7 5 2 | | |
| V _{OL} | LOW level | V _{IN} =V _{IH} | l _{OL} =20μA | 2 0 4 5 6 0 | | | 0 1 0 1 0 1 | | 0 1 0 1 0 1 | | 0 1 0 1 0 1 | v |
| | output voltage | or V _{IL} | I _{OL} =4mA I _{OL} =5 2mA | 4 5 6.0 | | 0.17 0.15 | 0.26 0.26 | | 0.33 0.33 | | 0 4 0 4 | |
| [I _{IN}] | Input leakage Current | V _{IN} =\ | CC or GND | 60 | | | 0 1 | | 10 | | 1 0 | μΑ |
| lcc | Quiescent Supply Current | V _{IN} =\ I _{out} =(| / _{CC} or GND DµA | 60 | | | 4 | | 40 | | 80 | μΑ |

DC Electrical Characteristics for HCT

| SYMBOL | PARAMETER | TEST | CONDITION | v _{cc} | Т | A=25° | С | GD74I | HCT74 | GD54 | HCT 74 | UNIT |
|-----------------|-----------------------------|----------------------------------|---|------------------|-------------|------------|-------------|-------------|-------------|------------|--------|------|
| | | | | (V) | MIN | TYP | МАХ | MIN | МАХ | MIN | MAX | |
| V _{IH} | HIGH level input Voltage | | | 4 5 to 5 5 | 20 | | | 20 | | 20 | | ٧ |
| V _{IL} | LOW level | | | 4 5 to 5 5 | | | 08 | | 08 | | 08 | ٧ |
| V _{OH} | HIGH level output voltage | V _{IN} =V _{IH} | i _{OH} =-20μA i _{OH} =-4mA | 4 5 4 5 | 4 4 3 98 | 4 5 4 3 | | 4 4 3 84 | | 4 4 3 7 | | ٧ |
| V _{OL} | LOW level output voltage | v _{IN} =v _{IH} | I _{OL} =20μA | 4 5 4 5 | | 0 17 | 0 1 0 26 | | 0 1 0 33 | | 01 | ٧ |
| I _{IN} | Input leakage Current | V _{IN} = | V _{CC} or GND | 5 5 | | | 01 | | 10 | | 10 | μΑ |
| lcc | Quiescent Supply Current | V _{IN} = | V _{CC} or GND DµA | 5 5 | | | 4 | | 40 | | 80 | Αц |

Timing Requirements for HC: t_r = t_t =6ns C_L =50 pF

| 0,4501 | 0.0 | ALIETED | v _{cc} | 1 | A=25° | С | GD74I | HC 74 | GD54HC74 | | UNIT |
|------------------|-----------------|----------------------|-------------------|----------------|---------------|-----------------|-----------------|-----------------|-----------------|-----|------|
| SYMBOL | PAH | AMETER | (V) | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| | PR or CLR (low) | 2 0 4 5 6 0 | 80 16 14 | 30 10 8 | | 100 20 18 | | 120 25 22 | | ns | |
| t _w | Pulse width | CLK (high or low) | 2 0 4 5 6 0 | 80 16 14 | 30 10 8 | | 100 20 18 | | 120 25 22 | | ns |
| t _{su} | Setup time | Data before CLK † | 2 0 4.5 6.0 | 60 15 14 | 30 10 8 | | 80 18 16 | | 100 20 18 | | ns |
| t _{rec} | Recovery time | PR or CLR inactive | 2 0 4 5 6 0 | 5 5 5 | 0 0 | | 5 5 5 | | 5 5 5 | | ns |
| t _h | Hold time | Data after CLK † | 2 0 4 5 6.0 | 3 3 3 | 0 0 0 | | 3 3 3 | | 3 3 3 | | ns |

AC Characteristics for HC: t_r = t_t =6ns C_L=50 pF

| SYMBOL | PARAMETER | V _{CC} | T _A =25°C | | | GD74 | HC74 | GD54HC74 | | UNIT |
|--------------------|--|-------------------|----------------------|----------------|-----------------|---------------|-----------------|---------------|-----------------|------|
| J T M DOL | (AIVANETELL | (V) | MIN. | TYP. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| f _{max} | Maximum Clock Pulse Frequency | 2.0 4.5 6.0 | 6 30 35 | 20 65 75 | | 5 25 30 | | 4 20 25 | | MHz |
| t _{PLH} / | Propagation Delay Time nCLK to nQ, nQ | 2.0 4.5 6.0 | | 45 15 14 | 170 30 28 | | 210 40 35 | | 250 50 45 | ns |
| t _{PLH} / | Propagation Delay Time | 2.0 4.5 6.0 | | 45 14 13 | 180 32 28 | | 220 42 35 | | 260 52 45 | ns |
| t _{PLH} / | Propagation Delay Time | 2.0 4.5 6.0 | | 45 14 13 | 180 32 28 | | 220 42 35 | | 260 52 45 | ns |
| t _{TLH} / | Output Transition Time | 2.0 4.5 6.0 | | 25 8 7 | 70 15 13 | | 85 18 16 | | 100 22 18 | ns |

Timing Requirements for HCT: $t_{\rm r}$ = $t_{\rm r}$ =6ns $C_{\rm L}$ =50 pF

| SYMBOL | DAD | PARAMETER | | T _A =25°C | | | GD74HCT74 | | GD54HCT74 | | UNIT |
|----------------------------|----------------------|--------------------|-----|----------------------|-----|-----|-----------|-----|-----------|-----|------|
| STWIBOL | FAID | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| ¹ w Pulse width | PR or CLR (low) | 4 5 | 18 | 10 | | 20 | | 25 | | ns | |
| | CLK (high or low) | 4 5 | 16 | 10 | | 20 | | 25 | | ns | |
| t _{su} | Setup time | Data before CLK † | 4 5 | 15 | 10 | | 18 | | 20 | | ns |
| trec | Recovery time | PR or CLR inactive | 4 5 | 5 | 0 | | 5 | | 5 | | ns |
| t _h | Hold time | Data after CLK † | 4 5 | 3 | 0 | | 3 | | 3 | | ns |

AC Characteristics for HCT: t_r = t_f =6ns C_L =50 pF

| SYMBOL | PARAMETER | v _{cc} | T _A =25°C | | | GD74HCT74 | | GD54HCT74 | | UNIT |
|--------------------|---|-----------------|----------------------|-----|-----|-----------|------|-----------|-----|------|
| | | (V) | MIN | TYP | MAX | MiN | MAX. | MIN | MAX | |
| f _{max} | Maximum Clock Pulse Frequency | 45 | 27 | 54 | | 22 | | 18 | | MHz |
| t _{PLH} / | Propagation Delay Time nCLK to nQ, nQ | 45 | | 18 | -35 | | 44 | | 53 | ns |
| t _{PLH} / | Propagation Delay Time ⊓PR to nQ, nQ | 45 | | 20 | 35 | | 44 | | 53 | ns |
| t _{PLH} / | Propagation Delay Time $n\overline{\text{CLR}}$ to nQ , $n\overline{Q}$ | 45 | | 20 | 35 | | 44 | | 53 | ns |
| t _{TLH} / | Output Transition Time | 45 | | 8 | 15 | | 18 | | 22 | ns |

AC Waveform

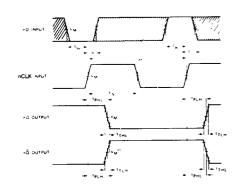


Fig. 3 Waveforms showing the clock (nCLK) to output (nQ $n\overline{Q}$) propagation delays the clock pulse width the nD to nCLK set up the nCLK to nD hold times the output transition times and the maximum clock pulse frequency

Note to Fig. 3

The shaded areas indicate when the input is permitted to change for predictable output per formance.

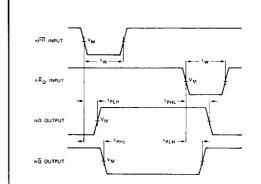


Fig. 4 Waveforms showing the preset and clear input to output $(nQ, n\overline{Q})$ propagation delays and the preset and clear pulse width

Note to AC waveforms

(1) HC $V_M = 50^{\circ} \circ V = GND$ to V_{CC} HCT $V_M = 1$ 3V $V_i = GND$ to 3V