Phase detector and Phase locked loop

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Aim:

- To study the workings of Phase Detector and Phase Locked Loop by constructing a phase detector and phase-locked loop
- To find the variation of phase difference with potentiometer resistance, and output DC.
- To study the relationship between Phase Difference and the DC control signal of PLL.
- Calculate the lock range and the capture range for different capacitor values.

Apparatus:

- IC565 Op-Amp
- DC Power Supply
- Oscilloscope
- Function Generator
- Multimeter
- 10K Potentiometer
- Resistors and Capacitors of required values

Setup:

Observations:

$V_{pp} = 12\text{V}$, $f = 5\text{kHz}$

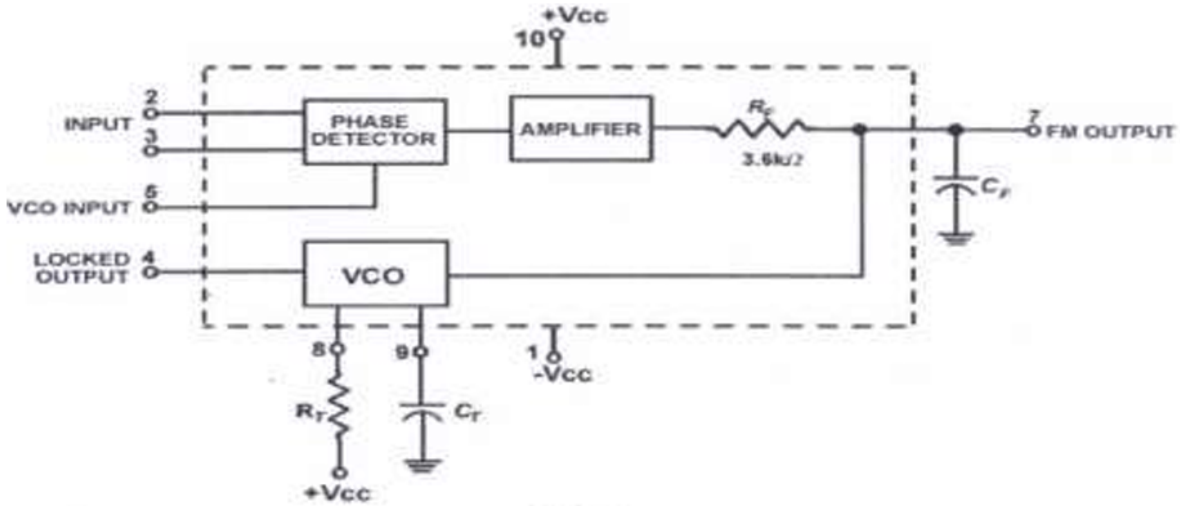

Figure 1: Block Diagram of PLL-565

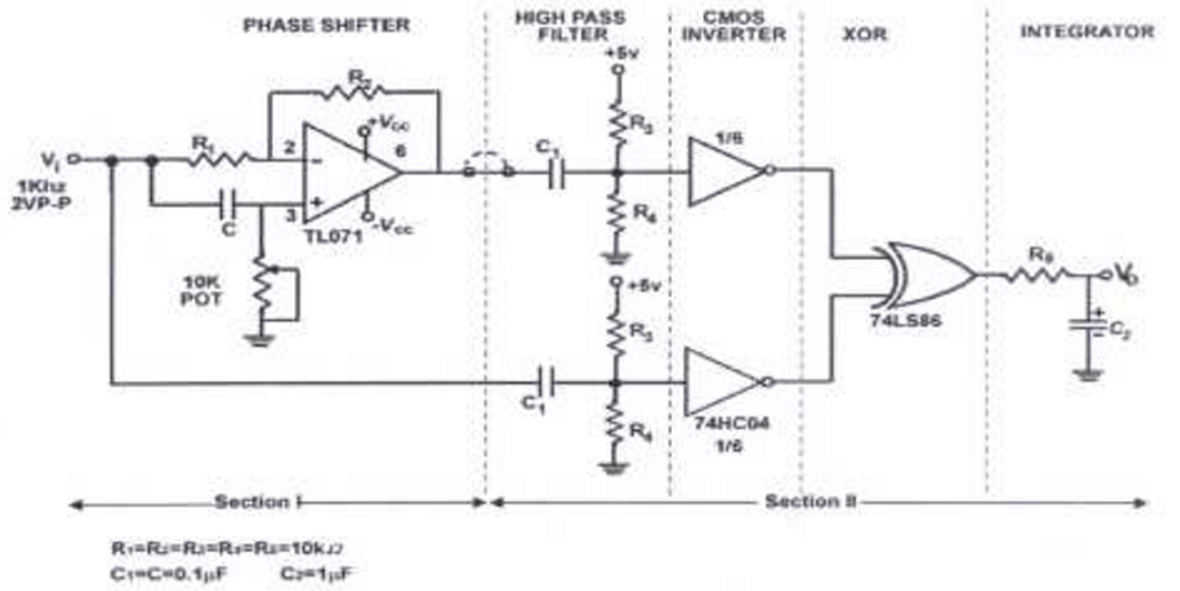

Figure 2: Circuit Diagram of Phase Shifter

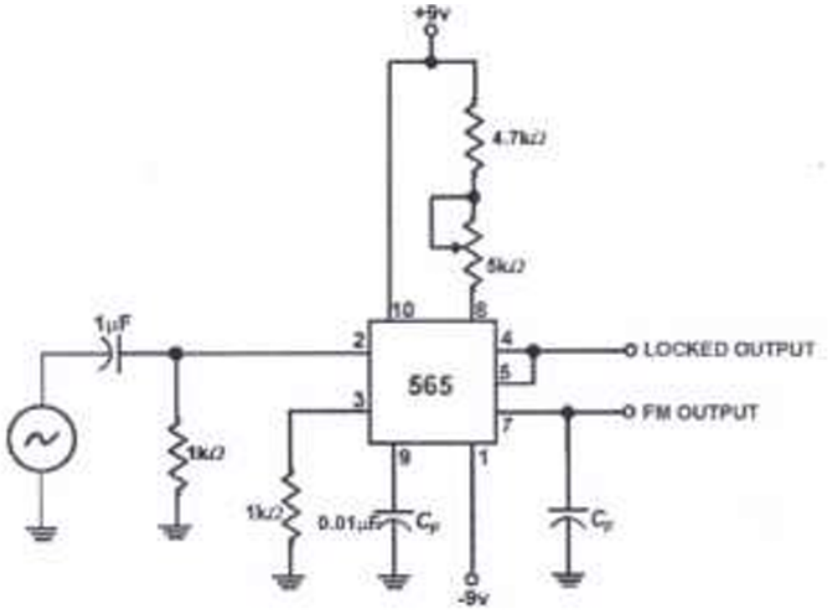

Figure 3: Experimental PLL Circuit

Sl. No	**Resistance (in kΩ)**	**Phase Difference φ (in $^\circ$)**
1	0.0063	180
2	0.0566	170
3	0.1018	160
4	0.155	150
5	0.2112	140
6	0.2725	130
7	0.342	120
8	0.418	110
9	0.507	100
10	0.591	90
11	0.683	80
12	0.806	70
13	0.919	60
14	1.180	50
15	1.472	40
16	1.898	30
17	2.898	20
18	6.5	10

Table 1: Variation of Phase Difference with Resistance

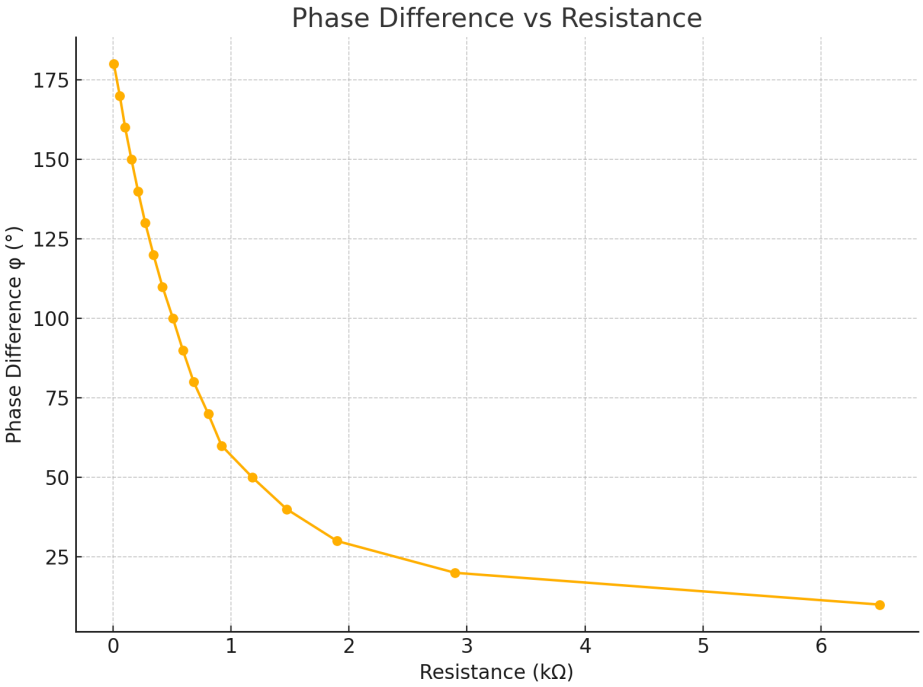

Figure 4: Plot of Phase Difference vs Resistance

Sl.No	C_f (in μF)	$f_{\max}$ (kHz)	$f_{\min}$ (kHz)	B_c (kHz)
1	0.1	6.0	3.2	2.8
2	0.2	6.5	2.7	3.8
3	0.047	7.0	2.7	4.3

Table 2: Capture Range Data

Sl.No	**Frequency (kHz)**	**Voltage (V)**
1	4	9.24
2	5	8.53
3	6	8.88

Table 3: FM Output Readings

Error Analysis:

- Error in Resistance(ΔR) = 0.1 kHz
- Error in Phase Difference ($\Delta\phi$) = 1°
- Error in Voltage (ΔV) = 0.001 V

Error in Capture Range:

- $\Delta f_{min} = 0.01$kHz
- $\Delta f_{max} = 0.01$kHz
- Error in measuring $\Delta B_c = \Delta f_{min} + \Delta f_{max} = 0.02$kHz
- For $C_f = 0.1\mu$F, $B_c = 2.8 \pm 0.02$kHz
- For $C_f = 0.2\mu$F, $B_c = 3.8 \pm 0.02$kHz
- For $C_f = 0.047\mu$F, $B_c = 4.3 \pm 0.02$kHz

Results:

- Phase difference between input and output voltage and resistance is nearly linear decreasing but decays with increase in resistance.
- The control DC voltage from the phase detector seemingly decreases with decrease in the phase difference in an almost linear relationship.
- We can see the capture range always falls withing the lock in range and decreases with increase in the capacitance value.
- The FM output voltage decreases with increase in input frequency.

Discussion:

- We can thus see the use of phase locked loops for clock generation and synchronization in digital systems. Through it, we obtain stable and precise timing across various components.
- We can generate higher frequency clocks from a low frequency reference using frequency multipliers, which find use in microprocessors and communication systems.
- The nonlinear nature of the FM output voltage trend with input frequency demonstrates the filtering and demodulation behavior of the loop filter and VCO.

- By tuning the capacitor C_f, we directly influenced the capture range, which demonstrates how loop dynamics depend on component selection—this is important for real-world applications like data recovery in noisy conditions.