	REVISIONS	
REV	DESCRIPTION	
F	F RELEASE/CHANGE PER ECO-R179973	

Test Protocol CPU Board PB540, PB560

COVIDIEN
6135 Gunbarrel Avenue
Boulder, CO 80301

TITLE: Test Protocol, CPU Board, PB540, PB560 10027876

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REV F

10027876

1.0 INTRODUCTION

1.1 Purpose

The purpose of this protocol is to test the CPU board used for PB540, PB560, PB520 and future ventilators.

1.2 Revision History

Revision	Author	Change Description	
Α		Incorporated review action items.	
В		Clarification and/or correction of test steps.	
С		ncorporate action Items from Design Verification Review	
D		dd FiO2 testing to cover all the test for the PB560	
Е		add USB Communication test to cover all the test for the	
		PB560.	
F		Corrected table in 3.3.4. Removed refs to 640. Removed test	
		75 as its not executed in this procedure – pointer to validation.	

1.3 Scope

This protocol shall test the operational ranges and mechanical properties of the CPU board. Packaging standards, and tests which require an environmental chamber are excluded from this test protocol.

1.4 Reference Documents

1.4.1 Internal Documents

	Ref	Part Number	Rev	Document Title	
	1	10024980	В	CPU Board Requirements	
	2	10035480	Α	PRD PB560	
Г	3	10038637	Α	PB560 Trace Matrix	

1.5 Roles and Responsibilities

This section will define the roles and responsibilities required to release and execute this procedure.

R&D Engineer

The R&D Engineer will be responsible for the following activities:

- Generation of the Test Protocol
- Review of the Protocol
- Release of the Protocol, prior to execution

R&D Engineer / Test Engineer

An R&D Engineer or Test Engineer will be responsible for the following activities:

- Execution of the protocol
- Recording of test results
- · Documentation of issues encountered
- Signing for completion

Review Team

The review team will consist of an R&D Engineer, the individual executing the protocol, a Quality Engineer, and an independent Reviewer.

The team will be responsible for the following activities:

- · Review of the results
- Approval and acceptance of the execution results

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1.6 Issue Tracking

For the purpose of this protocol, issues will be logged in the following areas:

Issues encountered as part of development will be captured in Tracker, or as part of the action items during the review of the document.

Issues encountered during the execution of this protocol will be logged in the comments section of this document. Additional documents can be attached if required.

Issues discussed/encountered after execution will be captured as part of the review minutes or in Tracker.

1.7 Test Equipment

Test Equipment Description	Calibration ID	Calibration Due Date
PC with "ST10Flasher_BE" and "PICFlasher" software		
Digital power supply 0-36 VDC @ 4A		
Two multimeters with at least 4 digits of accuracy, and the ability to measure DC current.	Meter 1:	
	Meter 2:	
Digital oscilloscope.		
Current probe for oscilloscope.		
3020, 2588, 2228, 1924, and 1668 Ohm resistors, 1%, 0.1W	N/A	N/A
250 k Ohm variable resistor	N/A	N/A
Function generator able to generate a pulse with duty cycle adjustable from 50 to 80%, with frequency adjustable from 2 Hz to 1000 Hz, 0.1 % frequency accuracy.		
Flow meter from 0 to 1000 sccm with a ± (3% of reading + 25 sccm) accuracy		
Pressure meter from -200 to +200 mbar ± 0.1mbar		
Absolute pressure meter from 600 to 1100 mbar ± 0.1mbar		
Sound Pressure Level meter		

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1.8 Test Units

	1
Product Serial Number:	Unit 1:
	Unit 2:
	Unit 3:
	Unit 4:
	Unit 5:
	Unit 6:
Board Revision:	Unit 1:
	Unit 2:
	Unit 3:
	Unit 4:
	Unit 5:
	Unit 6:
Firmware version number:	Unit 1:
	Unit 2:
	Unit 3:
	Unit 4:
	Unit 5:
	Unit 6:
Software version number:	Unit 1:
	Unit 2:
	Unit 3:
	Unit 4:
	Unit 5:
	Unit 6:

2.0 ACCEPTANCE CRITERIA

The acceptance criteria will be included as part of the procedure to allow the individual executing the protocol to make the pass/fail determination.

For results that do not fall within the acceptance criteria, circle "Fail" and provide as much information in the comment section.

Some of the tests that have potential variation will have six (6) samples taken. The samples must satisfy a tolerance interval of 95% / 95% or have a rationale for not meeting the criteria.

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3.0 SAMPLE SIZE RATIONALE

The sample size will be based on the parameter type and verification method performed.

Initial testing will be performed to verify functionality by execution and analysis. Based on the test and parameter type, tests may be executed with multiple samples.

Testing will be conducted as specified in the criteria below

3.1 Visual

Parameters verified by visual examination, or analysis will be conducted with a sample size of 1.

3.1.1 Visual Exam

Verification of information contained on labels, confirmation of coloring, or verification of routing or hardware configuration is not expected to have significant variation

3.1.2 Datasheet / Specification Sheet Review

Verification done by review of data or specification sheets is not expected to have significant variation.

3.1.3 Design Analysis

Verification done through analysis is not expected to have significant variation.

3.2 Potential variation

A subset of the tests with parameters that have the potential for variation and have reproducible results will be tested with an initial sample of 6. Tests with variable input that have a variable range will not be used for data analysis.

Parameters that provide accuracy, peak values, or maximum thresholds that have variable (analog) data will be considered to have the potential of variation. The exception to this will be where a single, off the shelf, component influences the results (a parameter review may be sufficient to demonstrate adherence to the requirement).

3.2.1 Variable Measurements

3.2.1.	1 Ac	curacy

3.2.1.2 Maximum level

3.2.1.3 Peak thresholds

3.2.1.4 Position

3.3 Insignificant variation

Testing of parameters, that are not expected to have significant variation (insignificant variation), will be conducted with three (3) samples as recommended in Sample Size Procedure (#10006201).

The following measurement types are not expected to provide significant variation.

3.3.1 Range

Verification that confirms operation or measurement of a range (non-accuracy) is not expected to have significant variation.

3.3.2 Single device/component verification

Verification of an output where a single off the shelf device (component) provides the resultant output is not expected to have significant variation. The specification of the device should demonstrate adherence to the requirement.

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3.3.3 Interconnect

Verification of an interconnect such as a trace or connector is not expected to have significant variation.

3.3.4 Digital

Measurements that provide binary, crystal controlled pulse widths, communication, Digital status, do not provide results where variation is expected or quantifiable.

- 3.3.4.1 Communication Interface
- 3.3.4.2 Digital I/O
- 3.3.4.3 Memory tests
- 3.3.4.4 Clocks
- 3.3.4.5 Pulse Width Modulation (PWM)
- 3.3.4.6 Initial Setting
- 3.3.4.7 Function/sequence operation

Range	3
Range	3
Maximum limit	6
Peak threshold	6
Single Device	3
Single Device	3
Single Device	3
	3
	3
Single Device	3
Single Device	3
Digital	3
Range	3
Digital	3
Digital	3
Accuracy	6
Digital	3
Range	3
Digital	3
Digital	3
Digital	3
Digital	3
Digital	3
Digital	٥
Digital	3
Digital	3
Digital	3
_	_
Digital	3
Digital	3
	Peak threshold Single Device Digital Range Digital Accuracy Digital Range Digital

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Test Procedure	Parameter/Test Type	Sample Size
Power Supply Communication Interface –	Range (accuracy)	6
Battery Voltage Monitor	Digital	2
Buzzer Board Interface – PWM	Digital	3
Buzzer Board Interface – Logic Levels	Digital	
Buzzer Board Interface – Inhibit Key	Digital	3
Buzzer Board Interface – Voltage Monitor Remote Alarm Interface – N.C. Relay Contacts	Range (accuracy) Interconnect	6 3
·	This test verifies resistance of the relay contacts similar to an interconnect	
Remote Alarm Interface – N.O. Relay Contacts	Interconnect This verifies an open circuit (resistance of open relay).	3
Keyboard Interface – "Down" Key	Digital	3
Keyboard Interface – "Up" Key	Digital	3
Keyboard Interface – "Ventil" Key	Digital	3
Keyboard Interface – "Navig" Key	Digital	3
Keyboard Interface – "Valid" Key	Digital	3
Keyboard Interface – "Inhib" Key	Digital	3
Keyboard Interface – Battery LED	Digital	3
Keyboard Interface – DC Presence LED	Digital	3
Keyboard Interface – AC Presence LED	Digital	3
Keyboard Interface – Other LEDs	Digital	3
Display Interface	Digital	3
O2 Flow Sensor Interface (Future option)	Digital	3
O2 Flow Sensor Interface (Future option)	Digital	3
O2 Valve Interface – PWM and Current Drive	Range	3
Consider Doole on Domestic Interference Consideration	Digital - PWM	2
Security Back-up Buzzer Interface – Secondary Alarm	Digital	3
Security Back-up Buzzer Interface – Primary Alarm	Digital	3
RAM Memory	Digital	3
Event Memory	Digital	3
Event Memory – Erase/Program Cycles	Digital	3
Ventilation Settings Memory	Digital	3
Ventilation Settings Memory – Erase/Program	Digital	3
Cycles	Digital	3
Monitoring Memory	Digital	3
Monitoring Memory – Erase/Program Cycles	Digital	3
Watchdog – Power Supervisor	Single device	3
Watchdog – Timeout interval	Digital	3
Watchdog – PFI Trap Function	Digital	3
Clock – Functional Test	Digital	3
Clock – Battery Timekeeping Mode	Digital	3
Device Model ID	Digital	3
Inspiratory Flow Measurement	Accuracy	6
Exhalation Flow Measurement	Accuracy	6
Proximal Pressure Measurement	Accuracy	6
Internal Pressure Measurement	Accuracy	6
Expiratory Valve Pressure Measurement	Accuracy	6
Atmospheric Pressure Measurement	Accuracy	6
O2 Pressure Measurement (Future option)	Accuracy	6
PCB – Size	Controlled on Drawing	3
PCB – Mounting	Controlled on Drawing	3
PCB – Labeling	Content	1

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Test Procedure	Parameter/Test Type	Sample Size
Printed Circuit Board Fabrication Standards	Visual	1
FiO2 Measurement	Accuracy	6

4.0 TEST COVERAGE

The test cases in this procedure shall map to the component specification of the device.

For the initial release all test cases shall be executed.

A trace matrix will be included as part of the procedure, or attached, which shows 100% testing of the requirements contained in the component specification of the device, except packaging tests and system standards conformance which will be covered as part of system level testing.

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5.0 TEST PROCEDURES

5.1 24 Volt Supply Monitor

Test Number TCHWSCPB1; Referenced Requirement HWSCPB1.

- 5.1.1 Test Steps
 - 1 Disconnect the cable from the Power Management Board to the CPU board at the Power Management Board end.
 - 2 Connect the positive lead of a variable power supply, adjusted to 22 VDC, to J7-3 (+24VUTIL).
 - 3 Hold down the Inhibit key, then connect the negative lead of the power supply to J7-24 (Ground). Keep the key held down during startup to place the device into Maintenance Mode.
 - 4 Select "Measurements Check" from the menu.
 - 5 Verify that the displayed value of "24 V Check:" is 22 ± 0.5 VDC.
 - 6 Adjust the power supply to 24 VDC.
 - 7 Verify that the displayed value of "24 V Check:" is 24 ± 0.5 VDC.
 - 8 Adjust the power supply to 26 VDC.
 - 9 Verify that the displayed value of "24 V Check:" is 26 ± 0.5 VDC.

5.1.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
5 - Verify that the displayed "24 V Check:" voltage is 22 ± 0.5 VDC.	21.5 to 22.5		Pass / Fail
7 - Verify that the displayed "24 V Check:" voltage is 24 ± 0.5 VDC.	23.5 to 24.5		Pass / Fail
9 - Verify that the displayed "24 V Check:" voltage is 26 ± 0.5 VDC.	25.5 to 26.5		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.2 Power Failure Indicator

Test Number TCHWSCPB2; Referenced Requirement HWSCPB2.

5.2.1 Test Steps

- 1 Disconnect the cable from the Power Management Board to the CPU board at the Power Management Board end.
- 2 Connect the positive lead of a variable power supply, adjusted to 22 VDC, to J7-3 (24V UTIL).
- 3 Hold down the Inhibit key, then connect the negative lead of the power supply to J7-24 (Ground). Keep the key held down during startup to place the device into Maintenance Mode.
- 4 Select "Measurements Check" from the menu.
- 5 Verify that the displayed voltage value of "Watchdog:" is 22 ± 0.5 VDC.
- 6 Adjust the power supply to 24 VDC.
- 7 Verify that the displayed voltage value of "Watchdog:" is 24 ± 0.5 VDC.
- 8 Adjust the power supply to 26 VDC.
- 9 Verify that the displayed voltage value of "Watchdog:" is 26 \pm 0.5 VDC.

5.2.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
5 - Verify that the "Watchdog:" voltage value is 22 ± 0.5 VDC.	21.5 to 22.5		Pass / Fail
7 - Verify that the "Watchdog:" voltage value is 24 ± 0.5 VDC.	23.5 to 24.5		Pass / Fail
9 - Verify that the "Watchdog:" voltage value is 26 ± 0.5 VDC.	25.5 to 26.5		Pass / Fail

Comments:	 	
Test Operator Signature/Date:	 	

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5.3 Inrush Current

Test Number TCHWSCPB3; Referenced Requirement HWSCPB3.

5.3.1 Test Steps

- 1 Disconnect the cable from the Power Management Board to the CPU board at the Power Management Board end.
- 2 Use the regulated, Variable DC Power Supply (adjusted for 24 VDC) to provide power for the CPU Board. Set the power supply current limit to 3 A. Connect the positive power supply lead to J7-3 (24V UTIL), and the negative power supply lead to J7-24 (Ground).
- 3 Use an oscilloscope with a current probe to monitor the current passing through the positive supply lead that is connected to J7-3.
- 4 Turn on the power supply and capture the output of the current probe (the inrush current waveform) on the oscilloscope.
- 5 Verify that the inrush current does not exceed 2 A.
- 6 Verify that the inrush current is 100 ms or less in duration.

5.3.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
5 - Verify that the inrush current does not exceed 2 A.	< 2 A		Pass / Fail
6 - Verify that the inrush current is 100 mS or less in duration.	< 100 mS		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.4 CPU Board Power Consumption

Test Number TCHWSCPB4; Referenced Requirement HWSCPB4.

5.4.1 Test Step

- 1 Disconnect the cable from the Power Management Board to the CPU board at the Power Management Board end.
- 2 Use the regulated, Variable DC Power Supply (adjusted for 24 VDC) to provide power for the CPU Board. Set the power supply current limit to 3 A. Connect the positive power supply lead to J7-3 (24V UTIL), and the negative power supply lead to J7-24 (Ground).
- 3 Use an ammeter in-line with the positive supply lead (or the digital meter in the power supply, if available) to monitor the power supply current.
- 4 Turn on the Power Supply and record the current to the CPU Board, in mA. (_____ mA)
- 5 Calculate and record the power consumption (in milliwatts) as:

Power = 24 * (measured current in mA).

mW)	١

6 - Verify that the power consumed from the 24 V Power Supply (calculated in the previous step) does not exceed 15000 mW (15 Watts.)

5.4.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that the power consumed from the 24 V Power Supply does not exceed 15000 mW (15 Watts.)	< 15000 mW		Pass / Fail

Comments:		
Test Operator Signature/Date:	 	

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5.5 3.3 Volt Supply

Test Number TCHWSCPB5; Referenced Requirement HWSCPB8, HWSCPB9 and HWSCPB10.

5.5.1 Test Steps

- 1 Referring to the specification sheet for the 3.3 Volt Regulator (IC26, LF33CDT) verify that the Output voltage is 3.3 ± 0.15 VDC at output currents between 0 and 400 mA DC, when provided an input voltage between 4.75 and 5.25 VDC.
- 2 Connect a voltmeter to measure the DC voltage from the Output pin of IC26 to Ground.
- 3 Verify that the voltmeter value is 3.3 ± 0.15 VDC.

5.5.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
1 - Verify that the regulator can provide an output voltage of 3.3 ± 0.15 VDC at output currents from 0 to 400 mA, when provided an input voltage from 4.75 to 5.25 VDC.	3.15 to 3.45 VDC		Pass / Fail
3 - Verify that the voltmeter value is 3.3 ± 0.15 VDC.	3.15 to 3.45 VDC		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.6 5 Volt Supply

Test Number TCHWSCPB6; Referenced Requirement HWSCPB5, HWSCPB6 and HWSCPB7.

5.6.1 Test Steps

- 1 Referring to the specification sheet for the 5 Volt Regulator (IC29, TPS5430): Verify that the IC29 output voltage is 5 ± 0.25 VDC at output currents from 0 to 3 A, when provided an input voltage from 22.8 to 25.2 VDC.
- 2 Measure the voltage across C106 with a voltmeter.
- 3 Verify that the voltmeter value is 5 ± 0.25 VDC.

5.6.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
1 - Verify that the regulator can provide an output voltage of 5 ± 0.25 VDC at output currents from 0 to 3 A, when provided an input voltage from 22.8 to 25.2 VDC.	4.75 to 5.25 VDC		Pass / Fail
3 - Verify that the voltmeter value is 5 ± 0.25 VDC.	4.75 to 5.25 VDC		Pass / Fail

Comments:		
Test Operator Signature/Date		

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5.7 10 Volt Reference

Test Number TCHWSCPB7; Referenced Requirement HWSCPB11, HWSCPB12 and HWSCPB13.

5.7.1 Test Steps

- 1 Referring to the specification sheet for the 10 Volt Reference (IC23, LTS1236ACS8-10): Verify that the IC23 output voltage is 10 ± 0.1 VDC at output currents from 0 to 10 mA, when provided an input voltage from 22.8 to 25.2 VDC.
- 2 Measure the voltage across C85 with a voltmeter.
- 3 Verify that the voltmeter value is 10 ± 0.1 VDC.

5.7.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
1 - Verify that the regulator can provide an output voltage of 10 ± 0.1 VDC at output currents from 0 to 10 mA, when provided an input voltage from 22.8 to 25.2 VDC.	9.9 to 10.1 VDC		Pass / Fail
3 - Verify that the voltmeter value is 10 ± 0.1 VDC.	9.9 to 10.1 VDC		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.8 5 Volt Reference

Test Number TCHWSCPB8; Referenced Requirement HWSCPB14, HWSCPB15 and HWSCPB16.

5.8.1 Test Steps

- 1 Referring to the specification sheet for the 5 Volt Reference Regulator (IC21, LTS1236ACS8-5): Verify that the IC21 output voltage is 5 ± 0.05 VDC at output currents from 0 to 10 mA, when provided an input voltage from 22.8 to 25.2 VDC.
- 2 Measure the voltage across C81 with a voltmeter.
- 3 Verify that the voltmeter value is 5 ± 0.05 VDC.

5.8.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
1 - Verify that the regulator can provide an output voltage of 5 ± 0.05 VDC at output currents from 0 to 10 mA, when provided an input voltage from 22.8 to 25.2 VDC.	4.95 to 5.05 VDC		Pass / Fail
3 - Verify that the voltmeter value is 5 ± 0.05 VDC.	4.95 to 5.05 VDC		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.9 3.3 Volt Monitor

Test Number TCHWSCPB9; Referenced Requirement HWSCPB19 and HWSCPB20.

5.9.1 Test Steps

- 1 Disconnect the cable between the CPU Board and the Power Management Board.
- 2 Connect the positive lead of a programmable DC Power Supply (adjusted to 3.3 VDC) to IC36-3. Connect the negative power supply lead to Ground (J7-24).
- 3 Record the logic level value present on pin P2.5 (IC4-52, +3.3V-FAILURE).
- 4 Verify that a HIGH logic level is present at P2.5 (IC4-52.).
- 5 Observe P2.5 (IC4-52), while slowly decreasing the power supply voltage until pin P2.5 switches to a LOW logic level. Record the power supply voltage at which the signal on P2.5 went LOW.
- 6 Verify that the power supply voltage is greater than or equal to 3 VDC.
- 7 Adjust the programmable power supply to produce a repeating voltage which is at 3.3 VDC for 900 mS, and at 2.8 VDC for 100 mS of each cycle.
- 8 Observe pin P2.5 (IC4-52) with an oscilloscope, and record the pulsewidth of the LOW-going portion.
- 9 Verify that the P2.5 remains at a LOW logic level for at least 140 mS of each cycle.

5.9.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that a HIGH logic level is present at P2.5 (IC4-52.)	HIGH logic level		Pass / Fail
6 - Verify that the power supply voltage is greater than or equal to 3 VDC.	>= 3 VDC		Pass / Fail
9 - Verify that the P2.5 remains at a LOW logic level for at least 140 mS of each cycle.	LOW logic level		Pass / Fail
9 - Verify that the P2.5 remains at a LOW logic level for at least 140 mS of each cycle.	>= 140 mS		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.10 5 Volt Reference Monitor

Test Number TCHWSCPB10; Referenced Requirement HWSCPB17 and HWSCPB18.

5.10.1 Test Steps

- 1 Disconnect the cable between the CPU Board and the Power Management Board.
- 2 Connect the positive lead of a programmable DC Power Supply (set to 5 VDC) to IC24-3. Connect the negative power supply lead to Ground (J7-24). Monitor the power supply voltage with a voltmeter
- 3 Record the logic level value present on pin P2.6 (IC4-53, +5VREF-FAILURE).
- 4 Verify that a HIGH logic level is present at P2.6 (IC4-53).
- 5 Observe P2.6 (IC4-53), while slowly decreasing the power supply voltage until pin P2.6 switches to a LOW logic level. Record the power supply voltage at which the signal on P2.6 went LOW.
- 6 Verify that the power supply voltage is greater than or equal to 4.5 VDC.
- 7 Adjust the programmable power supply to produce a repeating voltage which is at 5 VDC for 900 mS, and at 4 VDC for 100 mS of each cycle.
- 8 Observe pin P2.6 (IC4-53) with an oscilloscope, and record the pulsewidth of the LOW-going portion of the signal.
- 9 Verify that the P2.6 remains at a LOW logic level for at least 140 mS of each cycle.

5.10.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that a HIGH logic level is present at P2.6 (IC4-53).	HIGH logic level		Pass / Fail
6 - Verify that the power supply voltage is greater than or equal to 4.5 VDC.	>= 4.5 VDC		Pass / Fail
9 - Verify that P2.6 remains at a LOW logic level for at least 140 mS of each cycle.	LOW logic level		Pass / Fail
9 - Verify that P2.6 remains at a LOW logic level for at least 140 mS of each cycle.	>= 140 mS		Pass / Fail

Comments:		
Test Operator Signature/Date:	 	

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5.11 10 Volt Reference Monitor

Test Number TCHWSCPB11; Referenced Requirement HWSCPB21 and HWSCPB22.

5.11.1 Test Steps

- 1 Disconnect the cable between the CPU Board and the Power Management Board.
- 2 Connect the positive lead of a 24 VDC power supply to J7-3, and the negative lead to J7-24 to provide power the CPU board.
- 3 Unsolder the "top" end of R66 (the end furthest from the edge of the CPU Board) so that it does not make electrical contact with the CPU Board.
- 4 Connect the positive lead of a programmable DC Power Supply (set to 10 VDC) to the "top" of R66. Connect the negative power supply lead to Ground (J7-24).
- 5 Record the logic level value present on pin P2.7 (IC4-54, +10VREF-FAILURE).
- 6 Verify that a HIGH logic level is present at P2.7 (IC4-54).
- 7 Observe P2.7 (IC4-54), while slowly decreasing the power supply voltage until pin P2.7 switches to a LOW logic level. Record the power supply voltage at which the signal on P2.7 went LOW.
- 8 Verify that the power supply voltage is greater than or equal to 8.9 VDC.
- 9 Adjust the programmable power supply to produce a repeating voltage which is at 10 VDC for 900 mS, and at 8 VDC for 100 mS of each cycle.
- 10 Observe pin P2.7 (IC4-54) with an oscilloscope, and record the pulsewidth of the LOW-going portion of the signal.
- 11 Verify that the P2.7 remains at a LOW logic level for at least 140 mS of each cycle.
- 12 Reattach R66 to the CPU board as it originally was.

5.11.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that a HIGH logic level is present at P2.7 (IC4-54).	HIGH logic level		Pass / Fail
8 - Verify that the power supply voltage is greater than or equal to 8.9 VDC.	>= 8.9 VDC		Pass / Fail
11 - Verify that P2.7 remains at a LOW logic level for at least 140 mS of each cycle.	LOW logic level		Pass / Fail
11 - Verify that P2.7 remains at a LOW logic level for at least 140 mS of each cycle.	>= 140 mS		Pass / Fail

Comments:
Test Operator Signature/Date:

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5.12 Exhalation Valve Interface – PWM

Test Number TCHWSCPB12; Referenced Requirement HWSCPB23, HWSCPB25 and HWSCPB26.

5.12.1 Test Steps

- 1 Generate a 14.975 kHz PWM signal with a pulsewidth of 33.38 uS on microcontroller Port P7.1 (IC4-20) by setting the appropriate registers.
- 2 Measure the frequency of the signal at G-T21 (CD-VALVE), using an oscilloscope.
- 3 Verify that the frequency of the signal is $14.975 \text{ kHz} \pm 10\%$.
- 4 Generate a 14.975 kHz PWM signal with a pulsewidth of approximately 25 nS on pin P7.1 (IC4-20) by setting the appropriate registers.
- 5 Measure the pulsewidth with the oscilloscope.
- 6 Generate a 14.975 kHz PWM signal with a pulsewidth of approximately 50 nS on P7.1 by setting the appropriate registers.
- 7 Measure the pulsewidth with the oscilloscope.
- 8 Verify that the difference between first and second pulsewidth measurement is 25 ± 5 nS.

5.12.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the frequency of the signal is 14.975 kHz ± 10%.	13.4775 to 16.4725		Pass / Fail
5 - Measure the pulsewidth with the oscilloscope.	25 nS		N/A
7 - Measure the pulsewidth with the oscilloscope.	50 nS		N/A
8 - Verify that the difference between first and second pulsewidth measurement is 25 ± 5 nS.	20 to 30 nS		Pass / Fail

Comments:	
Test Operator Signature/Date:	

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5.13 Exhalation Valve Interface - Current

Test Number TCHWSCPB13; Referenced Requirement HWSCPB24, HWSCPB27 and HWSCPB28. 5.13.1 Test Steps

- 1 Unplug the J19 (Exhalation Valve) connector.
- 2 Generate a HIGH logic level signal on P7.1 (IC4-20) by setting the appropriate microcontroller registers.
- 3 Read the digital value of the MES-I-VALVE signal at P5.11 (IC4-40) by setting the appropriate microcontroller registers.
- 4 Verify that the digital value is 0 ± 21 .
- 5 Connect a 750 Ohm resistor, in series with an ammeter, between J19-1 and J19-2.
- 6 Read the digital value of P5.11 (IC4-40) by setting the appropriate registers.
- 7 Verify that the digital value is equal to (Ammeter value * 20460) \pm 21.
- 8 Connect a 1500 Ohm resistor, in series with an ammeter, between J19-1 and J19-2.
- 9 Read the digital value of P5.11 (IC4-40) by setting the appropriate registers.
- 10 Verify that the digital value is equal to (Ammeter value * 20460) ± 21.

5.13.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the digital value is 0 ± 21.	-21 to 21		Pass / Fail
7 - Verify that the digital value is equal to (Ammeter value * 20460) ± 21.	(Av * 20460) ± 21		Pass / Fail
10 - Verify that the digital value is equal to (Ammeter value * 20460) ± 21.	(Av * 20460) ± 21		Pass / Fail

Comments:	 	
Test Operator Signature/Date:	 	

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5.14 Turbine Interface - Speed Control PWM

Test Number TCHWSCPB14; Referenced Requirement HWSCPB29 and HWSCPB30.

5.14.1 Test Steps

- 1 Generate a 9.765 kHz PWM signal with a pulsewidth of 102.4 uS on P7.0 (IC4-19) by setting the appropriate registers.
- 2 Observe the signal at J4-5 (SPEED-SETPOINT) with an oscilloscope:
- 3 Verify that the frequency of the PWM signal is $9.765 \text{ kHz} \pm 10\%$.
- 4 Generate a 9.765 kHz PWM signal with a pulsewidth of approximately 50 nS on pin P7.0 (IC4-19) by setting the appropriate registers.
- 5 Measure the pulsewidth with the oscilloscope.
- 6 Generate a 9.765 kHz PWM signal with a pulsewidth of approximately 75 nS on pin P7.0 (IC4-19) by setting the appropriate registers.
- 7 Measure the pulsewidth with the oscilloscope.
- 8 Verify that the difference between first and second pulsewidth measurement is 25 ± 5 nS.

5.14.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the frequency of the PWM signal is 9.765 kHz ± 10%.	8.7885 to 10.7415 kHz		Pass / Fail
5 - Measure the pulsewidth with the oscilloscope.	50 nS		N/A
7 - Measure the pulsewidth with the oscilloscope.	75 nS		N/A
8 - Verify that the difference between first and second pulsewidth measurement is 25 ± 5 nS.	20 to 30 nS		Pass / Fail

Comments:	
Test Operator Signature/Date:	

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5.15 Turbine Interface - Brake PWM

Test Number TCHWSCPB15; Referenced Requirement HWSCPB31 and HWSCPB32.

5.15.1 Test Steps

- 1 Generate a 15.060 kHz PWM signal with a pulsewidth of 33.2 uS on P2.1 (IC4-48) by setting the appropriate registers.
- 2 Observe the signal at J4-4 (BRAKE/) with the oscilloscope, and measure its frequency.
- 3 Verify that the frequency is $15.060 \text{ kHz} \pm 10\%$.
- 4 Generate a 15.060 kHz PWM signal with a pulsewidth of approximately 400 nS on P2.1 (IC4-48) by setting the appropriate registers.
- 5 Measure pulsewidth with the oscilloscope.
- 6 Generate a 15.060 kHz PWM signal with a pulsewidth of approximately 800 nS on P2.1 (IC4-48) by setting the appropriate registers.
- 7 Measure pulsewidth with the oscilloscope.
- 8 Verify that the difference between first and second pulsewidth measurement is 400 ± 80 nS.

5.15.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the frequency is 15.060 kHz ± 10%.	13.554 to 16.566 kHz		Pass / Fail
5 - Measure the pulsewidth with the oscilloscope.	400 nS		N/A
7 - Measure the pulsewidth with the oscilloscope.	800 nS		N/A
8 - Verify that the difference between first and second pulsewidth measurement is 400 ± 80 nS.	320 to 480 nS		Pass / Fail

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est Operator Signature/Date:

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5.16 Turbine Interface - Speed Measurement

Test Number TCHWSCPB16; Referenced Requirement HWSCPB33.

5.16.1 Test Steps

- 1 Connect a function generator to J4-6 (SPEED-MEASURE) and apply a 0-to-5V 1 kHz square wave signal.
- 2 Download approved "CPU Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 3 Start ventilator in "Setup" mode, then run the Maintenance page.
- 4 Verify that the turbine speed measurement displayed on ventilator is 60,000 RPM ± 1%
- 5 Change function generator frequency to 500 Hz.
- 6 Verify that the turbine speed measurement displayed on ventilator is 30,000 RPM ± 1%
- 7 Change function generator frequency to 16.67 Hz.
- 8 Verify that the turbine speed measurement displayed on ventilator is 1,000 RPM ± 1%

5.16.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the turbine speed measurement displayed on ventilator is 60,000 RPM ± 1%	59,400 to 60,600 RPM		Pass / Fail
6 - Verify that the turbine speed measurement displayed on ventilator is 30,000 RPM ± 1%	29,700 to 30,300 RPM		Pass / Fail
8 - Verify that the turbine speed measurement displayed on ventilator is 1,000 RPM ± 1%	990 to 1,010 RPM		Pass / Fail

comments:
est Operator Signature/Date:

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5.17 Turbine Interface – Enable Signal

Test Number TCHWSCPB17; Referenced Requirement HWSCPB34.

5.17.1 Test Steps

- 1 Generate a LOW logic level at pin P2.3 (IC4-50, ENABLE-TURB) by setting the appropriate registers.
- 2 Verify that a LOW logic level is present on J4-2 (ENABLE).
- 3 Generate a HIGH logic level at pin P2.3 (IC4-50) by setting the appropriate registers.
- 4 Verify that a HIGH logic level is present on J4-2.

5.17.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that a LOW logic level is present on J4-2 (ENABLE).	LOW logic level		Pass / Fail
4 - Verify that a HIGH logic level is present on J4-2.	HIGH logic level		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.18 Turbine Interface – Temperature Measurement

Test Number TCHWSCPB18; Referenced Requirement HWSCPB35.

5.18.1 Test Steps

- 1 Connect a resistance decade box (or use suitable fixed resistors) between J4-10 (TURBINE-TEMP) and J4-9 (0VANA).
- 2 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Mgmt. Board.
- 3 Start ventilator in "Partial Tests" mode, then run the Blower Interface test.
- 4 Adjust resistance to 3020 Ohms.
- 5 Verify that the blower temperature measurement displayed on the ventilator is 60 ± 1 °C.
- 6 Adjust resistance to 2588 Ohms.
- 7 Verify that the blower temperature displayed is 65 ± 1 °C.
- 8 Adjust resistance to 2228 Ohms.
- 9 Verify that the blower temperature displayed is 70 \pm 1 °C.
- 10 Adjust resistance to 1924 Ohms.
- 11 Verify that the blower temperature displayed is 75 \pm 1 °C.
- 12 Adjust resistance to 1668 Ohms.
- 13 Verify that the blower temperature displayed is 80 ± 1 °C.

5.18.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
5 - Verify that the blower temperature measurement displayed on the ventilator is 60 ± 1 °C.	59 to 61 °C		Pass / Fail
7 - Verify that the blower temperature displayed is 65 ± 1 °C.	64 to 66 °C		Pass / Fail
9 - Verify that the blower temperature displayed is 70 ± 1 °C.	69 to 71 °C		Pass / Fail
11 - Verify that the blower temperature displayed is 75 ± 1 °C.	74 to 76 °C		Pass / Fail
13 - Verify that the blower temperature displayed is 80 ± 1 °C.	79 to 81 °C		Pass / Fail

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5.19 Power Supply Communication Interface – Communication speed µC

Test Number TCHWSCPB19; Referenced Requirement HWSCPB36.

5.19.1 Test Steps

- 1 Observe pin J7-BR6 with an oscilloscope, and record the signal.
- 2 Verify that the frequency of the signal is between 1.71Mbit/s and 1.89Mbit/s. Warning: Measure only the frequency include into the burst.

5.19.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
(2) Communication shall have a transfer rate of 1.8Mbit/s +/-5%.	1.71Mbit/s to 1.89Mbit/s		Pass / Fail

Comments:	 	
Test Operator Signature/Date		

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5.20 Power Supply Communication Interface – USB Communication speed (PB560, PB520, Future option)

Test Number TCHWSCPB76; Referenced Requirement HWSCPB117.

5.20.1 Test Steps

- 1 Observe pin J7-BR5 with an oscilloscope, and record the signal.
- 2 Verify that the frequency of the signal is between 1.71Mbit/s and 1.89Mbit/s. Warning: Measure only the frequency include into the burst.

5.20.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
(2) Communication shall have a transfer rate of 1.8Mbit/s +/-5%.	1.71Mbit/s to 1.89Mbit/s		Pass / Fail

Comments:			
Test Operator Signature/Da	ato:		

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5.21 Power Supply Communication Interface – USB Busy Signal (PB560, PB520, Future Option)

Test Number TCHWSCPB77; Referenced Requirement HWSCPB44.

5.21.1 Test Steps

- 1 Generate a LOW logic level on J7-12 (USB-BUSY).
- 2 Verify a LOW logic level at pin P2.10 (IC4-59) by setting the appropriate registers.
- 3 Generate a HIGH logic level on J7-12 (USB-BUSY).
- 4 Verify a HIGH logic level at pin P2.10 (IC4-59) by setting the appropriate registers.

5.21.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify a LOW logic level.	LOW logic level		Pass / Fail
4 - Verify a HIGH logic level.	HIGH logic level		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.22 Power Supply Communication Interface – USB Reset Signal

Test Number TCHWSCPB20; Referenced Requirement HWSCPB43.

5.22.1 Test Steps

- 1 Generate a LOW logic level at pin P3.5 (IC4-70) by setting the appropriate registers.
- 2 Place a voltmeter on J7-11 (RESET-USB)
- 3 Verify that the voltage is 0 ± 0.5 VDC.
- 4 Generate a HIGH logic level at P3.5 by setting the appropriate registers.
- 5 -Verify that the voltage is 5 ± 0.5 VDC.

5.22.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the voltage is 0 ± 0.5 VDC.	-0.5 to 0.5 VDC		Pass / Fail
5 -Verify that the voltage is 5 ± 0.5 VDC.	4.5 to 5.5 VDC		Pass / Fail

Comments:		 	
Test Operator Signature/Dat	e:		

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5.23 Power Supply Communication Interface – Power Indicators

Test Number TCHWSCPB22; Referenced Requirement HWSCPB37, HWSCPB38 and HWSCPB39.

5.23.1 Test Steps

- 1 Use a regulated power supply to apply 0 VDC to J7-15 (LED-PRESENCE-AC).
- 2 Verify that the AC Power LED is OFF.
- 3 Read the logic level of pin P8.0 (IC4-9, AC-PRESENCE).
- 4 Verify that a LOW logic level is present at P8.0 (IC4-9).
- 5 Use a regulated power supply to apply 5 VDC to J7-15.
- 6 Verify that the AC Power LED is ON.
- 7 Read the logic level of pin P8.0 (IC4-9, AC-PRESENCE).
- 8 Verify that a HIGH logic level is present at P8.0 (IC4-9).
- 9 Use a regulated power supply to apply 0 VDC to J7-16 (LED-PRESENCE-DC).
- 10 Verify that the DC Power LED is OFF.
- 11 Use a regulated power supply to apply 5 VDC to J7-16.
- 12 Verify that the DC Power LED is ON.
- 13 Use a regulated power supply to apply 0 VDC to J7-17 (LED-BAT).
- 14 Verify that the Internal Battery LED is OFF.
- 15 Use a regulated power supply to apply 5 VDC to J7-17.
- 16 Verify that the Internal Battery LED is ON.

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5.23.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the AC Power LED is OFF.	LED off		Pass / Fail
4 - Verify that a LOW logic level is present at P8.0 (IC4-9).	LOW logic level		Pass / Fail
6 - Verify that the AC Power LED is ON.	LED on		Pass / Fail
8 - Verify that a HIGH logic level is present at P8.0 (IC4-9).	HIGH logic level		Pass / Fail
10 - Verify that the DC Power LED is OFF.	LED off		Pass / Fail
12 - Verify that the DC Power LED is ON.	LED on		Pass / Fail
14 - Verify that the Internal Battery LED is OFF.	LED off		Pass / Fail
16 - Verify that the Internal Battery LED is ON.	LED on		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.24 Power Supply Communication Interface – Data transfer speed

Test Number TCHWSCPB23; Referenced Requirement HWSCPB40.

5.24.1 Test Steps

- 1 Connect the PB540 to a PC with the USB cable.
- 2 Open "ST10Flasher_BE" software (this software has a communication rate set to 115,200bauds by default). Check "LEGENDAIR US" in the windows "S/N" on the right. Automatically the number "40971K" is written on the box bellow. Complete the S/N by the actual number of the PB540 tested 6 numbers XXXXXX and click on the button "Ecriture S/N". This function will write and read the S/N on the device, and will allow us to test the communication.
- 3 Verify that on the bottom of the main windows of the software, the following phrase is written: "Numero de série 40971Kxxxxxx ecrit avec success".

 That's means that the software read the S/N in the device to ensure it has been written right.

5.24.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
(2) Communication shall be capable of data transfers with a baud rate of 115200.	Verify the phrase "Numero de série 40971Kxxxxxx ecrit avec success » on the PC software		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

5.25 Power Supply Communication Interface - Software Download

Test Number TCHWSCPB24; Referenced Requirement HWSCPB41.

5.25.1 Test Steps

- 1 Use "ST10Flasher" software to download an approved "CPU Test Software" version to the CPU Board at 256000 baud.
- 2 Verify that the "Init Monitor", "Load File", "Erase Flash", and "Program Flash" fields have a status of "OK".

5.25.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the "Init Monitor" field has a status of "OK".	"Init Monitor" OK		Pass / Fail
2 - Verify that the "Load File" field has a status of "OK".	"Load File" OK		Pass / Fail
2 - Verify that the "Erase Flash" field has a status of "OK".	"Erase Flash" OK		Pass / Fail
2 - Verify that the "Program Flash" field has a status of "OK".	"Program Flash" OK		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.26 Power Supply Communication Interface – Bootstrap Mode

Test Number TCHWSCPB25; Referenced Requirement HWSCPB42.

5.26.1 Test Steps

- 1 Turn main power switch OFF.
- 2 Use "ST10Flasher" software to enter bootstrap mode.
- 3 Turn main power switch ON.
- 4 Verify that the "Bootstrap" button changes to "Programming", and the device screen stays cleared.

5.26.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the bootstrap button changes to "Programming".	"Programming"		Pass / Fail
4 - Verify that the device screen stays cleared.	Screen clear		Pass / Fail

Comments:		 	
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5.27 Power Supply Communication Interface – Battery Voltage Monitor

Test Number TCHWSCPB26; Referenced Requirement HWSCPB45.

5.27.1 Test Steps

- 1 Remove the battery from the device.
- 2 Cover the positive battery terminal with tape, and reinstall the battery into the device.
- 3 Hold down the "Inhibit" key while turning the device on to enter Maintenance mode.
- 4 Select "Maintenance", then "Measurement Check", and then "Internal Battery Menu" from the menu screens.
- 5 Use a variable power supply to apply 0 VDC to J7-14 (VBAT).
- 6 Verify that the displayed Battery Voltage value is 0 ± 0.3 VDC.
- 7 Adjust the variable power supply to apply 15 VDC to J7-14 (VBAT).
- 8 Verify that the displayed Battery Voltage value is 15 ± 0.3 VDC.
- 9 Adjust the variable power supply to apply 30 VDC to J7-14 (VBAT).
- 10 Verify that the displayed Battery Voltage value is 30 ± 0.3 VDC.
- 11 Remove the battery, remove tape from positive terminal, and reinstall battery.

5.27.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that the displayed Battery Voltage value is 0 ± 0.3 VDC.	-0.3 to 0.3 VDC		Pass / Fail
8 - Verify that the displayed Battery Voltage value is 15 ± 0.5 VDC.	14.7 to 15.3 VDC		Pass / Fail
10 - Verify that the displayed Battery Voltage value is 30 ± 0.5 VDC.	29.7 to 30.3 VDC		Pass / Fail

Comments:		
Test Operator Signature/Date:		

5.28 Buzzer Board Interface - PWM

Test Number TCHWSCPB27; Referenced Requirement HWSCPB46, HWSCPB47 and HWSCPB48.

5.28.1 Test Steps

- 1 Observe the signal at J18-3 with an oscilloscope.
- 2 Generate a 60 kHz PWM signal with a pulsewidth of 8.33 uS on pin P7.3 (IC4-22, PWM-BUZ) by setting the appropriate registers.
- 3 Verify with the oscilloscope that the modulated carrier frequency is 60 kHz ± 10%.
- 4 Generate an 880 Hz PWM signal with a pulsewidth of 0.57 mS on pin P7.4 (IC4-23) by setting the appropriate registers.
- 5 Verify with the oscilloscope that the modulating signal frequency is 880 Hz \pm 10%.
- 6 Generate a 1000 Hz PWM signal with a pulsewidth of 0.5 mS on pin P7.4 (IC4-23) by setting the appropriate registers.
- 7 Verify with the oscilloscope that the modulating signal frequency is 1000 Hz ± 10%.
- 8 Generate a 60 kHz PWM signal with a pulsewidth of approximately 300 nS on pin P7.3 (IC4-22) by setting the appropriate registers.
- 9 Measure pulsewidth with the oscilloscope.
- 10 Generate a 60 kHz PWM signal with a pulsewidth of approximately 350 nS on pin P7.3 (IC4-22) by setting the appropriate registers.
- 11 Measure pulsewidth with the oscilloscope.
- 12 Verify that the difference between step 9 and step 11 pulsewidth measurements is 50 ± 10 ns.

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5.28.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify with the oscilloscope that the modulated carrier frequency is 60 kHz ± 10%.	54 to 66 kHz		Pass / Fail
5 - Verify with the oscilloscope that the modulating signal frequency is 880 Hz ± 10%.	792 to 968 Hz		Pass / Fail
7 - Verify with the oscilloscope that the modulating signal frequency is 1000 Hz ± 10%.	900 to 1100 Hz		Pass / Fail
9 - Measure pulsewidth with the oscilloscope.	N/A		N/A
11 - Measure pulsewidth with the oscilloscope.	N/A		N/A
12 - Verify that the difference between step 9 and step 11 pulsewidth measurements is 50 ± 10ns.	40 to 60 ns		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.29 Buzzer Board Interface - Logic Levels

Test Number TCHWSCPB28; Referenced Requirement HWSCPB49.

5.29.1 Test Steps

- 1 Use an oscilloscope to capture and measure the voltage levels on J18-4 during startup.
- 2 Verify that the LOW logic level voltage at J18-4 is 0 ± 0.5 VDC.
- 3 Verify that the HIGH logic level voltage at J18-4 is 5 ± 0.5 VDC.

5.29.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the LOW logic level voltage at J18-4 is 0 ± 0.5 VDC.	-0.5 to 0.5 VDC		Pass / Fail
3 - Verify that the HIGH logic level voltage at J18-4 is 5 ± 0.5 VDC.	4.5 to 5.5 VDC		Pass / Fail

Comments:	 	
Test Operator Signature/Date		

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5.30 Buzzer Board Interface - Inhibit Key

Test Number TCHWSCPB29; Referenced Requirement HWSCPB50.

5.30.1 Test Steps

- 1 Connect an oscilloscope to J18-7 (INHIBIT_STOP_INV).
- 2 Start ventilation with the ventilator
- 3 Press the "Inhibit" key.
- 4 Verify that J18-7 goes to a LOW logic level when the "Inhibit" key is pressed.
- 5 Ensure ventilator is in ventilating
- 6 Switch OFF the device.
- 7 Press the "Inhibit" key.
- 8 Verify that J18-7 goes to a LOW logic level when the "Inhibit" key is pressed.

5.30.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that J18-7 goes to a LOW logic level when the "Inhibit" key is pressed.	LOW logic level		Pass / Fail
8 - Verify that J18-7 goes to a LOW logic level when the "Inhibit" key is pressed.	LOW logic level		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.31 Buzzer Board Interface – Voltage Monitor

Test Number TCHWSCPB30; Referenced Requirement HWSCPB51.

5.31.1 Test Steps

- 1 Hold down the "Inhibit" key while turning the device on to enter Maintenance mode.
- 2 Select "Maintenance", then "Measurement Check" from the menus.
- 3 Use a variable power supply to apply 0 VDC to J18-5 (TESTBUZ).
- 4 Verify that the displayed Buzzer voltage is 0 ± 0.1 VDC.
- 5 Adjust the power supply to apply 2.5 VDC to J18-5.
- 6 Verify that the displayed Buzzer voltage is 2.5 ± 0.1 VDC.
- 7 Adjust the power supply to apply 5 VDC to J18-5.
- 8 Verify that the displayed Buzzer voltage is 5 ± 0.1 VDC.

5.31.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the displayed Buzzer voltage is 0 ± 0.1 VDC.	-0.1 to 0.1 VDC		Pass / Fail
6 - Verify that the displayed Buzzer voltage is 2.5 ± 0.1 VDC.	2.4 to 2.6 VDC		Pass / Fail
8 - Verify that the displayed Buzzer voltage is 5 ± 0.1 VDC.	4.9 to 5.1 VDC		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.32 Remote Alarm Interface – N.C. Relay Contacts

Test Number TCHWSCPB31; Referenced Requirement HWSCPB52 and HWSCPB54.

5.32.1 Test Steps

- 1 Generate a LOW logic level on pin P2.14 (IC4-63) by setting the appropriate registers.
- 2 Place a 24 VDC regulated power supply, in series with a 240 Ohm resistor and an ammeter, between J2-1 and J2-2.
- 3 Verify that the measured current is 100 mA \pm 10%.
- 4 Generate a HIGH logic level on pin P2.14 (IC4-63) by setting the appropriate registers.
- 5 Verify that the measured current is 0 A.

5.32.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the measured current is 100 mA ± 10%.	90 mA to 110 mA		Pass / Fail
5 - Verify that the measured current is 0 A.	0 A		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.33 Remote Alarm Interface - N.O. Relay Contacts

Test Number TCHWSCPB32; Referenced Requirement HWSCPB53 and HWSCPB54.

5.33.1 Test Steps

- 1 Generate a LOW logic level on pin P2.14 (IC4-63) by setting the appropriate registers.
- 2 Place a 24 VDC regulated power supply, in series with a 240 Ohm resistor and an ammeter, between J2-1 and J2-3.
- 3 Verify that the measured current is 0 A.
- 4 Generate a HIGH logic level on pin P2.14 (IC4-63) by setting the appropriate registers.
- 5 Verify that the measured current is 100 mA \pm 10%.

5.33.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the measured current is 0 A.	0 A		Pass / Fail
5 - Verify that the measured current is 100 mA ± 10%.	90 mA to 110 mA		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.34 Keyboard Interface – "Down" Key

Test Number TCHWSCPB33; Referenced Requirement HWSCPB55.

5.34.1 Test Steps

- 1 Generate a LOW logic level on pin P3.0 (IC4-65) by setting the appropriate registers.
- 2 Read the logic level on pin P3.3 (IC4-68).
- 3 Verify that a HIGH logic level is present on P3.3 (IC4-68).
- 4 Press the "Down" key.
- 5 Verify that a LOW logic level is present on pin P3.3.

5.34.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that a HIGH logic level is present on P3.3 (IC4-68).	HIGH logic level		Pass / Fail
5 - Verify that a LOW logic level is present on pin P3.3.	LOW logic level		Pass / Fail

Comments:			
Test Operator Signature/Da	e.		

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5.35 Keyboard Interface - "Up" Key

Test Number TCHWSCPB34; Referenced Requirement HWSCPB56.

5.35.1 Test Steps

- 1 Generate a LOW logic level on pin P3.2 (IC4-67) by setting the appropriate registers.
- 2 Read the logic level on pin P3.4 (IC4-69).
- 3 Verify that a HIGH logic level is present on P3.4 (IC4-69).
- 4 Press the "Up" key.
- 5 Verify that a LOW logic level is present on pin P3.4.

5.35.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that a HIGH logic level is present on P3.4 (IC4-69).	HIGH logic level		Pass / Fail
5 - Verify that a LOW logic level is present on pin P3.4.	LOW logic level		Pass / Fail

Comments:		 	
Test Operator Signature/Date	a·		

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5.36 Keyboard Interface – "Ventil" Key

Test Number TCHWSCPB35; Referenced Requirement HWSCPB57.

5.36.1 Test Steps

- 1 Generate a LOW logic level on pin P3.1 (IC4-66) by setting the appropriate registers.
- 2 Read the logic level on pin P3.4 (IC4-69).
- 3 Verify that a HIGH logic level is present on pin P3.4.
- 4 Press the "Ventil" key.
- 5 Verify that a LOW logic level is present on pin P3.4.

5.36.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that a HIGH logic level is present on pin P3.4.	HIGH logic level		Pass / Fail
5 - Verify that a LOW logic level is present on pin P3.4.	LOW logic level		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.37 Keyboard Interface - "Navig" Key

Test Number TCHWSCPB36; Referenced Requirement HWSCPB58.

5.37.1 Test Steps

- 1 Generate a LOW logic level on pin P3.2 (IC4-67) by setting the appropriate registers.
- 2 Read the logic level on pin P3.3 (IC4-68).
- 3 Verify that a HIGH logic level is present on pin P3.3.
- 4 Press the "Navig" key.
- 5 Verify that a LOW logic level is present on pin P3.3.

5.37.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that a HIGH logic level is present on pin P3.3.	HIGH logic level		Pass / Fail
5 - Verify that a LOW logic level is present on pin P3.3.	LOW logic level		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.38 Keyboard Interface - "Valid" Key

Test Number TCHWSCPB37; Referenced Requirement HWSCPB59.

5.38.1 Test Steps

- 1 Generate a LOW logic level on pin P3.1 (IC4-66) by setting the appropriate registers.
- 2 Read the logic level on pin P3.3 (IC4-68).
- 3 Verify that a HIGH logic level is present on pin P3.3.
- 4 Press the "Valid" key.
- 5 Verify that a LOW logic level is present on pin P3.3.

5.38.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that a HIGH logic level is present on pin P3.3.	HIGH logic level		Pass / Fail
5 - Verify that a LOW logic level is present on pin P3.3.	LOW logic level		Pass / Fail

Comments:		 	
Test Operator Signature/Date	a·		

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5.39 Keyboard Interface - "Inhib" Key

Test Number TCHWSCPB38; Referenced Requirement HWSCPB60.

5.39.1 Test Steps

- 1 Read the logic level on pin P3.6 (IC4-73).
- 2 Verify that a HIGH logic level is present on pin P3.6.
- 3 Press the "Inhib Alarm" key.
- 4 Verify that a LOW logic level is present on pin P3.6.

5.39.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that a HIGH logic level is present on pin P3.6.	HIGH logic level		Pass / Fail
4 - Verify that a LOW logic level is present on pin P3.6.	LOW logic level		Pass / Fail

Comments:			
Test Operator Signature/Date:			

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5.40 Keyboard Interface - Battery LED

Test Number TCHWSCPB40; Referenced Requirement HWSCPB39.

5.40.1 Test Steps

- 1 Use a regulated power supply to apply 0 VDC to J7-17 (LED-BAT).
- 2 Verify that the "Battery" LED is OFF.
- 3 Use a regulated power supply to apply 5 VDC to J7-17 (LED-BAT).
- 4 Verify that the "Battery" LED is ON.
- 5 Turn the main power switch to the OFF position.
- 6 Verify that the "Battery" LED is ON.
- 7 Turn the main power switch to the ON position.

5.40.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the "Battery" LED is OFF.	LED is OFF		Pass / Fail
4 - Verify that the "Battery" LED is ON.	LED is ON		Pass / Fail
6 - Verify that the "Battery" LED is ON.	LED is ON		Pass / Fail

Comments:		 	
Test Operator Sign	nature/Date:		

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5.41 Keyboard Interface – DC Presence LED

Test Number TCHWSCPB41; Referenced Requirement HWSCPB38.

5.41.1 Test Steps

- 1 Use a regulated power supply to apply 0 VDC to J7-16 (LED-PRESENCE-DC).
- 2 Verify that the "DC Presence" LED is OFF.
- 3 Use a regulated power supply to apply 5 VDC to J7-16 (LED-PRESENCE-DC).
- 4 Verify that the "DC Presence" LED is ON.
- 5 Turn the main power switch to the OFF position.
- 6 Verify that the "DC Presence" LED is ON.
- 7 Turn the main power switch to the ON position.

5.41.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the "DC Presence" LED is OFF.	LED is OFF		Pass / Fail
4 - Verify that the "DC Presence" LED is ON.	LED is ON		Pass / Fail
6 - Verify that the "DC Presence" LED is ON.	LED is ON		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.42 Keyboard Interface – AC Presence LED

Test Number TCHWSCPB42; Referenced Requirement HWSCPB37.

5.42.1 Test Steps

- 1 Use a regulated power supply to apply 0 VDC to J7-15 (LED-PRESENCE-AC).
- 2 Verify that the "AC Presence" LED is OFF.
- 3 Use a regulated power supply to apply 5 VDC to J7-15 (LED-PRESENCE-AC).
- 4 Verify that the "AC Presence" LED is ON.
- 5 Turn the main power switch to the OFF position.
- 6 Verify that the "AC Presence" LED is ON.
- 7 Turn the main power switch to the ON position.

5.42.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the "AC Presence" LED is OFF.	LED is OFF		Pass / Fail
4 - Verify that the "AC Presence" LED is ON.	LED is ON		Pass / Fail
6 - Verify that the "AC Presence" LED is ON.	LED is ON		Pass / Fail

Comments:		
Test Operator Signature/Date		

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5.43 Keyboard Interface – Other LEDs

Test Number TCHWSCPB43; Referenced Requirement HWSCPB63, HWSCPB64 and HWSCPB65.

5.43.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start the ventilator.
- 3 Verify that the "Ventil" LED lights at startup.
- 4 Verify that the Red Alarm LED lights at startup.
- 5 Verify that the Orange Alarm LED lights at startup.

5.43.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the "Ventil" LED lights at startup.	LED is ON @ startup		Pass / Fail
4 - Verify that the Red Alarm LED lights at startup.	LED is ON @ startup		Pass / Fail
5 - Verify that the Orange Alarm LED lights at startup.	LED is ON @ startup		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.44 Display Interface

Test Number TCHWSCPB44; Referenced Requirement HWSCPB66, HWSCPB67 and HWSCPB68.

5.44.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start the ventilator.
- 3 Verify proper function of Display Interface.

5.44.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify proper function of Display Interface.	Displays Test Menu		Pass / Fail

Comments:		 	
Test Operator Signature/Da	ate.		

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5.45 O₂ Flow Sensor Interface (Future option)

Test Number TCHWSCPB46; Referenced Requirement HWSCPB71.

5.45.1 Test Steps

- 1 Use a regulated power supply to apply 0 VDC between J20-1 and J20-3.
- 2 Read the digital value of pin P5.10 (IC4-39, Q-O2-MEAS) by setting the appropriate registers.
- 3 Verify that the digital value of pin P5.10 is 0 ± 11 .
- 4 Use a regulated power supply to apply 2.5 VDC between J20-1 and J20-3.
- 5 Read the digital value of pin P5.10 by setting the appropriate registers.
- 6 Verify that the digital value of pin P5.10 is 512 ± 11 .
- 7 Use a regulated power supply to apply 5 VDC between J20-1 and J20-3.
- 8 Read the digital value of pin P5.10 by setting the appropriate registers.
- 9 Verify that the digital value of pin P5.10 is 1023 ± 11 .

5.45.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the digital value of pin P5.10 is 0 ± 11.	-11 to 11		Pass / Fail
6 - Verify that the digital value of pin P5.10 is 512 ± 11.	501 to 523		Pass / Fail
9 - Verify that the digital value of pin P5.10 is 1023 ± 11.	1012 to 1034		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.46 O₂ Flow Sensor Interface (Future option)

Test Number TCHWSCPB47; Referenced Requirement HWSCPB72.

5.46.1 Test Steps

- 1 Connect an air compressor in series with an air flow regulator, a flow meter, and the O2 flow sensor in the device.
- 2 Read the digital value of pin P5.10 (IC4-39, Q-O2-MEAS) by setting the appropriate registers.
- 3 Regulate air flow in order to measure values with the calibrated flow meter from 0 to 50 sccm, in accordance with the table. Compare the flow readings of the device to those indicated by the calibrated flow meter.
- 4 Verify that the device readings agree with those measured by the flow meter, to within the tolerances specified in the table below:

Flow,	Tolerance %		
sccm	10lerance %		
50	5		
40	5		
20	8		
5	10		
0	N/A		

5.46.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - 50 ± 5% sccm	47.5 to 52.5 sccm		Pass / Fail
4 - 40 ± 5% sccm	38 to 42 sccm		Pass / Fail
4 - 20 ± 8% sccm	18.4 to 21.6 sccm		Pass / Fail
4 - 5 ± 10% sccm	4.5 to 5.5 sccm		Pass / Fail
4 - 0 ± N/A% sccm	0 sccm		Pass / Fail

Comments:
Fest Operator Signature/Date:

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5.47 O₂ Valve Interface – PWM and Current Drive

Test Number TCHWSCPB48; Referenced Requirement HWSCPB73, HWSCPB74, HWSCPB75 and HWSCPB76.

5.47.1 Test Steps

- 1 Generate a 14.975 kHz PWM signal with a pulsewidth of 33.38 uS on pin P7.2 by setting the appropriate registers.
- 2 Connect an oscilloscope to pin 7.2, and measure the frequency.
- 3 Verify that the frequency is 14.975 kHz \pm 10%.
- 4 Generate a 14.975 kHz PWM signal with a pulsewidth of approximately 50 nS on pin P7.2 by setting the appropriate registers.
- 5 Measure pulsewidth with the oscilloscope.
- 6 Generate a 14.975 kHz PWM signal with a pulsewidth of approximately 75 nS on pin P7.2 by setting the appropriate registers.
- 7 Measure pulsewidth with the oscilloscope.
- 8 Verify that the difference between first and second pulsewidth measurement is 25 ± 5 nS.
- 9 Unplug J21 (the O2 Valve connector).
- 10 Generate a HIGH logic level signal on P7.2 (IC4-21, CD-O2) by setting the appropriate microcontroller registers.
- 11 Connect a 110 Ohm, 5 Watt resistor, in series with an ammeter, between J21-1 and J21-2.
- 12 Verify that the current through the resistor ≥ 190 mA.

5.47.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the frequency is 14.975 kHz ± 10%.	13.4775 to 16.4725 kHz		Pass / Fail
5 - Measure pulsewidth with the oscilloscope.	N/A		N/A
7 - Measure pulsewidth with the oscilloscope.	N/A		N/A
8 - Verify that the difference between first and second pulsewidth measurement is 25 ± 5 nS.	20 to 30 nS		Pass / Fail
12 - Verify that the current through the resistor is ≥ 190 mA.	≥ 190 mA		Pass / Fail

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5.48 Security Back-up Buzzer Interface – Secondary Alarm

Test Number TCHWSCPB49; Referenced Requirement HWSCPB77.

5.48.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Run "Buzzer Test", and skip to the "Security Buzzer" test..
- 3 Run the "Security Buzzer Test".
- 4 Verify that the secondary audible alarm sounds when the device resets.
- 5 Verify that the secondary audible alarm's Sound Pressure Level is at least 80 dB (A-weighted) at a distance of 10 cm.

5.48.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the secondary audible alarm sounds when the device resets.	Alarm sounds		Pass / Fail
5 - Verify that the secondary audible alarm's Sound Pressure Level is at least 80 dB (A-weighted) at a distance of 10 cm.	80 dB		N/A

Comments:		
Test Operator Signature/Date:		

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5.49 Security Back-up Buzzer Interface – Primary Alarm

Test Number TCHWSCPB50; Referenced Requirement HWSCPB78.

5.49.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start ventilator in "Partial Tests" mode.
- 3 Run the "Buzzer Test".
- 4 Verify that the primary audible alarm sounds when the device resets.
- 5 Verify that the primary audible alarm's Sound Pressure Level is at least 90 dB (A-weighted) at a distance of 10 cm.

5.49.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the primary audible alarm sounds when the device resets.	Alarm sounds		Pass / Fail
5 - Verify that the primary audible alarm's Sound Pressure Level is at least 90 dB (A-weighted) at a distance of 10 cm.	90 dB		N/A

Comments:		
Test Operator Signature/Date:		

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5.50 RAM Memory

Test Number TCHWSCPB51; Referenced Requirement HWSCPB79.

5.50.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start the ventilator in "Partial Tests" mode.
- 3 Run "RAM Memory" test.
- 4 Verify that the result of the RAM Memory test is "OK".

5.50.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the result of the RAM Memory test is "OK".	ОК		Pass / Fail

Comments:			
Test Operator Signature/Date):		

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5.51 Event Memory

Test Number TCHWSCPB52; Referenced Requirement HWSCPB80.

5.51.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start the ventilator in "Partial Tests" mode.
- 3 Run "Event Memory" test.
- 4 Verify that the result of the Events Memory test is "OK".

5.51.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the result of the Events Memory test is "OK".	ОК		Pass / Fail

Comments:			
Test Operator Signature/Date):		

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5.52 Event Memory – Erase/Program Cycles

Test Number TCHWSCPB53; Referenced Requirement HWSCPB81.

5.52.1 Test Steps

- 1 Refer to the specifications for the non-volatile memory.
- 2 By inspection of the specifications, verify that the memory will support at least 1,00,000 erase/program cycles.

5.52.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - By inspection verify that the memory will support at least 1,000,000 erase and program cycles.	>= 1,00,000		Pass / Fail

Comments:		 	
Test Operator Signature/Date	·		

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5.53 Ventilation Settings Memory

Test Number TCHWSCPB54; Referenced Requirement HWSCPB82.

5.53.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start the ventilator in "Partial Tests" mode.
- 3 Run "Parameters EEPROM Memory" test.
- 4 Verify that the result of the test is "OK".

5.53.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the result of the Parameters EEPROM Memory test is "OK".	OK		Pass / Fail

Comments:	
Fest Operator Signature/Date:	

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5.54 Ventilation Settings Memory – Erase/Program Cycles

Test Number TCHWSCPB55; Referenced Requirement HWSCPB83.

5.54.1 Test Steps

- 1 Refer to the specifications for the non-volatile memory.
- 2 By inspection of the specifications, verify that the memory will support at least 1,000,000 erase/program cycles.

5.54.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - By inspection verify that the memory will support at least 1,000,000 erase and program cycles.	>= 1,000,000		Pass / Fail

Comments:		 	
Test Operator Signature/Da	ite:		

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Test Protocol, CPU Board, PB540, PB560

10027876

5.55 Monitoring Memory

Test Number TCHWSCPB56; Referenced Requirement HWSCPB84.

5.55.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start the ventilator in "Partial Tests" mode.
- 3 Run "Monitoring Memory" test.
- 4 Verify that the result of the Monitoring Memory test is "OK".

5.55.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the result of the Monitoring Memory test is "OK".	ОК		Pass / Fail

Comments:			
Test Operator Signature/Date):		

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Test Protocol, CPU Board, PB540, PB560

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5.56 Monitoring Memory – Erase/Program Cycles

Test Number TCHWSCPB57; Referenced Requirement HWSCPB85.

5.56.1 Test Steps

- 1 Refer to the specifications for the non-volatile memory.
- 2 By inspection of the specifications, verify that the memory will support at least 100,000 erase/program cycles.

5.56.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - By inspection verify that the memory will support at least 100,000 erase and program cycles.	>= 100,000		Pass / Fail

Comments:		 	
Test Operator Signature/Date	·		

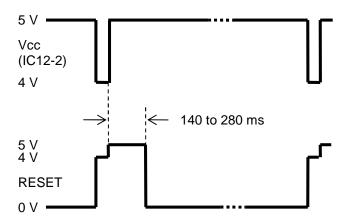
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5.57 Watchdog - Power Supervisor

Test Number TCHWSCPB58; Referenced Requirements HWSCPB89, HWSCPB90, HWSCPB91, and HWSCPB92.

5.57.1 Test Steps

- 1 Turn off the unit and disconnect it from AC power.
- 2 Disconnect one end of the cable between the CPU Board and the Power Management Board.
- 3 Connect a variable, programmable power supply to the input of IC26 (the pin closest to the long edge of the CPU board) and Ground, to substitute for the +5V supply voltage.
- 4 Connect oscilloscope channel 1 to T3-Drain (RESET). The Drain lead is on the side of T3 that has only one lead.
- 5 Slowly reduce the power supply voltage until the RESET signal on oscilloscope channel 1 goes to a HIGH logic level, and record the voltage at which this occurs.
- 6 Verify that the voltage reading is between 4.5 and 4.75 VDC.
- 7 Slowly increase the power supply voltage until the RESET signal on oscilloscope channel 1 goes LOW again, and record the voltage at which this occurs.
- 8 Verify that the voltage reading in step 7 is at least 0.01 VDC higher than the reading from step 6.
- 9 Adjust the power supply to produce a repeating voltage waveform that is at 5 VDC for 4.9 seconds. and at 4 VDC for 0.1 seconds.
- 10 Connect oscilloscope channel 1 to the power supply output, and connect channel 2 to T3-Drain (RESET).
- 11 Verify that the pulsewidth of the 5 V portion of the RESET signal on scope channel 2 has a pulsewidth of at least 140 ms, and no more than 280 ms, as shown in the diagram below.

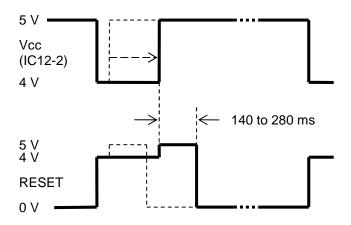


12 - While observing the oscilloscope, increase the length of time that the power supply voltage is at 4 V to 400 ms.

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13 - Verify that RESET continues to stay high for 140 to 280 ms after Vcc returns to normal, as shown in the diagram below.



14 - Turn off the power supply and disconnect it from IC12-2, and reconnect the cable between the CPU Board and Power Management Board.

5.57.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that the voltage at which RESET goes high is between 4.5 and 4.75 VDC.	4.5 to 4.75 VDC		Pass / Fail
8 - Verify that the voltmeter reading is at least 0.01 VDC higher than the previous reading.	>= 0.01 VDC higher than previous reading		Pass / Fail
11 - Verify that the 5 V portion of the RESET pulse is between 140 and 280 ms in duration.	140 to 280 ms		Pass / Fail
13 - Verify that RESET goes low again between 140 and 280 ms after Vcc returns to normal.	140 to 280 ms		Pass / Fail

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5.58 Watchdog – Timeout interval

Test Number TCHWSCPB59; Referenced Requirement HWSCPB86 and HWSCPB88.

5.58.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Connect oscilloscope channel 1 to IC12-6 (WDOG), and channel 2 to T3-Drain (RESET).
- 3 Start ventilator in "Partial Tests" mode.
- 4 Run "Watchdog Function" test, and capture the signals displayed on the oscilloscope.
- 5 Verify that the delay between the last level transition of oscilloscope channel 1 (WDOG), and oscilloscope channel 2 (RESET) going high is between 1.0 and 2.25 seconds.
- 6 Verify that the pulsewidth of oscilloscope ch. 2 (RESET) is between 140 and 280 mS.

5.58.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
5 - Verify that the delay between the last level transition of oscilloscope ch. 1 (WDOG), and oscilloscope ch. 2 (RESET) going high is between 1.0 and 2.25 seconds.	1.0 to 2.25 seconds		Pass / Fail
6 - Verify that the pulsewidth of oscilloscope ch. 2 (RESET) is between 140 and 280 mS.	140 to 280 mS		Pass / Fail

Comments:
Test Operator Signature/Date:

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5.59 Watchdog – PFI Trap Function

Test Number TCHWSCPB73; Referenced Requirement HWSCPB93.

5.59.1 Test Steps

- 1 Disconnect the cable from the Power Management Board to the CPU board at the Power Management Board end.
- 2 Connect the positive lead of a variable power supply, adjusted to 24 VDC, to J7-3 (+24VUTIL). Connect the negative power supply lead J7-24 (Ground). Monitor the power supply's voltage with its built-in meter, or with an external voltmeter.
- 3 Wait until the unit proceeds to the ventilation status screen. Disregard any error messages that may appear in the status area.
- 4 Reduce the power supply voltage to 14 VDC. Do not allow the voltage to go below 14 VDC during this adjustment.
- 5 While observing the unit's LCD display, slowly decrease the power supply voltage until the LCD display goes black.
- 6 Verify that the power supply voltage is between 12.19 VDC and 13.83 VDC.
- 7 Allow the unit to reset, to silence the power failure alarm.

5.59.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that the power supply voltage measures from 12.19 to 13.83 VDC.	12.19 to 13.83 VDC		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.60 Clock - Functional Test

Test Number TCHWSCPB60; Referenced Requirement HWSCPB94.

5.60.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start ventilator in "Partial Tests" mode.
- 3 Run the "Real Time Clock" test.
- 4 Verify that the result of the Real Time Clock test is "OK".

5.60.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
4 - Verify that the result of the Real Time Clock function test is "OK".	ОК		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.61 Clock - Battery Timekeeping Mode

Test Number TCHWSCPB61; Referenced Requirement HWSCPB95.

5.61.1 Test Steps

- 1 Refer to the specifications for the button cell battery and DS1305E clock.
- 2 By inspection verify that the button cell's capacity is sufficient to allow the DS1305E clock chip to operate in battery timekeeping mode for a minimum of three years, even if the device is not supplied with power.

5.61.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - By datasheet inspection, verify that the button cell's capacity is sufficient to allow the DS1305E clock chip to operate in battery timekeeping mode for a minimum of three years, even if the device is not supplied with power.	> 3 years		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.62 Device Model ID

Test Number TCHWSCPB62; Referenced Requirement HWSCPB96.

5.62.1 Test Steps

- 1 Read the logic level of pin P8.2 (IC4-11).
- 2 Verify that a HIGH logic level is present on pin P8.2.
- 3 Read the logic level of pin P8.3 (IC4-12).
- 4 Verify that a HIGH logic level is present on pin P8.3.

5.62.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail / N/A
2 - Verify that a HIGH logic level is present on pin P8.2.	HIGH		Pass / Fail
4 - Verify that a HIGH logic level is present on pin P8.3.	HIGH		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.63 Inspiratory Flow Measurement

Test Number TCHWSCPB63; Referenced Requirement HWSCPB97 and HWSCPB98.

5.63.1 Test Steps

- 1 Connect an air compressor in series with an air flow regulator, a flow meter and the inhalation flow sensor.
- 2 Read the digital value of the signal on pin P5.1 (IC4-28, QI-MEAS) by setting the appropriate registers.
- 3 Regulate air flow in order to measure values with the flow meter from 0 to 1000 sccm, in increments of 100 sccm.
- 4 Verify that the digital value matches following table values:

Flow sccm	Nominal Voltage V (from sensor data-sheet)	Tolerance ± V DC	Tolerance %. Not Calibrated. Sensor only.	Result
1000	5.00	0.5000	10.00%	
900	4.90	0.5050	10.31%	
800	4.80	0.5100	10.63%	
700	4.66	0.5130	11.01%	
600	4.42	0.5110	11.56%	
500	4.18	0.5090	12.18%	
400	3.82	0.5010	13.12%	
300	3.41	0.4605	13.50%	
200	2.96	0.4180	14.12%	
100	2.30	0.3550	15.43%	
0	1.00	0.2500	25.00%	

Flow I/min	Tolerance % Calibrated. With whole supply chain measure.	Result
145	5.00%	
135	5.00%	
90	5.00%	
60	5.00%	
37	5.00%	
12	8.00%	
5	10.00%	
0	N/A	

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5.63.2 Results

Description Of Expected Result	Expected Result	Pass / Fail
Verify inspiratory air flow sensor's accuracy.	Per above tables.	Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.64 Exhalation Flow Measurement

Test Number TCHWSCPB64; Referenced Requirement HWSCPB99 and HWSCPB100.

5.64.1 Test Steps

- 1 Connect an air compressor in series with an air flow regulator, a flow meter and the exhalation flow sensor.
- 2 Read the digital value of the signal on pin P5.7 (IC4-28, QI-MEAS) by setting the appropriate registers.
- 3 Regulate air flow in order to measure values with the flow meter from 0 to 1000 sccm, in increments of 100 sccm.
- 4 Verify that the digital value matches following table values:

Flow sccm	Nominal Voltage V (from sensor data-sheet)	Tolerance ± V DC	Tolerance %. Not Calibrated. Sensor only.	Result
1000	5.00	0.5000	10.00%	
900	4.90	0.5050	10.31%	
800	4.80	0.5100	10.63%	
700	4.66	0.5130	11.01%	
600	4.42	0.5110	11.56%	
500	4.18	0.5090	12.18%	
400	3.82	0.5010	13.12%	
300	3.41	0.4605	13.50%	
200	2.96	0.4180	14.12%	
100	2.30	0.3550	15.43%	
0	1.00	0.2500	25.00%	

Flow I/min	Tolerance % Calibrated. With whole supply chain measure.	Result
145	5.00%	
135	5.00%	
90	5.00%	
60	5.00%	
37	5.00%	
12	8.00%	
5	10.00%	
0	N/A	

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5.64.2 Results

Description Of Expected Result	Expected Result	Pass / Fail
Verify expiratory air flow sensor's accuracy.	Per above tables.	Pass / Fail

Comments:		 	
Test Operator Signature/F	late.		

5.65 Proximal Pressure Measurement

Test Number TCHWSCPB65; Referenced Requirement HWSCPB101.

5.65.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start ventilator in "Partial Tests" mode.
- 3 Run "Pressure Sensor" test.
- 4 Use a pressure meter to measure the pressure applied to the proximal pressure sensor.
- 5 Apply a -10 mbar constant proximal pressure (suction) to the proximal pressure sensor with a syringe.
- 6 Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.
- 7 Apply a 50 mbar constant proximal pressure with a syringe.
- 8 Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.
- 9 Apply a 100 mbar constant proximal pressure with a syringe.
- 10 Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.

5.65.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.	-11.5 to -8.5 mbar		Pass / Fail
8 - Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.	48.5 to 51.5 mbar		Pass / Fail
10 - Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.	98.5 to 101.5 mbar		Pass / Fail

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5.66 Internal Pressure Measurement

Test Number TCHWSCPB66; Referenced Requirement HWSCPB102.

5.66.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start ventilator in "Partial Tests" mode.
- 3 Run "Pressure Sensor" test.
- 4 Use a pressure meter to measure the pressure applied to the inspiratory pressure sensor.
- 5 Apply a -10 mbar constant internal pressure (suction) to the inspiratory pressure sensor with a syringe.
- 6 Verify that the measured internal pressure matches that displayed by the device, to within 1.5 mbar
- 7 Apply a 50 mbar constant internal pressure with a syringe.
- 8 Verify that the measured internal pressure matches that displayed by the device, to within 1.5 mbar.
- 9 Apply a 100 mbar constant internal pressure with a syringe.
- 10 Verify that the measured internal pressure matches that displayed by the device, to within 1.5 mbar.

5.66.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that the measured pressure matches the internal pressure displayed by the device, to within 1.5 mbar.	-11.5 to -8.5 mbar		Pass / Fail
8 - Verify that the measured pressure matches the internal pressure displayed by the device, to within 1.5 mbar.	48.5 to 51.5 mbar		Pass / Fail
10 - Verify that the measured pressure matches the internal pressure displayed by the device, to within 1.5 mbar.	98.5 to 101.5 mbar		Pass / Fail

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5.67 Expiratory Valve Pressure Measurement

Test Number TCHWSCPB67; Referenced Requirement HWSCPB103.

5.67.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start ventilator in "Partial Tests" mode.
- 3 Run "Pressure Sensor" test.
- 4 Use a pressure meter to measure the pressure applied to the expiratory valve pressure sensor.
- 5 Apply a -10 mbar constant internal pressure (suction) to the expiratory valve pressure sensor with a syringe.
- 6 Verify that the measured internal pressure matches that displayed by the device, to within 1.5 mbar
- 7 Apply a 50 mbar constant pressure with a syringe.
- 8 Verify that the measured internal pressure matches that displayed by the device, to within 1.5 mbar.
- 9 Apply a 100 mbar constant pressure with a syringe.
- 10 Verify that the measured expiratory valve pressure matches that displayed by the device, to within 1.5 mbar.

5.67.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.	-11.5 to -8.5 mbar		Pass / Fail
8 - Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.	48.5 to 51.5 mbar		Pass / Fail
10 - Verify that the measured pressure matches the proximal pressure displayed by the device, to within 1.5 mbar.	98.5 to 101.5 mbar		Pass / Fail

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5.68 Atmospheric Pressure Measurement

Test Number TCHWSCPB68; Referenced Requirement HWSCPB104.

5.68.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start ventilator in "Partial Tests" mode.
- 3 Run "Pressure Sensor" test.
- 4 Use an absolute pressure meter to measure absolute pressure.
- 5 Verify that the measured absolute pressure matches device displayed ambient pressure value within 15 mbar.
- 6 Apply a negative pressure on absolute pressure sensor with a syringe until the device displays an ambient pressure of 600 mbar.
- 7 Use an absolute pressure meter to measure this pressure.
- 8 Verify that the measured pressure is equal to 600 ± 15 mbar.
- 9 Apply a positive pressure on absolute pressure sensor with a syringe until the device displays an ambient pressure of 1100 mbar.
- 10 Use an absolute pressure meter to measure this pressure.
- 11 Verify that the measured pressure is equal to 1100 ± 15 mbar.

5.68.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
5 - Verify that the measured absolute pressure matches device displayed ambient pressure value within 10 mbar.	(Ambient – 15) to (Ambient + 15) mbar		Pass / Fail
8 - Verify that the measured pressure is equal to 600 ± 15 mbar.	585 to 615 mbar		Pass / Fail
11 - Verify that the measured pressure is equal to 1100 ± 15 mbar.	1085 to 1115 mbar		Pass / Fail

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5.69 O₂ Pressure Measurement (Future option)

Test Number TCHWSCPB69; Referenced Requirement HWSCPB105.

5.69.1 Test Steps

- 1 Download approved "CPU Test Software" version to the CPU Board, and approved "Soft carte alim pour test CPU" software version to the Power Supply Management board.
- 2 Start ventilator in "Partial Tests" mode.
- 3 Run "Pressure Sensor" test.
- 4 Use a pressure meter to measure O2 pressure.
- 5 Apply a 0 bar constant O2 pressure with a syringe.
- 6 Verify that the measured O2 pressure matches device displayed O2 pressure value to within 150 mbar.
- 7 Apply a 3.5 bar constant O2 pressure with a syringe.
- 8 Verify that the measured O2 pressure matches device displayed O2 pressure value to within 150 mbar.
- 9 Apply a 6.5 bar constant O2 pressure with a syringe.
- 10 Verify that the measured O2 pressure matches device displayed O2 pressure value to within 150 mbar.

5.69.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
6 - Verify that the device-displayed O2 pressure matches the measured O2 pressure value to within 150 mbar.	(Measured – 150) to (Measured + 150) mbar		Pass / Fail
8 - Verify that the measured O2 pressure matches device displayed O2 pressure value to within 150 mbar.	3.35 to 3.65 mbar		Pass / Fail
10 - Verify that the measured O2 pressure matches device displayed O2 pressure value to within 150 mbar.	6.35 to 6.65 mbar		Pass / Fail

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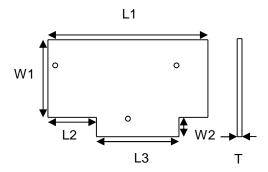
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5.70 PCB - Size

Test Number TCHWSCPB70; Referenced Requirement HWSCPB106, HWSCPB107, HWSCPB108, HWSCPB109, HWSCPB110 and HWSCPB111.

5.70.1 Test Steps

1 - Measure the dimensions of the CPU Board's PCB, as shown in the following diagram:



- 2 Verify that the length (L1) is 190 \pm 1 mm.
- 3 Verify that the length (L2) is 58.5 ± 1 mm.
- 4 Verify that the length (L3) is 96.5 ± 1 mm.
- 5 Verify that the width (W1) is 100 ± 1 mm.
- 6 Verify that the width (W2) is 20 ± 1 mm.
- 7 Verify that the thickness (T) is 1.6 ± 0.5 mm.

5.70.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the length (L1) is 190 ± 1 mm	189 to 191 mm		Pass / Fail
3 - Verify that the length (L2) is 58.5 ± 1 mm.	57.5 to 59.5 mm		Pass / Fail
4 - Verify that the length (L3) is 96.5 ± 1 mm.	95.5 to 97.5 mm		Pass / Fail
5 - Verify that the width (W1) is 100 ± 1 mm.	99 to 101 mm		Pass / Fail
6 - Verify that the width (W2) is 20 ± 1 mm.	19 to 21 mm		Pass / Fail
7 - Verify that the thickness (T) is 1.6 ± 0.5 mm.	1.1 to 2.1 mm		Pass / Fail

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5.71 PCB - Mounting

Test Number TCHWSCPB71; Referenced Requirement HWSCPB112.

5.71.1 Test Steps

- 1 Measure the diameter of the three PCB mounting holes, shown in the PCB Size test case.
- 2 Verify that the holes are 3.5 ± 0.2 mm in diameter.

5.71.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the first hole is 3.5 mm in diameter.	3.3 to 3.7 mm		Pass / Fail
2 - Verify that the second hole is 3.5 mm in diameter.	3.3 to 3.7 mm		Pass / Fail
2 - Verify that the third hole is 3.5 mm in diameter.	3.3 to 3.7 mm		Pass / Fail

Comments:	 	
Test Operator Signature/Date:		

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5.72 PCB - Labeling

Test Number TCHWSCPB72; Referenced Requirement HWSCPB114.

5.72.1 Test Steps

- 1 Inspect the markings on the PCB.
- 2 Verify that the PCB is labeled with its Name, Part Number, and Revision, and that the markings are human-readable.

5.72.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
2 - Verify that the PCB is labeled with its Name, and that the markings are human-readable.	Name		Pass / Fail
2 - Verify that the PCB is labeled with its Part Number, and that the markings are human-readable.	Part Number		Pass / Fail
2 - Verify that the PCB is labeled with its Revision, and that the markings are human-readable.	Revision		Pass / Fail

Comments:		
Test Operator Signature/Date:		

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5.73 Printed Circuit Board Fabrication Standards

CPU Card fabrication documentation set (in Agile):

Test Number TCHWSCPB73; Referenced Requirement HWSCPB113.

Verify that the CPU Card is specified to be fabricated according to the following standards and exceptions:

- IPC-A-610D Class III: 2005, Acceptability for Electronic Assemblies.
- Any exceptions to these standards are listed on the fabrication drawings.

5.73.1 Test Steps

5.73.2 Test Results

Part Number:

1 - Verify that specification or statement exists in the CPU Card's fabrication documentation set indicating that it must comply with IPC-610D Class III: 2005 and that exceptions, if any, to this standard are stated. Attach a copy of the document page(s), with the location highlighted of the specification(s) or statement(s) found providing evidence that this requirement has been met.

Revision

escription of Expected Result	Expected Result	Actual Result	Pass / Fail
) CPU Card Assembly drawing	PCB Fab Dwg includes		
ates PCB meets IPC-610D	statement that it meets		5 /= "
lass III: 2005 and exceptions, if	IPC-610D Class III: 2005		Pass / Fail
ny, are noted.	and exceptions, if any,		
	are noted		
Attach copies of pages, with c	orresponding statements hig	ghlighted, where the	e above results
, , , ,	orresponding statements hig	ghlighted, where the	e above results
, , , ,	orresponding statements hig	ghlighted, where the	e above results
, , , ,	orresponding statements hig	ghlighted, where the	e above results

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5.74 FiO2 Measurement (PB560, Future option)

Test Number TCHWSCPB74; Referenced Requirement HWSCPB69.

5.74.1 Test Steps

- 1 Do a short-circuit between J11-1 and J11-2 to apply 0 VDC.
- 2 Read the digital value of pin P5.5 (IC4-32, FiO2-MEAS) by setting the appropriate registers.
- 3 Verify that the digital value of pin P5.5 is 0 ± 10 .
- 4 Use a regulated power supply to apply 33mVDC between J11-1 and J11-2.
- 5 Read the digital value of pin P5.5 by setting the appropriate registers.
- 6 Verify that the digital value of pin P5.5 is 500 ± 10 .
- 7 Use a regulated power supply to apply 66mVDC between J11-1 and J11-2.
- 8 Read the digital value of pin P5.5 by setting the appropriate registers.
- 9 Verify that the digital value of pin P5.5 is 1000 ± 10 .

5.74.2 Results

Description Of Expected Result	Expected Result	Actual Result	Pass / Fail
3 - Verify that the digital value of pin P5.5 is 0 ± 10.	-10 to 10		Pass / Fail
6 - Verify that the digital value of pin P5.5 is 500 ± 10.	490 to 510		Pass / Fail
9 - Verify that the digital value of pin P5.5 is 1000 ± 10.	990 to 1010		Pass / Fail

Comments:		
Test Operator Signature/Date:	 	

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TEST SUMMARY

Test Cases	Requirements	Pass / Fail
TCHWSCPB1	HWSCPB1	Pass / Fail
TCHWSCPB2	HWSCPB2	Pass / Fail
TCHWSCPB3	HWSCPB3	Pass / Fail
TCHWSCPB4	HWSCPB4	Pass / Fail
TCHWSCPB5	HWSCPB8, HWSCPB9, HWSCPB10	Pass / Fail
TCHWSCPB6	HWSCPB5, HWSCPB6, HWSCPB7	Pass / Fail
TCHWSCPB7	HWSCPB11, HWSCPB12, HWSCPB13	Pass / Fail
TCHWSCPB8	HWSCPB14, HWSCPB15, HWSCPB16	Pass / Fail
TCHWSCPB9	HWSCPB19, HWSCPB20	Pass / Fail
TCHWSCPB10	HWSCPB17, HWSCPB18	Pass / Fail
TCHWSCPB11	HWSCPB21, HWSCPB22	Pass / Fail
TCHWSCPB12	HWSCPB23, HWSCPB25, HWSCPB26	Pass / Fail
TCHWSCPB13	HWSCPB24, HWSCPB27, HWSCPB28	Pass / Fail
TCHWSCPB14	HWSCPB29, HWSCPB30	Pass / Fail
TCHWSCPB15	HWSCPB31, HWSCPB32	Pass / Fail
TCHWSCPB16	HWSCPB33	Pass / Fail
TCHWSCPB17	HWSCPB34	Pass / Fail
TCHWSCPB18	HWSCPB35	Pass / Fail
TCHWSCPB19	HWSCPB36	Pass / Fail
TCHWSCPB20	HWSCPB43	Pass / Fail
TCHWSCPB22	HWSCPB37, HWSCPB38, HWSCPB39	Pass / Fail
TCHWSCPB23	HHWSCPB40	Pass / Fail
TCHWSCPB24	HWSCPB41	Pass / Fail
TCHWSCPB25	HWSCPB42	Pass / Fail
TCHWSCPB26	HWSCPB45	Pass / Fail
TCHWSCPB27	HWSCPB46, HWSCPB47, HWSCPB48	Pass / Fail
TCHWSCPB28	HWSCPB49	Pass / Fail
TCHWSCPB29	HWSCPB50	Pass / Fail
TCHWSCPB30	HWSCPB51	Pass / Fail
TCHWSCPB31	HWSCPB52, HWSCPB54	Pass / Fail
TCHWSCPB32	HWSCPB53, HWSCPB54	Pass / Fail
TCHWSCPB33	HWSCPB55	Pass / Fail
TCHWSCPB34	HWSCPB56	Pass / Fail
TCHWSCPB35	HWSCPB57	Pass / Fail
TCHWSCPB36	HWSCPB58	Pass / Fail
TCHWSCPB37	HWSCPB59	Pass / Fail
TCHWSCPB38	HWSCPB60	Pass / Fail
TCHWSCPB40	HWSCPB39	Pass / Fail
TCHWSCPB41	HWSCPB38	Pass / Fail
TCHWSCPB42	HWSCPB37	Pass / Fail
TCHWSCPB44	HWSCPB63, HWSCPB64, HWSCPB65	Pass / Fail
TCHWSCPB44	HWSCPB66, HWSCPB67, HWSCPB68	Pass / Fail
TCHWSCPB46	HWSCPB71	Pass / Fail
TCHWSCPB47	HWSCPB72	Pass / Fail
TCHWSCPB48	HWSCPB73, HWSCPB74, HWSCPB75, HWSCPB76	Pass / Fail
TCHWSCPB49	HWSCPB77	Pass / Fail
TCHWSCPB50	HWSCPB78	Pass / Fail
TCHWSCPB51	HWSCPB79	Pass / Fail
TCHWSCPB52	HWSCPB80	Pass / Fail

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TCHWSCPB53	HWSCPB81	Pass / Fail
TCHWSCPB54	HWSCPB82	Pass / Fail
TCHWSCPB55	HWSCPB83	Pass / Fail
TCHWSCPB56	HWSCPB84	Pass / Fail
TCHWSCPB57	HWSCPB85	Pass / Fail
TCHWSCPB58	HWSCPB89, HWSCPB90, HWSCPB91, HWSCPB92	Pass / Fail
TCHWSCPB59	HWSCPB86, HWSCPB88	Pass / Fail
TCHWSCPB73	HWSCPB93	Pass / Fail
TCHWSCPB60	HWSCPB94	Pass / Fail
TCHWSCPB61	HWSCPB95	Pass / Fail
TCHWSCPB62	HWSCPB96	Pass / Fail
TCHWSCPB63	HWSCPB97, HWSCPB98	Pass / Fail
TCHWSCPB64	HWSCPB99, HWSCPB100	Pass / Fail
TCHWSCPB65	HWSCPB101	Pass / Fail
TCHWSCPB66	HWSCPB102	Pass / Fail
TCHWSCPB67	HWSCPB103	Pass / Fail
TCHWSCPB68	HWSCPB104	Pass / Fail
TCHWSCPB69	HWSCPB105	Pass / Fail
TCHWSCPB70	HWSCPB106, HWSCPB107, HWSCPB108, HWSCPB109, HWSCPB110, HWSCPB111	Pass / Fail
TCHWSCPB71	HWSCPB112	Pass / Fail
TCHWSCPB72	HWSCPB114	Pass / Fail
TCHWSCPB73	HWSCPB93, HWSCPB113	Pass / Fail
TCHWSCPB74	HWSCPB69	Pass / Fail
TCHWSCPB76	HWSCPB117	Pass / Fail
TCHWSCPB77	HWSCPB44	Pass / Fail

Comments:
Test Operator Signature/Date:
Test Operator Printed Name:
De la Facilita de Oliverto de Data
Review Engineer Signature/Date:
Review Engineer Printed Name:

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