Manufacturing Test Specification
CPU PCB
PB540/PB560

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Revision History

Revision	Change Order	Author	Approva by	Approval Date	Summary of Change
00	ECO-R163871	[redacted]	See Agile	See Agile	Initial Draft
A	ECO-R167338	[redacted]	See Agile	See Agile	Initial Release
B	ECO-R170566	[redacted]	See Agile	See Agile	Add ReqPro Tags
C	ECO-R181354	[redacted]	See Agile	See Agile	Add new PCB P/N 3845800 in Section 1 and references to PB560

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1. SCOPE

This specification defines the functional test requirements for the PB540/PB560 CPU PCBA, P/N 3821300/3845800

2. REFERENCE DOCUMENTS

The manufacturing test specification is developed with reference to the appropriate issue of the following documents at the time of this document preparation.

[1] CPU Board Hardware Requirements Specification (HRS) P/N 10024980

[2] PB540 CPU PCB, Schematic P/N 4096600E03.000

[3] CPU SRS, P/N 10025034

3.DEFINITIONS

AC	-	Alternating Current
CPU	-	Central Processing Unit
DC	-	Direct Current
FET	-	Field Effect Transistor
GND	-	Electrical Ground
IC	-	Integrated Circuit
ICSP	-	In Circuit Serial Programmer
I/O	-	Input/Output
MB	-	Megabyte (1 MB = 2^20 = 1048576 bytes)
LED	-	Light Emitting Diode
NVRAM	-	Non Volatile Random Access Memory
PCB	-	Printed Circuit Board
SPI	-	Serial Peripheral Interface
RAM	-	Random Access Memory
RTC	-	Real Time Clock
LCD	-	Liquid Crystal Display
UART	-	Universal Asynchronous Receiver Transmitter
UUT	-	Unit Under Test
rpm	-	Revolutions per minute
0xn	-	Hex number format

4. BOARD TEST

4.1 DC Voltage Measurements

+24VDC is supplied to the CPU board from the Power Management PCB and the following voltages/references are produced on the CPU PCB. Measure each voltage as follows:

4.1.1 +5VDC Supply [HRS[1], HWSCPB6]

Measure +5VDC at the output of the 5V regulator supply. Check that the voltage is +5V ± 0.25V.

4.1.2 +3.3VDC Supply [HRS[1], HWSCPB9]

Measure +3.3VDC at the output of the 3.3V regulator supply. Check that the voltage is +3.3V ± 0.15V

4.1.3 +5V Reference [HRS[1], HWSCPB15]

Measure +5VDC Reference at the output of the +5V reference circuit . Check that the voltage is +5V ± 0.05V

4.1.4 +10V Reference [HRS[1], HWSCPB12]

Measure +10VDC Reference at the output of the +10V reference circuit. Check that the voltage is +10V ± 0.1V

4.2 LCD Contrast Adjustment [SRS[3], SFSYSTHMI8]

The LCD Contrast Adjustment test is to check that the adjustment of the LCD contrast has a sufficient range of contrast available.

4.3 Keypad Interface

Keypad Buttons [HRS[1], HWSCPB55, 56, 57, 59, 60]:

The Keypad Interface test will check the Ventilate '+' , '-', Accept(√), and Alarm Inhibit keypad buttons individually for switch closure by pressing each one as directed by the test and check for the switch closure. The test will indicate a failure if an incorrect keypad button is pressed.

Keypad Leds [HRS[1], HWSCPB63, 64, 65]:

The test will turn ON/OFF the Red and Orange Alarm Leds and the Ventilate Led individually so that each led can be verified to be ON or OFF.

4.4 RAM Memory [HRS[1], HWSCPB79]

The CPU Board RAM memory space 0x200000-0x27FFFF is to be tested by writing in 0xAAAA (16 bit) data values throughout the address locations, and then reading back to verify the data read matches the data written. The test is repeated with 0x5555 (16 bit), 0xAA (8 bit) and 0x55 (8 bit) data values. The test will indicate any verification failures.

4.5 Real Time Clock [HRS[1], HWSCPB94]

The test will check that the Real Time Clock is operating correctly. The RTC will be initialized, set to a defined time/date setting and set to run. A separate reference clock will be set to the same hour, minutes and seconds value as the RTC under test. The RTC under test and the reference clock will be set to run for a short period of time. The RTC under test will then be compared to the reference clock. If the two clocks differ by more than 1 second, or 1 minute or 1 hour then the test will fail

4.6 EEPROM Memory [HRS[1], HWSCPB82]

The 32K bit SPI EEPROM test will write and read data to the 32 bytes in each of the 128 pages of memory. The test will first initialize the memory by writing 0xFF to the memory locations. The test will then write a specific address value to the 32 bytes in each of the 128 pages, then read back and verify the data read matches the written test value. The test will finish by initializing the memory by writing 0xFF to all the memory locations.

4.7 NAND Flash Memory [HRS[1], HWSCPB84]

The NAND Flash is used to store monitoring data. Due to the very large memory capacity of the NAND Flash, the Flash shall be checked by reading the flash identification information stored at the first 4 bytes starting at address 0x500000. The first byte location is the flash manufacturer ID and shall be read as one of the IDs below otherwise the test fails. The second byte location contains the ID for the memory characteristics and shall be read as on of the Characteristic IDs shown otherwise the test fails.

NAND Flash Information Table			
Manuf ID	**Manufacturer**	**Characteristic ID**	**Characteristics**
0x20	ST	0xF1	1Gb, 3V, 8 bits
0xEC	Samsung	0xDA	2Gb, 3V, 8 bits
0x2C	Micron	0xDC	4Gb, 3V, 8 bits
		0xD3	8Gb, 3V, 8 bits

4.8 Event Flash Memory [HRS[1], HWSCPB80]

The 4 Mbit (512K X 8) Event Flash has the address range from 0x100000 to 0x17FFFF and shall be first checked by reading the manufacturer ID to see if it matches one of the recognized manufacturers (See Event Flash Information Table below) .

The flash device is to be erased and verified that all locations are erased. The test will then write the 16 bit value of the address as the data value to each memory location. The data values are to be read back and checked to match the data value written. The test will indicate any verification failures.

Event Flash Information Table	
Manuf ID	**Manufacturer**
0x2223	AM29F400BT AMD MEMORY
0x22AB	AM29F400BB AMD MEMORY
0x00D6	M29F400BB ST MEMORY

4.9 Buzzers

The CPU PCB ST10 uController drives two independent buzzer circuits: the Buzzer PCB and the Security Buzzer on the CPU PCB.

1. [HRS[1], HWSCPB49, 51]: The test will check the operation of the Buzzer PCB interface by driving the INV_STOP signal HIGH to turn ON the Buzzer PCB and check the A/D value of the TESTBUZ feedback voltage to be greater than 300. The test will drive the INV_STOP signal LOW to turn OFF the Buzzer PCB and check the A/D value of the TESTBUZ feedback voltage to be less than 300. Note: 300 corresponds to 1.46V.
2. [HRS[1], HWSCPB48, 51]: The test will check the operation of the Buzzer PCB interface by driving the PWM3 signal PWM-BUZ and check the A/D value of the TESTBUZ feedback voltage to be greater than 300. The test will turn OFF the PWM3 signal PWM-BUZ to turn OFF the Buzzer PCB and check the A/D value of the TESTBUZ feedback voltage to be less than 300. Note: 300 correspond to 1.46V.
3. [HRS[1], HWSCPB77]: The test will check the operation of the Security Buzzer on the CPU PCB by driving SEC-BUZ HIGH to turn ON the Buzzer PCB and verify that the Security Buzzer is ON. The test will drive SEC-BUZ LOW to turn OFF the Buzzer PCB and verify that the Security Buzzer is OFF.

4.10 O2 Valve [HRS[1], HWSCPB73]

The test will check the Oxygen (O2) Valve command signal (02-VALVE) level at J21 in the OFF and ON states. The O2 Valve is ON when the 02-VALVE signal is LOW.

4.11 Exhalation Valve Control [HRS[1], HWSCPB23]

The test will check the operation of the CPU PCB valve (V2) used to control the air flow for the operation of the exhalation valve in the patient circuit. The test will measure the V2 valve current in the uC A/D converted analog value for the valve in the ON and OFF state. When the valve is ON, the A/D value is to be > 500, and when the valve is OFF the A/D value is to be < 500. The test passes if the two measurements are within these limits. Note: 500 correspond to 2.44V.

4.12 Flow Sensors [HRS[1], HWSCPB97, 99]

The test will check the Inspiratory and Expiratory flow sensors at zero flow. The flow sensors expected output at zero flow is 1V ±0.1V and the ST10 uController A/D converted measurement shall measure greater than 184 and less than 225. (Note: 0 Lpm = CAN 215 for inspiratory flow sensor and 0 Lpm = CAN 210 for the expiratory flow sensor.) The test will indicate an error if the measurement is not within these limits.

4.13 Pressure Sensors [HRS[1], HWSCPB102, 103, 101, 104]

The CPU Board uses the following four pressure sensors for operation: Internal (Patient), Exhalation Valve, Proximal, and Barometric pressure. The test will read, process and display the pressure measurements for these sensors at zero (null) pressure. The test will indicate an error if the measurement is not within these limits.

1. Internal (Patient) Pressure Sensor : Test the A/D processed sensor value to be between 152-201. O cmH2O = CAN 175
2. (Exhalation) Valve Pressure Sensor : Test the A/D processed sensor value to be between 152-201. O cmH2O = CAN 175
3. Proximal Pressure Sensor : Test the A/D processed sensor value to be between 152-201. O cmH2O = CAN 175
4. Barometric Pressure Sensor : Test the A/D processed sensor value to be between 640-820mBar.

4.14 FIO2 Sensor Input [HRS[1], HWSCPB69]

The FIO2 input is to be tested by applying a voltage of 13.16mV (Acceptable applied voltage range is 12.49mv-13.83mV) at J11.2. This voltage will simulate a 21% ± 1% FIO2 measurement. The test software will display the converted A/D value which shall measure between 188 (20%) and 209 (22%). The test will indicate an error if the measurement is not within these limits.

4.15 Power Supply Interface [HRS[1], HWSCPB36, 117]

Communication between the CPU PCB and the Power Management PCB is provided by 2 SPI channels. SPI 0 connects to the PIC Microcontroller and SPI 1 connects to the USB Host Controller on the Power Management PCB. Each test will verify the operation of the SPI channel by the successful transfer of data.

4.16 Alarm Repeater [HRS[1], HWSCPB52, 53]

The Alarm Repeater or External Alarm relay shall be tested in the open and close states by testing the relay contact for continuity. The external alarm UART shall be tested by sending and receiving data on the J2 TX/RX RAP Alarm pins. The test shall verify that the UART data received back is correct.

4.17 Turbine Interface [HRS[1], HWSCPB33, 34, 35]

The turbine interface test shall check the ability of the CPU board to set the turbine speed, measure the turbine speed, and set the turbine brake and enable signals.

The turbine speed will be checked with the turbine enabled and then disabled. With the turbine is enabled, the brake is OFF and the PWM signal set to 2500, the speed shall be checked to be greater than or equal to 15,000 RPM, With the turbine disabled, the speed shall be checked to be less than or equal to 15,000 RPM.

The turbine speed will be checked with the PWM 0 signal set to 4096, toggling the brake ON and OFF and the speed shall be less than or equal to 5000 RPM.

The turbine temperature will be checked to be between 20-30º C.

4.18 Watchdog Timer [HRS[1], HWSCPB86]

The watchdog timer is part of the Microprocessor Supervisor IC. The watchdog input (WDI) must change state within 1.6 seconds or else a reset pulse is sent to the ST10 uController. The watchdog timer test will verify the operation of the watchdog timer by preventing the toggling of the watchdog input (WDI) and check that the board resets. If the board does not reset, the test fails.

4.19 Board ID [HRS[1], HWSCPB96]

The CPU PCB uses hardwired jumpers to set the board configuration (Legendair M2, S2, or XL2). When the PCB boots up the board type configured is displayed briefly.