Program for verification

Instruction	Bin Code	COE	Addr	Type	Comment
lw r1, $20(r0)	100011_00000_00001_0000000000010100	8c010014	0	6	r1=1
lw r2,$21(r0)	100011_00000_00010_0000000000010101	8c020015	1	6	r2=4
add r3,r1,r2	000000_00001_00010_00011_00000_100000	00221820	2	1	r3=5 stall, forwarding
sub r4,r1,r3	000000_00001_00011_00100_00000_100010	00232022	3	2	r4=0xffff_fffc forwarding
sllv r6,r1,r4	000000_00001_00100_00110_00000_000100	00243004	4	f	r6=0xffff_fff8
srlv r7,r1,r4	000000_00001_00100_00111_00000_000110	00243806	5	f	r7=0x7fff_fffe(logical)
srav r8,r1,r4	000000_00001_00100_01000_00000_000111	00244007	6	f	r8=0xffff_fffe(arithmetic)
sll r9,r4,16	000000_00000_00100_01001_10000_000000	00044C00	7	c	r9=0xfffc_0000
srl r10,r4,16	000000_00000_00100_01010_10000_000010	00045402	8	d	r10=0x0000_ffff(logical)
sra r11,r4,16	000000_00000_00100_01011_10000_000011	00045C03	9	e	r11=0xffff_ffff(arithmetic)
beq r8,r11,-6	000100_01000_01011_1111111111111010	110BFFFA	a	8	not taken
add r12,r2,r7	000000_00010_00111_01100_00000_100000	00476020	b	1	r12=0x8000_0002 overflow
addu r13,r2,r7	000000_00010_00111_01101_00000_100001	00476821	c	f	r13=0x8000_0002 no overflow
sub r14,r7,r8	000000_00111_01000_01110_00000_100010	00E87022	d	2	r14=0x8000_0000 overflow
subu r15,r7,r8	000000_00111_01000_01111_00000_100011	00E87823	e	f	r15=0x8000_0000 no overflow
beq r14,r15,2	000100_01110_01111_0000000000000010	11CF0002	f	8	taken
addi r31,r31,1	001000_11111_11111_0000000000000001	23FF0001	10	f	r31=1 (branch slot)
add r31,r1,r2	000000_00001_00010_11111_00000_100000	0022F820	11	1	pass the instruction
sw r7,$22(r0)	101011_00000_00111_0000000000010110	AC070016	12	7	
and r5,r3,r4	000000_00011_00100_00101_00000_100100	00642824	13	3	r5=4
xor r6,r3,r4	000000_00011_00100_00110_00000_100110	00643026	14	f	r6=0xffff_fff9
or r7,r3,r4	000000_00011_00100_00111_00000_100101	00643825	15	4	r7=0xffff_fffd
nor r8,r3,r4	000000_00011_00100_01000_00000_100111	00644027	16	5	r8=2
slt r9,r11,r1	000000_01011_00001_01001_00000_101010	0161482A	17	b	r9= 1 (ffff_ffff<1)
sltu r10,r1,r11	000000_00001_01011_01010_00000_101011	002B502B	18	f	r10=1(1<ffff_ffff)
lw r8, $22(r0)	100011_00000_01000_0000000000010110	8C080016	19	6	r8=0x7fff_fffe
addi r9,r8,2	001000_01000_01001_0000000000000010	21090002	1a	f	r9=0x8000_0000 overflow stall
addiu r10,r8,2	001001_01000_01010_0000000000000010	250A0002	1b	f	r10=0x8000_0000 no overflow
andi r11,r8,3	001100_01000_01011_0000000000000011	310B0003	1c	f	r11=2
ori r12,r8,3	001101_01000_01100_0000000000000011	350C0003	1d	f	r12=0x7fff_ffff
xori r13,r8,3	001110_01000_01101_0000000000000011	390D0003	1e	f	r13=0x7fff_fffd

slti r14,r11,ffff	001010_01011_01110_1111111111111111	296EFFFF	1f	f	r14=0(r11=2>-1)
sltiu r15,r11, ffff	001011_01011_01111_1111111111111111	2D6FFFFF	20	f	r15=1(2<0x0000_ffff)
lui r14, 3	001111_00000_01110_0000000000000011	3C0E0003	21	f	r14=0x0003_0000
bne r14,r15,2	000101_01110_01111_0000000000000010	15CF0002	22	f	taken
addi r31,r31,1	001000_11111_11111_0000000000000001	23FF0001	23	f	r31=2 (branch slot)
jr r31	000000_11111_00000_00000_00000_001000	03E00008	24	f	pass the instruction no jump
j L1	000010_00000000000000000000101001	08000029	25	9	jump to L1
addi r1,r1,1	001000_00001_00001_0000000000000001	20210001	26	f	pass the instruction(stall)
L2: jr r31	000000_11111_00000_00000_00000_001000	03E00008	27	f	jump to PC(L1)+"4"
addi r2,r2,-1	001000_00010_00010_1111111111111111	2042FFFF	28	f	pass the instruction(stall)
L1: jal L2	000011_00000000000000000000100111	0C000027	29	f	jump to L2 r31=PC+4 → 2a forwarding
beq r1,r31,-6	000100_00001_11111_1111111111111010	103FFFFA	2a	8	not taken
addi r31,r31,1	001000_11111_11111_0000000000000001	23FF0001	2b	f	r31=2b
beq r2,r31,-6	000100_00010_11111_1111111111111010	105FFFFA	2c	8	not taken