Ports

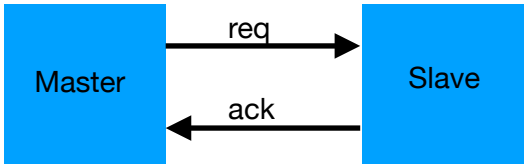
Master

Input: clk
Input: reset_n
Input: ack
Output: req

Slave

Input: clk
Input: reset_n
Input: req
Output: ack

Block Diagram



Master Requirements

1. The master de-asserts the req output while idle.
2. The master asserts the req output to initiate a slave operation.
3. The master keeps the req output asserted until the ack input is asserted.
4. The master de-asserts the req output after the ack input is asserted.
5. The master waits for the ack input to be de-asserted before returning to idle and issuing a new request.

Slave Requirements

1. The slave de-asserts the ack output while idle.
2. The slave remains idle while the req input is de-asserted.
3. The slave performs an operation when the req input is asserted.
4. The slave asserts the ack output once the operation is completed.
5. The slave keeps the ack output asserted until the req input is de-asserted.
6. The slave waits until the req input is de-asserted before returning to idle.

Example Timing