Corrigendum: Coding-Aware Rate Splitting for Distributed Coded Edge Learning

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In the version of this article initially published, there was an error in equation (14). Specifically, the equation (14) should be

$$T_n^u = \max_{\mathcal{V}_i : n \in \mathcal{V}_i} \frac{\alpha |\mathcal{D}_{\mathcal{V}_i}|}{k R_{\mathcal{V}_i}}. \tag{1}$$

Based on this rectification, the figures of simulation results presented in Sec. V should be
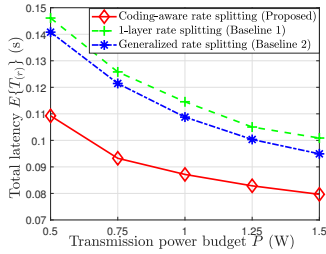

Fig. 1. Latency versus (vs.) transmission power budget P under balanced RS code.
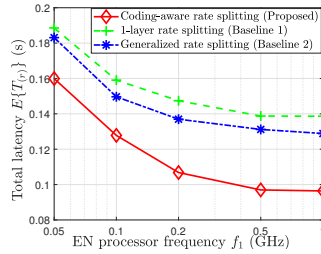

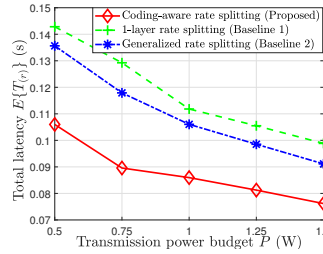Fig. 2. Latency vs. EN processor frequency f_1 under balanced RS code.

Fig. 3. Latency vs. transmission power budget P under heterogeneous code.
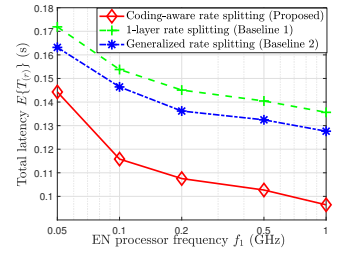

Fig. 4. Latency vs. EN processor frequency f_1 under heterogeneous code.

Accordingly, in the third paragraph in the Sec. V, when transmission power budget $P = 0.5$ (W), the latency of the proposed scheme should be 0.109 (s). Similarly, in the fourth paragraph in the Sec. V, when $f_1 = 0.2$ (GHz), the latency of the proposed scheme should be 0.107 (s).