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Daegu, Korea

H. Yun

H. Yun

Heuijee

Heuijee Yun

English Native
Korean Native

Heuijee Yun

Ph.D student

Experience and Awards

Teaching

C Programming Practice (ELEC420) **2023 F**

Kyungpook National University

Project

ARM MPU Design **Mar 2023 - Dec 2023**

Kyungpook National University

- ARM cortex M0 internal core RTL design
- RTL Synthesis, PnR backend process

SNN-based CIM MPW **Aug 2023 - Nov 2023**

Kyungpook National University

- SNN neuron, circuit pspice production
- RRAM circuit fabrication

Awards

KNU Ph.D Fellow Scholarship Award (10,000,000 Won) **2024**

Kyungpook National University

Education

Integrated Ph.D. Student in Electrical and Electronic engineering **MAR 2022 -**

Kyungpook National University

Research on image-based autonomous driving neural network algorithm processing for lightweight embedded boards

Research on process simplification from the RTL stage to the backend, in addition to deep learning-based accelerator design

BSc. in Electronic engineering **MAR 2018 - FEB 2022**

Kyungpook National University

Four years of studying and taking courses in microprocessors, computer architecture

Continued research of autonomous driving as an undergraduate research student

Publications

H.Yun, D. Park. **High-Speed Energy-Efficient Model based Dynamic Pruning using Pattern-based Alignment for Convolutional Spiking Neural Network Hardware Accelerators** *IEMEK Journal of Embedded Systems and Applications (2024)*

H.Yun, D. Park. **Low-Power Lane Detection Unit based on Sliding-based Parallel Segment Detection Accelerator for Lightweighted Automotive Microcontrollers** *ACCESS (2024)*

H.Yun, D. Park. **Efficient Object Detection based on Masking Semantic Segmentation Region for Lightweight Embedded Processors** *SENSORS (2022)*

H.Yun, D. Park. **Efficient Object Recognition by Masking Semantic Pixel Difference Region of Vision Snapshot for Lightweight Embedded Systems** *Journal of the Korea Institute of Information and Communication Engineering (2022)*

H.Yun, D. Park. **Virtualization of Self-Driving Algorithms by Interoperating Embedded Controllers on Game Engine for Digital Twining Autonomous Vehicle** *Electronics (2021)*

Conferences

H.Yun, D. Park. **Deep Learning based Human Detection using Thermal-RGB Data Fusion for Safe Automotive Guided-Driving** *PerVehicle 2024*

H.Yun, D. Park. **Parallel Processing of 3D Object Recognition by Fusion of 2D Images and LiDAR for Autonomous Driving** *ICEIC 2024*

J.Kwon, H.Yun, D. Park. **Dynamic MAC Unit Pruning Techniques in Runtime RTL Simulation for Area-Accuracy Efficient Implementation of Neural Network Accelerator** *MWSCAS 2023*

H.Yun, D. Park. **Low-Power Parallel Lane Detection Unit for Lightweight Automotive Processors** *IEEE COOLChips 2023*

H.Yun, D. Park. **FPGA Realization of Lane Detection Unit using Sliding-based Parallel Segment Detection for Buffer Memory Reduction** *IEEE ICCE 2023*

H.Yun, D. Park. **Mitigating Overflow of Object Detection Tasks Based on Masking Semantic Difference Region of Vision Snapshot for High Efficiency** *2022 IEEE International Conference on Artificial Intelligence in Information and Communication (ICAIIC)*

H.Yun, D. Park. **Yolo-based Realtime Object Detection using Interleaved Redirection of Time-Multiplxed Streamline of Vision Snapshot for Lightweighted Embedded Processors** *2021 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*

H.Yun, D. Park. **Simulation of Self-driving System by implementing Digital Twin with GTA5** *ICEIC 2021*

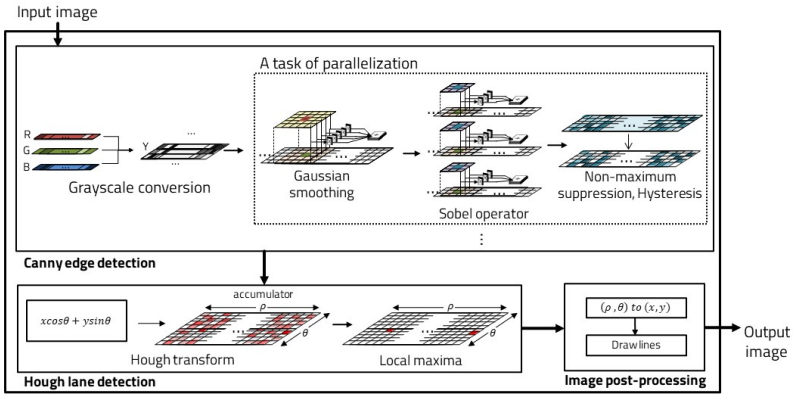
Field of Reasearch Interest

SW

Autonomous driving neural network application using image processing

Deep learning image parallel processing for autonomous driving with python

Image-based deep learning for multiple ADAS functions in parallel



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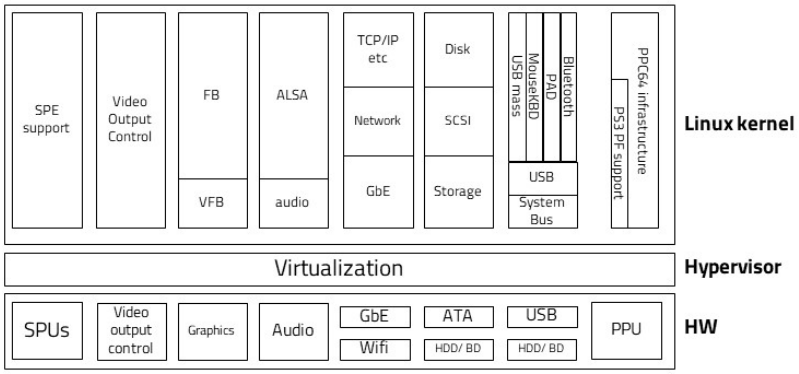
OS

Custom OS with Hypervisor structure for ligthweighted board

Designing Hypervisor for lightweighted board



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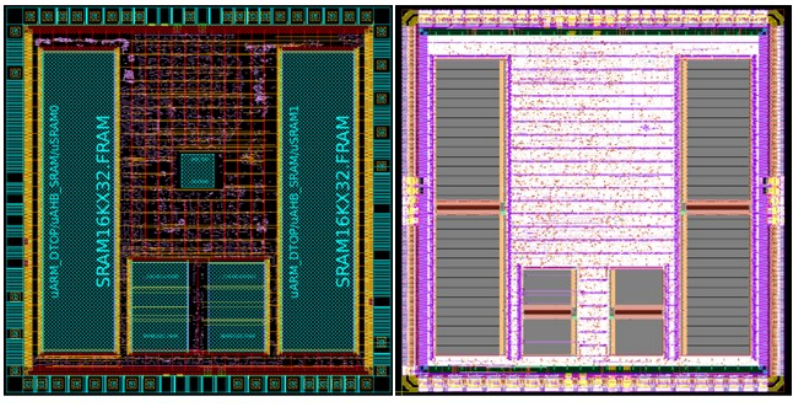
HW

Parallel compute accelerator hardware for NN

Core design and ISA generation using verilog

Back-end DRC/LVS validation of the design and post sim



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Skills

Software AI

ADAS programming

Implement ADAS required for autonomous driving using Python and C
Implement and test ADAS functions using motors and cameras on an embedded board
Build multiple simulation environments using Unity and Matlab

Deep Learning optimization

Implementation of deep learning model structure and learning method
Use and implement a detection model that receives images as input

Operation System and System SW

Custom OS and Hypervisor

x86-based custom OS and hypervisor implementation
ARM-based custom OS and hypervisor implementation, applied to STM32 board and raspberry pi

Deep Learning compiler

Runtime optimization tuning operator for deep learning
For limited resourcese in embedded hardware, hardware aware scheduling and real-location is performed

Hardware

RTL design

Design the core part of ARM based chip

Synthesis

RTL designed parts are synthesized through the design compiler

Placement and Route

Pnr the chip using ICC and ICC2

Post Simulation

Testing the pnr results and whether they are in accordance with the RTL design and intent.

Software

- Verilog
- VHDL
- C / C++
- Python (Jupyter)
- Matlab
- LaTeX