

## EDUCATION

### Kyungpook National University

*Ph.D. in Electrical and Electronic engineering*

Daegu, South Korea

2022 - 2028 (*expected*)

- Advisor: Prof. Daejin Park
- Research area: Event-based low-power AI edge learning

### Kyungpook National University

*BSc. in Electronic engineering*

Daegu, South Korea

2018 - 2022

- GPA: 0.00/4.00, Rank: 64/64.

## PUBLICATIONS

1. **H.Yun**, D. Park. High-Speed Energy-Efficient Model based Dynamic Pruning using Pattern-based Alignment for Convolutional Spiking Neural Network Hardware Accelerators. *IEMEK Journal of Embedded Systems and Applications*, 2024.
2. **H.Yun**, D. Park. Low-Power Lane Detection Unit based on Sliding-based Parallel Segment Detection Accelerator for Lightweighted Automotive Microcontrollers. *ACCESS* (2024)
3. **H.Yun**, D. Park. Efficient Object Detection based on Masking Semantic Segmentation Region for Lightweight Embedded Processors. *SENSORS* (2022)
4. **H.Yun**, D. Park. Efficient Object Recognition by Masking Semantic Pixel Difference Region of Vision Snapshot for Lightweight Embedded Systems. *Journal of the Korea Institute of Information and Communication Engineering*, 2022.
5. **H.Yun**, D. Park. Virtualization of Self-Driving Algorithms by Interoperating Embedded Controllers on Game Engine for Digital Twinning Autonomous Vehicle. *Electronics*, 2021.

## CONFERENCES

1. **H.Yun**, D. Park. Deep Learning based Human Detection using Thermal-RGB Data Fusion for Safe Automotive Guided-Driving. *PerVehicle 2024*
2. **H.Yun**, D. Park. Parallel Processing of 3D Object Recognition by Fusion of 2D Images and LiDAR for Autonomous Driving. *ICEIC 2024*
3. J.Kwon, **H.Yun**, D. Park. Dynamic MAC Unit Pruning Techniques in Runtime RTL Simulation for Area-Accuracy Efficient Implementation of Neural Network Accelerator. *MWSCAS 2023*
4. **H.Yun**, D. Park. Low-Power Parallel Lane Detection Unit for Lightweight Automotive Processors. *IEEE COOLChips 2023*
5. **H.Yun**, D. Park. FPGA Realization of Lane Detection Unit using Sliding-based Parallel Segment Detection for Buffer Memory Reduction. *IEEE ICCE 2023*
6. **H.Yun**, D. Park. Mitigating Overflow of Object Detection Tasks Based on Masking Semantic Difference Region of Vision Snapshot for High Efficiency. *2022 IEEE International Conference on Artificial Intelligence in Information and Communication (ICAIIIC)*
7. **H.Yun**, D. Park. Yolo-based Realtime Object Detection using Interleaved Redirection of Time-Multiplexed Streamline of Vision Snapshot for Lightweighted Embedded Processors. *2021 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*
8. **H.Yun**, D. Park. Simulation of Self-driving System by implementing Digital Twin with GTA5. *ICEIC 2021*

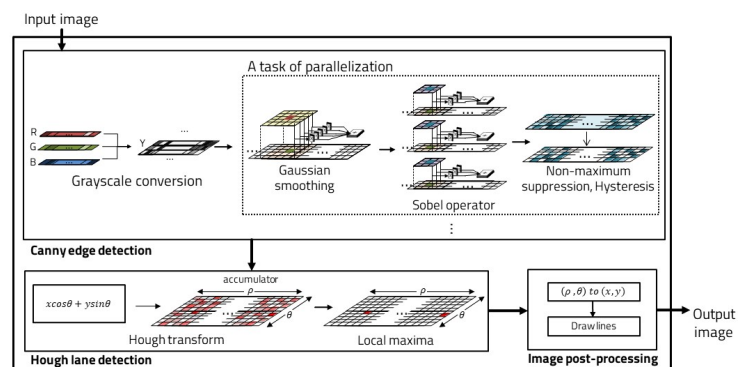
PROJECTS	<b>Reconfigurable CNN Accelerator for Adaptive AI Workloads</b> <i>Kyungpook National University</i>	2024.03 - 2024.08
	<b>Custom ISA Compatible with Arm Cortex-M0+</b> <i>Kyungpook National University</i>	2023.4 - 2024.01
	<b>SNN-based Compute-In-Memory (CIM) architecture</b> <i>Kyungpook National University</i>	2023.8 - 2023.11

TEACHING	<b>C Programming Practice (ELEC420)   Kyungpook National University</b> 2023.06	2023.03 -
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AWARDS AND HONORS	• <b>Scholarship Award</b> , KNU Ph.D Fellow Scholarship Award	2024
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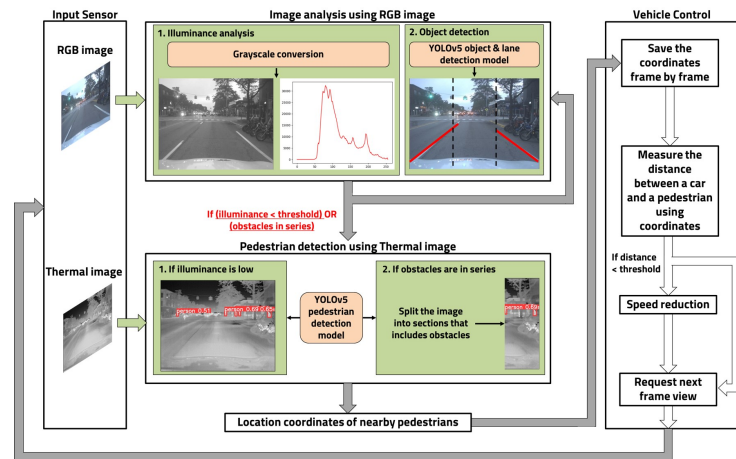
SKILLS	<b>Languages:</b> Korean, English. <b>Programming:</b> Python, C/C++, MATLAB, Verilog, Latex.
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FIELD OF RESEARCH INTEREST	<b>Mitigating Overflow of Object Detection Tasks</b>
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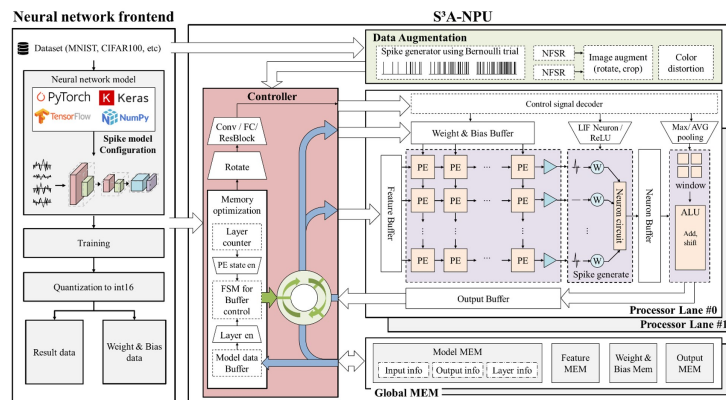
- Memory and computation-efficient image processing for embedded systems
- Parallelized Canny edge detection for lightweight lane recognition
- Optimized filtering and grayscale conversion for efficient processing

## Sensor Fusion Accelerators for Efficient Processing



- Multi-modal data fusion (thermal-RGB, LiDAR)
- Specialized hardware for real-time processing
- Low-power architectures for automotive applications

## Hardware Accelerator for Spiking Self-Supervised Learning



- High-performance hardware accelerator for spiking SSL models
- Optimized memory, parallel processing, and pipelined architecture
- Efficient low-power learning for edge AI and resource-limited environments